17V CMOS Analog Multiplexers/Switches

Features

- Low On-resistance: 60Ohm typ, with ±5V Supplies, Minimizes Distortion
- On-Resistance Matching between Channels Better than 6Ohm
- Guaranteed Low Leakage Currents: <0.1nA at +25°C
- Rail-to-Rail Analog Signal Range
- Low Distortion: <0.04% (600Ohm)
- Low Crosstalk: –90dB @100kHz
- TTL/CMOS Compatible (with +5V or ±5V Supplies)
- Low Power Consumption.
- 16-pin Narrow SOIC and QSOP Packages save board area
- Pin-compatible upgrades for 74HC4051/4052/4053

Applications

- Audio and Video Switching and Routing
- Lab and Medical Instrumentation
- Low-Voltage Data-Acquisition and Process Control Systems
- Battery-Powered Communication Systems

Description

The PS4051/PS4052/PS4053 are precision low-voltage CMOS analog multiplexers/switches.

The PS4051 is an eight-channel single-ended mux designed to select one of eight inputs to a common output. What input is selected depends on the status of three address bits (ADDA-ADDC). The PS4052 is a differential four-channel mux, controlled by two address bits: ADDA, and ADDB. The PS4053 is a triple 2-to-1 mux (or triple SPDT, single-pole double-throw, switch).

The INH (inhibit) pin can be driven high, to open all switches regardless of address bit status. All control inputs are TTL compatible when V+ = +5V.

These devices are designed to operate with power supplies from ±2.7V to ±8V. Single-supply operation is possible from +2.7V to +16V.

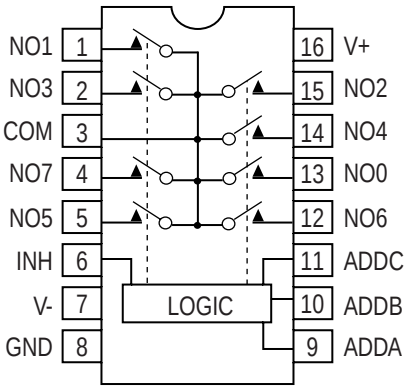
When on, each switch conducts current equally well in either direction and can handle rail-to-rail analog signals. In the off -state each switch blocks voltages up to the power-supply rails. Off-leakage current is guaranteed to be less than 0.1nA at +25°C, and < 2.5nA at +85°C.

These devices are available in 16-pin DIP, Narrow SOIC, and QSOP packages for operation over the –40°C to +85°C temperature range.

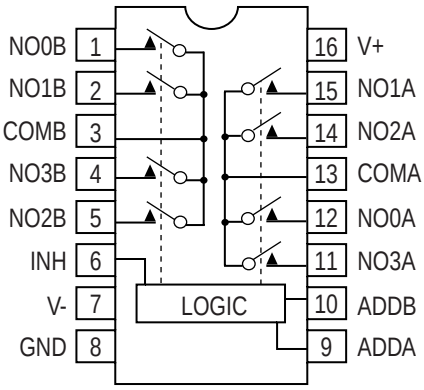
Functional Block Diagrams and Pin Configurations

Top Views

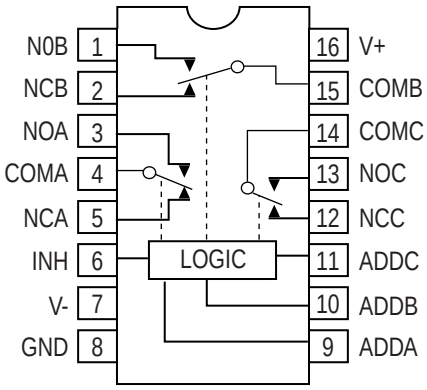
PS4051



PS4052



PS4053



For free samples and the latest literature: ***www.pericom.com****, or phone* 1-800-435-2336

Truth Tables

PS4051				
INH	**ADDC**	**ADDB**	**ADDA**	**On Switch**
1	X	X	X	None
0	0	0	0	NO0
0	0	0	1	NO1
0	0	1	0	NO2
0	0	1	1	NO3
0	1	0	0	NO4
0	1	0	1	NO5
0	1	1	0	NO6
0	1	1	1	NO7

PS4053						
INH	**ADDC**	**ADDB**	**ADDA**	**On Switches**		
1	X	X	X	None		
0	0	0	0	NOC	NOB	NOA
0	0	0	1	NOC	NOB	NCA
0	0	1	0	NOC	NCB	NOA
0	0	1	1	NOC	NCB	NCA
0	1	0	0	NCC	NOB	NOA
0	1	0	1	NCC	NOB	NCA
0	1	1	0	NCC	NCB	NOA
0	1	1	1	NCC	NCB	NCA

PS4052			
INH	**ADDB**	**ADDA**	**On Switch**
1	X	X	None
0	0	0	NO0A,B
0	0	1	NO1A,B
0	1	0	NO2A,B
0	1	1	NO3A,B

Logic "0", $V_{AL} \leq 0.8V$
Logic "1", $V_{IH} \geq 2.4V$

Absolute Maximum Ratings

Voltages Referenced to V–

V+ ..... –0.3V to + 17V

GND ..... –0.3V to + 17V

GND ..... -0.3V to (V+) + 0.3V

V_{IN}, V_{COM}, V_{NO}(1) ..... (V-) –2V to (V+) + 2V
or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA

ESD per method 3015.7 ..... >2000V

Thermal Information

Continuous Power Dissipation

Plastic DIP (derate 10.5mW/°C above +70°C) 800mW

Narrow SO and QSOP
(derate 8.7mW/°C above +70°C) 650mW

Storage Temperature ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1:

Signals on NO, COM, or logic inputs exceeding V+ or V– are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Dual Supplies

(V± = ± 5V ±10%, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp.(°C)	Min(2)	Typ(1)	Max(2)	Units
Analog Switch								
Analog Signal Range (3)	V_{ANALOG}			Full	V–		V+	V
On Resistance	R_{ON}	V+ = 5V, V– = –5V, V_{COM} = ±3V, I_{NO} = 1mA		25		60	100	Ohm
				Full			125	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{COM} or V_{NC} = ±3V, I_{NO} = 1mA, V+ = 5V, V– = –5V		25			12	
				Full			18	
On-Resistance Flatness(5)	$R_{FLAT (ON)}$	V+ = 5V, V– = –5V, I_{NO} = 1mA, V_{COM} = ±3V, 0V		25			10	
				Full			15	
NO Off Leakage Current(6)	I_{NO} (OFF)	V+ = 5.5V, V– = –5.5V, V_{COM} = ±4.5V, V_{NO} = ∓4.5V		25	–0.1		50	nA
				Full	–1.0		100	
COM-Off Leakage Current(6)	I_{COM} (OFF)	V+ = 5.5V, V– = –5.5V, V_{COM} = ± 4.5V, V_{NO} = ∓4.5V	PS4051	25	–0.1		50	
				Full	–2.5		100	
			PS4052 PS4053	25	–0.1		50	
				Full	–1.5		100	
COM On Leakage Current(7)	$I_{COM (ON)}$	V_{COM} = ∓4.5V	PS4051	25	–0.1		50	
				Full	–5		100	
			PS4052 PS4053	25	–0.1		50	
				Full	–2.5		100	
Logic Input								
Logic High Input Voltage	V_{AH} , V_{IH}			Full	2.4			V
Logic Low Input Voltage	V_{AL} , V_{IL}						0.8	
Input Current with Input Voltage High or Low	I_{IH} , I_{IL}	$V_A = V_I$ = V+, 0V			-0.1		0.1	µA

Electrical Specifications - Dual Supplies (continued)
(V± = ±5V ±10%, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Dynamic								
Transition Time	t_{TRANS}	Figure 1		25		75	250	ns
Break-Before-Make TimeDelay	t_{OPEN}	Figure 3			2	10		
Turn-OnTime	t_{ON}	Figure 2				50	175	
				Full			225	
Turn-Off Time	t_{OFF}	Figure 2		25		40	150	
				Full			200	
Charge Injection(3)	Q	C_L= 1nF, V_S = 0V, R_S = 0Ohm,		25		2	10	pC
Off Isolation(7)	OIRR	C_L = 15pF, V_{INH} = 5V, R_L = 50Ohm, f = 100kHz, V_{NO} = $1V_{RMS}$				–90		dB
Crosstalk	X_{TALK}	C_L = 15pF, R_L = 50Ohm, f = 100kHz, Figure 6, V_{NO} = $1V_{RMS}$				–92		
Logic Input Capacitance	C_{IN}	f=1MHz				8		pF
NO Off Capacitance	$C_{NO\ (OFF)}$	f=1MHz, V_{NO} = 0V				2		
COM Off Capacitance	$C_{COM\ (OFF)}$	f=1MHz, V_{COM} =0V	PS4051			2		
			PS4052 PS4053			2		
COM On Capacitance	$C_{COM\ (ON)}$	f=1MHz, V_{COM} = 0V	PS4051			8		
			PS4052 PS4053			8		
Supply								
Power-Supply Range				Full	±2.7		±8	V
Positive Supply Current	I+	$V_{INH} = V_A$ = 0V or V+, V+ =5.5V, V– = –5.5V					10	µA
Negative Supply Current	I–				–10			

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum values of on-resistance measured over the specific analog signal range, i.e., V_{NO} = 3V to 0 and 0V to –3V.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}\ V_{COM} / V_{NO}$. See Figure 5.

Electrical Characteristics - Single 5V Supply

(V+ = +5V ±10%, V– = 0V, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Switch								
Analog Signal Range(3)	V_{ANALOG}			Full	0		V+	V
On Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		25		125	225	Ohm
				Full			280	
NO-Off Leakage Current(8)	$I_{NO (OFF)}$	V_{NO} = 0V, V_{COM} = 4.5V, V+ = 5.5V		25	–0.1		50	nA
				Full	–10		100	
COM-Off Leakage Current(8)	$I_{COM (OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} =0V, or V_{COM} = 0V, V_{NO} = 4.5V	PS4051	25	–1		50	
				Full	–10		100	
			PS4052 PS4053	25	–1		50	
				Full	–5		100	
COM-On Leakage Current(8)	$I_{COM (ON)}$	$V_{COM} = V_{NO}$ = 4.5V, V+ = 5.5V	PS4051	25	–1		50	
				Full	–10		100	
			PS4052 PS4053	25	–1		50	
				Full	–10		100	
Digital Logic Input								
Logic High Input Voltage	V_{AH} , V_{IH}			Full	2.4			V
Logic Low Input Voltage	V_{AL} , V_{IL}						0.8	
Input Current with Input Voltage High or Low	I_{IH} , I_{IL}	$V_A = V_I$ = V +, 0V			–1		1	µA
Supply								
Positive-Supply Current	I+	$V_A = V_I$ = 0V or V+		25	–1.0		1.0	µA
				Full			10	

Electrical Characteristics - Single 5V(continued)

(V+ = +5V ±10%, V– = 0V, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Dynamic							
Turn-OnTime	t_{ON}		25		90	200	ns
			Full			275	
Turn-Off Time	t_{OFF}		25		60	125	
			Full			175	
Break-Before-Make Interval	t_{OPEN}		25		30		
Charge Injection(3)	Q	C_L = 1nF, V_S = 0V, R_S = 0Ohm			1.5	5	pC

Electrical Characteristics - Single 3V Supply

(V+ = +3.3V ±10%, V– = 0V, GND = 0V, $V_{AH} = V_{IH} = +2.4V$, $V_{AL} = V_{IL_L} = +0.8V$)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 1.5V, V+ = 3V	25		250	525	ohm
			Full			700	
Dynamic							
Transition Time(3)	t_{TRANS}	Figure 1, V_{IN} = 2.4V, V_{NO1} = 1.5V, V_{NO8} = 0V	25		230	575	ns
Turn-OnTime(3)	t_{ON}	Figure 2, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V			200	500	
Turn-Off Time(3)	t_{OFF}	Figure 2, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V			75	400	
Charge Injection (3)	Q	C_L = 10nF, V_S = 0V, R_S = 0Ohm			1	5	pC

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, VNO = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Test Circuits/Timing Diagrams

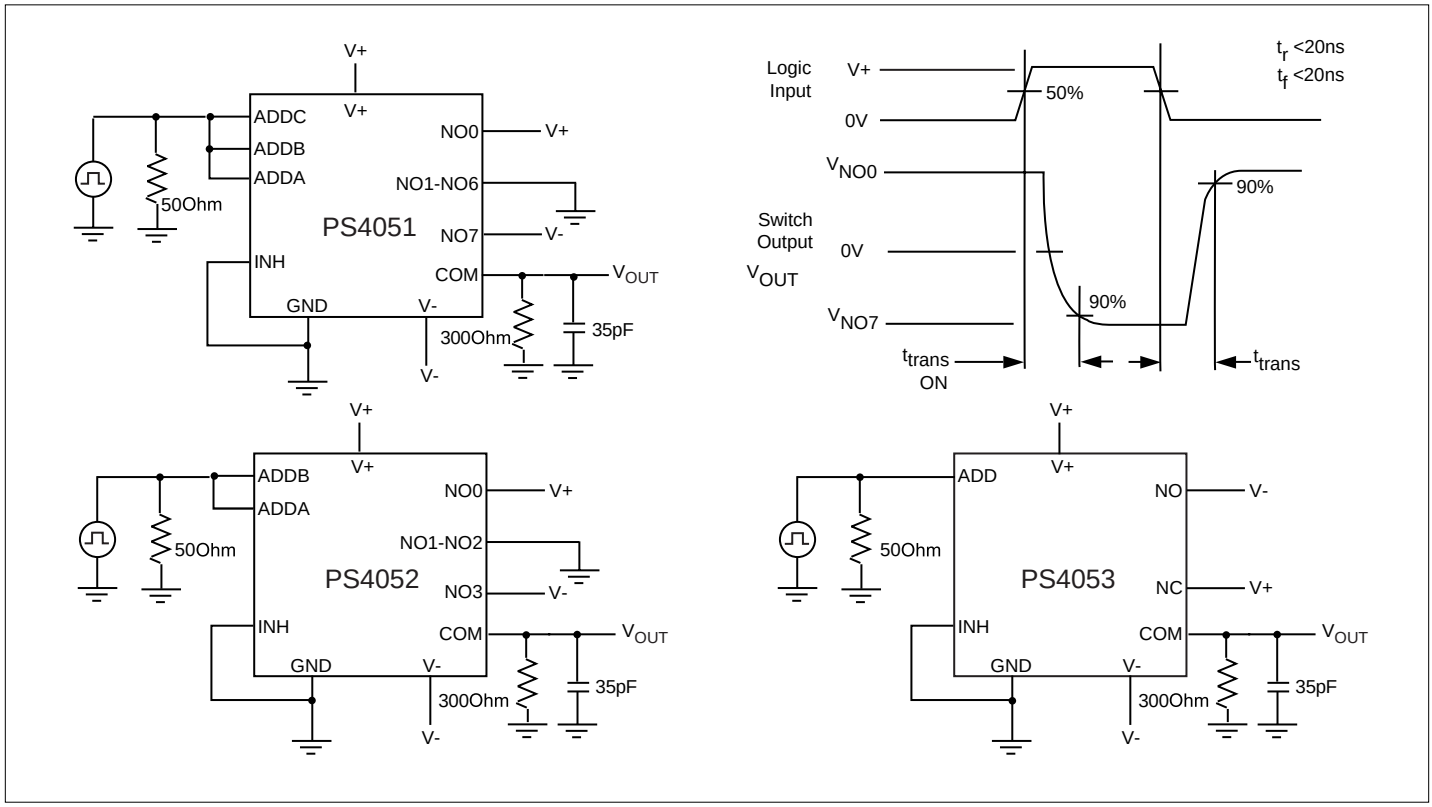


Figure 1. Transition Time

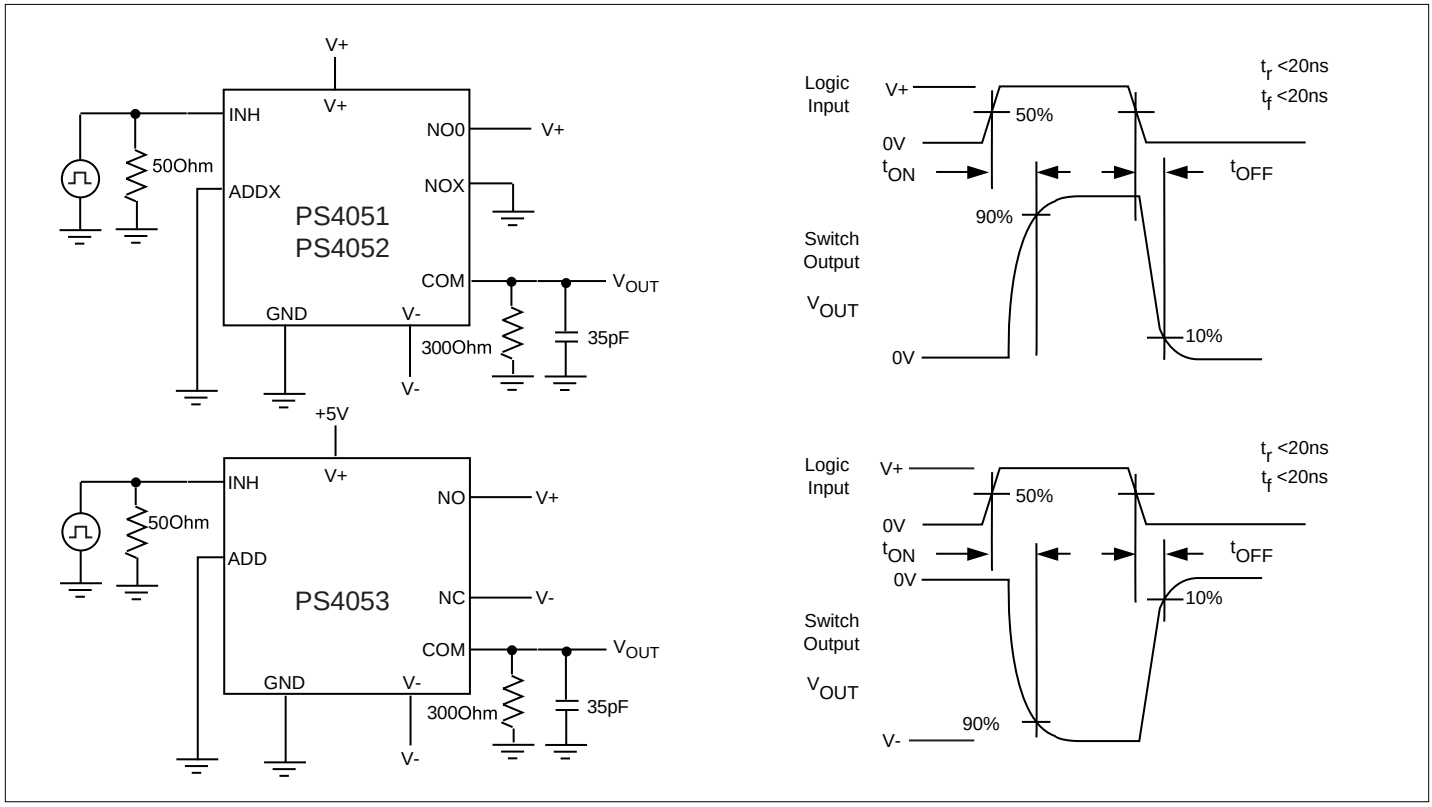


Figure 2. Switching Times

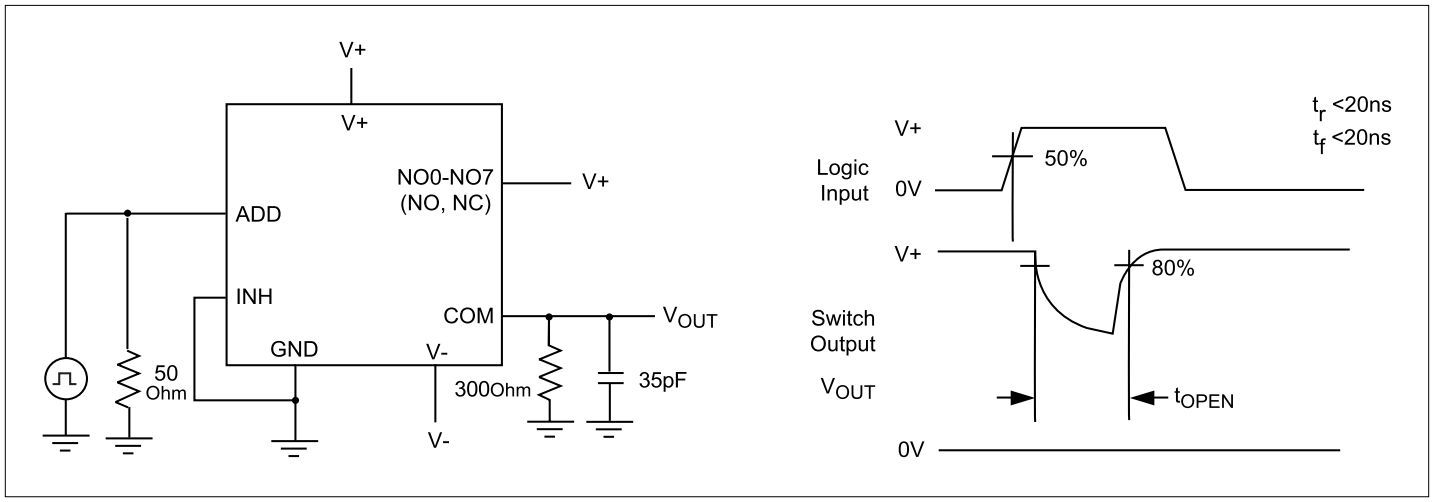


Figure 3. Break-Before-Make Interval

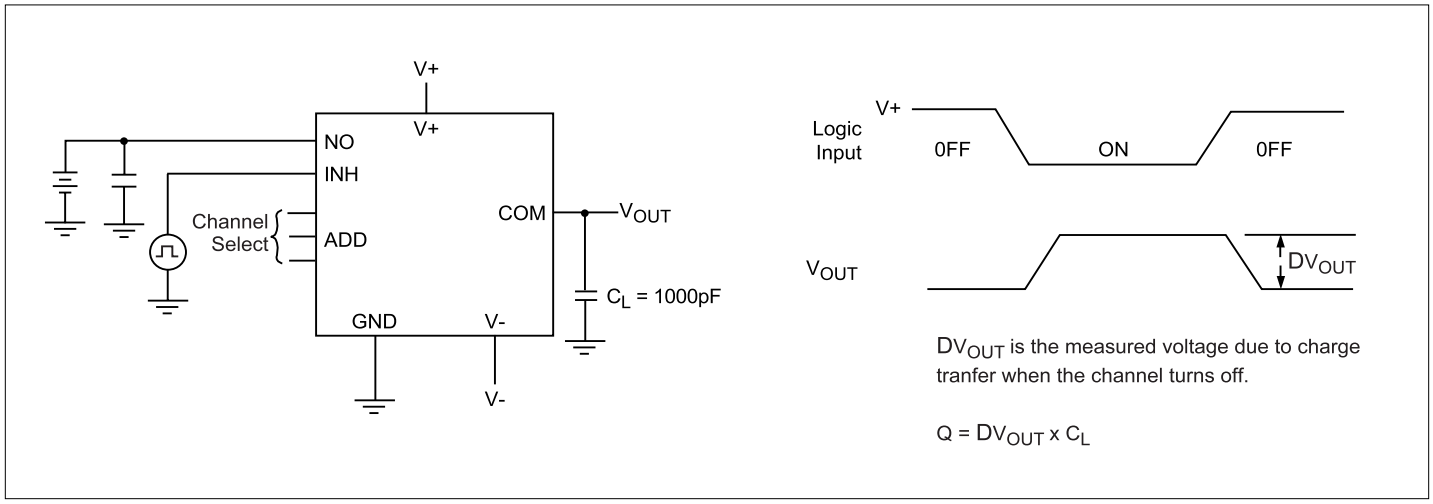


Figure 4. Charge Injection

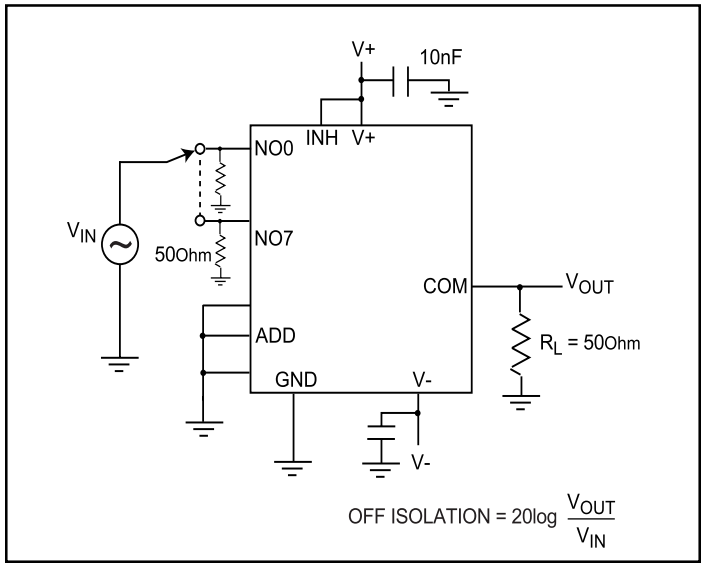


Figure 5. Off Isolation

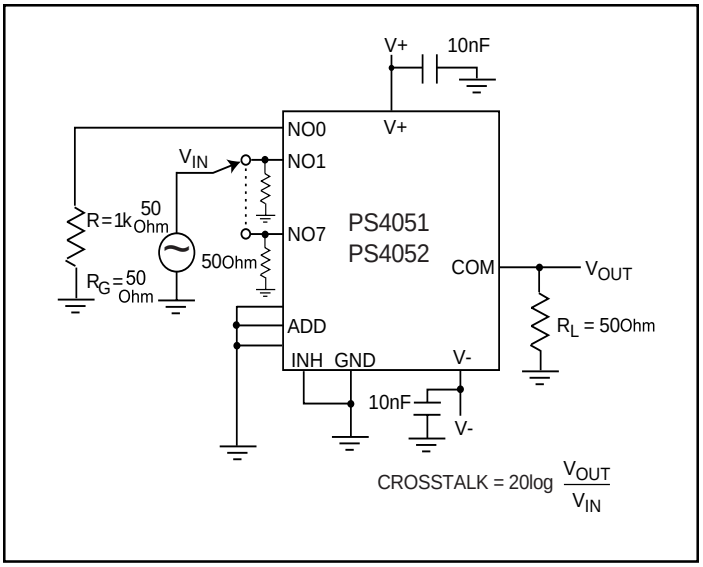


Figure 6. Crosstalk

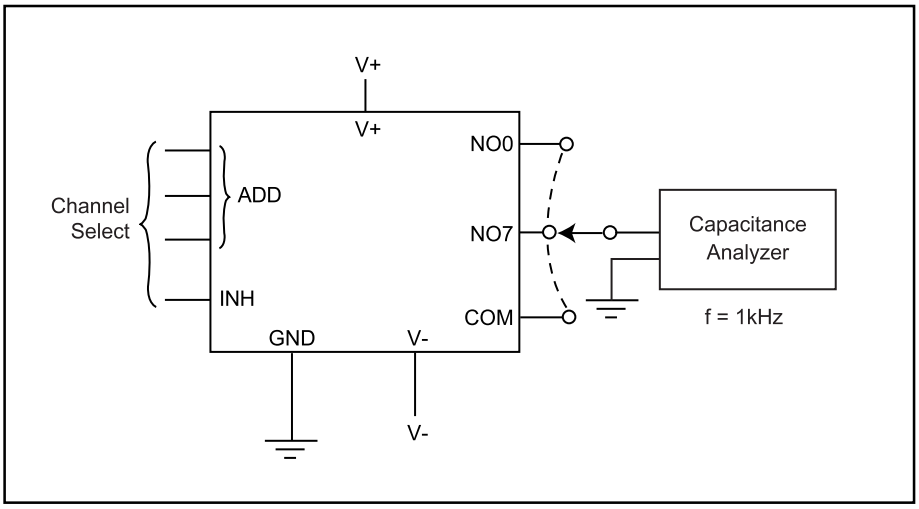


Figure 8. NO/COM Capacitance

Ordering Information

Part Number	Temperature	Package
PS4051CPE	0ºC to +70ºC	PDIP-16
PS4051CSE	0ºC to +70ºC	Narrow SOIC-16
PS4051CEE	0ºC to +70ºC	QSOP-16
PS4051EPE	–40ºC to +85ºC	PDIP-16
PS4051ESE	–40ºC to +85ºC	Narrow SOIC-16
PS4051EEE	–40ºC to +85ºC	QSOP-16
PS4052CPE	0ºC to +70ºC	PDIP-16
PS4052CSE	0ºC to +70ºC	Narrow SOIC-16
PS4052CEE	0ºC to +70ºC	QSOP-16

Part Number	Temperature	Package
PS4052EPE	–40ºC to +85ºC	PDIP-16
PS4052ESE	–40ºC to +85ºC	Narrow SOIC-16
PS4052EEE	–40ºC to +85ºC	QSOP-16
PS4053CPE	0ºC to +70ºC	PDIP-16
PS4053CSE	0ºC to +70ºC	Narrow SOIC-16
PS4053CEE	0ºC to +70ºC	QSOP-16
PS4053EPE	–40ºC to +85ºC	PDIP-16
PS4053ESE	–40ºC to +85ºC	Narrow SOIC-16
PS4053EEE	–40ºC to +85ºC	QSOP-16