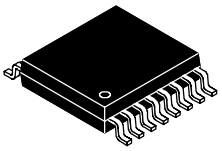
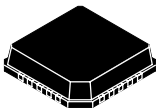




LOW-VOLTAGE AND LOW-POWER STEREO AUDIO DIGITAL-TO-ANALOG CONVERTER WITH LINEOUT AMPLIFIER

FEATURES

- **Multilevel DAC Including Lineout Amplifier**
- **Analog Performance (V_{CC1}, V_{CC2} = 2.4 V):**
  - **Dynamic Range: 98 dB Typ**
  - **THD+N at 0 dB: 0.007% Typ**
- **1.6-V to 3.6-V Single Power Supply**
- **Low Power Dissipation: 6 mW at V_{CC1}, V_{CC2} = 2.4 V**
- **System Clock: $128f_S$, $192f_S$, $256f_S$, $384f_S$**
- **Sampling Frequency: 5 kHz to 50 kHz**
- **Software Control (PCM1772):**
  - **16-, 20-, 24-Bit Word Available**
  - **Left-, Right-Justified and I2S**
  - **Slave/Master Selectable**
- **Digital Attenuation:**
  - **0 dB to –62 dB, 1 dB/Step**
  - **44.1-kHz Digital De-Emphasis**
  - **Zero Cross Attenuation**
  - **Digital Soft Mute**
  - **Monaural Analog-In With Mixing**
  - **Monaural Speaker Mode**
- **Hardware Control (PCM1773):**
  - **Left-Justified and I2S**
  - **44.1-kHz Digital De-Emphasis**
  - **Monaural Analog-In With Mixing**
- **Pop-Noise-Free Circuit**
- **3.3-V Tolerant**
- **Packages: TSSOP-16 and VQFN-20, Lead Free**

APPLICATIONS

- **Portable Audio Player**
- **Cellular Phone**
- **PDA**
- **Other Applications Requiring Low Voltage Operation**

DESCRIPTION

The PCM1772 and PCM1773 devices are CMOS, monolithic, integrated circuits which include stereo digital-to-analog converters, lineout circuitry, and support circuitry in small TSSOP-16 and VQFN-20 packages.

The data converters utilize TI's enhanced multilevel Δ-Σ architecture, which employs noise shaping and multilevel amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1772 and PCM1773 devices accept several industry standard audio data formats with 16- to 24-bit data, left-justified, I2S, etc., providing easy interfacing to audio DSP and decoder devices. Sampling rates up to 50 kHz are supported. A full set of user-programmable functions are accessible through a 3-wire serial control port, which supports register write functions.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION

PRODUCT PACKGE	PACKAGE	PACKAGE CODE	T_A	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM1772PW	TSSOP–16	16PW	–25°C to 85°C	PCM1772	PCM1772PW	Tube
					PCM1772PWR	Tape and Reel
PCM1773PW	TSSOP–16	16PW	–25°C to 85°C	PCM1773	PCM1773PW	Tube
					PCM1773PWR	Tape and Reel
PCM1772RGA	VQFN–20	20RGA	–25°C to 85°C	PCM1772	PCM1772RGA	Tray
					PCM1772RGAR	Tape and Reel
PCM1773RGA	VQFN–20	20RGA	–25°C to 85°C	PCM1773	PCM1773RGA	Tray
					PCM1773RGAR	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	PCM1772 PCM1773
Supply voltage: V_{CC1}, V_{CC2}	4 V
Supply voltage differences: V_{CC1}, V_{CC2}	±0.1 V
Ground voltage differences	±0.1 V
Digital input voltage	–0.3 V to 4 V
Input current (any terminals except supplies)	±10 mA
Operating temperature	–40°C to 125°C
Storage temperature	–55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C, 10 s

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 2.4 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution					24		Bits
DATA FORMAT							
Audio data interface format		(PCM1772)	Standard, I2S, left justified				
		(PCM1773)	I2S, left justified				
Audio data bit length			16-, 20-, 24-bit selectable				
Audio data format			MSB first, twos complement				
Sampling frequency (f_S)				5		50	kHz
Internal system clock frequency				128f_S, 192f_S, 256f_S, 384f_S			
DIGITAL INPUT/OUTPUT(1)							
Logic family			CMOS compatible				
V_{IH}	Input logic level			0.7V_{CC1}			Vdc
V_{IL}						0.3V_{CC1}	Vdc
I_{IH}	Input logic current		V_{IN} = V_{CC1}			10	µA
I_{IL}			V_{IN} = 0 V			–10	µA
V_{OH}	Output logic level(2)		I_{OH} = –2 mA	0.7V_{CC1}			Vdc
V_{OL}			I_{OL} = 2 mA			0.3V_{CC1}	Vdc
DYNAMIC PERFORMANCE							
LINE OUTPUT							
Full scale output voltage			0 dB		0.75V_{CC2}		V_{P-P}
Dynamic range			EIAJ, A-weighted	90	98		dB
Signal-to-noise ratio			EIAJ, A-weighted	90	98		dB
THD+N			0 dB		0.007%	0.015%	
Channel separation				70	80		dB
Load resistance				10			kΩ
dc ACCURACY							
Gain error					±2	±8	%FSR
Gain mismatch, channel-to-channel					±2	±8	%FSR
Bipolar zero error			V_{OUT} = 0.5V_{CC1} at BPZ		±30	±75	mV
ANALOG LINE INPUT (MIXING CIRCUIT)							
Analog input voltage range						0.584V_{CC2}	V_{P-P}
Gain (analog input to line output)					0.91		
Analog input impedance					10		kΩ
THD+N			AIN = 0.56V_{CC2} (peak-to-peak)		0.1%		
DIGITAL FILTER PERFORMANCE							
Passband						0.454f_S	
Stopband				0.546f_S			
Passband ripple						±0.04	dB
Stop band attenuation				–50			dB
Group delay					20/f_S		
44.1-kHz de-emphasis error					±0.1		dB

(1) All logic inputs are 3.3-V tolerant and not terminated internally.
(2) LRCK and BCK terminals

ELECTRICAL CHARACTERISTICS (continued)

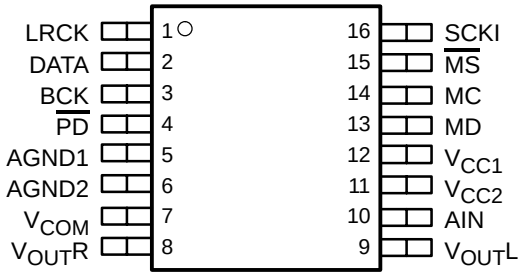
all specifications at T_A = 25°C, V_{CC1} = V_{CC2} = 2.4 V, f_S = 44.1 kHz, system clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG FILTER PERFORMANCE						
Frequency response		at 20 kHz		±0.2		dB
POWER SUPPLY REQUIREMENTS						
Voltage range, V_{CC1}, V_{CC2}			1.6	2.4	3.6	Vdc
I_{CC1}	Supply current	BPZ input		1.5	2.5	mA
I_{CC2}		BPZ input		1	2.5	
I_{CC1} + I_{CC2}		Power down(3)		5	15	µA
Power dissipation		BPZ input		6.0	12	mW
		Power down(3)		12	36	µW
TEMPERATURE RANGE						
Operation temperature			–25		85	°C
θ_{JA}	Thermal resistance	PCM1772PW, –73PW: 16-terminal TSSOP		150		°C/W
		PCM1772RGA, –73RGA: 20-terminal VQFN		130		

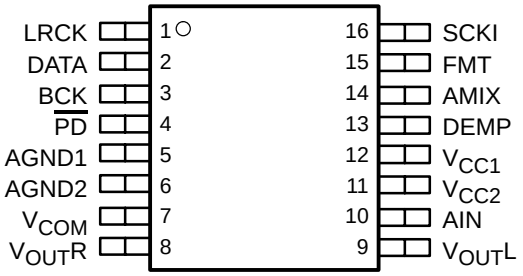
(1) All logic inputs are 3.3-V tolerant and not terminated internally.
(2) LRCK and BCK terminals
(3) All input signals are held static.

PIN ASSIGNMENTS

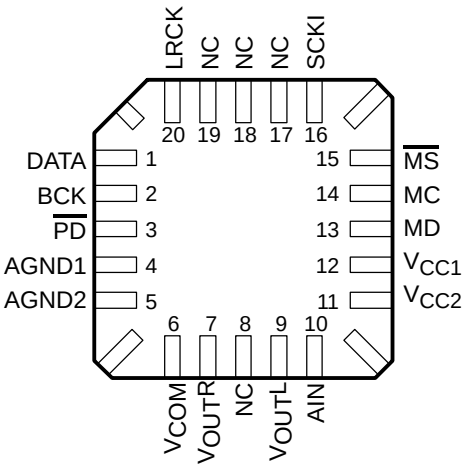
PCM1772
PW PACKAGE
(TOP VIEW)



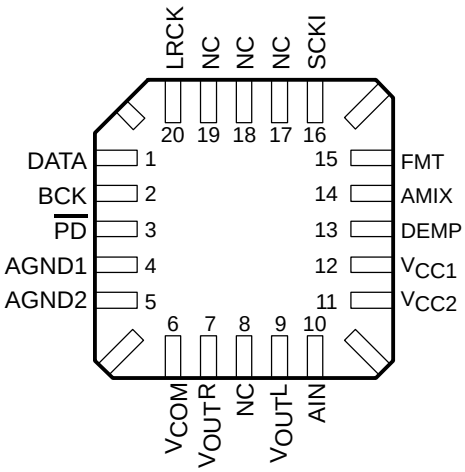
PCM1773
PW PACKAGE
(TOP VIEW)



PCM1772
RGA PACKAGE
(TOP VIEW)



PCM1773
RGA PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

PCM1772PW

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTIONS
LRCK	1	I/O	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the LRCK output to an external device.
DATA	2	I	Serial audio data input
BCK	3	I/O	Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from external device. In master interface mode, the PCM1772 device generates the BCK output to an external device.
$\overline{PD}$	4	I	Reset input. When low, the PCM1772 device is powered down and all mode control registers are reset to default settings.
AGND1	5	–	Analog ground. This is a return for V_{CC1}.
AGND2	6	–	Analog ground. This is a return for V_{CC2}.
V_{COM}	7	–	Decoupling capacitor connection. An external 10-μF capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
$V_{OUT}R$	8	O	R-channel analog signal output of the lineout amplifiers
$V_{OUT}L$	9	O	L-channel analog signal output of the lineout amplifiers
AIN	10	I	Monaural analog signal mixer input. The signal can be mixed with the output of L- and R-channel DACs.
V_{CC2}	11	–	Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V_{CC1}.
V_{CC1}	12	–	Analog power supply for all analog circuits except the lineout amplifier.
MD	13	I	Mode control port serial data input. Controls the operation mode on the PCM1772 device.
MC	14	I	Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD.
$\overline{MS}$	15	I	Mode control port select. The control port is active when this terminal is low.
SCKI	16	I	System clock input

PCM1772RGA

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTIONS
DATA	1	I	Serial audio data input
BCK	2	I/O	Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the BCK output to an external device.
$\overline{PD}$	3	I	Reset input. When low, the PCM1772 device is powered down and all mode control registers are reset to default settings.
AGND1	4	–	Analog ground. This is a return for V_{CC1}.
AGND2	5	–	Analog ground. This is a return for V_{CC2}.
V_{COM}	6	–	Decoupling capacitor connection. An external 10-μF capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
$V_{OUT}R$	7	O	R-channel analog signal output of lineout amplifiers.
NC	8, 17, 18, 19	–	No connect
$V_{OUT}L$	9	O	L-channel analog signal output of lineout amplifiers.
AIN	10	I	Monaural analog signal mixer input. The signal can be mixed with output of L- and R-channel DACs.
V_{CC2}	11	–	Analog power supply for lineout amplifier circuits. The voltage level must be the same as V_{CC1}.
V_{CC1}	12	–	Analog power supply for all analog circuits except lineout amplifier.
MD	13	I	Mode control port serial data input. Controls the operation mode on the PCM1772 device.
MC	14	I	Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD.
$\overline{MS}$	15	I	Mode control port select. The control port is active when this terminal is low.
SCKI	16	I	System clock input
LRCK	20	I/O	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the LRCK output to an external device.

Terminal Functions

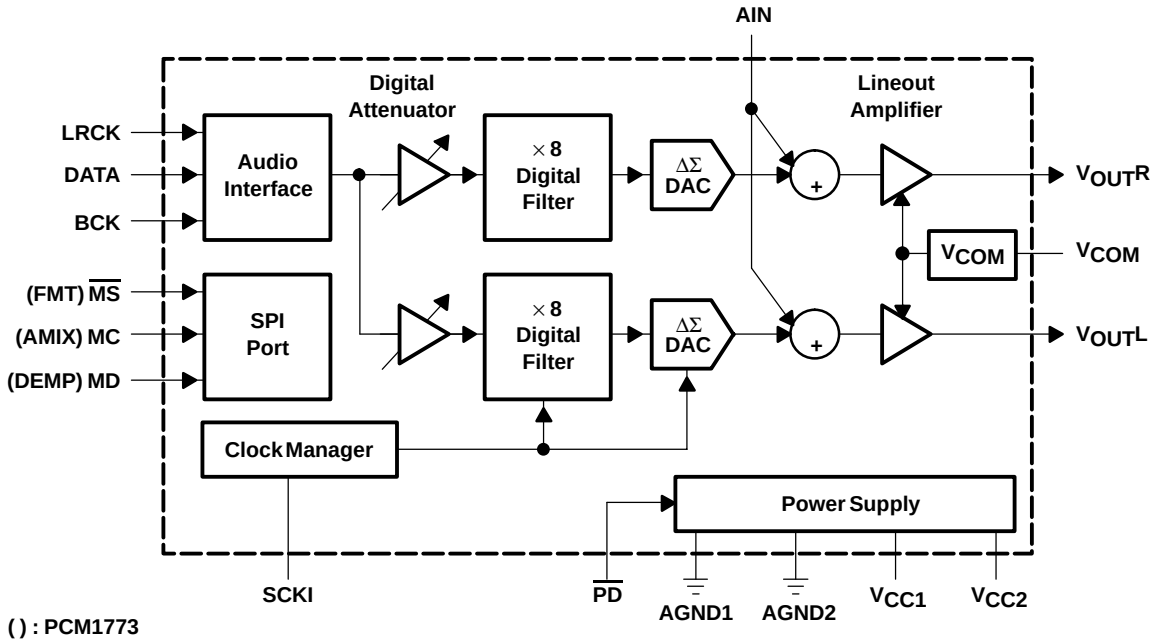
PCM1773PW

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTIONS
LRCK	1	I	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate.
DATA	2	I	Serial audio data input
BCK	3	I	Serial bit clock. Clocks the individual bits of the audio data input, DATA.
$\overline{PD}$	4	I	Reset input. When low, the PCM1773 device is powered down and all mode control registers are reset to default settings.
AGND1	5	–	Analog ground. This is a return for V_{CC1}.
AGND2	6	–	Analog ground. This is a return for V_{CC2}.
V_{COM}	7	–	Decoupling capacitor connection. An external 10-µF capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
$V_{OUT}R$	8	O	R-channel analog signal output of the lineout amplifiers
$V_{OUT}L$	9	O	L-channel analog signal output of the lineout amplifiers
AIN	10	–	Monaural analog signal mixer input. The signal can be mixed with the output of L- and R-channel DACs.
V_{CC2}	11	–	Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V_{CC1}.
V_{CC1}	12	–	Analog power supply for all analog circuits except the lineout amplifier
DEMP	13	I	De-emphasis control
AMIX	14	I	Analog mixing control
FMT	15	I	Data format select
SCKI	16	I	System clock input

PCM1773RGA

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTIONS
DATA	1	I	Serial audio data input
BCK	2	I	Serial bit clock. Clocks the individual bits of the audio data input, DATA.
$\overline{PD}$	3	I	Reset input. When low, the PCM1773 device is powered down and all mode control registers are reset to default settings.
AGND1	4	–	Analog ground. This is a return for V_{CC1}.
AGND2	5	–	Analog ground. This is a return for V_{CC2}.
V_{COM}	6	–	Decoupling capacitor connection. An external 10-µF capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
$V_{OUT}R$	7	O	R-channel analog signal output of the lineout amplifiers
NC	8, 17, 18, 19	–	No connect
$V_{OUT}L$	9	O	L-channel analog signal output of the lineout amplifiers
AIN	10	–	Monaural analog signal mixer input. The signal can be mixed with output of L- and R-channel DACs.
V_{CC2}	11	–	Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V_{CC1}.
V_{CC1}	12	–	Analog power supply for all analog circuits except the lineout amplifier
DEMP	13	I	De-emphasis control
AMIX	14	I	Analog mixing control
FMT	15	I	Data format select
SCKI	16	I	System clock input
LRCK	20	I	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DIGITAL FILTER

Digital Filter (De-Emphasis Off)

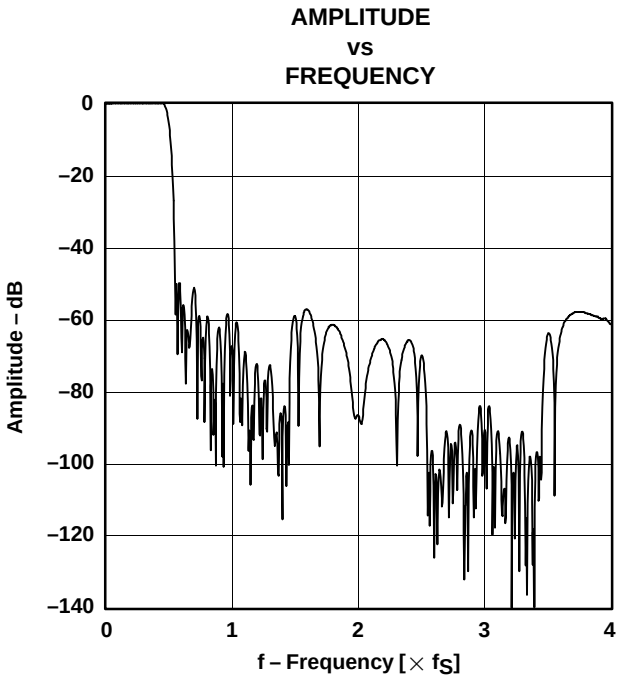


Figure 1

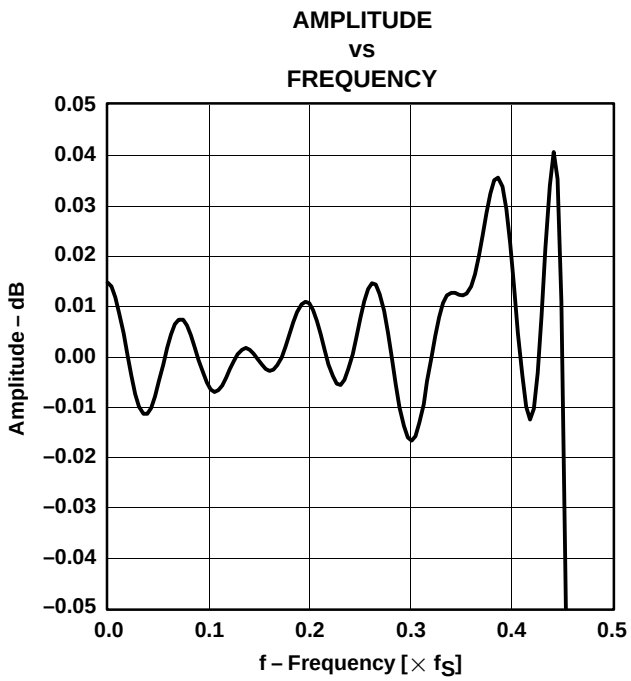


Figure 2

Electrical characteristics, all specifications at T_A = 25°C, V_{CC1} = V_{HP} = 2.4 V, f_S = 44.1 kHz, System clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted.

TYPICAL CHARACTERISTICS

De-Emphasis Curves

DE-EMPHASIS LEVEL
vs
FREQUENCY

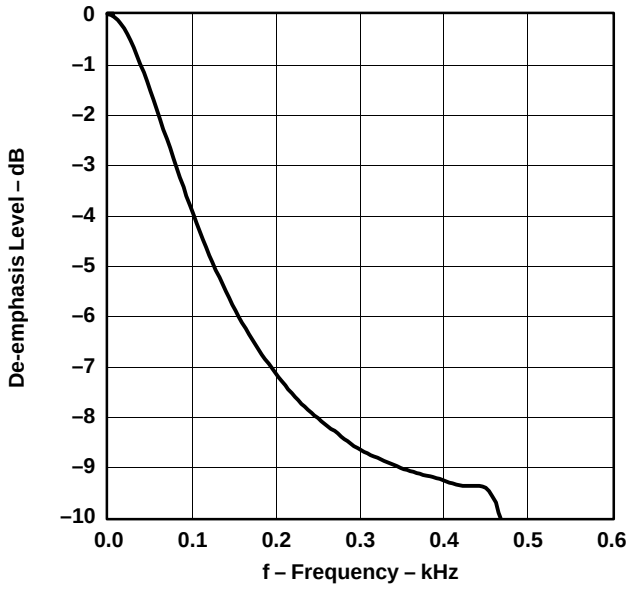


Figure 3

DE-EMPHASIS ERROR
vs
FREQUENCY

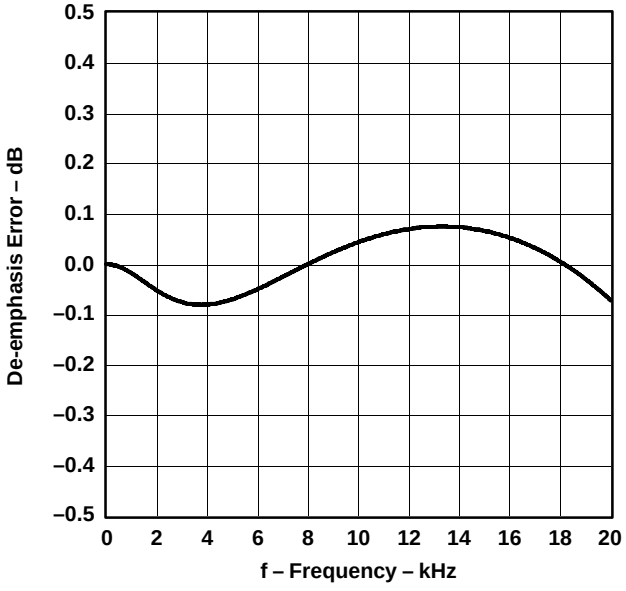


Figure 4

TOTAL HARMONIC DISTORTION + NOISE
vs
SUPPLY VOLTAGE

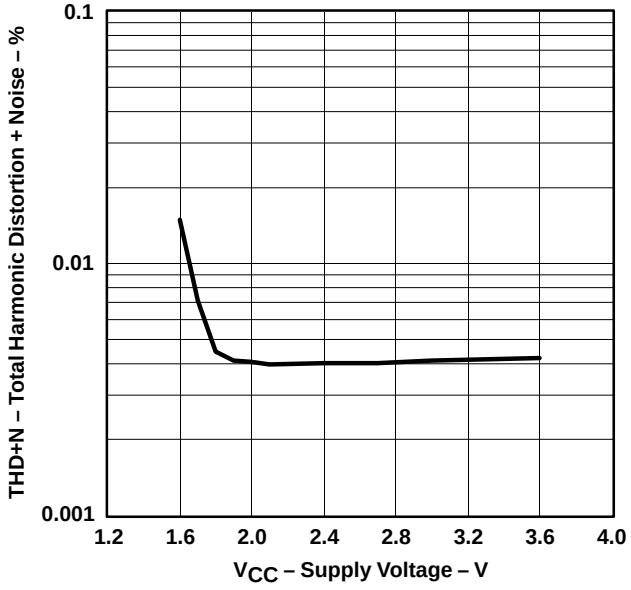


Figure 5

DYNAMIC RANGE
vs
SUPPLY VOLTAGE

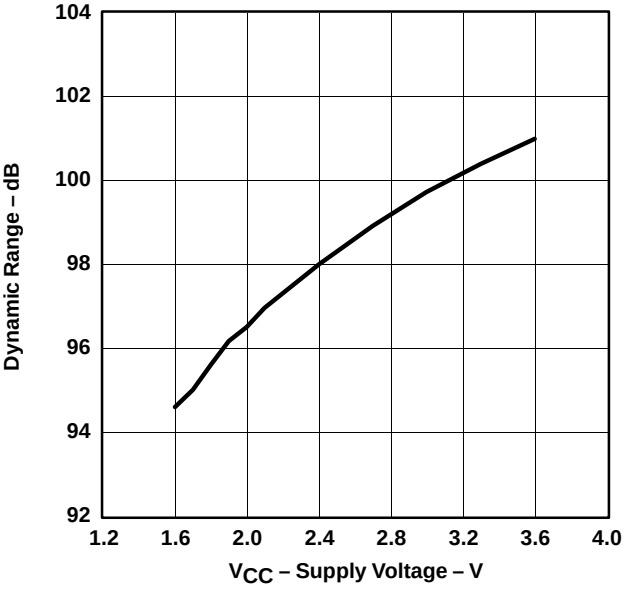


Figure 6

Electrical characteristics, all specifications at T_A = 25°C, V_{CC1} = V_{HP} = 2.4 V, f_S = 44.1 kHz, System clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted.

TYPICAL CHARACTERISTICS

SNR vs SUPPLY VOLTAGE

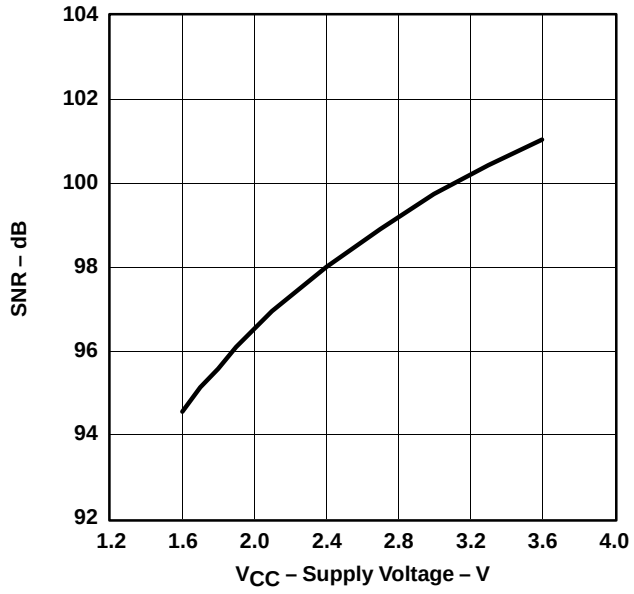


Figure 7

CHANNEL SEPARATION vs SUPPLY VOLTAGE

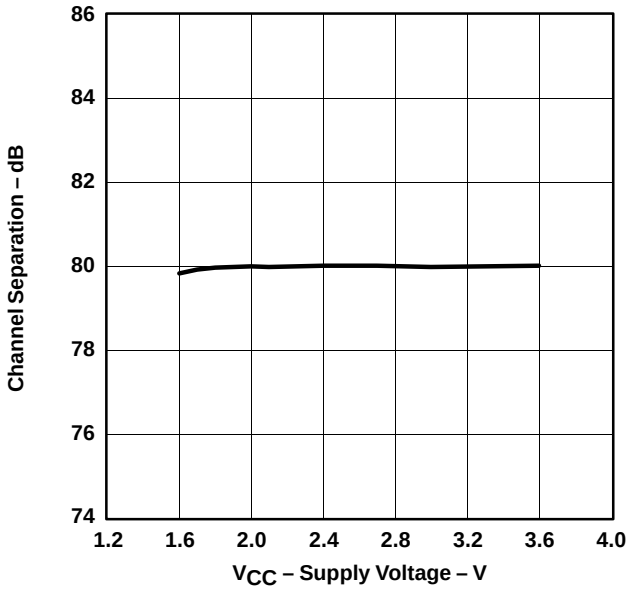


Figure 8

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

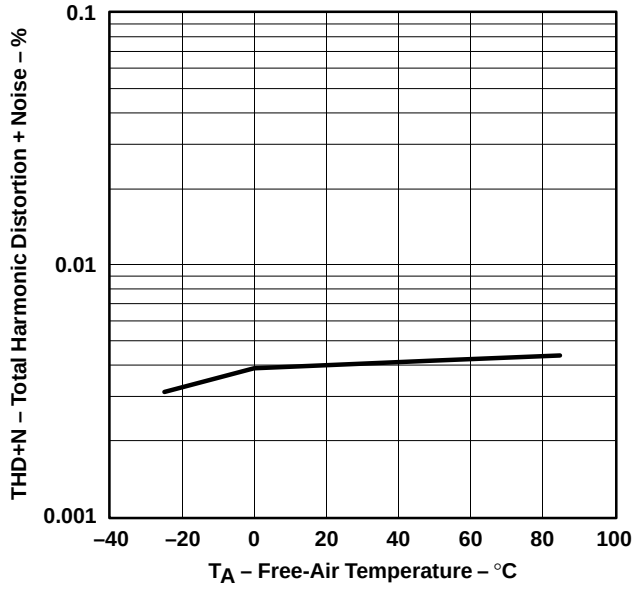


Figure 9

DYNAMIC RANGE vs FREE-AIR TEMPERATURE

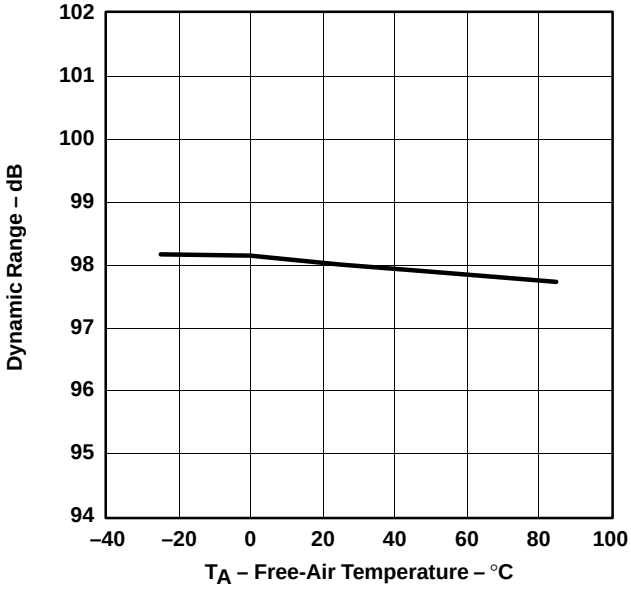


Figure 10

Electrical characteristics, all specifications at T_A = 25°C, V_{CC1} = V_{HP} = 2.4 V, f_S = 44.1 kHz, System clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted.

TYPICAL CHARACTERISTICS

SNR
vs
FREE-AIR TEMPERATURE

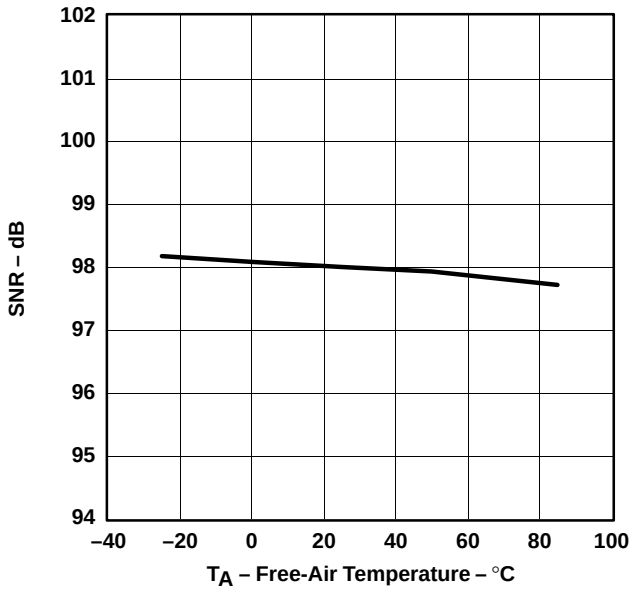


Figure 11

CHANNEL SEPARATION
vs
FREE-AIR TEMPERATURE

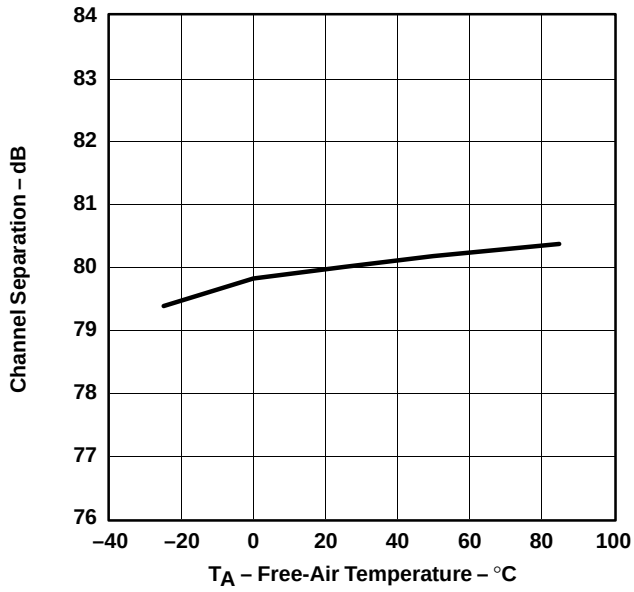


Figure 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

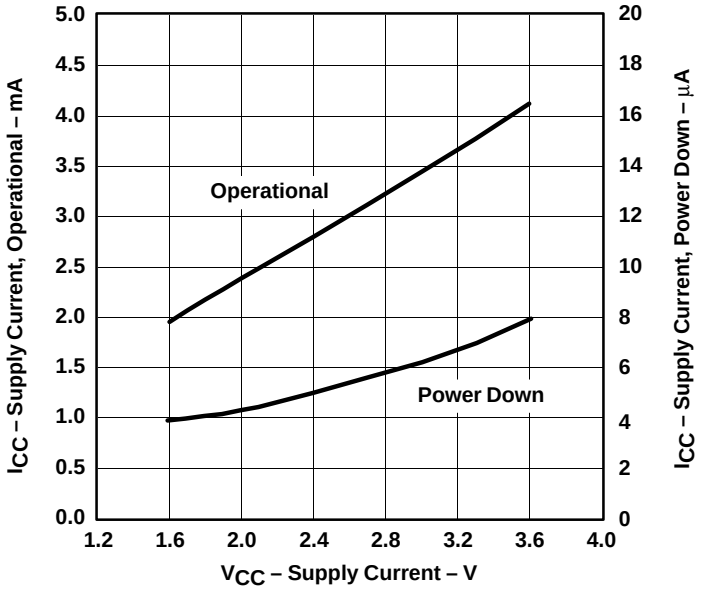


Figure 13

Electrical characteristics, all specifications at T_A = 25°C, V_{CC1} = V_{HP} = 2.4 V, f_S = 44.1 kHz, System clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted.

TYPICAL CHARACTERISTICS

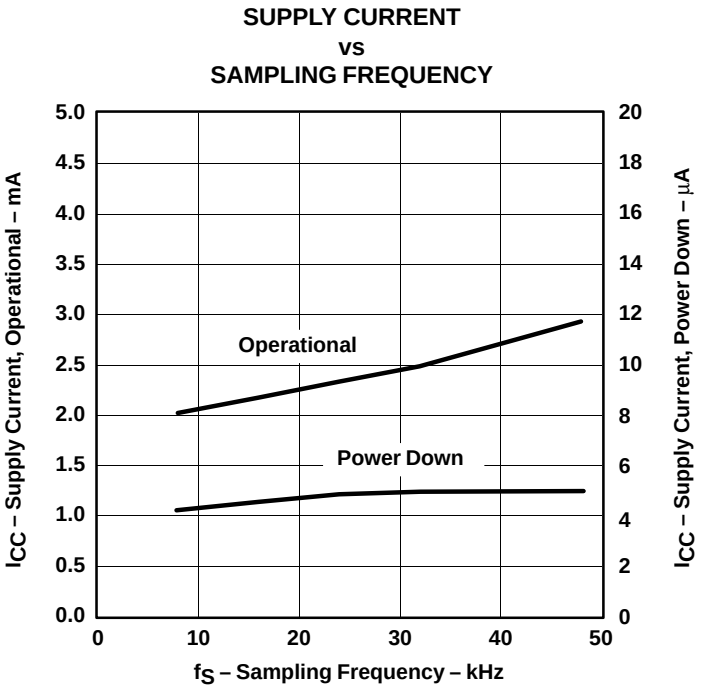


Figure 14

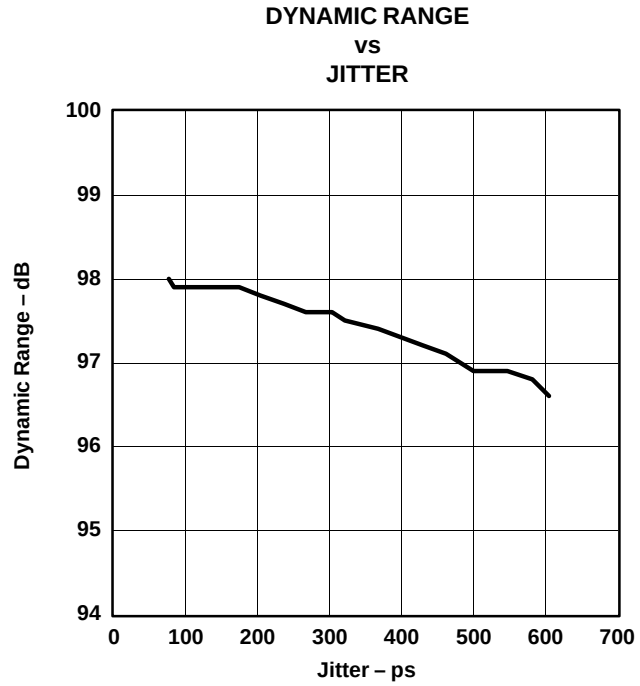


Figure 15

Electrical characteristics, all specifications at T_A = 25°C, V_{CC1} = V_{HP} = 2.4 V, f_S = 44.1 kHz, System clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted.

TYPICAL CHARACTERISTICS

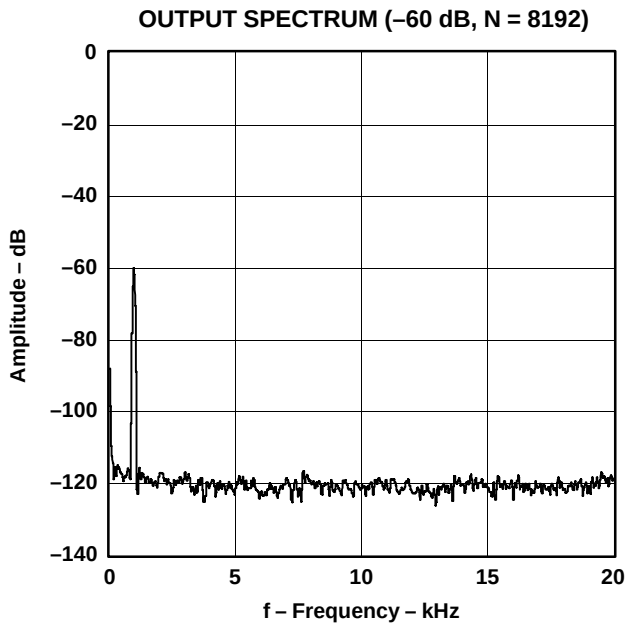


Figure 16

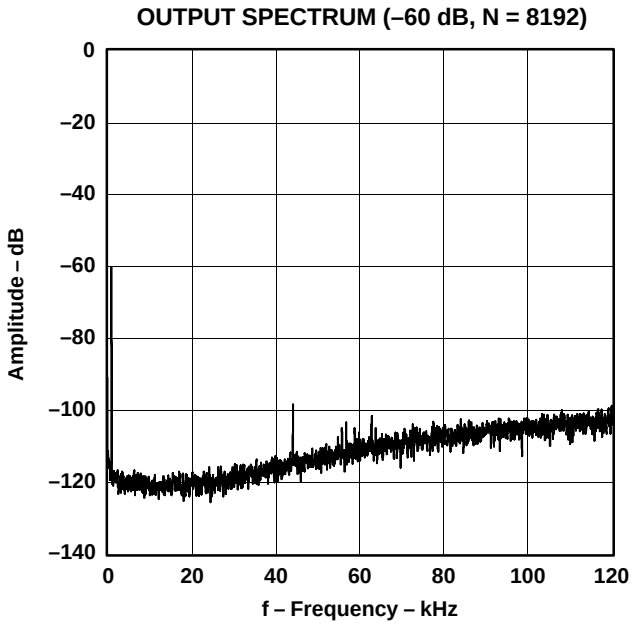


Figure 17

Electrical characteristics, all specifications at T_A = 25°C, V_{CC1} = V_{HP} = 2.4 V, f_S = 44.1 kHz, System clock = 256 f_S and 24-bit data, R_L = 10 kΩ, unless otherwise noted.

APPLICATION INFORMATION

CONNECTION DIAGRAMS

Figure 18 shows the basic connection diagram with the necessary power supply bypassing and decoupling components. It is recommended that the component values shown in Figure 18 be used for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the MCKI, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter that reduces high frequency noise emissions and helps to dampen glitches and ringing present on the clock and data lines.

POWER SUPPLIES AND GROUNDING

The PCM1772 and PCM1773 devices require a 2.4-V typical analog supply for V_{CC1} and V_{CC2}. These 2.4-V supplies power the DAC, analog output filter, and other circuits. For best performance, these 2.4-V supplies must be derived from the analog supply using a linear regulator, as shown in Figure 18.

Figure 18 shows the proper power supply bypassing. The 10-μF capacitors must be tantalum or aluminum electrolytic, while the 0.1-μF capacitors are ceramic (X7R type is recommended for surface-mount applications).

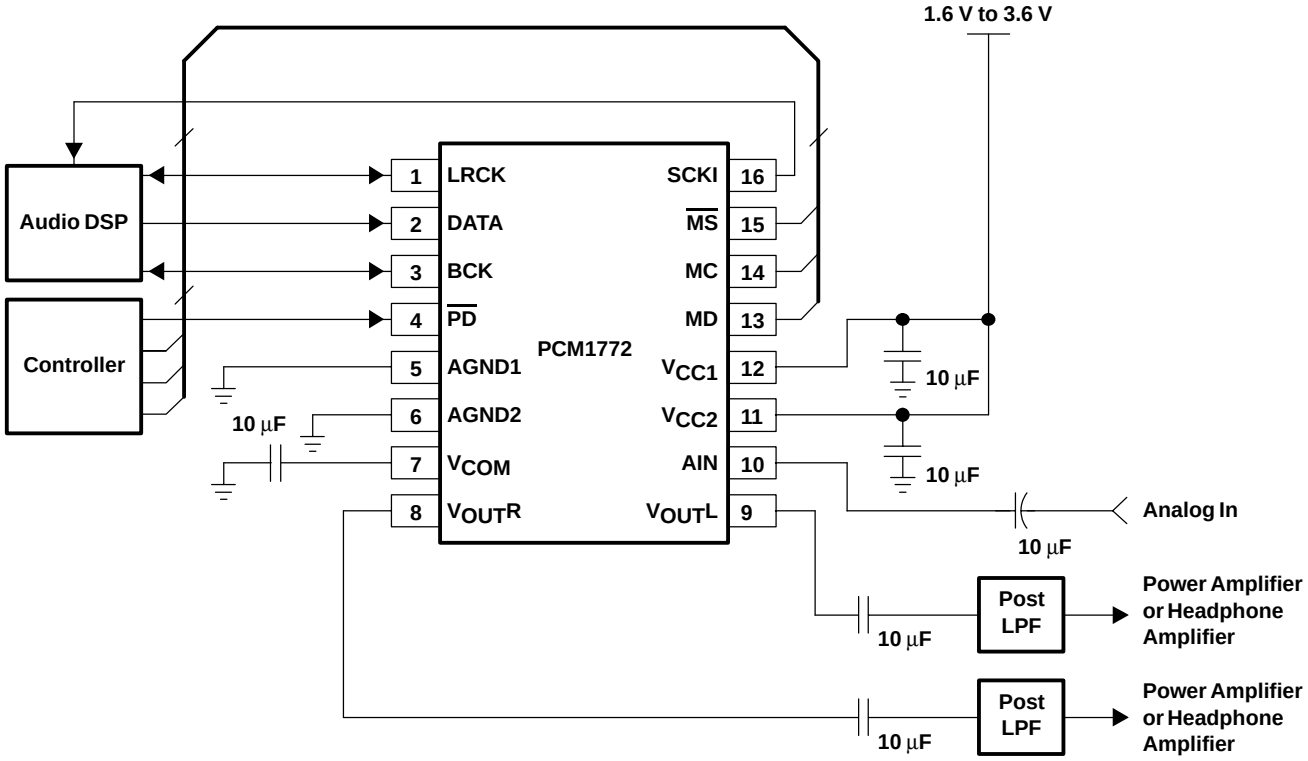


Figure 18. Basic Connection Diagram

DETAILED DESCRIPTION

SYSTEM CLOCK, RESET, AND FUNCTIONS

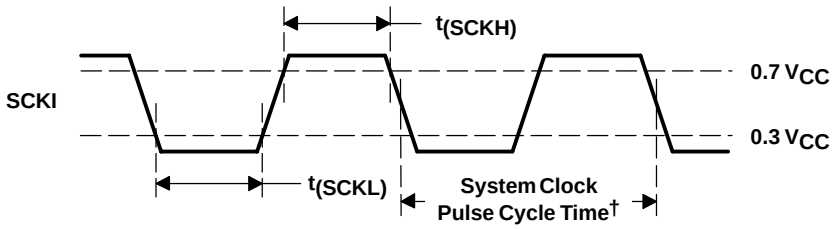
System Clock Input

The PCM1772 and PCM1773 devices require a system clock for operating the digital interpolation filters and multilevel Δ-Σ modulators. The system clock is applied at terminal 16 (SCKI). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 19 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low-phase jitter and noise.

Table 1. System Clock Frequency for Common Audio Sampling Frequencies

SAMPLING FREQUENCY, LRCK	SYSTEM CLOCK FREQUENCY, SCKI (MHz)			
	$128f_S$	$192f_S$	$256f_S$	$384f_S$
48 kHz	6.144	9.216	12.288	18.432
44.1 kHz	5.6448	8.4672	11.2896	16.9344
32 kHz	4.096	6.144	8.192	12.288
24 kHz	3.072	4.608	6.144	9.216
22.05 kHz	2.8224	4.2336	5.6448	8.4672
16 kHz	2.048	3.072	4.096	6.144
12 kHz	1.536	2.304	3.072	4.608
11.025 kHz	1.4112	2.1168	2.8224	4.2336
8 kHz	1.024	1.536	2.048	3.072



† 1/128 f_S, 1/192 f_S, 1/256 f_S, and 1/384 f_S.

PARAMETERS	SYMBOL	MIN	UNIT
System clock pulse width high	$t_{(SCKH)}$	7	ns
System clock pulse width low	$t_{(SCKL)}$	7	ns

Figure 19. System Clock Timing

POWER ON/OFF RESET

Setting terminal 4 ($\overline{PD}$) to high must be performed once after power on. The internal logic state is kept in reset when $\overline{PD}$ is low and during the 1024 system clock count after $\overline{PD}$ is high. Then the power-on sequence is started. In this sequence, terminals 9 ($V_{OUT}L$) and 8 ($V_{OUT}R$) increase gradually from ground level and output corresponding input data after 9334/f_S. When power is off, the $\overline{PD}$ terminal is reset to low first. Then $V_{OUT}L$ and $V_{OUT}R$ gradually decrease to ground level. In order not to generate pop noise when power is switched on or off, the power-on and power-off sequences shown in Figure 20 and Figure 21 are recommended. Any other power-on or power-off sequence may generate pop noise.

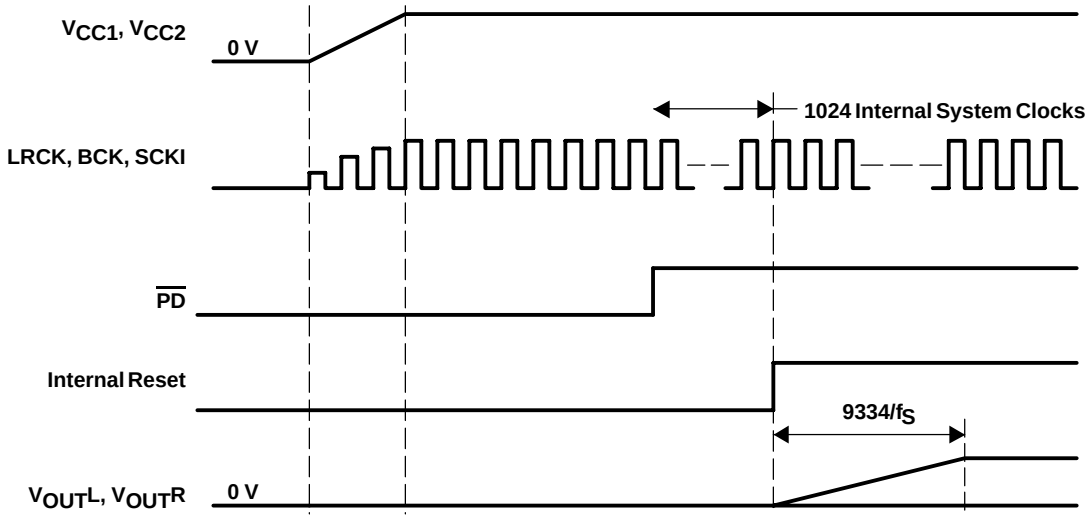


Figure 20. Power-On Sequence

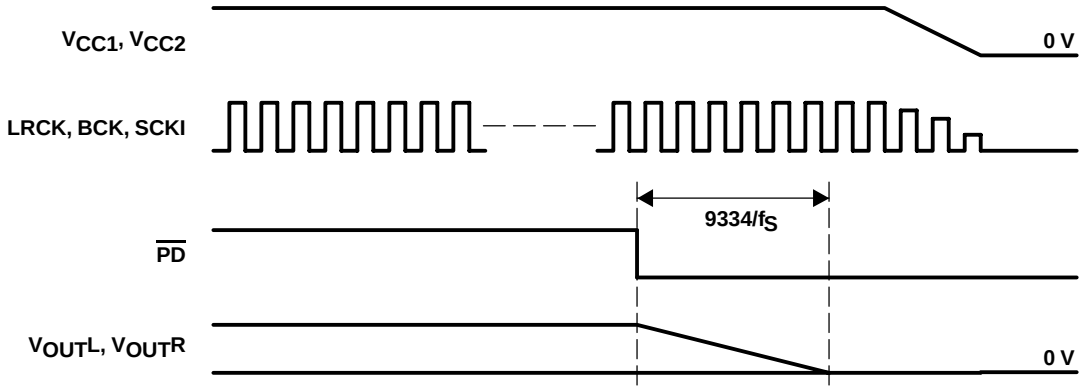


Figure 21. Power-Off Sequence

POWER-UP/-DOWN SEQUENCE AND RESET

The PCM1772 device has two kinds of power-up/-down methods: the $\overline{PD}$ terminal through hardware control and PWRD (register 4, B0) through software control. The PCM1773 device has only the $\overline{PD}$ terminal through hardware control for the power-up/-down sequence. The power-up or power-down sequence operates the same as the power-on or power-off sequence. When powering up or down using the $\overline{PD}$ terminal, all digital circuits are reset. When powering up or down using PWRD, all digital circuits are reset except for maintaining the logic states of the registers. Figure 22 shows the power-up/power-down sequence.

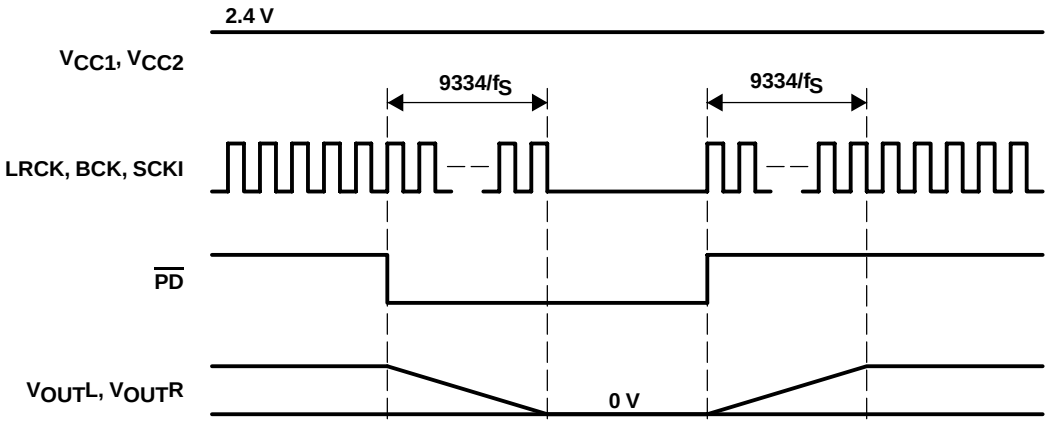


Figure 22. Power-Down and Power-Up Sequences

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1772 and PCM1773 devices is comprised of a 3-wire synchronous serial port. It includes terminals 1 (LRCK), 2 (DATA), and 3 (BCK). BCK is the serial audio bit clock, and it clocks the serial data present on DATA into the audio interface serial shift register. Serial data is clocked into the PCM1772 and PCM1773 devices on the rising edge of BCK. LRCK is the serial audio left/right word clock. It latches serial data into the serial audio interface internal registers.

Both LRCK and BCK of the PCM1772 device support the slave and master modes which are set by FMT (register 3). LRCK and BCK are outputs during the master mode and inputs during the slave mode.

In slave mode, BCK and LRCK are synchronous to the audio system clock, SCKI. Ideally, it is recommended that LRCK and BCK be derived from SCKI. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, and 64 times the sampling frequency.

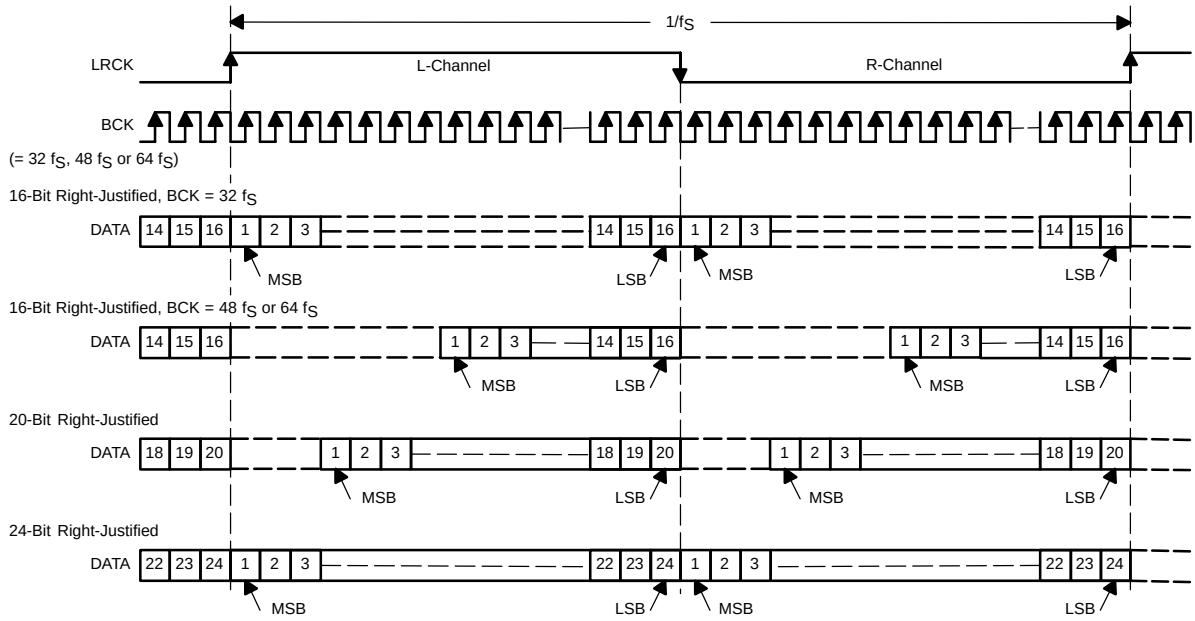
In master mode, BCK and LRCK are derived from the system clock and these terminals are outputs. The BCK and LRCK are synchronous to SCKI. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 64 times the sampling frequency.

The PCM1772 and PCM1773 devices operate under LRCK synchronized with the system clock. The PCM1772 and PCM1773 devices do not need a specific phase relationship between LRCK and the system clock, but do require the synchronization of LRCK and the system clock. If the relationship between the system clock and LRCK changes more than ±3BCK during one sample period, internal operation of the PCM1772 and PCM1773 devices halt within $1/f_S$, and the analog output is kept in last data until resynchronization between system clock and LRCK is completed.

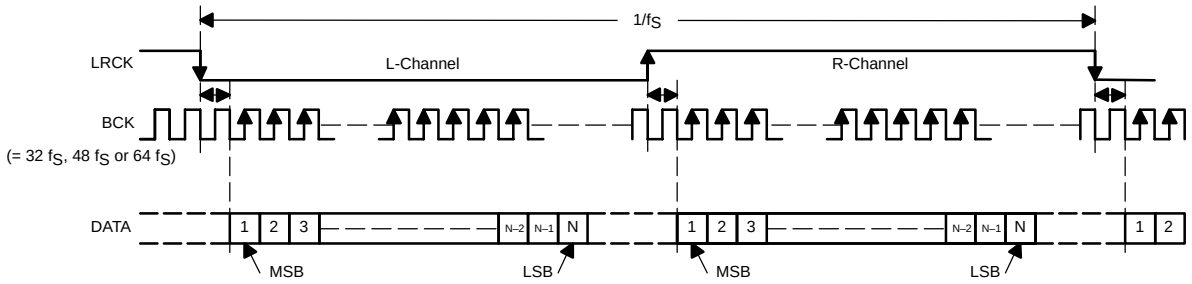
AUDIO DATA FORMATS AND TIMING

The PCM1772 device supports industry-standard audio data formats, including standard, I2S, and left justified. The PCM1773 device supports the I2S and left-justified data formats. Figure 23 shows the data formats. Data formats are selected using the format bits, FMT[2:0] of control register 3 in case of the PCM1772 device, and are selected using the FMT terminal in case of the PCM1773 device. The default data format is 24-bit, left-justified, slave mode. All formats require binary twos complement, MSB-first audio data. Figure 24 shows a detailed timing diagram for the serial audio interface in slave mode. Figure 25 shows a detailed timing diagram for the serial audio interface in master mode.

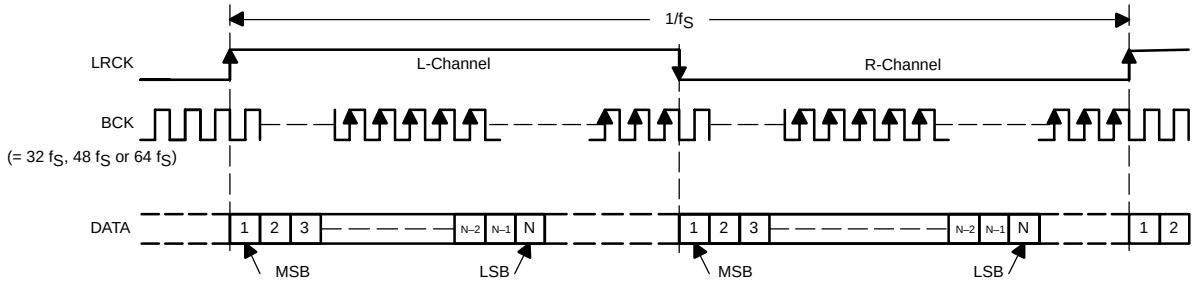
(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW (Slave Mode)



(2) I2S Data Format; L-Channel = LOW, R-Channel = HIGH (Slave Mode)



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (Slave Mode)



(4) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (Master Mode)
(The frequency of BCK is 64 f_S and SCKI is 256 f_S only)

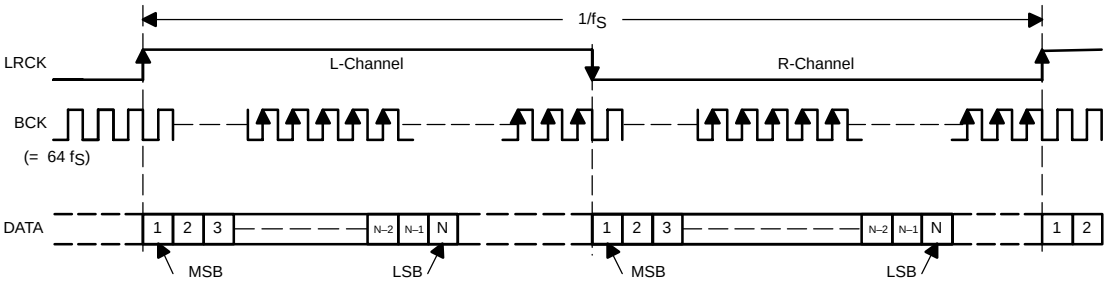
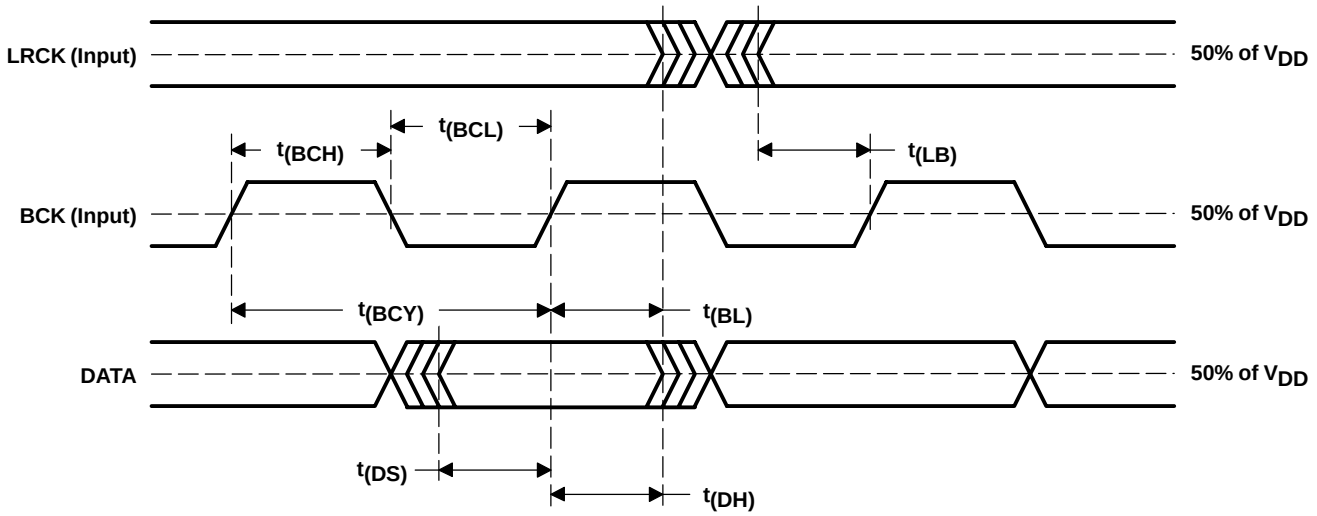


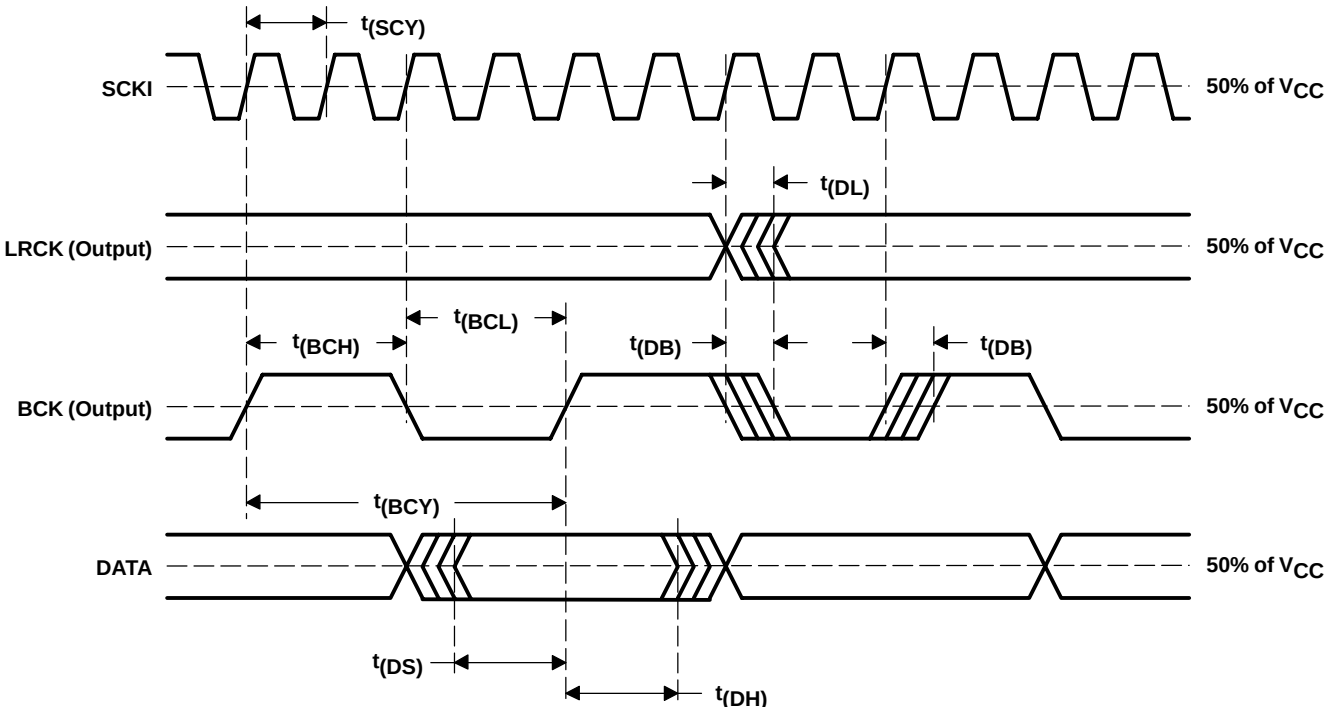
Figure 23. Audio Data Input Formats



PARAMETERS	SYMBOL	MIN	MAX	UNIT
BCK pulse cycle time	$t_{(BCY)}$		$32f_S/48f_S/64f_S$(1)	
BCK high-level time	$t_{(BCH)}$	35		ns
BCK low-level time	$t_{(BCL)}$	35		ns
BCK rising edge to LRCK edge	$t_{(BL)}$	10		ns
LRCK edge to BCK rising edge	$t_{(LB)}$	10		ns
DATA setup time	$t_{(DS)}$	10		ns
DATA hold time	$t_{(DH)}$	10		ns

(1) f_S is the sampling frequency.

Figure 24. Audio Interface Timing (Slave Mode)



PARAMETERS	SYMBOL	MIN	MAX	UNIT
SCKI pulse cycle time	$t_{(SCY)}$		256f_S only (1)	
LRCK edge from SCKI rising edge	$t_{(DL)}$	0	40	ns
BCK edge from SCKI rising edge	$t_{(DB)}$	0	40	ns
BCK pulse cycle time	$t_{(BCY)}$		64f_S only (1)	
BCK high-level time	$t_{(BCH)}$	146		ns
BCK low-level time	$t_{(BCL)}$	146		ns
DATA setup time	$t_{(DS)}$	10		ns
DATA hold time	$t_{(DH)}$	10		ns

(1) f_S is up to 48 kHz. f_S is the sampling frequency.

Figure 25. Audio Interface Timing (Master Mode)

HARDWARE CONTROL (PCM1773)

The digital functions of the PCM1773 device are capable of hardware control. Table 2 shows selectable formats, Table 3 shows de-emphasis control, and Table 4 shows analog mixing control.

Table 2. Data Format Select

FMT	DATA FORMAT
Low	16- to 24-bit, left-justified format
High	16- to 24-bit, I2S format

Table 3. De-Emphasis Control

DEMP	DE-EMPHASIS FUNCTION
Low	44.1-kHz de-emphasis OFF
High	44.1-kHz de-emphasis ON

Table 4. Analog Mixing Control

AMIX	ANALOG MIXING
Low	Analog mixing OFF
High	Analog mixing ON

SOFTWARE CONTROL (PCM1772)

The PCM1772 device has many programmable functions that can be controlled in the software control mode. The functions are controlled by programming the internal registers using $\overline{MS}$, MC, and MD.

The software control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is utilized to program the on-chip mode registers. MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. $\overline{MS}$ is the mode control port select signal.

REGISTER WRITE OPERATION (PCM1772)

All write operations for the serial control port use 16-bit data words. Figure 26 shows the control data word format. The most significant bit must be 0. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the write operation. The eight least significant bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 27 shows the functional timing diagram for writing to the serial control port. To write data into the mode register, data is clocked into an internal shift register on the rising edge of the MC clock. Serial data can change on the falling edge of the clock and must be stable on the rising edge of the clock. The $\overline{MS}$ signal must be low during the write mode and the rising edge of the $\overline{MS}$ signal must be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. The MC clock can run continuously between transactions while the $\overline{MS}$ signal is low.

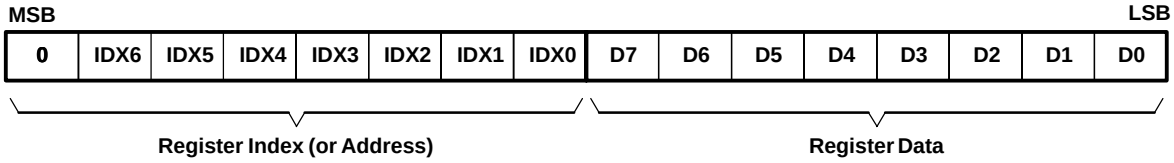


Figure 26. Control Data Word Format for MD

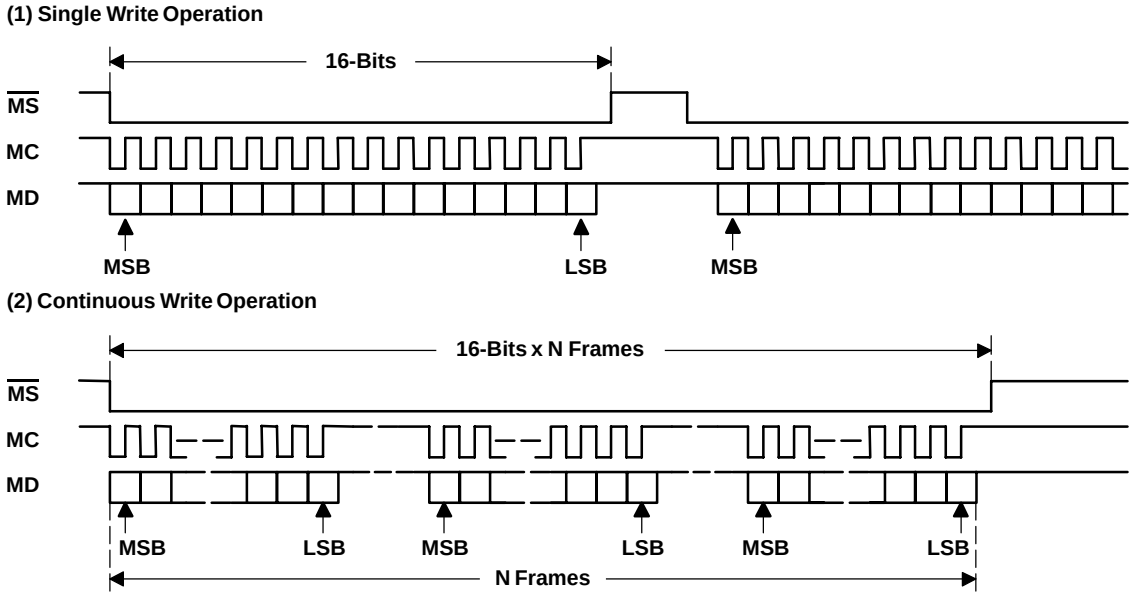
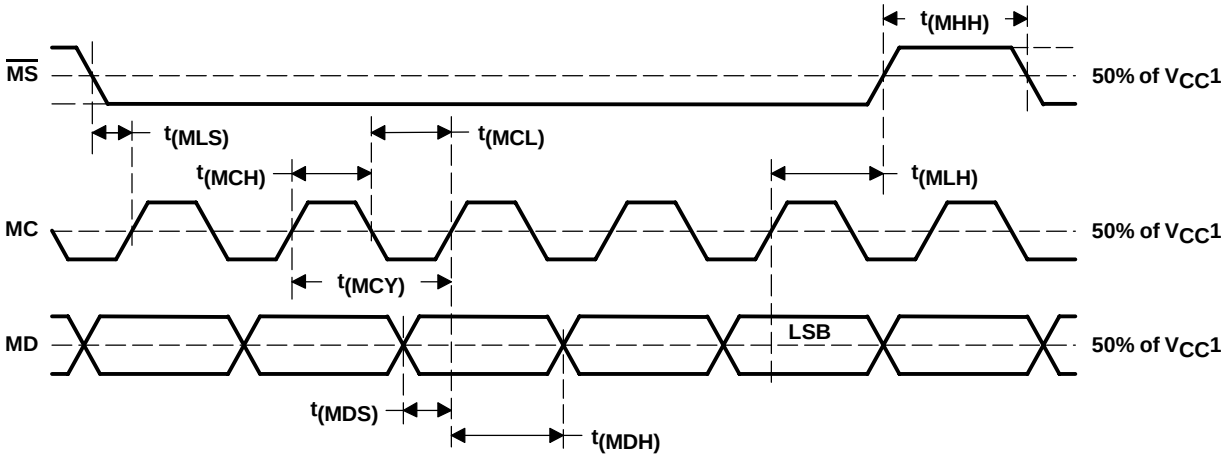


Figure 27. Register Write Operation

CONTROL INTERFACE TIMING REQUIREMENTS (PCM1772)

Figure 28 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
MC pulse cycle time	$t_{(MCY)}$	100(1)			ns
MC low-level time	$t_{(MCL)}$	50			ns
MC high-level time	$t_{(MCH)}$	50			ns
$\overline{MS}$ high-level time	$t_{(MHH)}$	(2)			ns
$\overline{MS}$ falling edge to MC rising edge	$t_{(MLS)}$	20			ns
$\overline{MS}$ hold time	$t_{(MLH)}$	20			ns
MD hold time	$t_{(MDH)}$	15			ns
MD setup time	$t_{(MDS)}$	20			ns

(1) When MC runs continuously between transactions, MC pulse cycle time is specified as $3/(128f_S)$, where f_S is sampling rate.
(2) $3/(128f_S)$ s (min), where f_S is sampling rate

Figure 28. Control Interface Timing

MODE CONTROL REGISTERS (PCM1772)

User-Programmable Mode Controls

The PCM1772 device has a number of user- programmable functions that can be accessed via mode control registers. The registers are programmed using the serial control interface. Table 5 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

Table 6 shows the mode control register map. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 5. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER NO.	BIT(S)
Soft mute control, L/R independently	Disabled	01	MUTL, MUTR
Digital attenuation level setting, 0 dB to –62 dB in 1.0-dB steps, L/R independently	0 dB	01, 02	ATL[5:0], ATR[5:0]
Oversampling rate control ($128f_S$, $192f_S$, $256f_S$, $384f_S$)	$128f_S$ oversampling	03	OVER
Polarity control for analog output for R-channel DAC	Not inverted	03	RINV
Analog mixing control for analog in, AIN (terminal 14)	Disabled	03	AMIX
44.1-kHz de-emphasis control	Disabled	03	DEM
Audio data format select	24-bit, left-justified format	03	FMT[2:0]
Zero cross attenuation	Disabled	04	ZCAT
Power down control	Disabled	04	PWRD

Table 6. Mode Control Register Map

REGISTER	IDX [6:0] (B14–B8)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 01	01h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MUTR	MUTL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 02	02h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 03	03h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV	RINV	AMIX	DEM	FMT2	FMT1	FMT0
Register 04	04h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	ZCAT	RSV	RSV	RSV	PWRD

NOTE: RSV: Reserved for test operation. It must be set to 0 during regular operation.

Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 01	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MUTL	MUTR	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0

IDX[6:0]: 0000 0001b

MUTx: Soft Mute Control

Where, x = L or R, corresponding to the line output $V_{OUT}L$ and $V_{OUT}R$.

Default Value: 0

MUTL, MUTR = 0	Mute disabled (default)
MUTL, MUTR = 1	Mute enabled

The mute bits, MUTL and MUTR, enable or disable the soft mute function for the corresponding line outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output are decreased from the current setting to the infinite attenuation, one attenuator step (1.0 dB) at a time. This provides pop-free muting of the line output.

By setting MUTx = 0, the attenuator is increased one step at a time to the previously programmed attenuation level.

ATL[5:0]: Digital Attenuation Level Setting for Line Output, $V_{OUT}L$

Default value: 11 1111b

Line output, $V_{OUT}L$ includes a digital attenuation function. The attenuation level can be set from 0 dB to –62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every $8/f_S$ time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level may be set to infinite attenuation (or mute).

Table 7 shows attenuation levels for various settings:

Table 7. Attenuation Level Setting

ATL[5:0]	ATTENUATION LEVEL SETTING
11 1111b	0 dB, no attenuation (default)
11 1110b	–1 dB
11 1101b	–2 dB
:	:
00 0010b	–61 dB
00 0001b	–62 dB
00 0000b	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 02	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

IDX[6:0]: 0000 0010b

ATL[5:0]: Digital Attenuation Level Setting for Line Output, $V_{OUT}R$

Default Value: 11 1111b

Line output, $V_{OUT}R$ includes a digital attenuation function. The attenuation level can be set from 0 dB to –62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every $8/f_S$ time internal until the programmed attenuator setting in reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

To set the attenuation levels for ATR[5:0], refer to the table above in ATL[5:0].

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 03	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RINV	AMIX	DEM	FMT2	FMT1	FMT0

IDX[6:0]: 0000 0011b

OVER: Over Sampling Control

Default Value: 0

OVER = 0	$128f_S$ oversampling
OVER = 1	$192f_S$, $256f_S$, $384f_S$ oversampling

The OVER bit controls the oversampling rate of the Δ-Σ D/A converters. When it operates at a low sampling rate, less than 24 kHz, this function is recommended.

RINV: Polarity Control for Line Output, $V_{OUT}R$

Default Value: 0

RINV = 0	Not inverted
RINV = 1	Inverted output

The RINV bits allow the user to control the polarity of the line output, $V_{OUT}R$. This function can be used to connect the monaural speaker with BTL connection method. This bit is recommended to be 0 during the power-up/-down sequence for minimizing audible pop noise.

AMIX: Analog Mixing Control for External Analog Signal, AIN

Default Value: 0

AMIX = 0	Disabled (not mixed)
AMIX = 1	Enabled (mixing to the DAC output)

AMIX bit allows the user to mix analog input (AIN) with line outputs ($V_{OUT}L$/$V_{OUT}R$) internally.

DEM: 44.1-kHz De-Emphasis Control

Default Value: 0

DEM = 0	Disabled
DEM = 1	Enabled

The DEM bit enables or disables the digital de-emphasis filter for 44.1-kHz sampling rate.

FMT[2:0]: Audio Interface Data Format

Default Value: 000

The FMT[2:0] bits select the data format for the serial audio interface. Table 8 shows the available format options.

Table 8. Audio Data Format Selection

FMT[2:0]	Audio Data Format Selection
000	16- to 24-bit, left-justified format (default)
001	16- to 24-bit, I2S format
010	24-bit right-justified data
011	20-bit right-justified data
100	16-bit right-justified data
101	16- to 24-bit, left-justified format, master mode
110	Reserved
111	Reserved

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 04	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	ZCAT	RSV	RSV	RSV	PWRD

IDX[6:0]: 0000 0100b

ZCAT: Zero Cross Attenuation

Default Value: 0

ZCAT = 0	Normal attenuation (default)
ZCAT = 1	Zero cross attenuation

This bit enables to change signal level on zero crossing during attenuation control or muting. If the signal does not cross BPZ beyond $512/f_S$ (11.6 ms at 44.1-kHz sampling rate), the signal level is changed similar to normal attenuation control. This function is independently monitored for each channel; moreover, change of signal level is alternated between both channels. Figure 29 shows an example of zero cross attenuation.

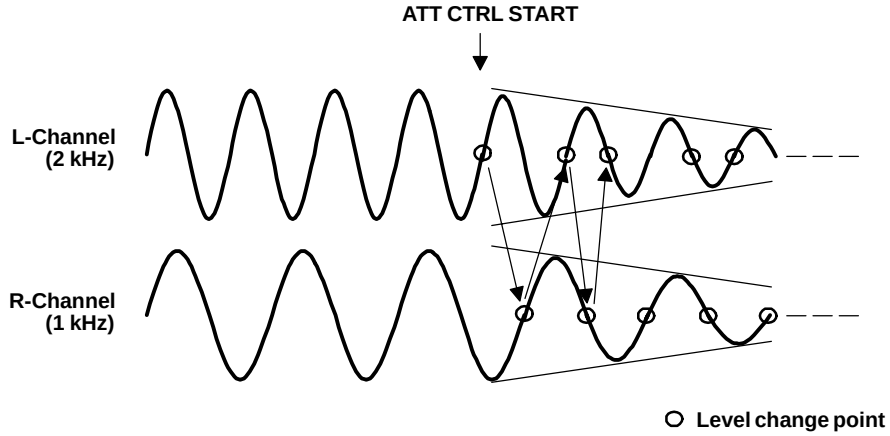


Figure 29. Example of Zero Cross Attenuation

PWRD: Power Down Control

Default Value: 0

PWRD = 0	Normal operation (default)
PWRD = 1	Power-down state

This bit is used to enter into low-power mode. Note that PWRD has no reset function.

When this bit is set to 1, the PCM1772 device enters low-power mode and all digital circuits are reset except the register states which remain unchanged.

ANALOG IN/OUT

LINE OUTPUT (STEREO)

The PCM1772 and PCM1773 devices have two independent lineout amplifiers and each amplifier output is provided at the $V_{OUT}L$ and $V_{OUT}R$ terminals. The capability of line output is designed for driving a 10-kΩ minimum load.

Monaural Output (BTL Mode/Monaural Speaker)

When the user needs monaural output, the PCM1772 device can provide it. The PCM1772 device has RINV bit on control register 03. Since this bit allows the user to invert the polarity of the line output for the right channel, the user can create a monaural output by summing the line output for left and right channels through the external power amplifier or headphone amplifier. The RINV bit is recommended to be 0 during power-up/-down sequence for minimizing audible pop noise.

Analog Input

The PCM1772 and PCM1773 devices have an analog input, AIN (terminal 10). The AMIX bit (PCM1772) or the AMIX terminal (PCM1773) allows the user to mix AIN with the line outputs ($V_{OUT}L$ and $V_{OUT}R$) internally. When in MIXING mode, an ac-coupling capacitor is needed for AIN. But if AIN is not used, AIN must be open and the AMIX bit (PCM1772) must be disabled or the AMIX terminal (PCM1773) must be low.

Since AIN does not have an internal low-pass filter, it is recommended that the bandwidth of input signal into AIN is limited less than 100 kHz. The source of signals connected to AIN must be connected by low impedance.

Although the maximum input voltage on AIN is designed to be as large as $0.584V_{CC2}$ [peak-to-peak], the user must attenuate the input voltage on AIN and control digital input data so that each line output ($V_{OUT}L$ and $V_{OUT}R$) does not exceed $0.75V_{CC2}$ [peak-to-peak] during mixing mode.

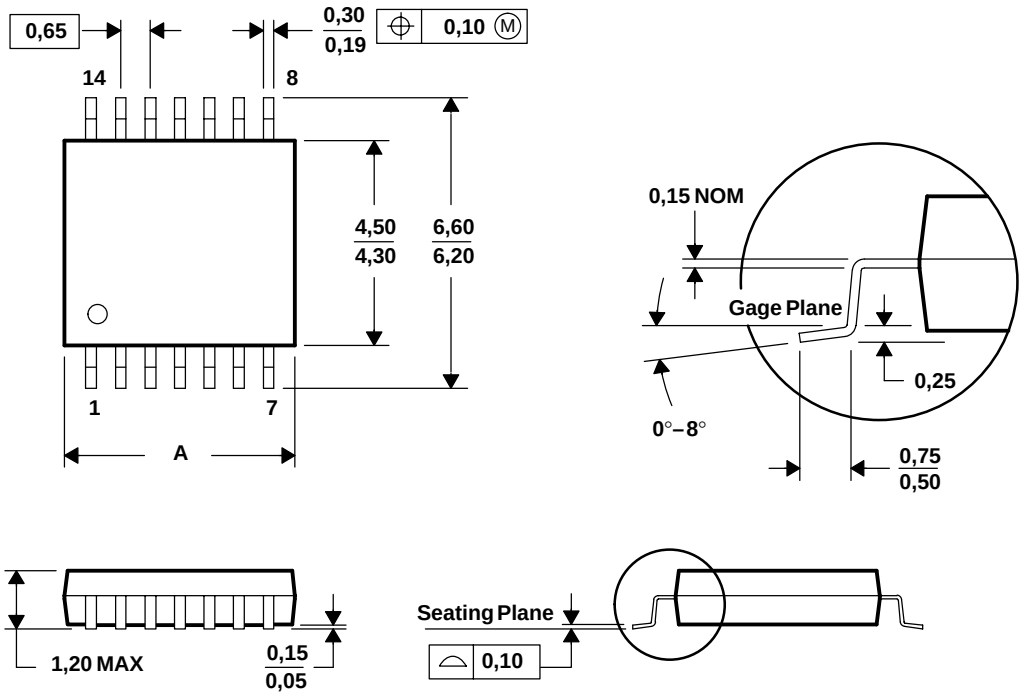
V_{COM} Output

One unbuffered common-mode voltage output terminal, V_{COM} is brought out for decoupling purposes. This terminal is nominally biased to a dc voltage level equal to $0.5V_{CC2}$ and connected to a 10-μF capacitor. In the case of a capacitor smaller than 10 μF, pop noise can be generated during the power-on/-off or power-up/-down sequences.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

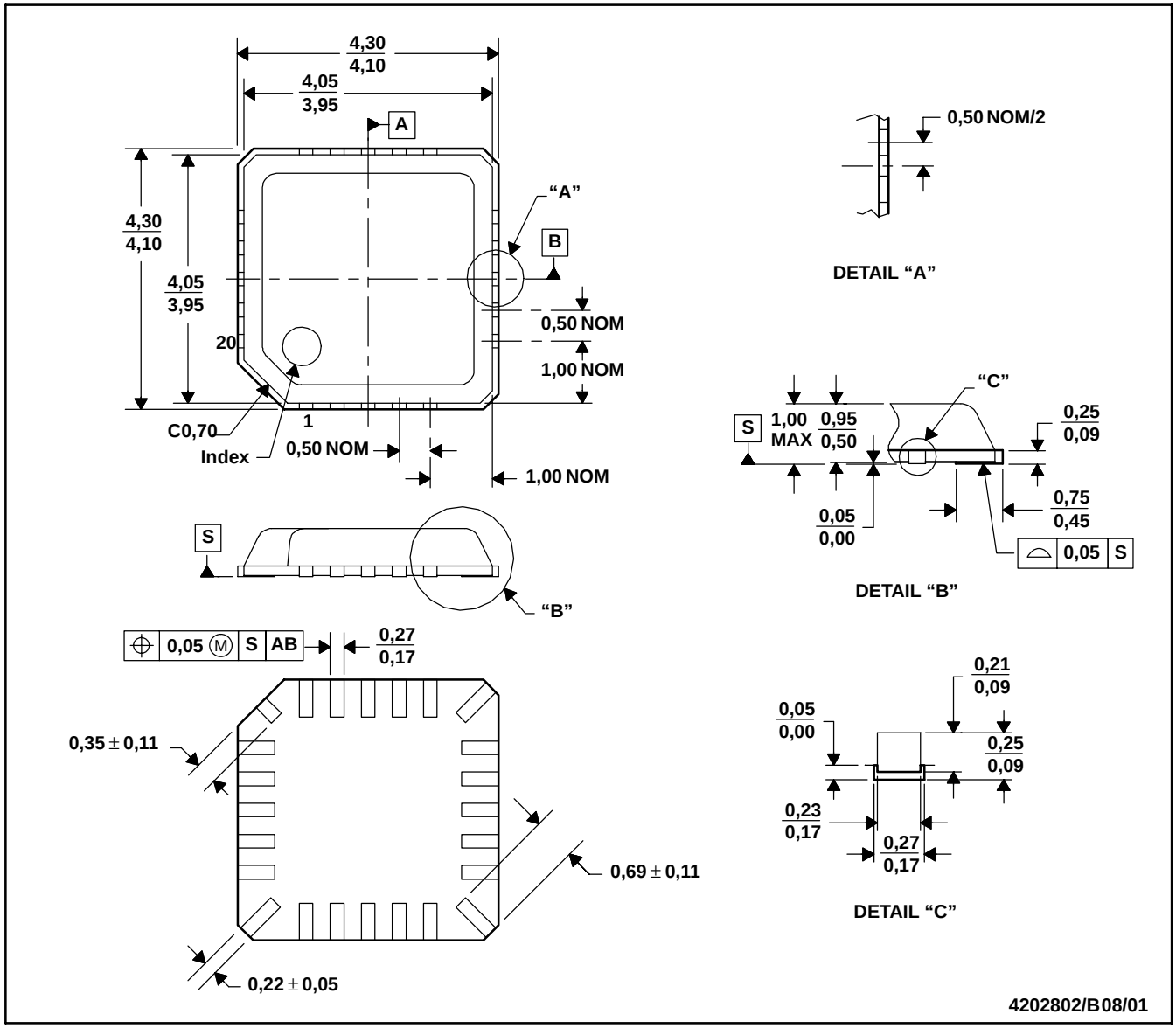


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F01/97

NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

RGA (S-PQFP-N20) PLASTIC QUAD FLATPACK



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. These dimensions include package bend.
D. Falls within EIAJ: EDR-7324.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265