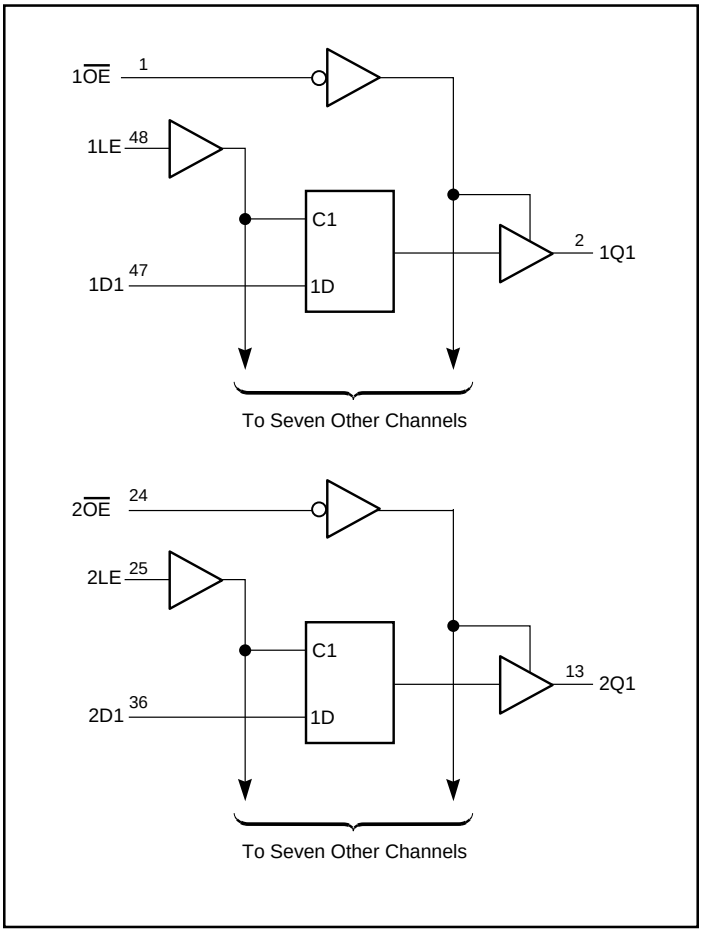
2.5V 16-Bit Transparent D-Type Latch with 3-State Outputs

Product Features

- PI74AVC+16373 is designed for low-voltage operation, V_{CC} = 1.65V to 3.6V
- True ±24mA Balanced Drive @ 3.3V
- Compatible with Philips and T.I. AVC Logic family
- I_{OFF} supports partial power-down operation
- 3.6V I/O Tolerant inputs and outputs
- All outputs contain a patented DDC (Dynamic DriveControl) circuit that reduces noise without degrading propagation delay.
- Industrial operation: –40°C to +85°C
- Available Packages:
  – 48-pin 240-mil wide plastic TSSOP
  – 48-pin 173-mil wide plastic TVSOP

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16373 is particularly suited for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the Latch Enable (LE) input is HIGH, the Q outputs follow the (D) inputs. When LE is taken LOW, the Q outputs are latched at the levels set up at the D inputs.

A buffered Output Enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state in which the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

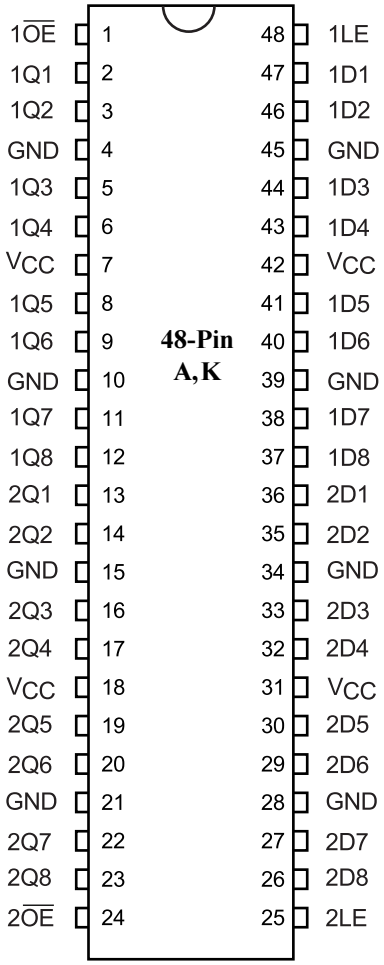
Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC} ..... –0.5V to +4.6V
Input voltage range, V_I ..... –0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, V_O[1] ..... –0.5V to +4.6V
Voltage range applied to any output in the high or low state, V_O[1,2] ..... –0.5V to V_{CC} +0.5V
Input clamp current, I_{IK} (V_I <0) ..... –50mA
Output clamp current, I_{OK} (V_O <0) ..... –50mA
Continuous output current, I_O ..... ±50mA
Continuous current through each V_{CC} or GND ..... ±100mA
Package thermal impedance, θ_{JA}[3]: package A ..... 64°C/W
package K ..... 48°C/W
Storage Temperature range, T_{stg} ..... –65°C to 150°C

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. Input & output negative-voltage ratings may be exceeded if the input and output curent rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD51.

Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
LE	Latch Enable (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
V_{CC}	Power

Truth Table[1]

Inputs			Outputs
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Notes:
1. H = High Signal Level
L = Low Signal Level
X = Don't Care or Irrelevant
Z = High Impedance

Recommended Operating Conditions(1)

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.4	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	V_{CC} = 1.2V	V_{CC}		
	V_{CC} = 1.4V to 1.6V	0.65 x V_{CC}		
	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
	V_{CC} = 2.3V to 2.7V	1.7		
	V_{CC} = 3V to 3.6V	2		
V_{IL} Low-level Input Voltage	V_{CC} = 1.2V		GND	
	V_{CC} = 1.4V to 1.6V		0.35 x V_{CC}	
	V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
	V_{CC} = 2.3V to 2.7V		0.7	
	V_{CC} = 3V to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OHS} High-level output current	V_{CC} = 1.4V to 1.6V		– 4	mA
	V_{CC} = 1.65V to 1.95V		– 6	
	V_{CC} = 2.3V to 2.7V		– 12	
	V_{CC} = 3V to 3.6V		– 24	
I_{OLS} Low-level output current	V_{CC} = 1.4V to 1.6V		4	
	V_{CC} = 1.65V to 1.95V		6	
	V_{CC} = 2.3V to 2.7V		12	
	V_{CC} = 3V to 3.6V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate	V_{CC} = 1.4V to 3.6V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Notes:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C +85°C)

Parameters		Test Conditions[1]	V_{CC}	Min.	Typ.	Max.	Units
V_{OH}		I_{OH} = –100µA	1.4V to 3.6V	V_{CC} –0.2V			V
		I_{OHS} = –4mA V_{IH} = 0.91V	1.4V	1.05			
		I_{OHS} = –6mA V_{IH} = 1.07V	1.65V	1.2			
		I_{OHS} = –12mA V_{IH} = 1.7V	2.3V	1.75			
		I_{OHS} = –24mA V_{IH} = 2V	3V	2.0			
V_{OL}		I_{OLS} = 100µA	1.4V to 3.6V			0.2	
		I_{OLS} = 4mA V_{IL} = 0.49V	1.4V			0.4	
		I_{OLS} = 6mA V_{IL} = 0.57V	1.65V			0.45	
		I_{OLS} = 12mA V_{IL} = 0.7V	2.3V			0.55	
		I_{OLS} = 24mA V_{IL} = 0.8V	3V			0.8	
I_I	Control Inputs	V_I = V_{CC} or GND	3.6V			±2.5	µA
I_{OFF}		V_I or V_O = 3.6V	0			±10	
I_{OZ}		V_O = V_{CC} or GND	3.6V			±10	
I_{CC}		V_I = V_{CC} or GND I_O = 0	3.6V			40	
C_I	Control Inputs	V_I = V_{CC} or GND	2.5V		3.5		pF
			3.3V		3.5		
	Data Inputs		2.5V		6		
			3.3V		6		
C_O	Outputs	V_O = V_{CC} or GND	2.5V		6.5		
			3.3V		6.5		

Note:
1. Typical values are measured at T_A = 25°C.

Timing requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

	V_{CC} = 1.2V		V_{CC} = 1.5V ± 0.1V		V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_w Pulse duration, LE HIGH					2.2		2		1.8		ns
t_{su} Setup time, data before LE↓	1.7		1.2		1.1		0.9		0.8		
t_h Hold time, data after LE↓	2		1.1		1.1		1.1		1		

Switching Characteristics

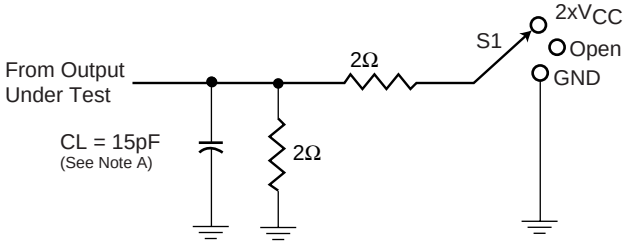
(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

Parameters	From (Input)	To (Output)	V_{CC} = 1.2V	V_{CC} = 1.5V ± 0.1V		V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Units
			Typ.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{pd}	D	Q	5.8	1.2	6.8	1	5.7	0.8	3.3	0.7	2.8	ns
	LE		7.2	1.4	8.3	1.1	6.6	0.8	4	0.7	3.2	
t_{en}	$\overline{OE}$	Q	7.4	1.6	8.8	1.6	6.7	1.4	4.3	0.7	3.4	
t_{dis}	$\overline{OE}$	Q	8.4	2.5	9.4	2.3	7.8	1.3	4.2	1.2	3.9	

Operating Characteristics, T_A=25°C

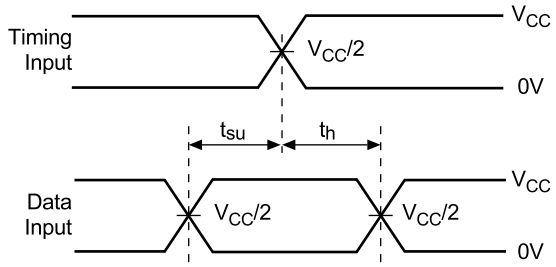
Parameters		Test Conditions	V_{CC} = 1.8V ±0.15V	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz	40	43	47	pF
	Outputs Disabled		20	22	24	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.2V and 1.5V ±0.1V

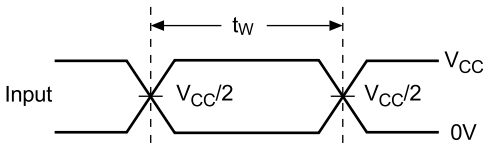


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

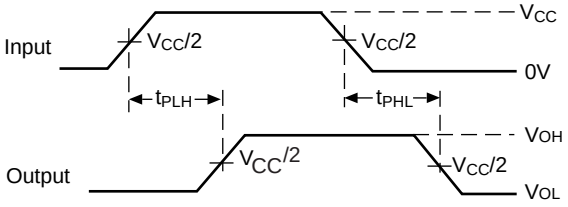
Load Circuit



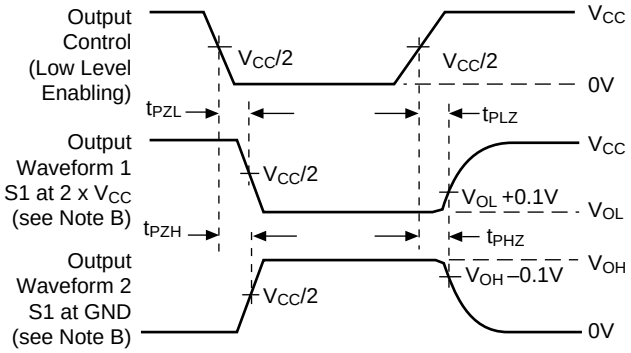
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



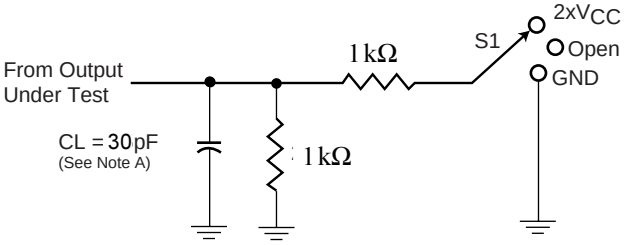
Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

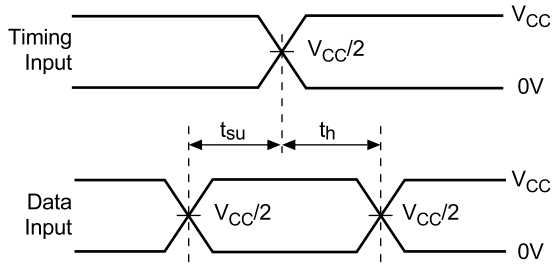
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8V ±0.15V

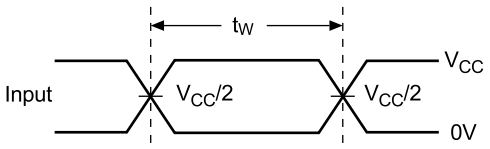


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

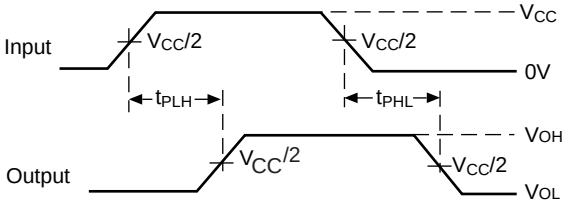
Load Circuit



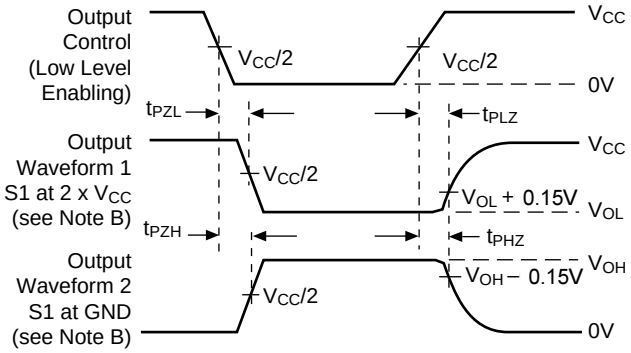
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



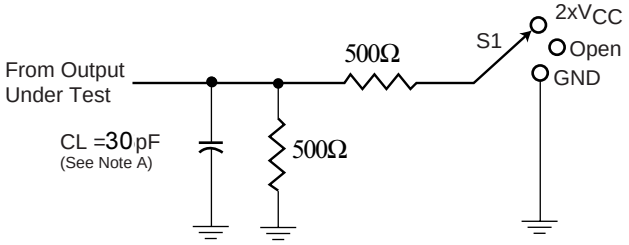
Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

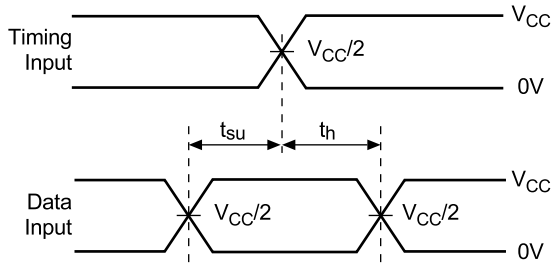
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

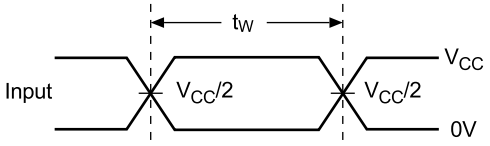


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

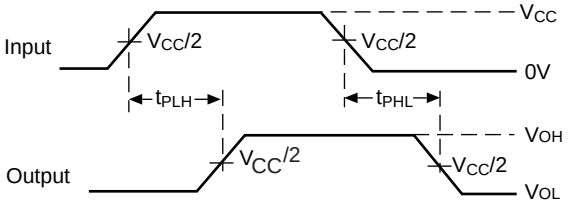
Load Circuit



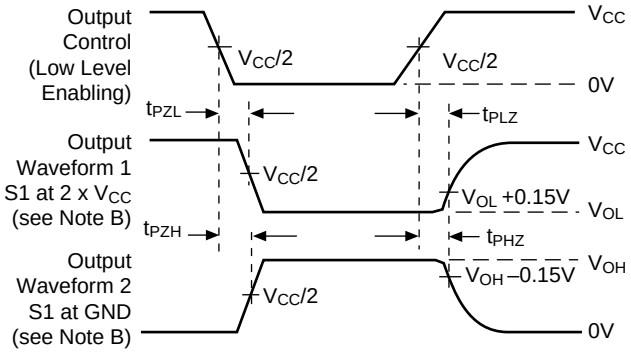
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



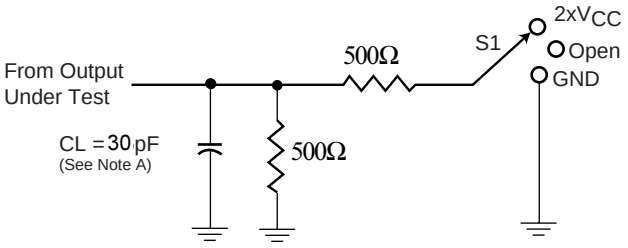
Voltage Waveforms
Enable and Disable Times

Figure 3. Load Circuit and Voltage Waveforms

Notes:

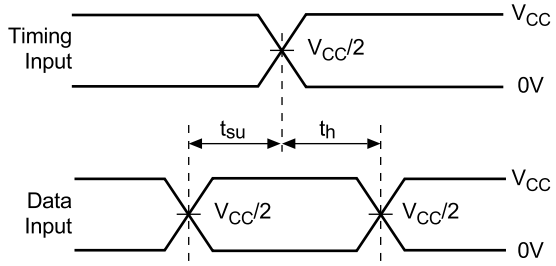
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3V ±0.3V

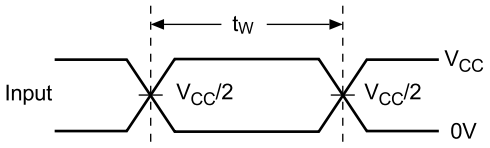


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

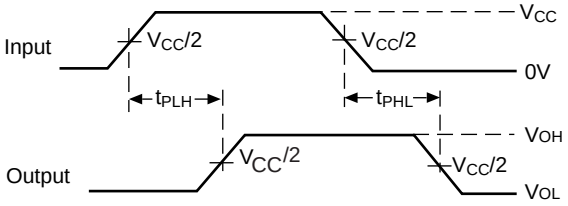
Load Circuit



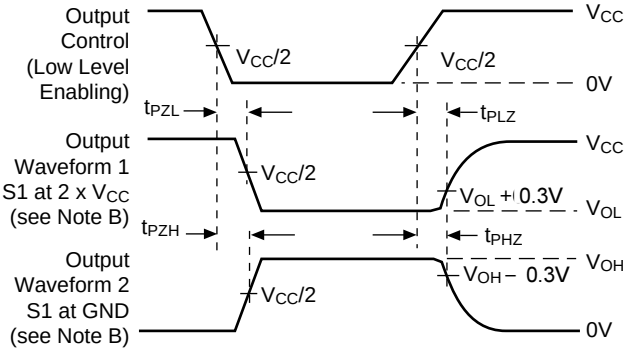
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
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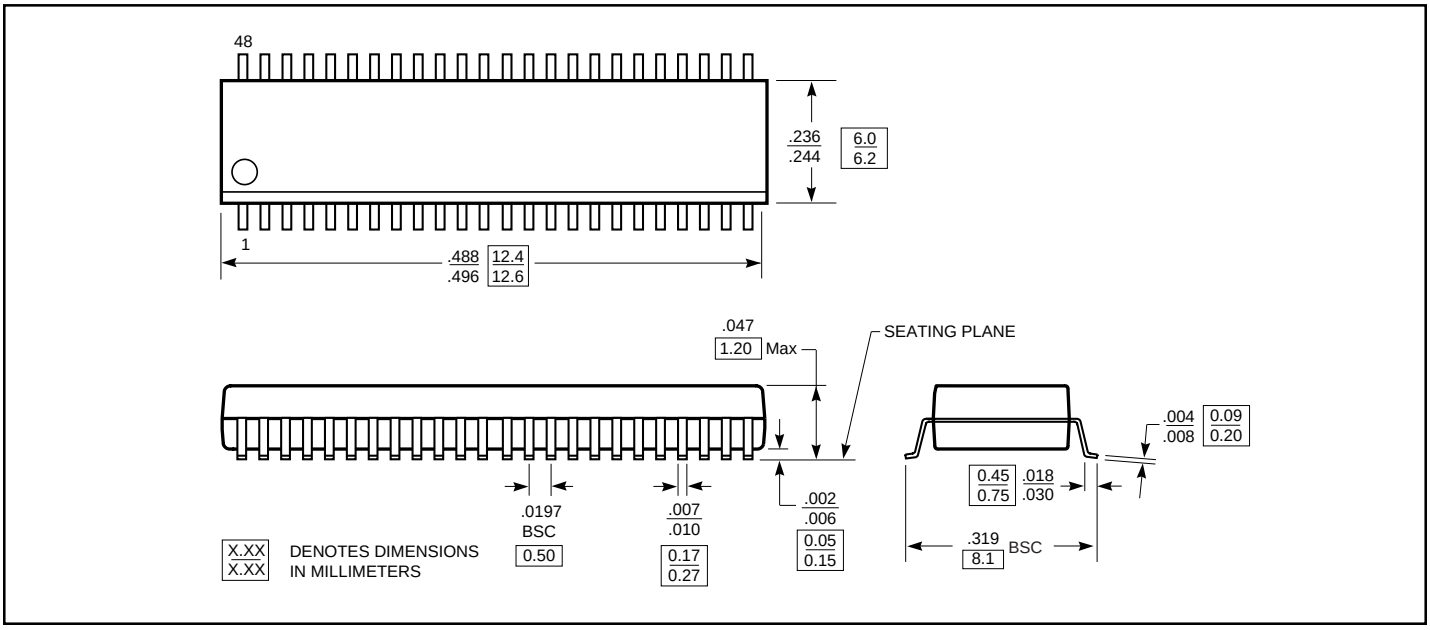
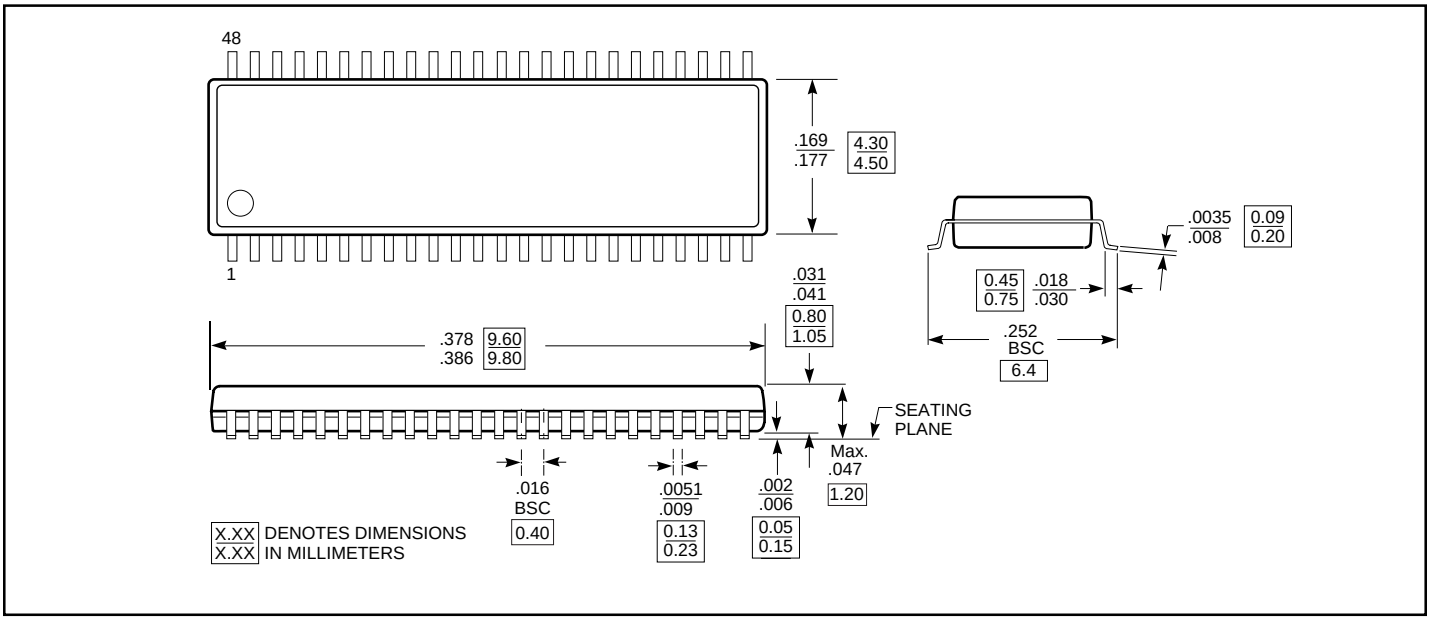
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

Packaging Mechanical - 48-pin TSSOP (A-package)



Packaging Mechanical - 48-pin TVSOP (TSSOP) (K-package)



Ordering Information

Ordering Code	Description
PI74AVC+16373A	48-pin, 240-mil wide plastic TSSOP
PI74AVC+16373K	48-pin, 173-mil wide plastic TVSOP