PERICOM

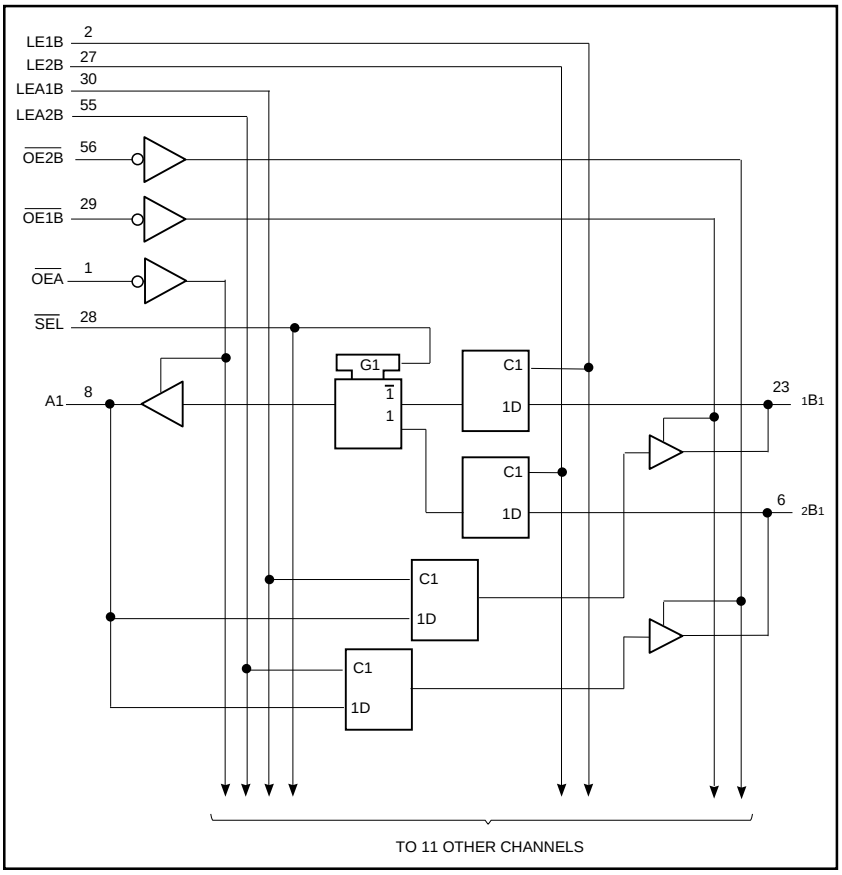
PI74ALVTC16268

2.5V 12-Bit to 24-Bit Registered Bus Exchanger with 3-State Outputs

Product Features

- PI74ALVTC16268 is designed for low voltage operation, V_{DD} = 1.65V to 3.6V
- Supports Live Insertion
- 3.6V I/O Tolerant Inputs and Outputs
- Bus Hold
- High Drive, –32/64mA @ 3.3V
- Uses patented noise reduction circuitry
- Power-off high impedance inputs and outputs
- Industrial operation at –40°C to +85°C
- Packages available:
  - 56-pin 240-mil wide plastic TSSOP (A56)
  - 56-pin 173-mil wide plastic TVSOP (K56)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74ALVTC series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The PI74ALVTC16268, 12-bit-to-24-bit registered bus exchanger, is designed for 1.65V to 3.6V V_{DD} operation. The device is used for applications in which data must be transferred from a narrow high-speed bus to a wide, lower frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock- enable (CLKEN) inputs are low. The select (SEL) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables (OEA, OEB). These control terminals are registered so bus direction changes are synchronous with CLK.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{DD} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver.

The family offers both I/O Tolerant, which allows it to operate in mixed 1.65/3.6V systems, and "Bus Hold," which retains the data input's last state preventing "floating" inputs and eliminating the need for pullup/down resistors.

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and OE should be tied to V_{DD} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver. Because OE is being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

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Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock
$\overline{SEL}$	Select (Active Low)
$\overline{CLKEN}$	Clock Enable (Active Low)
A,1B,2B	3-State Outputs
GND	Ground
V_{DD}	Power

Truth Tables(1)

Output Enable

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A to B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B0(2)	2B0(3)
L	X	↑	L	L(2)	X
L	X	↑	H	H(2)	X
X	L	↑	L	X	L
X	L	↑	H	X	H

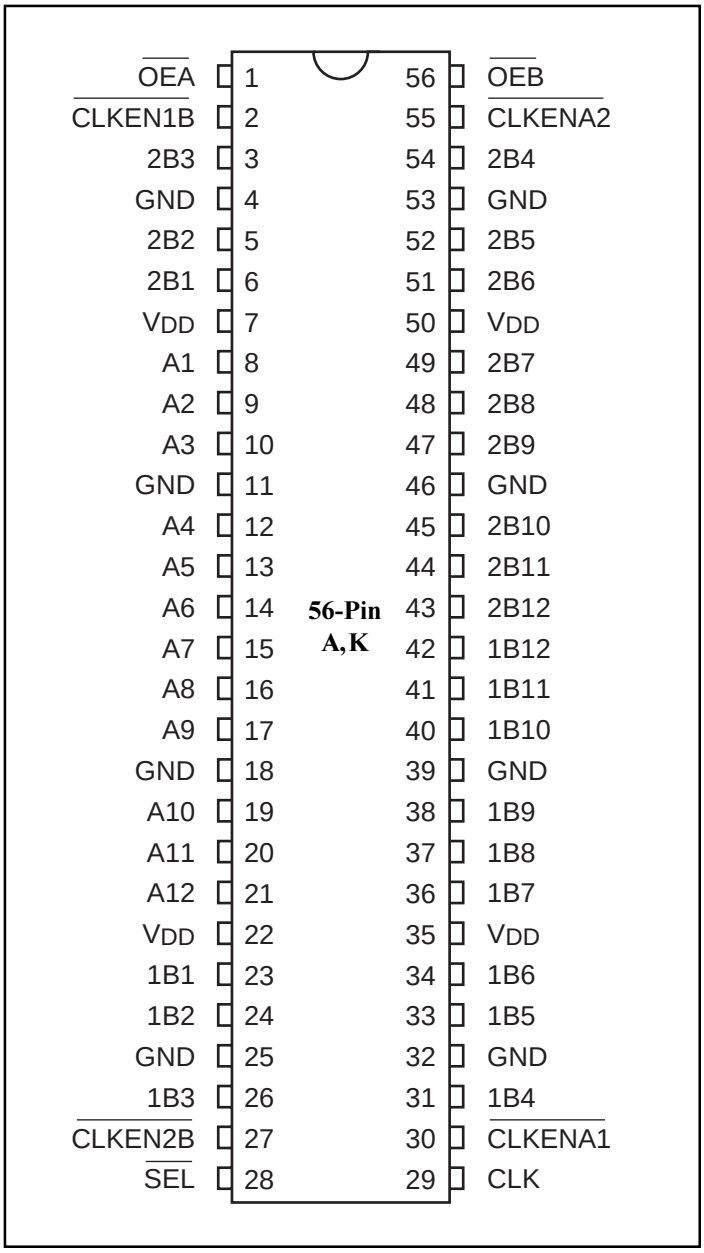
B to A STORAGE ($\overline{OEA}$ = L)

INPUTS						Outputs A
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	
H	X	X	H	X	X	A0(3)
X	H	X	L	X	X	A0(3)
L	L	↑	H	L	X	L
L	L	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

Notes:

1. H = High Signal Level, L = Low Signal Level, X = Irrelevant, Z = High Impedance, ↑ = Transition, Low to High
2. Two CLK edges are needed to propagate data
3. Output level before indicated steady state input conditions were established.

Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{DD} ..... –0.5V to 4.6V
Input Voltage Range, V_I ..... –0.5V to 4.6V
Output Voltage Range, V_O (3-Stated) ..... –0.5V to 4.6V
Output Voltage Range, V_O[1] (Active) ..... –0.5V to V_{DD} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0V ..... –50mA
DC Output Diode Current (I_{OK})
V_O < 0V ..... –50mA
V_O > V_{DD} ..... ±50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... –4/128mA
DC V_{DD} or GND Current per Supply Pin (I_{CC} or GND) ..... ±100mA
Storage Temperature Range, T_{stg} ..... –65°C to 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions[2]

			Min.	Max.	Units
V_{DD}	Supply voltage	Operating	1.65	3.6	V
		Data Retention Only	1.2	3.6	
V_{IH}	High-level input voltage	V_{DD} = 2.7V to 3.6V	2.0		
V_{IL}	Low-level input voltage	V_{DD} = 2.7V to 3.6V		0.8	
V_I	Input voltage		–0.3	3.6	
V_O	Output voltage	Active State	0	V_{DD}	
		Off State	0	3.6	
	Output current in I_{OH}/I_{OL}	V_{DD} = 3.0V to 3.6V V_{DD} = 3.0V to 3.6V V_{DD} = 2.3V to 2.7V V_{DD} = 1.65V to 1.95V		–32/64 ±24 ±18 ±6	mA
$\Delta t/\Delta v$	Input transistion rise or fall rate[3]		0	10	ns/V
T_A	Operating free-air temperature		–40	85	C

Notes:
1. Absolute maximum of I_O must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
3 As measured between 0.8V and 2.0V, V_{DD}=3.0V.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted)

DC Characteristics ($2.7V < V_{DD} \leq 3.6V$)

	Parameter	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	I_{IK} = –18mA	3.0			–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100µA	2.7 - 3.6	V_{DD} – 0.2			
		I_{OH} = –12mA	2.7	2.2			
		I_{OH} = –18mA	3.0	2.4			
		I_{OH} = –24mA		2.2			
		I_{OH} = –32mA		2.0			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.7 - 3.6			0.2	
		I_{OL} = 12mA	2.7			0.4	
		I_{OL} = 18mA	3.0			0.4	
		I_{OL} = 24mA				0.45	
		I_{OL} = 32mA				0.5	
		I_{OL} = 64mA				0.55	
I_I	Input Leakage Current	$V_I = V_{DD}$, or GND	3.6			±5.0	µA
I_{OZ}	3-State Output Leakage	V_O = 3.6V	2.7			±10	
I_{OFF}	Power-OFF Leakage Current	V_I or $V_O \leq$ 3.6V	0			10	
I_{HOLD}	Bus Hold Current A or B Outputs	V_I = 0.8V	3.0	75			
		V_I = 2.0V		–75			
		V_I = 0 to 3.6V	3.6			±500	
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.7 - 3.6			50	
		$V_{DD} \leq (V_I, V_O) \leq$ 3.6V				±50	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD}$ –0.6V, Other inputs at V_{DD} or Gnd				400	

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted; continued from previous page)

DC Characteristics ($2.3V \leq V_{DD} \leq 2.7V$)

Description	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	I_{IK} = –18mA	2.3			–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100µA	2.3 -2.7	V_{DD} – 0.2			
		I_{OH} = –12mA	2.3	1.8			
		I_{OH} = –18mA		1.7			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.3 - 2.7			0.2	
		I_{OL} = 12mA	2.3			0.4	
		I_{OL} = 18mA				0.5	
		I_{OL} = 24mA				0.55	
I_I	Input Leakage Current	V_I = V_{DD} or GND	2.7			±5.0	µA
I_{OZ}	3-State Output Leakage	V_O = 3.6V	2.3			±10	
I_{OFF}	Power-OFF Leakage Current	V_I or $V_O \leq$ 3.6V	0			10	
I_{HOLD}[1]	Bus Hold Current A or B Outputs	V_I = 0.7V	2.5		90		µA
		V_I = 1.7V			–90		
I_{DD}	Quiescent Supply Current	V_I = V_{DD} or GND	2.3 - 2.7			40	
		$V_{DD} \leq (V_I, V_O) \leq$ 3.6V				±40	
ΔI_{DD}	Increase in I_{DD} per input	V_{IH} = V_{DD} –0.6V, Inputs at V_{DD} or Gnd				400	

Note:

1. Not Guaranteed

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted; continued from previous page)

DC Characteristics ($1.65V \leq V_{DD} \leq 1.95V$)

Description	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	$I_{IK} = -18mA$	1.65			–1.2	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	1.65-1.95	$V_{DD} -0.2$			
		$I_{OH} = -6mA$	1.65	1.4			
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\mu A$				0.2	
		$I_{OL} = 6mA$				0.3	
I_I	Input Leakage Current	$V_I = V_{DD}$ or GND	1.95			±5.0	µA
I_{OZ}	3-State Output Leakage	$V_O = 3.6V$	1.65			±10	
I_{OFF}	Power-OFF Leakage Current	$V_I = V_O \leq 3.6V$	0			10	
I_{HOLD}(1)	Bus Hold Current A or B Outputs	$V_I = 0.4$	1.65		50		
		$V_I = 1.3$			–50		
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	1.65-1.95			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				±20	
ΔI_{DD}	Increase in I_{DD} per input	$V_I = V_{DD} -06V$, Other inputs at V_{DD} or Gnd				400	

Note:

1. Not Guaranteed

Timing Requirements Over Operating Range

Parameters	Description		V_{DD} = 1.8V ±0.15V		V_{DD} = 2.5V ±0.2V		V_{DD} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{clock}	Clock frequency					180		180	MHz
t_W	Pulse duration, CLK high or low				3		3		ns
t_{SU}	Setup time	A data before CLK↑			3.4		3		
		B data before CLK↑			1.0		0.8		
		$\overline{SEL}$ before CLK↑			1.3		1.1		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑			2.8		2.5		
		$\overline{CLKENB1}$ or $\overline{CLKENB2}$ before CLK↑			2.5		2.2		
		$\overline{OE}$ before CLK↑			3.2		2.8		
t_h	Hold time	A data after CLK↑			0.2		0.1		
		B data after CLK↑			1.3		1.1		
		$\overline{SEL}$ after CLK↑			1.0		0.8		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑			0.4		0.3		
		CLKENB1 or CLKENB2 after CLK↑			0.5		0.4		
		$\overline{OE}$ after CLK↑			0.2		0.1		

Note:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics Over Operating Range

Parameter	From (Input)	To (Output)	V_{DD} = 1.8V ±0.15V		V_{DD} = 2.5V ±0.2V		V_{DD} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}					180		180		MHz
t_{pd}	CLK	B			1.8	5.4	1.3	3.8	ns
		A(1B)			1.7	4.8	1.2	3.4	
		B(2B)			1.8	4.8	1.3	3.4	
		A(SEL)			2.4	5.8	1.7	4.1	
t_{en}	CLK	B			2.6	6.1	1.8	4.3	
t_{dis}		B			2.5	5.9	1.8	4.1	
t_{en}		A			1.8	5.1	1.3	3.6	
t_{dis}		A			2.1	5.0	1.5	3.5	

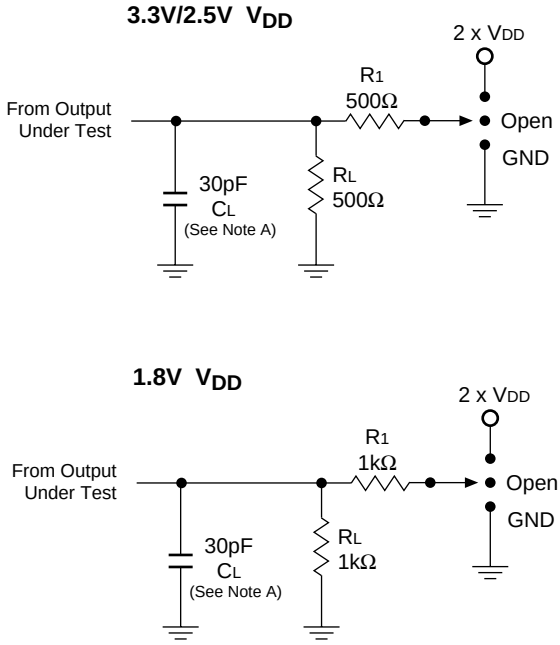
Notes:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A=25°C

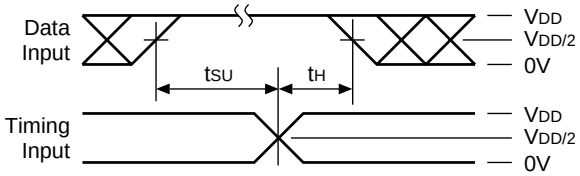
Parameters		Test Conditions	V_{DD} = 2.5V ±0.2V	V_{DD} = 3.3V ±0.3V	Units
			Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz	TBD	TBD	pF
	Outputs Disabled		TBD	TBD	

Test Circuits and Switching Waveforms

Parameter Measurement Information (V_{DD} = 1.65V - 3.6V)



Setup, Hold, and Release Timing



Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

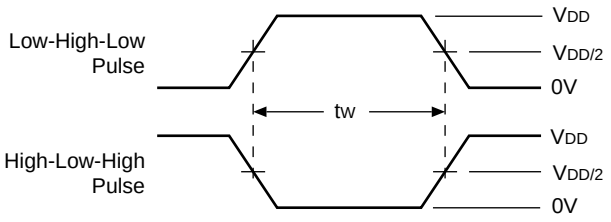
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns, ***measured from 10% to 90%, unless otherwise specified.***

D. The outputs are measured one at a time with one transition per measurement.

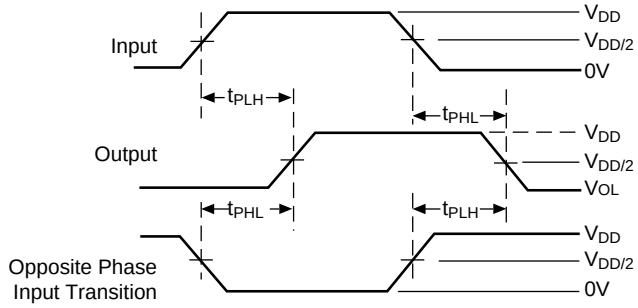
Switch Position

Test	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	GND

Pulse Width



Propagation Delay



Enable Disable Timing