SIEMENS

ICs for Communications

ATM Switching Preprocessor
ASP

PXB 4325 E Version 1.1

Preliminary Data Sheet 08.98

DS 1

PXB 4325 E **Revision History:**		**Current Version: 08.98**
Previous Version:		None
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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Edition 08.98

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL SP
Balanstraße 73,
81541 München

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1 Overview

1.1 ATM Layer Chip Set Overview

The ASP is a member of the Siemens ATM layer chip set. It consists of the six chips

- PXB 4310 E ATM Switching Matrix ASM
- PXB 4325 E ATM Switching Preprocessor ASP
- PXB 4330 E ATM Buffer Manager ABM
- PXB 4340 E ATM OAM Processor AOP
- PXB 4350 E ATM Layer Processor ALP
- PXB 4360 H ATM Content Addressable Memory Element CAME.

These chips form a complete chip set to build an ATM switch. A generic ATM switch consists of a switching fabric and switch ports as shown in **Figure 1**.

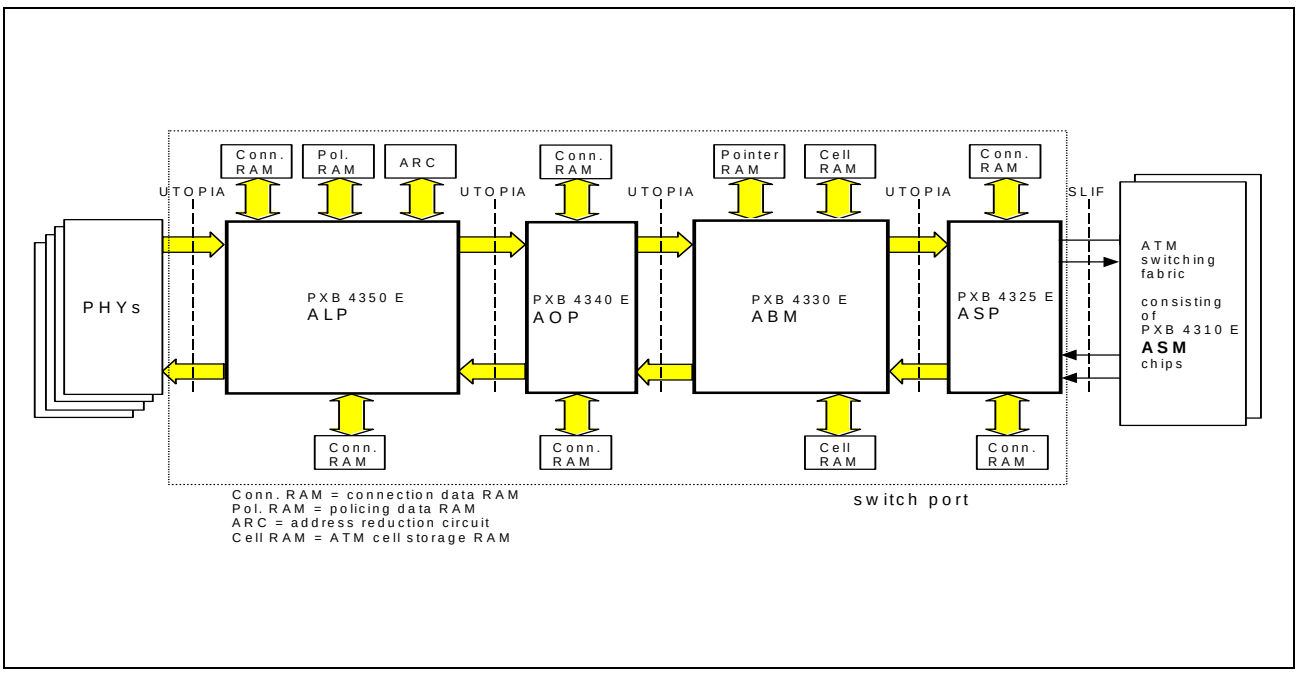


Figure 1 ATM Switch Basic Configuration

In the Siemens ATM layer chip set the switching fabric only does cell routing using the PXB 4310 E ASM, which can be used stand alone or in arrays to scale switching network throughput from 2.5 Gbit/s up to more than 40 Gbit/s. All other ATM layer functions are performed on the switch ports: policing, header translation and cell counting by the PXB 4350 E ALP, OAM functions by the PXB 4340 E AOP and traffic management by the PXB 4330 E ABM. The PXB 4325 E ASP is the access device to the switching fabric and adds/removes the routing header. It also supports redundant switching fabrics and does multicast.

Only two interfaces are used for data transfer: the industry standard UTOPIA [**5, 6**] Level 2 multi-PHY interfaces and the proprietary Switch Link InterFace SLIF. This is a serial, differential high speed link using LVDS [**7, 8**] levels.

For low end applications a single board switch with 622 Mbit/s throughput can be built with only one PXB 4350 E ALP and one PXB 4330 E ABM. Such a mini-switch is basically one switch port stand alone, without switching network access via the PXB 4325 E ASP. If the full OAM functionality is not needed the PXB 4340 E AOP chip can be omitted as shown in **Figure 2**. Minimum OAM and multicast functionality is also built into the PXB 4350 E ALP. No external Address Reduction Circuit ARC is required if the built-in address reduction is used.

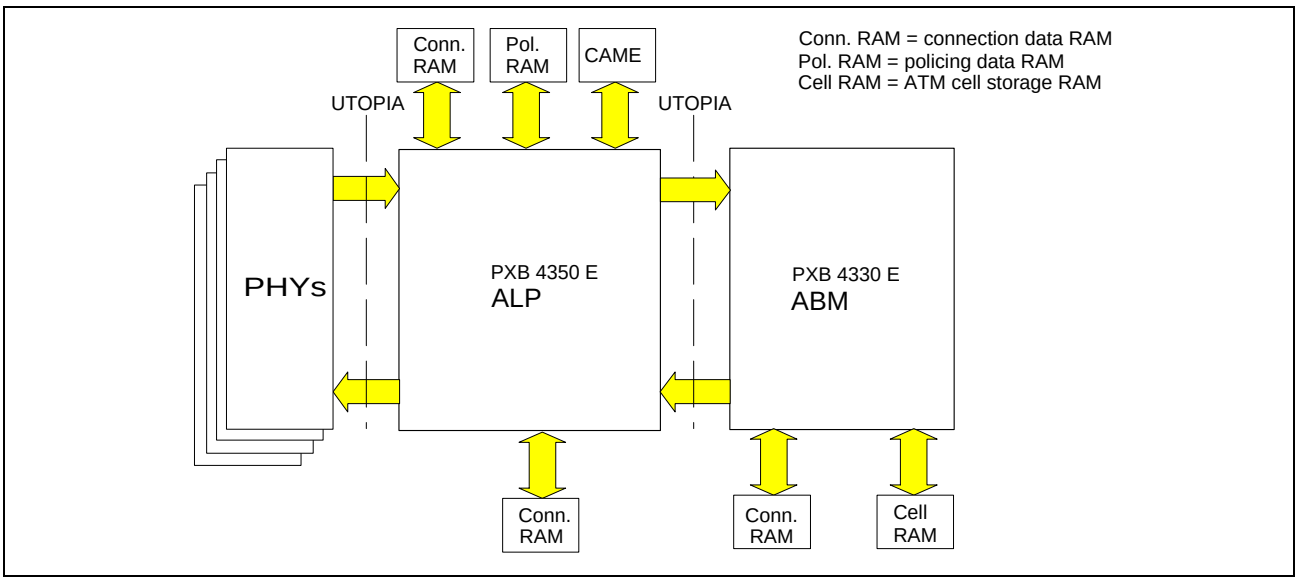


Figure 2 Mini Switch with 622 Mbit/s Throughput

Apart from the two applications of **Figure 1** and **2**, many other combinations of the chip set are possible in designing ATM switches. Functionality is selectable in many combinations due to the modular function split of the chip set. Address reduction, multicast, policing, redundant switching network and other functions can be implemented by appropriate chip combinations. The number of supported connections scales with the size of the external connection RAMs. The policing data RAM can be omitted if this function is not required.

Thus functionality and size of an ATM switch can be tailored exactly to what the respective application requires, without carrying the overhead of unnecessary functions.

1.2 Nomenclature

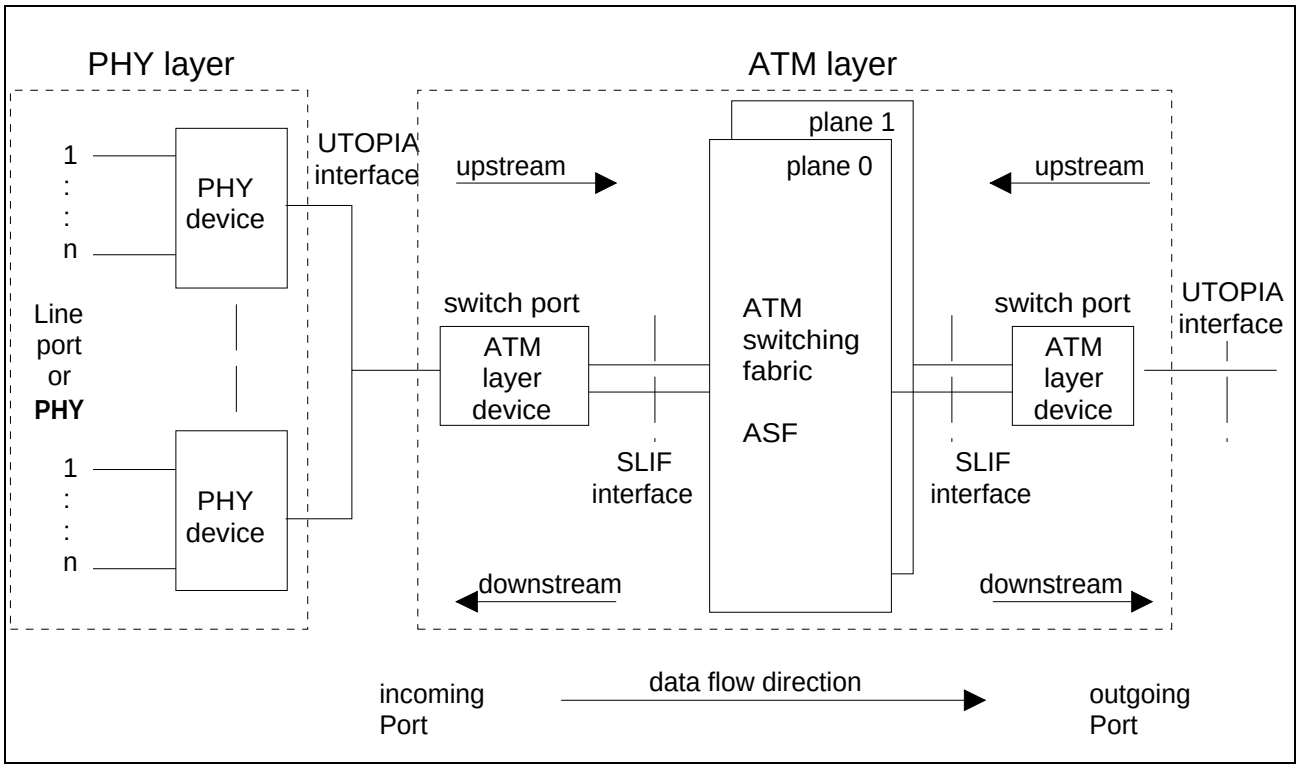


Figure 3 Nomenclature

- PHY = line port.
- PHY device = a component (chip) containing the PMD (physical media dependent) and TC (transmission convergence) sublayers of one or several line ports. Both PMD and TC together form the Physical or PHY layer. For the interface between PHY and ATM layer the UTOPIA interface is used.
- UTOPIA = Universal Test and OPerations Interface for ATM, defined by the ATM Forum in **[5]** and **[6]**.
- Switch port = in the Siemens ATM switching strategy performs all ATM layer functions except routing.
- ATM layer device = combinations of the chips PXB 4350 E ALP, PXB 4340 E AOP, PXB 4330 E ABM and PXB 4325 E ASP as shown e.g. in **Figure 1**. They perform the ATM layer functions as header translation, policing, OAM, traffic management etc. and are interconnected with the UTOPIA interface.
- ATM switching fabric ASF = array of PXB 4310 E ASM chips, does space switching of ATM cells (routing); including the buffering of cells for cell level congestion.
- Planes 0 and 1 = two redundant switching fabrics, which should be identical.
- Incoming / outgoing port = refers to a connection with the data flow direction as shown in **Figure 3**.
- Upstream / downstream = refer to the ATM switching network; the direction towards the ASF is upstream, coming from the ASF is downstream.

ATM Switching Preprocessor **PXB 4325 E**
ASP

Version 1.1 **CMOS**

1.3 Features

P-BGA-352-2

Performance

- Performance up to STM-4/OC-12 equivalent ATM layer processing
- Throughput up to 687 Mbit/s bi-directional
- Up to 16384 connections in both directions

UTOPIA Interface

- Multiport UTOPIA Level 2 interface
- UTOPIA frequency up to 51.84 MHz
- Up to 8 PHY devices with up to 25.92 MHz clock
- Up to 4 PHY devices with up to 51.84 MHz clock
- Up to 24 PHYs addressable
- 4-fold multi-PHY UTOPIA interface with 4 CLAV/$\overline{\text{EN}}$ pairs for up to 4 PHY groups
- Up to 4 UTOPIA Level 1 PHYs
- Polling of PHYs with rotating priority in 3 modes: 4x6, 3x8 or 2x12
- Cell level handshake
- Selectable 8 or 16-bit UTOPIA data bus single- or multiport
- Optional parity protection at UTOPIA interface
- One UTOPIA receive and transmit interface at the PHY side in master mode

Cell Format at UTOPIA Interface

- Support of standardized and proprietary UTOPIA cell format
- Proprietary cell format with 14 bit LCI in VPI and UDF1 field
- Standardized VPC only mode with 12 bit LCI in the VPI field
- Standardized VCC only mode with 14 bit LCI in the VCI field

Type	Ordering Code	Package
PXB 4325 E	Q67003-H9309	P-BGA-352-2

- Special mode for PXB 4220 IWE8 device with E1/T1 port number transmitted in the UDF1 octet

External RAM Interfaces

- Two indepedent interfaces for upstream and downstream external RAM
- Use of standard Synchronous Static RAM devices 1 M organized 32 bit wide
- RAM size scalable with number of connections: upstream 1-2 M, downstream 1-4 M
- Test mode for one connection only without external RAMs

Cell Flow

- Insertion and extraction of ATM cells e.g. for test purposes
- Provision of a 1 cell insertion buffer
- Insertion of cells from the microprocessor interface into cell stream in up- and downstream direction
- Extract/copy/discard of selected cells from up- or downstream direction
- Two 4 cell extraction buffers, one for each direction
- 4 fully programmable and maskable cell filters for detection of cells, 2 for each direction
- Built-in test loops
- Internal loop downstream to upstream at UTOPIA interface for tests
- Internal loop upstream to downstream at SLIF interface (**see Chapter 4.2, page 93**)
- The SLIF loop can be closed for each plane individually; mixed operation mode possible with only one loop closed

Switch Link Interface SLIF

- ASP interfaces directly to PXB 4310 E ATM Switching Matrix
- Connection to the switching fabric with serial, differential switch link interface SLIF with up to 207.36 Mbit/s per line
- Bundles of 1, 2 or 4 SLIF lines independently configurable for upstream and downstream direction
- Redundant inputs and outputs with identical bundle modes
- In transmit direction the cells are distributed cyclically on the lines of the bundle with an appropriate time delay as in the PXB 4310 E ASM
- In receive direction the input lines are scanned in the same way as in the PXB 4310 E ASM in order to guarantee the correct cell sequence
- Unused SLIF inputs and outputs can be switched off
- Individual bit phase adaptation for each SLIF line input for transmitter clock recovery

Cell Conversions

- Translation from standard 54 octet (16-bit UTOPIA) or 53 octet (8-bit UTOPIA) ATM cell format to switch internal 64 octet cell format and vice versa

- Generation and evaluation of Sync octet with bit toggle function
- Generation and evaluation of header and payload checksums FCS1 and FCS2
- In upstream direction translation of LCI into ECI or MCI, in downstream direction conversion from ECI or MCI into LCI or into multiple LCIs in case of multicast
- Transparent transport of CLP bit via the switching fabric
- Per connection optional overwriting of CLP bit in upstream direction

Redundant Switching Fabric Support

- Optional support of redundant switching fabric in 3 modes
  - Cell-by-cell redundancy in a connection basis
  - Load sharing on a connection basis
  - Hot stand-by
- Cell-by-cell redundancy is supported using the recombining algorithm with condition monitor and dead plane monitor

Multicast

- Full spatial and logical multicast at the downstream side
- Up to 64K multicast connections in the whole switch
- Up to 24 spatial multicast branches per connection with simultaneous copying function
- Logical multicast for up to 1024 logical multicast branches

Buffering

- Recombining buffer is provided for cell-by-cell redundancy with 85% internal load with $<10^{-11}$ cell loss rate
- Selective cell discard based on the internal CLP bit
- Speed reduction buffer dimensioned for 4 ports with 95% output load and $<10^{-11}$ cell loss rate
- 24 queues for the support of up to 24 addressable PHYs
- One programmable queue size (0...356 cells) common for all 24 queues
- No head of line blocking for up to 24 PHYs

Communication Interface (RSATM)

- Reduced Speed ATM (RSATM) interface in receive and transmit direction
- In upstream direction insertion of internal communication cells at serial interface
- In downstream direction extraction and buffering of internal communication cells and output at serial interface

Miscellaneous

- 16-bit universal microprocessor interface for control and operation of the chip
- Access to external connection RAMs via internal transfer register sets
- Support of Line Card (LIC) redundancy
- Boundary scan according to JTAG

Technology

- 0.35 µ CMOS, 3.3V
- Plastic BGA-352 package
- Temperature range from 0°C to 70°C (-40°C to 85°C upon request)
- Power dissipation 2.3 W (typical)

1.4 Logic Symbol

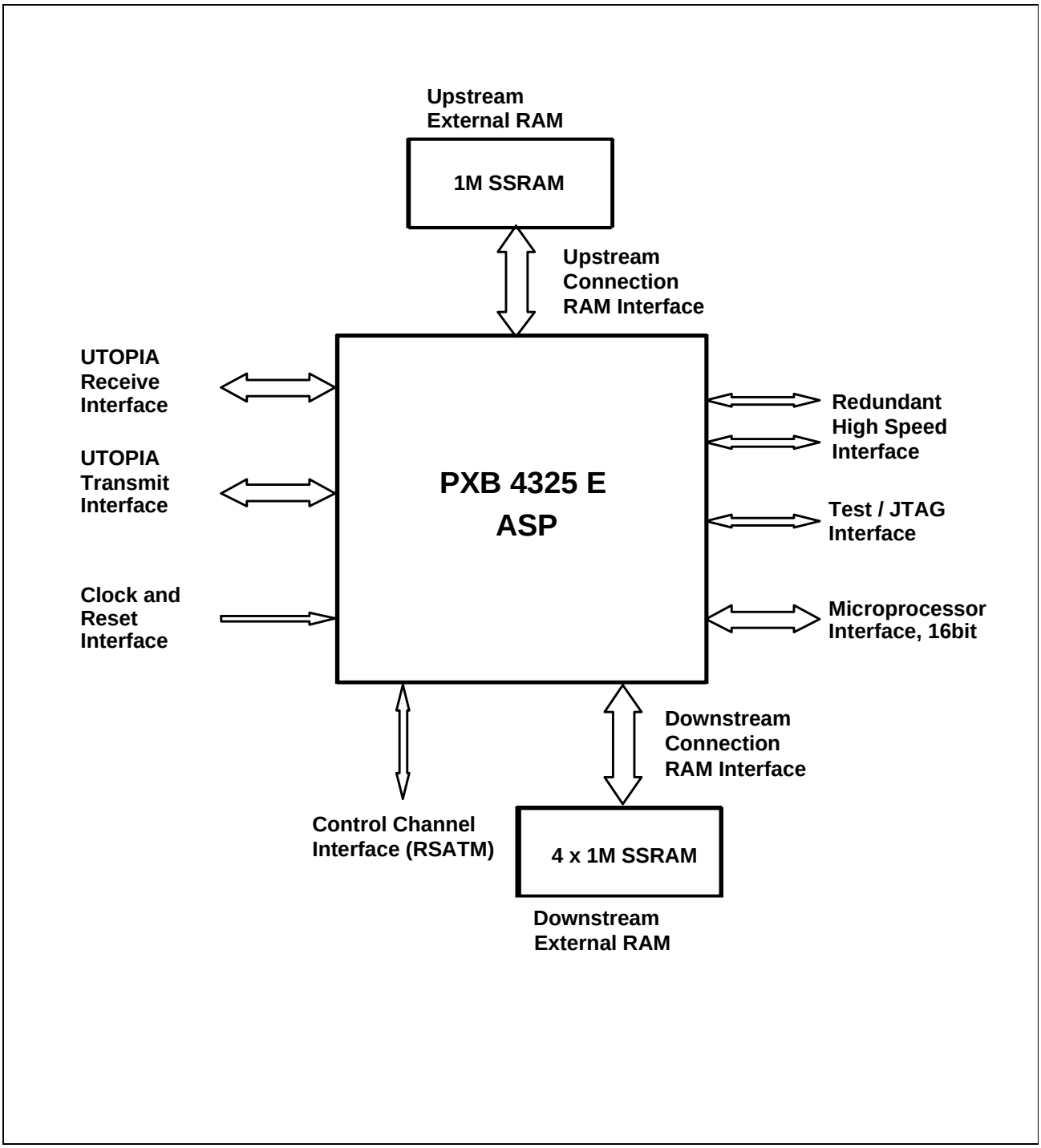


Figure 4 Logic Symbol

1.5 Functional Overview

The ASP is the access device of a switch port to the switching fabric. At the switch port side it has the industry standard UTOPIA Level 2 interface and at the switch side the Siemens proprietary Switch Link InterFace SLIF (**Chapter 4.2**, page 92). The SLIF allows easy interfacing to a switching fabric consisting of PXB 4310 E ASM switching matrix chips.

In upstream direction the ASP automatically generates the 64 octet SLIF cell format including routing field, sequence numbers and checksums. In downstream direction these fields are automatically analyzed and then removed.

Main functionalities of the PXB 4325 E ASP are the support of redundant switching fabric and the support of spatial and logical multicast.

The PXB 4325 E ASP features are in line with the other components of the ATM switching chip set consisting of PXB 4350 E ALP, PXB 4340 E AOP and PXB 4330 E ABM. This affects parameters as the maximum number or connections (16384) or PHYs (24) as well as common design blocks as microprocessor interface, UTOPIA interface blocks and others.

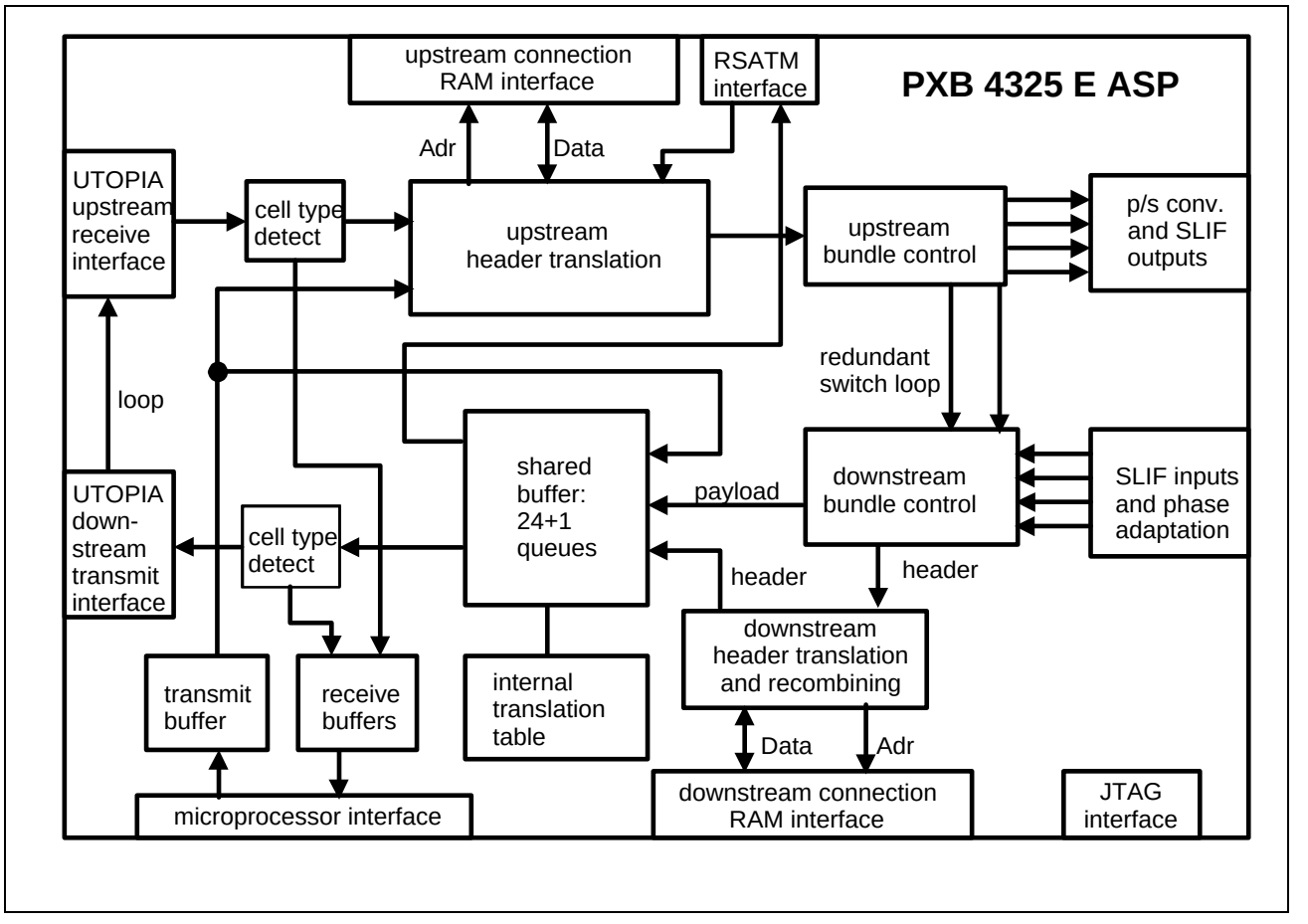


Figure 5 Block Diagram

1.6 Data Flow

The data flow inside the ASP is described here with reference to **Figure 5**.

1.6.1 Throughput

The maximum throughput of 687 Mbit/s comes from the fact that 32 clock cycles of 51.84 MHz are necessary for each cell. As a cell consists of 53 bytes or 26.5 words of 16 bit:

maximum throughput = 51.84 Mwords/s x 16 bit/word x 26.5/32 = 686.88 Mbit/s.

The effective throughput is limited to 622 MBit/s due to buffer management.

1.6.2 Upstream Data Flow

User cells are received from the UTOPIA upstream receive interface and forwarded via the **cell type detect block** to the upstream header translation block. The cell type detect block allows to detect two programmable header pattern from the cell stream. Optionally the detected cells can be extracted, deleted or copied.

The **upstream header translation** block gets ATM cells from 3 sources with different priorities:

1. UTOPIA upstream receive interface / UTOPIA downstream transmit interface in case of downstream **loop** (highest priority)
2. RSATM interface
3. transmit buffer (lowest priority).

If none of these cell types is available the bundle control block generates empty cells for cell rate de-coupling.

Cells from UTOPIA upstream receive interface and from transmit buffer are translated from UTOPIA cell format to internal, 64-octet SLIF format. The extended header is fetched from the external RAM. RSATM cells have amost the SLIF cell format except the FCS1, FCS2 and Sync octet which are computed by the **upstream bundle control** block. This block performs the distribution of cells to the active lines of the output bundle with a delay of 3 octet between cell boundaries on the SLIF lines. 3 bundle modes can be selected:

1. bundle of 1, SLIF line 0 is used
2. bundle of 2, SLIF line 0 and 1 are used
3. bundle of 4, SLIF line 0, 1, 2 and 3 are used.

Incoming cells are forwarded to one of the enabled SLIF lines but the chronological order is preserved as shown in **figure 6**.

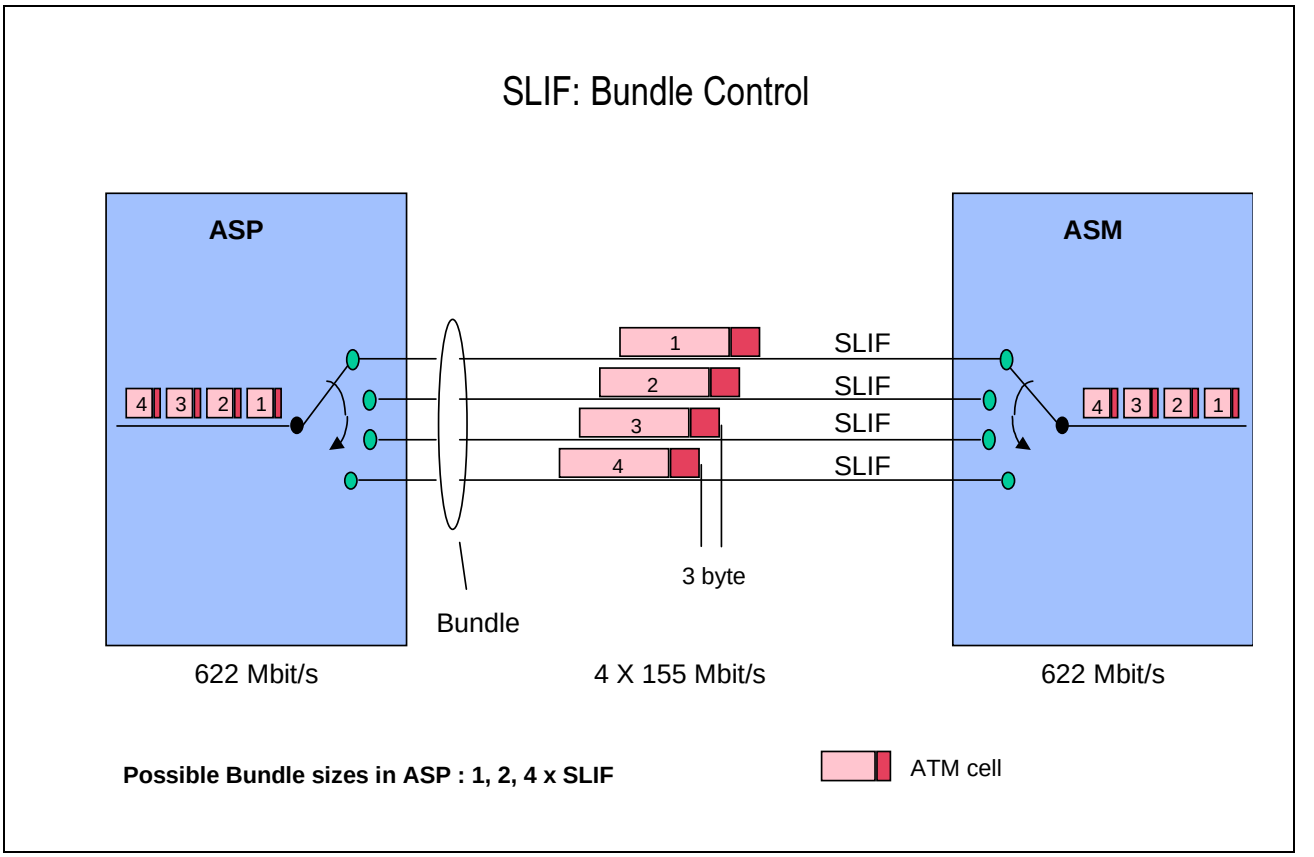


Figure 6 SLIF Bundle Control

Unused outputs can be switched to output a constant level, a measure which saves power and reduces the jitter on the active outputs.

The bundle modes can be selected independently for up- and downstream direction, so that systems with asymmetric throughput can be built. The bundle mode is always identical for both redundant outputs.

It can be selected on a per connection basis if the cells are forwarded to one of the two redundant output bundles or to both. In addition two global plane enable bits are provided, one for each plane. These global plane enable bits only affect cells from UTOPIA interface, not cells from transmit buffer or RSATM interface. This function allows to switch off individual planes by keeping the SLIF outputs synchronous and allowing to send RSATM cells for internal communication.

1.6.3 Downstream Data Flow

The **phase adaptation** block contains 8 phase adaptation circuits, as in the PXB 4310 E ASM.

The **downstream bundle control** scans the up to 4 active SLIF inputs for each plane and establishes the correct cell sequence for each plane.

Each plane can be connected individually to the upstream bundle control for the **redundant switch** loop. A mixed operation with one loop closed or also both loops closed is possible.

The cell headers are forwarded by the downstream bundle control to the **header translation** block which also contains the **recombining** function. This block makes a lookup for connection relevant data in the downstream external connection RAM, decides on the acceptance of the cell and does a header translation. The new header is forwarded to the shared buffer. In case the cell is not accepted a discard signal is sent to the shared buffer.

The cells from the bundle control are forwarded directly to the **shared buffer** with the translated header delivered by the header translation block.

The shared buffer has a total size of 356 cells and contains 25 queues for the 24 UTOPIA ports and one RSATM queue. For fairness reasons one common queue limit can be programmed for all queues and a common threshold value for all queues. Beyond the threshold value only low priority cells are accepted. Cell priority is determined by the internal priority bit iCLP.

The RSATM queue has a fixed size of 32 cells.

The shared buffer also has an input for cells from the **transmit buffer** which has one cell size. Cells are written there by the microprocessor and inserted either in upstream or downstream direction by command.

Cells can be extracted by the **cell type detect** block using two full programmable cell type detectors. This block also extracts internal test cells. The **UTOPIA downstream transmit** interface supports up to 24 queues.

1.7 Header Translation

The Siemens ATM switching chip set uses the strategy that the external connection identifiers VPI and VCI are replaced at the input port by the Logical Channel Identifier LCI. In case of a multi-PHY port also the PHY number PN is mapped to the LCI. This is called address reduction (AR). The resulting LCI is unique on the incoming switch port. All further addressing of connection tables within the switch is done using the LCI. When leaving the switch at the outgoing port the LCI is replaced by the VPI/VCI and the PHY number PN of the outgoing line. Within the switch the LCI is translated when leaving the incoming port in direction to the ASN, as at the outgoing port this LCI might be yet used by another connection.

The whole header translation scheme is shown in **Figure 7** for a bi-directional point-to-point connection: from left to right Port A is the incoming port where the address reduction from VPIa, VCIa and PNa to the LCIa is made. LCIa is unique on Port A. When leaving the switch port towards the switching fabric the LCIa is translated to the LCIb which is unique at the outgoing switch port (port B). Before leaving the switch finally the LCIb is translated to the desired VPIb, VCIb and PNb values. The same procedure holds for the inverse direction from Port B to Port A. Note that on the transmission lines as well as on each port the same identifiers are used for both directions.

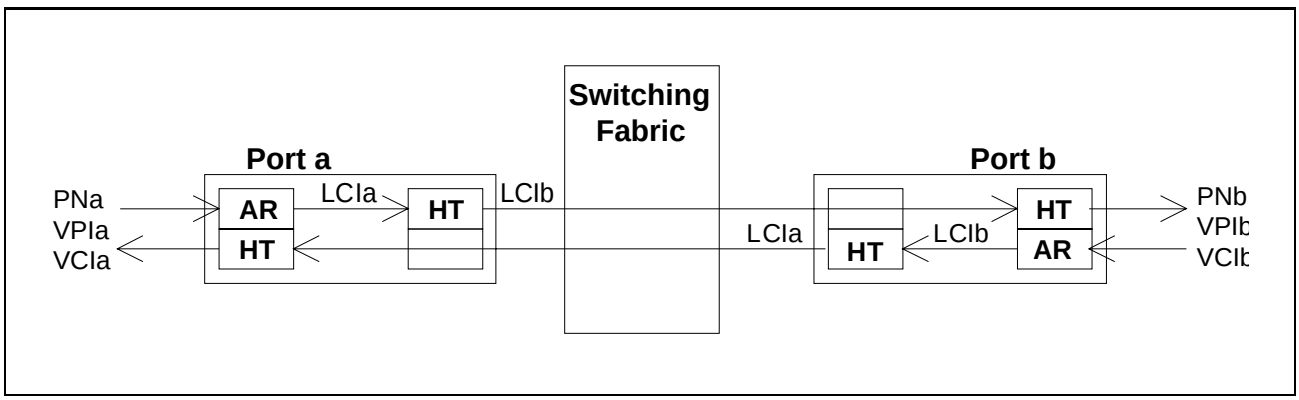


Figure 7 Header Translation for Point-to-Point Connection with AR = Address Reduction HT = Header Translation

The header translation for point-to-multipoint or multicast connections is slightly more complicated. A Multicast Connection Identifier MCI is assigned to each connection; this identifier is unique in the whole switch. At the downstream side an additional address translation is required to obtain the LCI for the respective outgoing ports.

The PXB 4325 E ASP supports spatial and logical multicast in addition to the spatial multicast in the switch. Spatial multicast is supported for up to 24 PHYs. The MCI of a multicast connection is translated into a base-LCI (BLCI) plus the PHY number, thus giving unique addresses for all branches. For logical multicast branches an additional address translation is done using an internal lookup table with 1024 entries.

In reverse direction a multipoint-to-point or merger connection is set-up. Different identifiers are required for the merger branches inside the ASN, as the merger connections come from different ports and have indepenently assigned sequence numbers. They use Egress Connection Identifiers ECI. The PXB 4325 E ASP on Port A translates the different ECIs into the same LCI.

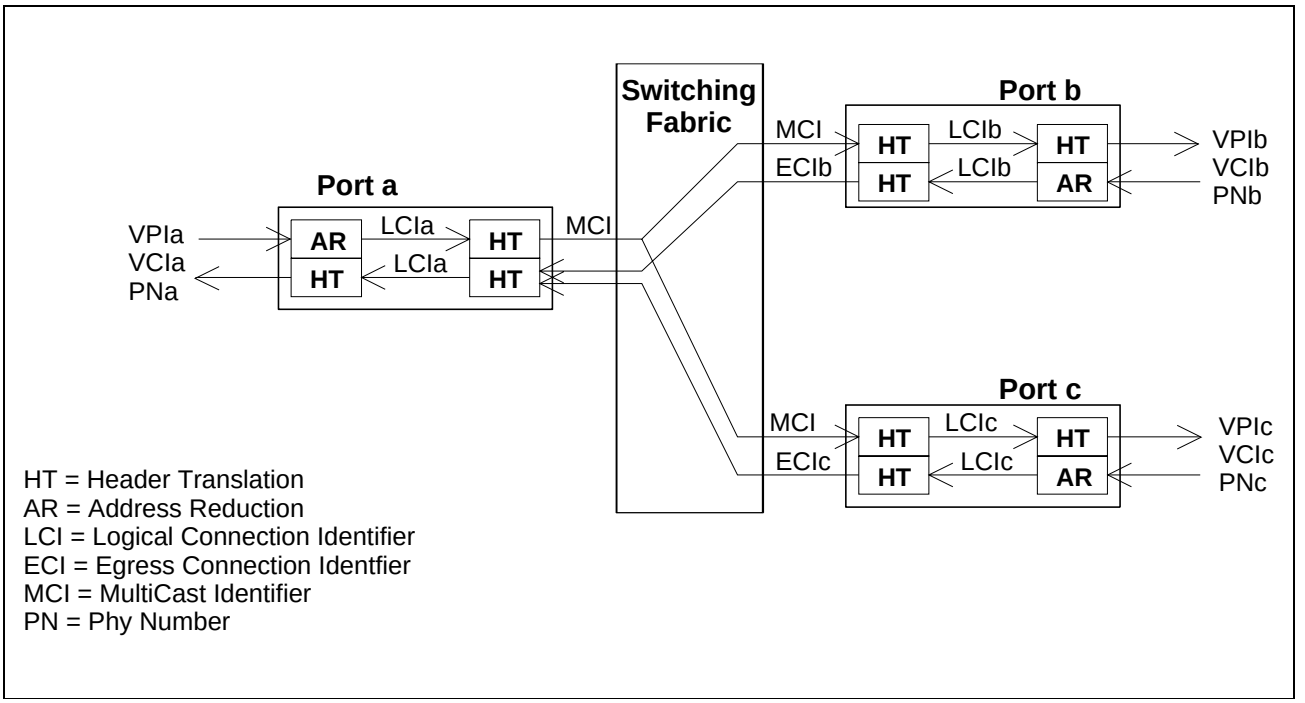


Figure 8 Header Translation for Multicast and Merger Connections with AR = Address Reduction HT = Header Translation

1.7.1 Upstream Address Reduction

Address reduction can be done in two different modes, with arbitrary LCI assignment and with fixed LCI assignment. Arbitrary LCI assignment means that the LCI value can be chosen freely anywhere in the range from 0 to 16383. Arbitrary LCI assignment is possible with the PXB 4350 E ALP and an external address reduction circuit as a pointer table or a content addressable memory. Fixed LCI assignment can be done by the PXB 4325 E ASP in various modes described below. It is used if PHYs are connected directly to the PXB 4325 E ASP.

If the PXB 4350 E ALP is used and does the address reduction it writes the LCI into the UTOPIA cell at the place of the VPI (12 bit) plus two addtional bits in the UDF1 field. Then the PXB 4325 E ASP uses this mode:

- LCI(13:0) = UDF1(7:6) x 4096 + VPI(11:0)

The upstream address reduction is provided optionally to generate the LCI from VPI, VCI and PN. It is used if PHY devices are connected to the ASP. Several modes are possible:

1. LCI(13:0) = VCI(10:0) x 8 + UDF1(2:0)	VCI mode for use with PXB 4220 IWE8
2. LCI(13:0) = VPI(10:0) x 8 + UDF1(2:0)	VPI mode for use with PXB 4220 IWE8
3. LCI(11:0) = VPI(11:0), LCI(13:12) = 00	single PHY mode, VPI only
4. LCI(13:0) = VPI(11:0) x 4 + PN(1:0)	4 PHY mode, VPI only
5. LCI(13:0) = VPI(10:0) x 8 + PN(2:0)	8 PHY mode, VPI only
6. LCI(13:0) = VPI(9:0) x 16 + PN(3:0)	16 PHY mode, VPI only
7. LCI(13:0) = VPI(8:0) x 32 + PN(4:0)	32 PHY mode (24 usable), VPI only
8. LCI(13:0) = VCI(13:0)	single PHY mode, VCI only
9. LCI(13:0) = VCI(11:0) x 4 + PN(1:0)	4 PHY mode, VCI only
10. LCI(13:0) = VCI(10:0) x 8 + PN(2:0)	8 PHY mode, VCI only
11. LCI(13:0) = VCI(9:0) x 16 + PN(3:0)	16 PHY mode, VCI only
12. LCI(13:0) = VCI(8:0) x 32 + PN(4:0)	32 PHY mode (24 usable), VCI only

Note: The unused high order bits of VPI and VCI will be ignored by the PXB 4325 E ASP and should be zero to avoid ambigous addresses.

1.7.2 Upstream Header Translation

The LCI is used to address the upstream external RAM containing the internal header. The internal header consists of routing tag, sequence number, some control bits and the egress/multicast connection identifier EMCI, the cell identifier for the outgoing port. The 16-bit wide EMCI is a ECI in case of a point-to-point connection and a MCI in case of a multicast connection. The ADI bits of the internal header determine if the EMCI is a point-to-point or multicast identifier.

1.7.3 Downstream Header Translation

The header translation at the downstream side uses two RAMs, an external RAM of up to 128K words of 32 bit and an internal translation table. The internal translation table contains LCIs which can be arranged in a linked list for logical multicast. Logical multicast denotes the repeated emission on one cell with different LCIs towards the same PHY.

The external RAM is segmented into two parts, an upper range used for translation of the 64K multicast identifiers into the 16K LCI and a lower part containing recombining entries, addressed with ECIs. The segmentation of the RAM can be programmed.

The EMCI of the cell received from the ASN is interpreted as ECI or MCI depending on the ADI(1:0) bits. The EMCI field is 16 bit wide, but not the whole range can be used. It is depending on the size of the downstream external connection RAM and on the programmed segmentation. The PXB 4325 E ASP checks for ECI values overlapping into the MCI range and discards these cells.

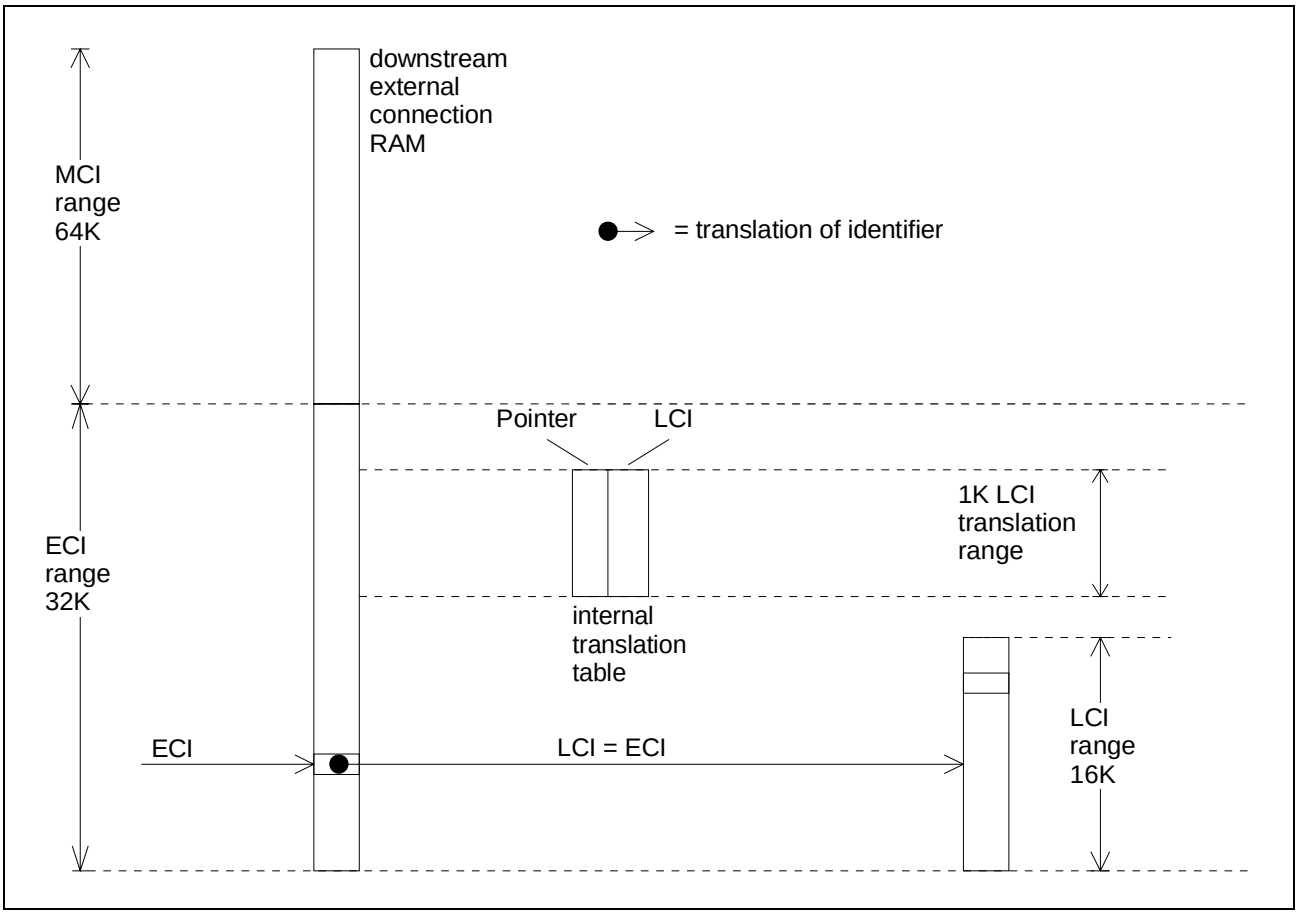


Figure 9 Downstream Header Translation for Point-to-Point Connections

For point-to-point connections (**Figure 9**) an ECI value in the LCI range of up to 16K entries is used to address the connection entry. This entry contains:

- data for cell acceptance (sequence, plane information etc, see **Chapter 1.13**, page 31)
- the LCI which normally is programmed equal to the ECI
- the PHY number (0..24) encoded in 5 bit

The LCIb shown in **Figure 7** is exactly the LCI in **Figure 9**.

The MCI range of the downstream external connection RAM and the internal translation table are unused for point-to-point connections.

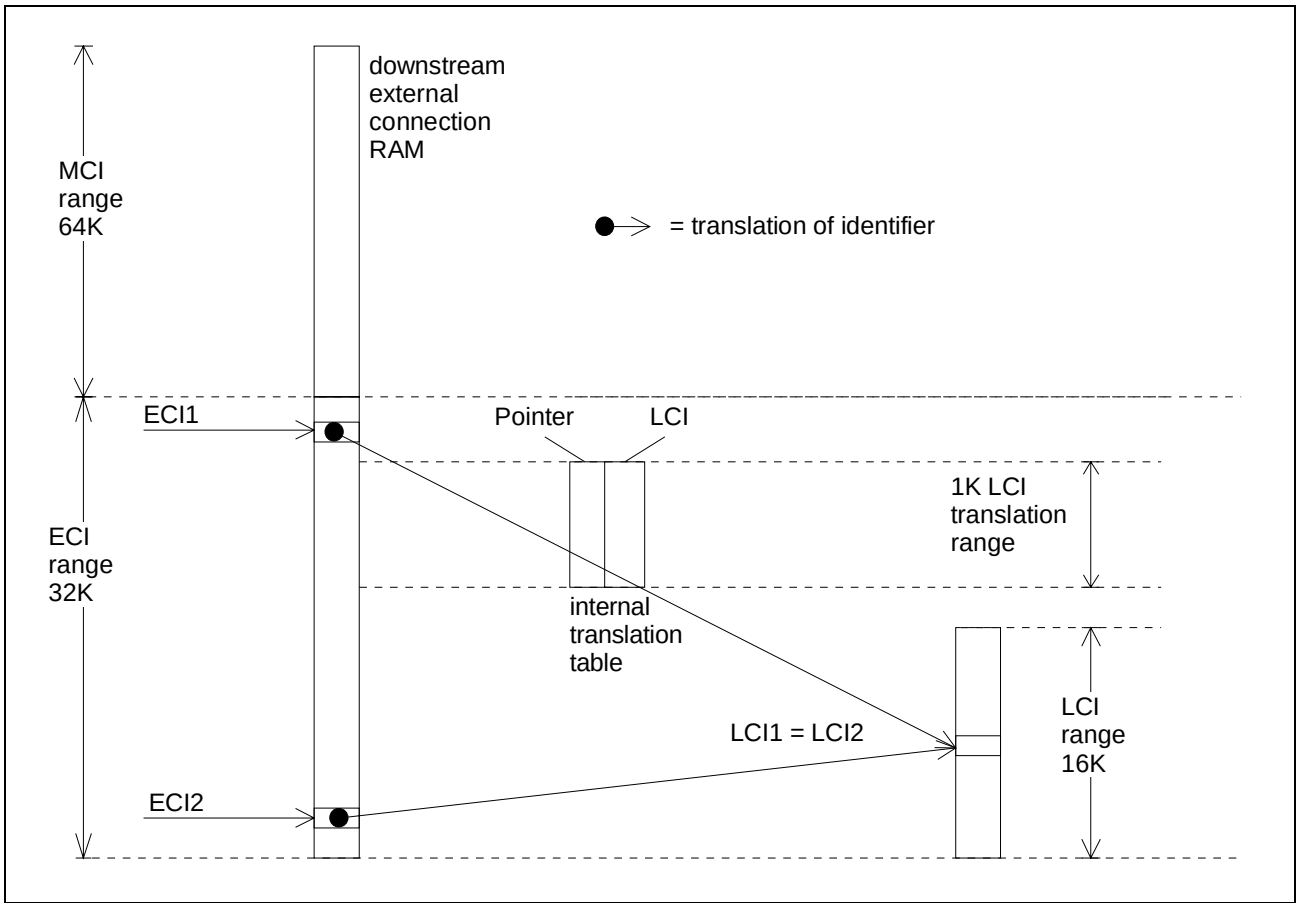


Figure 10 Downstream Header Translation for Merger Connections

Merger connections consist of several point-to-point connections with different ECIs which are all translated to the same LCI as shown in **Figure 10**. ECI values for merger connections can extend over the whole ECI address range of 32K.

The two different ECI values ECI1 and ECI2 correspond exactly to the ECIb and ECIc values of **Figure 8**.

As with point-to-point connections the MCI range of the downstream external connection RAM and the internal translation table are unused for merger connections.

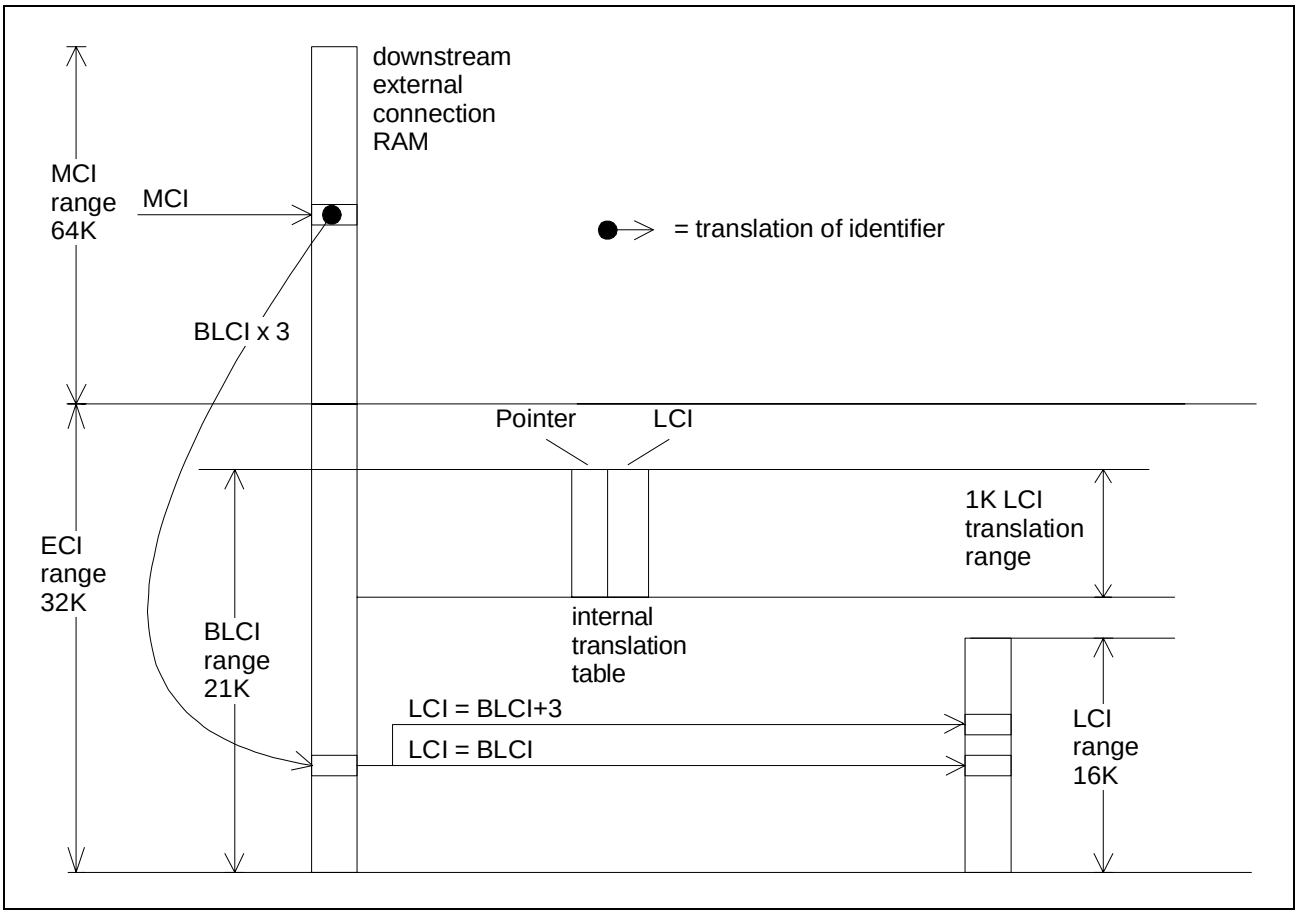


Figure 11 Spatial Multicast without Header Translation

There are two possibilities for multicast connections, with and without LCI translation. Without LCI translation more multicast connections are possible, but spatial multicast only. Logical multicast requires address translation which is achieved with an internal table of 1024 entries (**see Figure 12**).

For multicast connections without LCI translation (**Figure 11**) the EMCI is interpreted as MCI and is used to address the MCI range of the external RAM where pointer entries are contained. The pointer has the value BLCI x 3 (BLCI=base-LCI) and points to the desired connection entry. Up to 21K entries can be addressed. In case of multicast the entry contains:

- data for cell acceptance (sequence, plane information etc, see **Chapter 1.13**, page 31)
- a 24 bit vector indicating the PHYs where the cell is to be forwarded

No LCI is contained, so that no address translation is possible. In order to distinguish the cell copies the PHY number PN is added to the BLCI. This implies segmenting part of the external RAM into blocks of size N, with N the number of connected PHY chips.

The internal translation table is unused for spatial multicast without header translation.

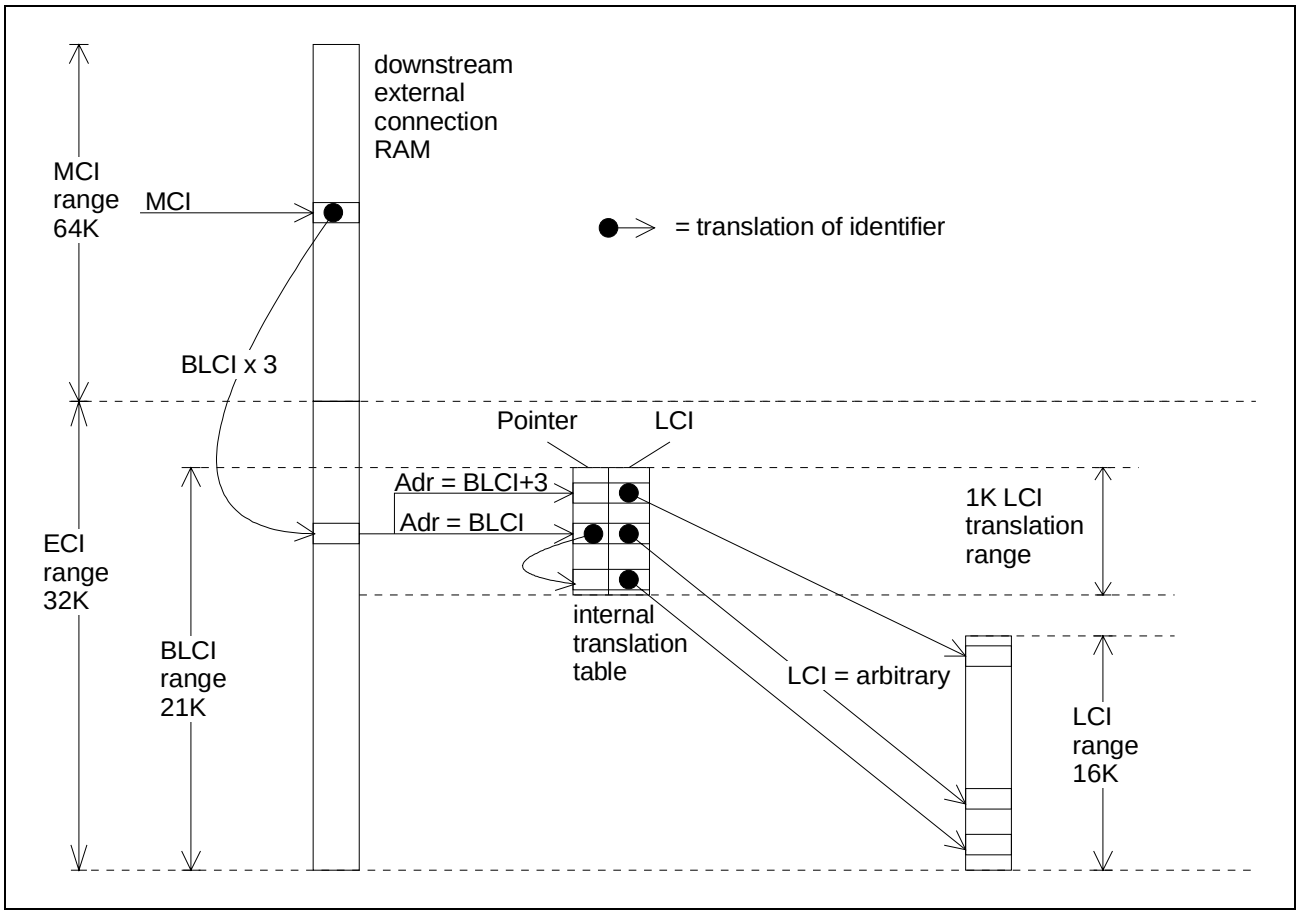


Figure 12 Mixed Spatial and Logical Multicast with Downstream Header Translation

For spatial multicast with LCI translation and for logical multicast an internal translation table is provided. Its location can be programmed in steps of 1K in the range 0..20K. If the BLCI + PN value of a cell is within the programmed range the table is addressed. It contains for each entry a LCI and an optional pointer to a subsequent entry. It is thus possible to define a linked list of entries for each BLCI + PN value. The current ATM cell is sent out repeatedly, once for each entry, with the respective LCI.

The definition of branches is completely free, only limited by the maximum number of 1024. As two extreme cases 512 connections with 2 branches or 1 connection with 1024 branches could be set-up.

In **Figure 12** an example is shown with two spatial and one logical multicast branches. The spatial branches are destined to PHY0 and PHY3, for PHY0 an additional logical branch is defined. Thus each cell of this connection is replicated and three copies are forwarded to the UTOPIA interface, each time with different LCI value.

It is recommended to locate the internal translation table outside the LCI range to facilitate connection managment.

The ECI range beyond the 21 K BLCIs can be used for merger connections and RSATM connections.

1.8 Shared Buffer

1.8.1 Shared Buffer Overview

Each queue of the shared buffer can store cells from all 8 high speed inputs within one cell cycle. Thus cell bursts produced by two redundant switch planes and bursts due to cell clumping are absorbed by the queues. Separate queues for each PHY avoid blocking of all PHYs due to one congested PHY.

The shared buffer contains 25 discrete fifo queues, 24 queues for the PHYs and one queue for RSATM interface. Unused queues can be disabled and do not consume buffer space.

The size of each active queue is limited by a common queue limit. The idea of the shared buffer is, that the sum of the queue limits is much higher than the total buffer size of 356 cells (**see Table 1**). This is possible as the probability that more than one queue reaches its maximum is very low. Using statistical methods and with the assumption of equally distributed, Bernoulli type traffic at all switch inputs the cell loss probability can be calculated. See the appendix of the PXB 4310 E ASM preliminary data sheet [**9**] and [**10**] for calculation details. The queue limit is programmed to such a value that the probabilities of

- overflow of the whole buffer and
- overflow of a single queue

have the same value, i.e. they are equilibrated.

Some examples for equilibated queue limits for a cell loss probability of 10^{-11} are shown in **Table 1**.

Table 1 Queue Sizes for Cell Loss Probability 10^{-11}

no. of queues	queue size	load per queue
1	356 cells	97%
4	256 cells	87%
16	170 cells	84%

In addition a common theshold for low priority cells can be programmed. If a buffer is filled beyond this threshold incoming low priority cells are not accepted. This measure reserves storage space for high priority cells. Cell priority can be selected on a connection

basis to be either the CLP of the standardized cell or a fixed priority. A recommended assignment of the internal cell priority for each traffic class are given in **Table 2**.

Table 2 Internal Cell Priority for Traffic Classes

traffic class	CLP bit	internal cell priority
CBR	0 and 1	high
VBR	0 and 1	= CLP
ABR	0 and 1	= CLP
UBR	0 and 1	low

The low priority threshold should be chosen in a way that the reserved queue space for high priority traffic is large enough for the required high priority cell load. E.g. for the single PHY/queue configuration the threshold could be set to 186 cells, which reserves a 170 cell buffer space for high priority cells - allowing up to 84% high priority cell load (**Table 1**).

Example for Spatial Multicast in the Buffer

The example of **Figure 13** shows a multicast connection with the MCI value MCI=25000d which is translated into a base-LCI of LCI=100d. The connection has branches to PHY #1 and PHY #3; thus the cells for PHY #1 will have the LCI=101d and the cells destined to PHY #3 will have the LCI=103d. The LCI values 100d and 102d are not used, but reserved, as at any time additional multicast branches may be added.

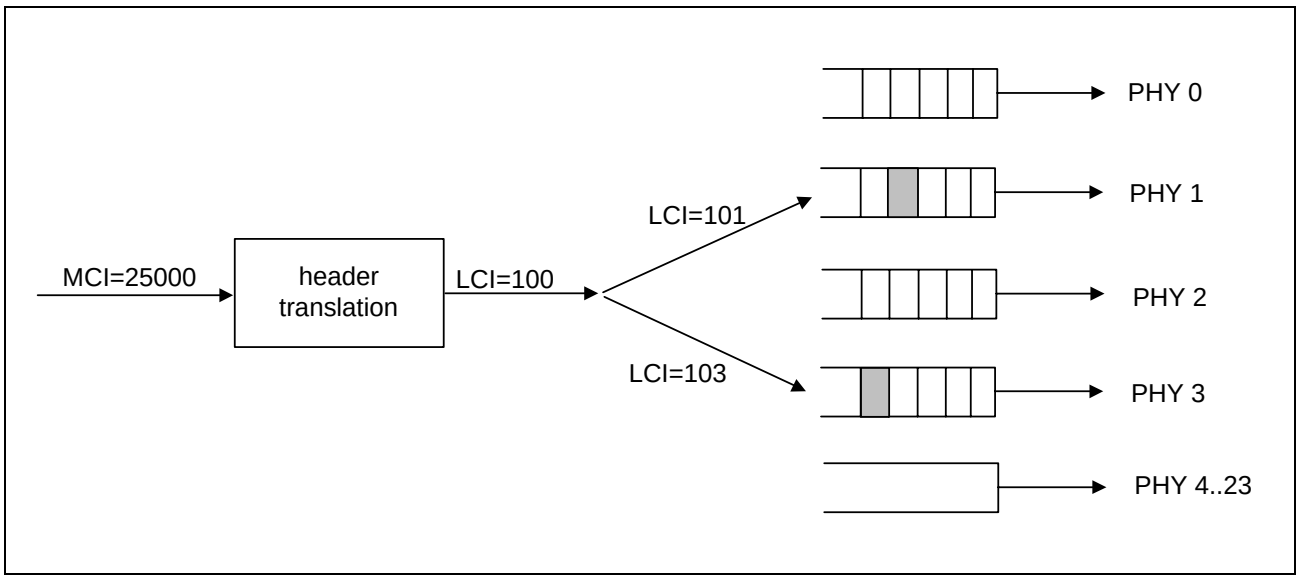


Figure 13 Example for Spatial Multicast

Note that in the example of **Figure 13** only 4 ports are configured and consequently only queues 0...3 are used and queues 4...23 are empty.

When a cell is read out of the buffer it could belong to a logical multicast connection. In this case the cell is not discarded after read out, but the header (BLCI) is replaced by another LCI according to the pointer chain in the logical multicast pointer RAM. This procedure is repeated until the last entry is reached. The read out of subsequent cells is blocked until the last entry of the pointer chain is worked off. The logical multicast connection thus produces an additional cell delay which should be taken into account.

1.9 Special Cell Type Recognition

Two full programmable cell type detectors are provided by the ASP for each direction. All compare the first four octets of the header plus the first payload octet. The comparators are located close to the UTOPIA interfaces and compare the UTOPIA cell format. Each bit of the comparators can individually be masked, with a masked bit always matching. Upon match 4 actions can be programmed:

1. ignore: no action, used to switch off the comparator
2. discard: a matching cell is discarded
3. drop: a matching cell is directed to the receive buffer
4. monitor: a matching cell is copied to the receive buffer and forwarded normally

1.10 Insertion and Extraction of Cells

Cells can be inserted into the cell stream in both up- and downstream direction using a common one-cell transmit buffer. This buffer is realized as registers in the microprocessor interface, so that each 16-bit word can be addressed directly. The cell format is slightly different for up- and downstream direction. For insertion in downstream direction a queue/PHY must be specified where the cell is to be inserted.

For cell extraction two separate buffers of 4 cells for each direction are implemented. For the microprocessor they appear as a single buffer. Cells are read by the microprocessor via successive reads from one address. Both up- and downstream direction have two full programmable cell type detectors allowing to extract cells, in downstream direction in addition all cells with housekeeping HK = 001 (test cells) are extracted.

1.11 Communication Channel (RSATM)

The ASP provides a bi-directional RSATM interface for communication between onboard controllers and main switch controller via the data links. Cells can be inserted and extracted serially with a speed of up to 25.92 Mbit/s at the RSATM interface. Inserted cells are transmitted via the high speed links towards the ASN.

In receive direction RSATM cells are extracted after the recombining function into a dedicated buffer of 32 cells. They pass normally the recombining algorithms and are detected by the housekeeping combinations HK = 110 and HK = 011.

An arbitrary number of communication channels can be set-up in the external downstream connection memory. They are treated as point-to-point connections, i.e. the cell identifier EMCI can be translated to any VCI.

1.12 Cell Synchronization of Downstream Dataflow

For the downstream cell stream (i.e. cells that arrive the ASP from the Switching fabric which consists of one or more ASMs) the ASP has to perform a cell synchronization for each one of the 8 input lines (4 input lines per plane 0 and plane 1).The first octet of the SLIF cell format (see page 93), so called SYNC-octet, is used by the ASP to derive cell synchronization. The SYNC-octet is a fixed bit pattern (so it can be recognized by the ASP as the first octet of a cell, respectively) where the MSB is toggled at each cell (i.e. SYNC-octet value = 1110 1000($E8_H$) or 0110 1000(68_H)). This is necessary to avoid that an other octet (which accidentally has the same bit pattern) of a cell will be incorrectly recognized by the ASP as the SYNC-octet.

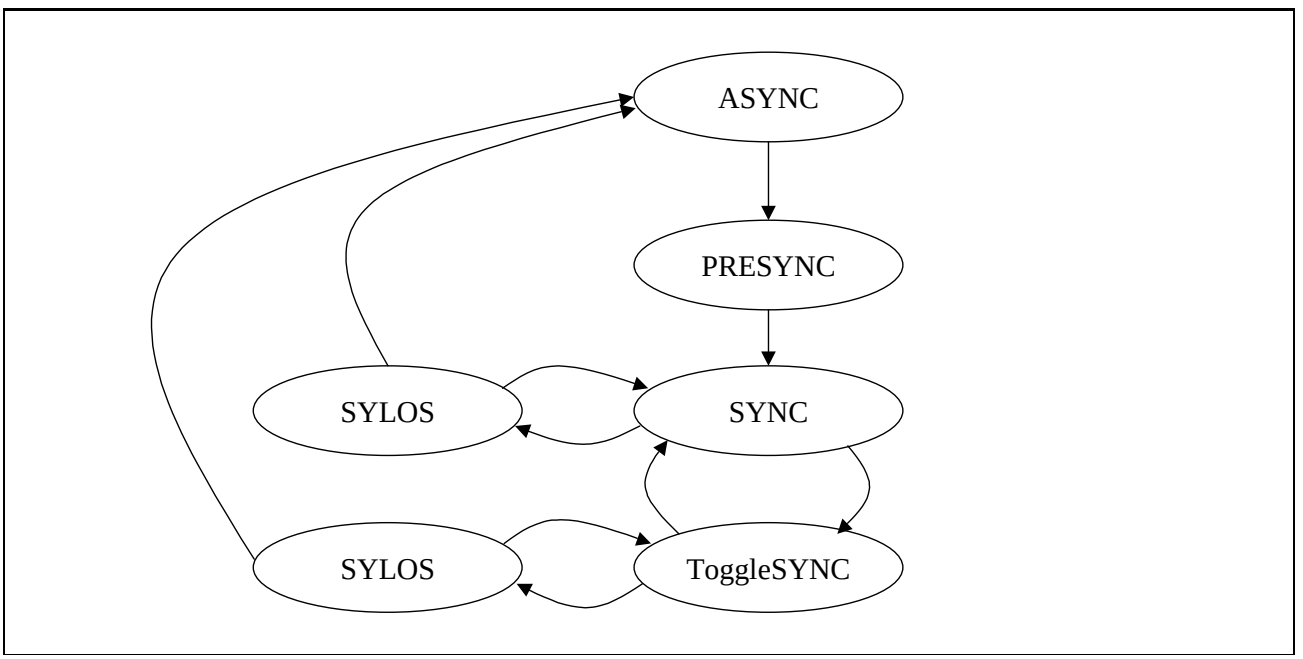


Figure 14 State Diagram of Cell Synchronization Algorithm

In **Figure 14** the possible states of the synchronization algorithm are depicted. By initialization the ASP are in the state ASYNC (input lines are asynchronous) and moves into state PRESYNC. The transition to state SYNC (the input line is synchronous, respectively) only happens if the SYNC-octet has been recognized in 3 subsequently arrived cells. If the SYNC-octets of the following cells are recognized then there are only transitions between the states SYNC and ToggleSYNC (combination 0/0 in **Table 3**; in

both states the corresponding input line is synchronous). For the first time the SYNC-octet can't be recognized the transition from SYNC/ToggleSYNC to state SYLOS happens but the corresponding input line is still synchronous. The corresponding bit of SYLOS(7:0), page 58 is set to '1' (combination 1/0 in **Table 3**). Even if the SYNC-octet of the following cell can't be matched then transition to state ASYNC occurs. The corresponding bit of ASYN(7:0), page 58 is set to '1' (combination 1/1 in **Table 3**). Otherwise there is a retransition to the state SYNC/ToggleSYNC.

Table 3 Possible Combinations of the SYLOS- and ASYN-Bit of each Input Line (SYLOS(7:0) and ASYN(7:0) of Register LINSTAT, page 58)

SYLOS-Bit/ASYN-Bit	Description
0/0	Cell synchronization works (synchronous)
1/0	Cell synchronization still works (synchronous)
0/1	There was never cell synchronization (asynchronous)
1/1	Cell synchronization not longer exists (asynchronous)

1.13 Recombining Function

This function recombines the two cell streams from the ASN planes, which may be partially redundant, into one unique cell stream. It includes supervising functions of the two planes to avoid cell duplication and cell loss. In particular it covers the following features:

- recombining function for redundant cell streams on a connection basis
- acceptance of non-redundant cell streams on a connection basis
- mixture of redundant and non-redundant connections
- the possibility to disable the recombining algorithm globally and hard select either plane 0 or plane 1 only
- the possibility to select per connection if all cells from both planes are accepted
- the support of Line Protection Switchover LPS
- monitoring of the quality of a plane with the condition monitor
- detection of a failed or missing plane using the dead plane monitor.

The recombining function includes 4 algorithms:

- cell acceptance algorithm
- dead plane monitor
- condition monitor
- line protection switch (LPS) function.

The **cell acceptance** algorithm assures that the cells from the two serial input bundles are recombined in an appropriate way. It interprets the sequence number of the ATM

cells coming from the two input planes. The sequence number together with measured performance parameters and configuration parameters determine if a cell is accepted or discarded.

The algorithm basically sticks to the leading plane even if sequence numbers are missing. A transition to the other plane normally occurs only when the slower plane overtakes the faster one. Then the next expected sequence number first comes from the former inactive plane which thus becomes the new leading plane.

The cell acceptance has the following configurations which can be selected for the whole chip and per connection

- normal sequence algorithm for hitless cell-by-cell redundancy
- disable of sequence algorithm (all cells from both planes are accepted)
- single plane mode (cells are accepted from one plane only, used for load sharing)

The cell acceptance algorithm also relies on measures of two algorithms measuring the performance of the ASN:

The **condition monitor** measures per connection the quality of an ASN plane concerning cell losses. If e.g. the faster plane often loses cells - which results in missing sequence numbers - the condition monitor declares the quality as poor, and the cell acceptance algorithm uses this information as an additional decision criterion. This could result in a transition to the other plane.

To detect missing cells the condition monitor uses the 6 LSBs of the sequence number. For each missing cell a counter is decremented by a programmable value (default ?) and for each cell in-sequence the counter is incremented by another programmable value (default ?). If the counter reaches zero the quality is declared as poor. To come back to good quality the counter must be incremented up to the maximum value again (hysteresis).

The **dead plane monitor** detects on a connection basis if an ASN plane does not deliver any cells. It uses a 4-bit counter for each plane. Each time a cell from a plane is received the counter of the other plane is incremented and the counter for this plane is reset to zero. If a counter reaches 15, an immediate jump to the other plane is initiated and in addition the quality is declared as poor. If cells are coming again from the dead plane the counter is reset to zero, but the quality is still poor. The former dead plane must first reach good quality according to the condition monitor.

The **LPS function** is basically the detection of Protection Switch Identifier (PSI) cells. If a switchover is enabled via the µP interface the first arriving PSI cell initiates the switchover. After that only cells from the new connection class are accepted. The two connection classes 0 and 1 are defined in the downstream external connection RAM. The LPS function can switch in both directions, from 0 to 1 and back again.

1.14 Line Protection Switch (LPS) Mechanism

The **LPS** mechanism uses a configuration with two redundant LICs connected to a PXB 4310 E ASM as shown in **Figure 15** for the downstream data flow. Both LICs must be connected to the same ASM, which in a multi-stage switch is in the last stage. In both LICs all connections of both classes are set-up. One class is used for redundant, the other for non-redundant connections. In normal operation the redundant connections are routed to the LIC #1, the non-redundant to LIC #2.

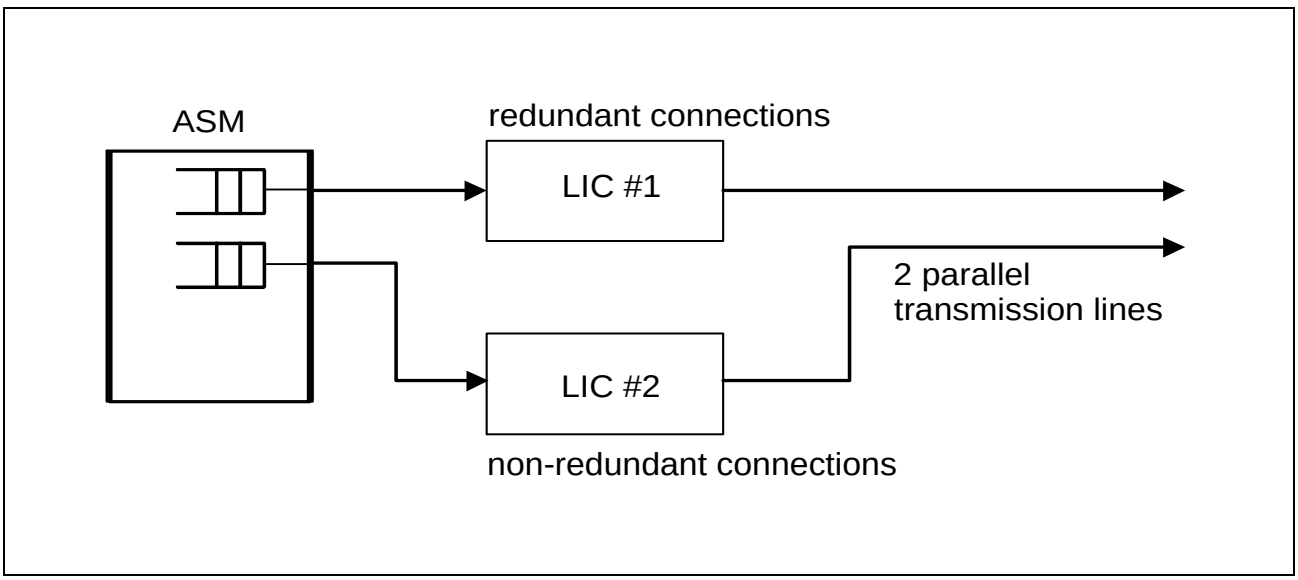


Figure 15 Redundant LIC Configuration in Normal Case (Downstream Direction)

If one of the transmission lines or one of the LICs fails the control SW of the switch initiates a switchover to the redundant LIC if necessary. If e.g. LIC #1 or the associated transmission line fails, the redundant connections are re-routed to LIC #2 and the non-redundant connections are dropped. This behavior has the advantage that the redundant line and the LIC can be used most of the time.

Disadvantage is that on both lines only half of the connections (LCI values) can be used. The LCI range must be divided into an upper and a lower half to support the switchover.

The switch control SW initiates a switchover via 2 commands:

1. In downstream direction the output queues of the PXB 4310 E ASM are connected to other outputs as shown in **Figure 16**.

2. In upstream direction the PXB 4350 E ALP switches from upper to lower half of the connection table or vice-versa. See the PXB 4350 E ALP data sheet for details.

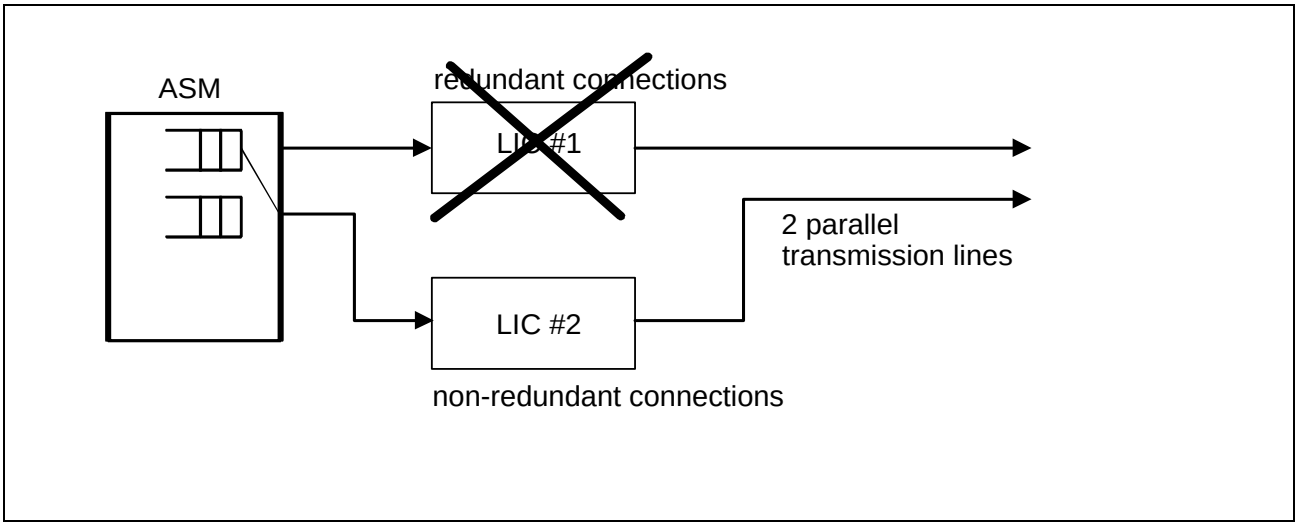


Figure 16 Redundant LIC Configuration in Failure Case (Upstream Direction)

The memory allocation for the ASP connection tables for the three possible cases: both LICs operating, LIC #1 failure and LIC #2 failure is shown in **Table 4**. In this table it is assumed that the lower memory range holds the redundant connections (LCIs).

	both LICs operating		LIC 1 failure		LIC 2 failure	
	redun-dant	status	redun-dant	status	redun-dant	status
LIC #1						
upper memory	no	inactive			no	inactive
lower memory	yes	active			yes	active
LIC #2						
upper memory	no	active	no	inactive		
lower memory	yes	inactive	yes	active		

Table 4 LIC Memory Overview for 3 Cases

This allocation of connections/LCI values within the connection tables is also valid for the PXB 4350 E ALP, PXB 4340 E AOP and PXB 4330 E ABM if they are used on the LIC.

1.15 Clocks

The ASP has the following clocks:

- main operating clock is the system clock SYSCLK of up to 51.84 MHz
- 1 high speed clock of 207.36 MHz exists for the 3 independent data paths: transmit, receive plane 0 and receive plane 1. High speed clock and main operation clock must be derived from the same clock source.
- the common UTOPIA clock for up- and downstream interface can be asynchronous to the system clock and has an upper limit of 51.84 MHz; it must be less than or equal to SYSCLK
- the microprocessor accesses are asynchronous to the SYSCLK
- the RSATM interface uses a clock of nominally 25.92 MHz which must be SYSCLK/2.

2 Register Description

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
Receive Cell Buffer Access Register					
00	RXR	Receive Cell Buffer Access Register	r	0000_H	43
Configuration Registers					
01	CONGEN	General Configuration Register	r/w	0000_H	45
02	CONFUP0	Configuration Register Upstream 0	r/w	0100_H	46
03	CONFUP1	Configuration Register Upstream 1	r/w	0000_H	47
04	UINTHED	Upstream Internal Header Register	r/w	0000_H	48
05	CONFDN	Configuration Register Downstream	r/w	0000_H	49
28	MCOF	Multicast RAM Part Offset Register	r/w	0060_H	61
29	QLEN	Queue Length Register High/Low Priority	r/w	$C080_H$	61
2A	MCRANGE	Internal Pointer RAM Location	r/w	0018_H	62
3D	RPCALG	RPC Algorithm Register	r/w	4003_H	74
Command Register					
06	CMR	Command Register	r/w	0000_H	50
Interrupt/Mask Registers					
07	ISR0	Interrupt Status Register 0	clear on write *)	0000_H	52
08	ISR1	Interrupt Status Register 1	clear on write *)	0000_H	53
09	IMR0	Interrupt Mask Register 0	r/w	0000_H	55
0A	IMR1	Interrupt Mask Register 1	r/w	0000_H	55
0B	UINTADR	Interrupt Header Capture Register Upstream	r	0000_H	56

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
0C	DHCR0	Downstream Header Capture 0	r	0000_H	56
0D	DHCR1	Downstream Header Capture 1	r	0000_H	57
0E	LINSTAT	High Speed Input Line Status	clear on read ***)	0000_H	58
0F	FECR	FCS1+FCS2 Error Counter Register	clear on read ***)	0000_H	59
Celltype Recognition/Mask Registers					
10	CTR00U	Cell Type 1 Recognition Register 0 upstream	r/w	0000_H	59
11	CTR01U	Cell Type 1 Recognition Register 1 upstream	r/w	0000_H	59
12	CTR02U	Cell Type 1 Recognition Register 2 upstream	r/w	0000_H	59
13	CTM00U	Cell Type 1 Mask Register 0 upstream	r/w	0000_H	59
14	CTM01U	Cell Type 1 Mask Register 1 upstream	r/w	0000_H	59
15	CTM02U	Cell Type 1 Mask Register 2 upstream	r/w	0000_H	59
16	CTR10U	Cell Type 2 Recognition Register 0 upstream	r/w	0000_H	59
17	CTR11U	Cell Type 2 Recognition Register 1 upstream	r/w	0000_H	59
18	CTR12U	Cell Type 2 Recognition Register 2 upstream	r/w	0000_H	59
19	CTM10U	Cell Type 2 Mask Register 0 upstream	r/w	0000_H	59
1A	CTM11U	Cell Type 2 Mask Register 1 upstream	r/w	0000_H	59
1B	CTM12U	Cell Type 2 Mask Register 2 upstream	r/w	0000_H	59
1C	CTR00D	Cell Type 1 Recognition Register 0 downstream	r/w	0000_H	59
1D	CTR01D	Cell Type 1 Recognition Register 1 downstream	r/w	0000_H	59
1E	CTR02D	Cell Type 1 Recognition Register 2 downstream	r/w	0000_H	59

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
1F	CTM00D	Cell Type 1 Mask Register 0 downstream	r/w	0000_H	59
20	CTM01D	Cell Type 1 Mask Register 1 downstream	r/w	0000_H	59
21	CTM02D	Cell Type 1 Mask Register 2 downstream	r/w	0000_H	59
22	CTR10D	Cell Type 2 Recognition Register 0 downstream	r/w	0000_H	59
23	CTR11D	Cell Type 2 Recognition Register 1 downstream	r/w	0000_H	59
24	CTR12D	Cell Type 2 Recognition Register 2 downstream	r/w	0000_H	59
25	CTM10D	Cell Type 2 Mask Register 0 downstream	r/w	0000_H	59
26	CTM11D	Cell Type 2 Mask Register 1 downstream	r/w	0000_H	59
27	CTM12D	Cell Type 2 Mask Register 2 downstream	r/w	0000_H	59
Upstream Connection RAM Data/Address Registers					
2C	URAM0L	Upstream RAM data register 0 (15:0)	r/w	0000_H	64
2D	URAM0H	Upstream RAM data register 0 (31:16)	r/w	0000_H	64
2E	URAM1L	Upstream RAM data register 1 (15:0)	r/w	0000_H	64
2F	URAM1H	Upstream RAM data register 1 (31:16)	r/w	0000_H	64
30	URAM2L	Upstream RAM data register 2 (15:0)	r/w	0000_H	64
31	URAM2H	Upstream RAM data register 2 (31:16)	r/w	0000_H	64
32	URADR	Address for Upstream RAM Entry	r/w	0000_H	66
Downstream Connection RAM Data/Address Registers					
33	DRADR	Address for Downstream RAM Entry	r/w	0000_H	67
34	DRAM0L	Downstream RAM data register 0 (15:0)	r/w	0000_H	67

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
35	DRAM0H	Downstream RAM data register 0 (31:16)	r/w	0000_H	67
36	DRAM1L	Downstream RAM data register 1 (15:0)	r/w	0000_H	67
37	DRAM1H	Downstream RAM data register 1 (31:16)	r/w	0000_H	67
38	DRAM2L	Downstream RAM data register 2 (15:0)	r/w	0000_H	67
39	DRAM2H	Downstream RAM data register 2 (31:16)	r/w	0000_H	67
Internal Translation Table Registers					
3A	PRAMADR	Pointer RAM Address	r/w	0000_H	72
3B	PRAMPT	Pointer RAM Pointer +E-Bit Entry	r/w	0000_H	73
3C	PRAMLCI	Pointer RAM LCI Entry	r/w	0000_H	73
Upstream/Downstream UTOPIA Transmit Registers					
2B	TXQSEL	TXR Queue Select Register	r/w	0000_H	63
40	TXR0	Cell Header for Upstream/Downstream Insertion	r/w	0000_H	75
41	TXR1	Cell Header for Upstream/Downstream Insertion	r/w	0000_H	75
42	TXR2	Cell Header for Upstream/Downstream Insertion	r/w	0000_H	75
43	TXR3	Cell Payload (TXR3..27)	r/w	0000_H	76
44	TXR4	Cell Payload (TXR3..27)	r/w	0000_H	76
45	TXR5	Cell Payload (TXR3..27)	r/w	0000_H	76
46	TXR6	Cell Payload (TXR3..27)	r/w	0000_H	76
47	TXR7	Cell Payload (TXR3..27)	r/w	0000_H	76

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
48	TXR8	Cell Payload (TXR3..27)	r/w	0000_H	76
49	TXR9	Cell Payload (TXR3..27)	r/w	0000_H	76
4A	TXR10	Cell Payload (TXR3..27)	r/w	0000_H	76
4B	TXR11	Cell Payload (TXR3..27)	r/w	0000_H	76
4C	TXR12	Cell Payload (TXR3..27)	r/w	0000_H	76
4D	TXR13	Cell Payload (TXR3..27)	r/w	0000_H	76
4E	TXR14	Cell Payload (TXR3..27)	r/w	0000_H	76
4F	TXR15	Cell Payload (TXR3..27)	r/w	0000_H	76
50	TXR16	Cell Payload (TXR3..27)	r/w	0000_H	76
51	TXR17	Cell Payload (TXR3..27)	r/w	0000_H	76
52	TXR18	Cell Payload (TXR3..27)	r/w	0000_H	76
53	TXR19	Cell Payload (TXR3..27)	r/w	0000_H	76
54	TXR20	Cell Payload (TXR3..27)	r/w	0000_H	76
55	TXR21	Cell Payload (TXR3..27)	r/w	0000_H	76
56	TXR22	Cell Payload (TXR3..27)	r/w	0000_H	76
57	TXR23	Cell Payload (TXR3..27)	r/w	0000_H	76
58	TXR24	Cell Payload (TXR3..27)	r/w	0000_H	76
59	TXR25	Cell Payload (TXR3..27)	r/w	0000_H	76
5A	TXR26	Cell Payload (TXR3..27)	r/w	0000_H	76
5B	TXR27	Cell Payload (TXR3..27)	r/w	0000_H	76

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
UTOPIA Configuration Registers					
5C	CONUT0	Utopia Configuration Register 0	r/w	0000_H	77
5D	CONUT1	Utopia Configuration Register 1	r/w	0000_H	78
5E	CONUT2	Utopia Configuration Register 2	r/w	0000_H	78
Test Registers					
60	DITC1L	Downstream Test Connection Register 1 Low Word	r/w	0000_H	79
61	DITC1H	Downstream Test Connection Register 1 High Word	r/w	0000_H	79
62	DITC2L	Downstream Test Connection Register 2 Low Word	r/w	0000_H	79
63	DITC2H	Downstream Test Connection Register 2 High Word	r/w	0000_H	79
64	UITC0L	Upstream Test Connection Register 1 Low Word	r/w	0000_H	80
65	UITC0H	Upstream Test Connection Register 1 High Word	r/w	0000_H	80
66	UITC1L	Upstream Test Connection Register 2 Low Word	r/w	0000_H	80
67	UITC1H	Upstream Test Connection Register 2 High Word	r/w	0000_H	80
68	UITC2L	Upstream Test Connection Register 3 Low Word	r/w	0000_H	80
69	UITC2H	Upstream Test Connection Register 3 High Word	r/w	0000_H	80
6A	TSTR0	Test Register 0	r/w	0079_H	81
6B	TSTR1	Test Register 1	r/w	0002_H	82
6C	TSTR2	Test Register 2	r/w	$00A0_H$	83
70	RBDONE0	RAM BIST Done Bits 0	clear on write **)	0000_H	83

Table 5 ASP Registers Overview

adr (hex)	register	description	µP	reset value	see page
71	RBDONE1	RAM BIST Done Bits 1	clear on write **)	0000_H	83
72	RBERRN0	RAM BIST ERRN Bits 0	clear on write **)	$7FFF_H$	83
73	RBERRN1	RAM BIST ERRN Bits 1	clear on write **)	$00FF_H$	84
ASP Version Registers					
6E	VERL	Version Register Low	r	4083_H	83
6F	VERH	Version Register High	r	1003_H	83

*Note: *) Single bits of this register can be reset by writing a '1' to them.*
***) A reset of this register occurs at each write access.*
****) A reset of this register occurs at each read access.*

Note: The addresses $3E_H$, $3F_H$, $5F_H$, $6D_H$ are reserved and 74_H...$7F_H$ are unused. Reset value 0000_H for all. Don't write in normal operation.

Note: Reserved bits can be read and written by the µP. Unused bits are not implemented as flip-flops, they can not be written by the µP and always read as zero.

2.1 Receive Cell Buffer Access Register (RXR)

Read only Address 00_H
Value after reset 0000_H

15							8
High byte(7:0)							
7							**0**
Low byte (7:0)							

Read cells from receive buffers, received from up- or downstream direction.

Read access to register RXR results in undefined values in the case that the receive buffer is empty.

The receive cell formats are illustrated in **figure 17**:

high 16-bit word 15					0	low 16-bit word 15									0
LCI/VPI(11:0)						VCI(15:0)								PT	C
LCIM	HK(2:0)		PN(2:0)	0 0 0	PNUT(4:0)	Payload Octet 1					Payload Octet 2				
Payload Octet 3				Payload Octet 4		Payload Octet 5					Payload Octet 6				
Payload Octet 7				Payload Octet 8		Payload Octet 9					Payload Octet 10				
...				...		...					...				
Payload Octet 43				Payload Octet 44		Payload Octet 45					Payload Octet 46				
Payload Octet 47				Payload Octet 48		F	S	R			D	L	INP	CT	

(shaded fields are unused)
C: CLP bit
PT: Payload Type bits
LCIM: LCI bit 13,12
HK: House Keeping bits
PN: PN of PADACK
PNUT: Port Number from UTOPIA
D: Direction bit, D='0' for upstream direction
CT: Cell Type recognition bits

high 16-bit word 15					0	low 16-bit word 15									0
LCI/VPI(11:0) or 00h						VCI(15:0) or 0,0,LCI(13:0)								PT	C
LCIM	HK(2:0)		PN(2:0)	0 0 0	PNUT(4:0)	Payload Octet 1					Payload Octet 2				
Payload Octet 3				Payload Octet 4		Payload Octet 5					Payload Octet 6				
Payload Octet 7				Payload Octet 8		Payload Octet 9					Payload Octet 10				
...				...		...					...				
Payload Octet 43				Payload Octet 44		Payload Octet 45					Payload Octet 46				
Payload Octet 47				Payload Octet 48		F	S	R			D	L	INP	CT	

(shaded fields are unused)
C: CLP bit
PT: Payload Type bits
LCIM: LCI bit 13,12
HK: House Keeping bits
PN: PN of PADACK
PNUT: Port Number from UTOPIA
S: RMS, Redundant Module Sender
R: RMR, Redundant Module Receiver
D: Direction bit, D='1' for downstream direction
L: Plane Bit
INP: Input Number
CT: Cell Type recognition bits

Figure 17 Receive Cell Formats

2.2 General Configuration Register (CONGEN)

Read/write Address 01_H
Value after reset 0000_H

15							8
unused							
7							**0**
unused							TSTEN

TSTEN Enables test mode:

0 Registers TSTRn (n=0..2) are read only. Used for normal operation.

1 Write access to registers TSTRn (n=0..2) enabled. (For test purposes only.)

2.3 Configuration Register Upstream 0 (CONFUP0)

Read/write Address 02_H
Value after reset 0100_H

15				8
unused				BIP8DIS
7				**0**
reserved	GEN1	GEN0	UTMULT(2:0)	LCIMOD(1:0)

BIP8DISC — If this bit is set cells received at the RSATM interface with BIP-8 error are discarded. If cleared cells are accepted regardless of the BIP-8.

GEN(1:0) — Global plane enable bits for plane 1 and 0, respectively :

- GEN(0)='0' Output bundle of plane 0 only outputs empty cells, cells from TXR and RSATM cells.
- GEN(0)='1' Normal operation.
- GEN(1)='0' Output bundle of plane 1 only outputs empty cells, cells from TXR and RSATM cells.
- GEN(1)='1' Normal operation.

UTMULT(2:0) — Specifies multiplexing of LCI or VPI with port numbers PN (IWE8) or PNUT (UTOPIA port number) to construct the LCI. Option 00x is used if the LCI is provided by the ALP, option 01x is appropriate if the IWE8 is connected to the ASP; the other options allow the direct connection of PHYs to the ASP.

- 00x LCI(13:0) = LCI(13:0) unchanged
- 01x LCI(13:0) = VPI(10:0) x 8 + PN(2:0)
- 100 LCI(13:0) = VPI(11:0) x 4 + PNUT(1:0)
- 101 LCI(13:0) = VPI(10:0) x 8 + PNUT(2:0)
- 110 LCI(13:0) = VPI(9:0) x 16 + PNUT(3:0)
- 111 LCI(13:0) = VPI(8:0) x 32 + PNUT(4:0)

LCIMOD(1:0) — Specifies the location of the LCI in the cell. Option 1x is appropriate if the ALP is used.

- 00 LCI(11:0) in VPI field, HK from UINTHEAD.
- 01 LCI(13:0) in VCI field, HK from UINTHEAD.
- 1x LCI(11:0) in VPI field, LCI(13:12) in UDF1(7:6), HK from cell.

2.4 Configuration Register Upstream 1 (CONFUP1)

Read/write Address 03_H
Value after reset 0000_H

15							8
unused						UTOP LOOP	UBMOD(1:0)

7							0
SLOUTEN(7:0)							
Line 3	Line 2	Line 1	Line 0	Line 3	Line 2	Line 1	Line 0
Output group 1				Output group 0			

UTOPLOOP Enable internal data loop downstream to upstream:

0 Loop disabled, normal operating mode

1 Loop from UTOPIA downstream to UTOPIA upstream enabled. Downstream data is monitored at the downstream UTOPIA interface, upstream UTOPIA interface does not accept data.

UBMOD(1:0) Upstream SLIF bundle configuration:

00 Bundle of one single SLIF line (line 0).

01 Bundle of 2 SLIF lines (lines 0 and 1).

1x Bundle of 4 SLIF lines (lines 0..3).

SLOUTEN(7:0) Enable/disable the 8 output lines. Each bit enables/disables the respective output line:

0 SLIF output is disabled and provides a constant low level

1 SLIF output enabled

2.5 Upstream Internal Header Register (UINTHED)

Read/write Address 04_H
Value after reset 0000_H

15			8
unused			
7			**0**
unused	Res(6:4)	RMS	HK(2:0)

Contains fixed bits of SLIF cell header for all cells (**see Figure 26**).

Res(6:4) Reserved bits 7, 2 and 1 of octet 1 of SLIF cell.

RMS Redundant Module Sender

HK(2:0) Housekeeping bits
These bits are inserted into the appropriate bit fields of the SLIF cell format:

value	description	action
000	empty cell	discarded by DBC
001	internal test cell (ITC)	extract in DWB
011	maintenance control cell (MTC)	to RSATM interface
110	ITP, communication cell	to RSATM interface
111	user cell	to Workbench (UTOPIA)

(not documented values are reserved)

2.6 Configuration Register Downstream (CONFDN)

Read/write Address 05_H
Value after reset 0000_H

15			8
ACS-PAUSEN	LCIMOD(1:0)	SLINEN(7:3)	

7			0
SLINEN(2:0)	RPCE	LOOP(1:0)	DBMOD(1:0)

ACSPAUSEN — Enable bit 11 of RPCALG register (for conditional and global single mode only).

LCIMOD(1:0) — LCIMOD for Downstream Workbench (DWB):

- 00 LCI in high dword.
- 01 LCI in VCI field.
- 1x LCI in high dword.

SLINEN(7:0) — Enable/disable the SLIF inputs of plane 1 and plane 0 independent on selected bundle and loop mode. :

- xxxxxxx1 Line0, plane 0 enabled.
- xxxxxx1x Line1, plane 0 enabled.
- xxxxx1xx Line2, plane 0 enabled.
- xxxx1xxx Line3, plane 0 enabled.
- xxx1xxxx Line0, plane 1 enabled.
- xx1xxxxx Line1, plane 1 enabled.
- x1xxxxxx Line2, plane 1 enabled.
- 1xxxxxxx Line3, plane 1 enabled.

RPCE — Selects ADI bit for multicast identification:

- 0 Normal mode, ADI(1) denotes multicast cells in ASP, ADI(0) in ASM.
- 1 Backward compatibility mode to work together with ASP-up, ADI(0) identifies multicast.

LOOP(1:0) — Selects internal loop from upstream to downstream for plane 1 and 0. :

- x1 Plane 0 is looped.
- 1x Plane 1 is looped.

DBMOD(1:0) Downstream bundle configuration:

00 Bundle of one single SLIF line (line 0).
01 Bundle of 2 SLIF lines (lines 0 and 1).
1x Bundle of 4 SLIF lines (lines 0..3).

2.7 Command Register (CMR)

Read/write Address 06_H
Value after reset 0000_H

15				8
SRES	EXERR	ERRSEL(2:0)	PRAMACC(1:0)	DRA-MACC(2)

7				0
DRAMACC(1:0)	DRAM-SEL	URAMACC(2:0)	TRANSM	DIR

SRES Soft reset:

1 Resets the whole chip. SRES is reset automatically after execution (0.2ms). During this period the ASIC cannot accept any data from any interface.

EXERR

1 Generates the error specified by ERRSEL. Cleared after execution. A set bit cannot be cleared by the µ*P*.

ERRSEL(2:0)

000 SYNCER0: a single sync octet error on both planes for line 0.
001 SYNCER1: a single sync octet error on both planes for line 1.
010 SYNCER2: a single sync octet error on both planes for line 2.
011 SYNCER3: a single sync octet error on both planes for line 3.

100 BIP8ERR: a single false BIP-8 in the next cell transmitted at the RSATM interface.
101 TXPERR: a single parity error in the parity bit P of the next cell sent out via TXR in upstream direction.
11x Unused, i.e. no action, EXERR is reset immediately.

PRAMACC(1)

1 Start access to internal pointer RAM. Cleared after execution. A set bit can not be cleared by the µP.

PRAMACC(0) Specify type of access to internal pointer RAM:

0 Read from RAM to register.
1 Write from register to RAM.

DRAMACC(2)

1 Start access to downstream external RAM. Cleared after execution. A set bit can not be cleared by the µP.

DRAMACC(1:0) Specifies type of downstream external RAM access:

00 Read 3 dwords.
01 Write 3 dwords.
10 Write dword 0 only.
11 Read dword 0 only.

DRAMSEL Specifies lower or upper address range of downstream external RAM, MSB to DRADR:

0 Lower range, 0...64K-1.
1 Upper range, 64K...128K-1.

URAMACC(2)

1 Start access to upstream external RAM. Cleared after execution. A set bit can not be cleared by the µP.

URAMACC(1:0) Defines type of upstream external RAM access:

00 Read 3 dwords.
01 Write 3 dwords.
1x Write dword 1 and 2.

TRANSM

1 Insert cell from TXR into cell stream. Cleared after execution. A set bit can not be cleared by the µP.

DIR Direction of inserted cell:

0 Upstream
1 Downstream; for downstream cell insertion a UTOPIA port must be selected using the TXQSEL register.

2.8 Interrupt Status Register 0 (ISR0)

Clear on write Address 07_H
Value after reset 0000_H

15							8
unused					PSS	BUFERR	UT-PRTY-ERR
7							**0**
UTSO-CERR	BIPERR	BEMPTY	BOV	ITQOVER	RXR-DOVER	RXRUO VER	RXRA-VAIL

Unlike typical Interrupt registers, Interrupt bits can be individually cleared by writing a ’1’. Writing a ’0’ does not affect the bit. In case of a static interrupt which could be still valid as RXCEL and BEMPTY, the bit will be reset again immediately by the ASP, so that for the µP it appears to be permanently set. RXCEL can only be cleared after complete readout of the receive buffer, BEMPTY can not be cleared as long as the shared buffer is empty. After reset this bit will be set immediately so that ISR0 reads as 0020.

PSS

1 Indicates that a plane switchover occurred but without prior reception of PSI cell.

BUFERR

1 Severe buffer error detected in the Downstream Shared Buffer (DSB) (MCCNT=’1F’).

UTPRTYERR

1 Parity error detected at UTOPIA upstream interface.

UTSOCERR

1 Start of cell error detected at UTOPIA upstream interface.

BIPERR

1 Bip-8 error detected at the RSATM input.

BEMPTY

1 Indicates that the shared buffer is empty (static interrupt).

BOV

1 Total shared buffer overflow.

ITQOVER

1 Overflow ITP queue.

RXRDOVER

1 Overflow receive buffer downstream.

RXRUOVER

1 Overflow receive buffer upstream.

RXRAVAIL

1 Cell available for readout in one of the receive buffers (static interrupt).

2.9 Interrupt Status Register 1 (ISR1)

Clear on write Address 08_H
Value after reset 0000_H

15						8
reserved			PHYIND(4:0)			
7						**0**
DSBOV	UTBU-FOV	reserved	PLASYN1	PLASYN0	DCPINT	URAMER

Interrupts in this register occur together with a load of the respective RAM address in the header capture registers UINTADR for upstream, DHCR0 and DHCR1 for downstream. After the first interrupt the respective registers are blocked and further interrupt events are lost until the µP has cleared the respective interrupt bit by writing a ’1’ to it. Up- and downstream side interrupts have independent header capture registers.

PHYIND(4:0) Encodes the queue/port number in case of QEVNT or TQOV. These Bits are locked until QEVNT or TQOV have been cleared by the µP; to which of the interrupts PHYIND belongs is selected with the OVSEL bit in the MCRANGE register. If more than one queue overflow at the same time (multicast) the queue with the lower number is indicated.

DSBOV

1 DSB queue overflow or low threshold overflow (selected by MCRANGE register, address 2A).

UTBUFOV

1 Utopia buffer overflow.

PLASYN1

1 One of the active lines of plane 1 (ASYN7..4 in register LINSTAT) is asynchronous, e.g. case DBMOD=00: PLASYN0=ASYN(4), case DBMOD=01: PLASYN0=ASYN(4) or ASYN(5), case DBMOD=1x: PLASYN0=ASYN(4) or ASYN(5) or ASYN(6) or ASYN(7).

PLASYN0

1 One of the active lines of plane 0 (ASYN3..0 in register LINSTAT) is asynchronous, e.g. case DBMOD=00: PLASYN0=ASYN(0), case DBMOD=01: PLASYN0=ASYN(0) or ASYN(1), case DBMOD=1x: PLASYN0=ASYN(0) or ASYN(1) or ASYN(2) or ASYN(3).

DCPINT

1 An error condition at the downstream address translation occurred. Locks DHCR0, DHCR1 which contain error type and connection identification.

URAMER

1 Error upstream external RAM; locks UINTADR which identifies the connection.

2.10 Interrupt Mask Register 0 and 1 (IMR0 and IMR1)

These bits have a one-to-one correspondence with the respective interrupt status register. They have no effect on the setting and clearing of the interrupt bits, but influence only the INT_n pin. Normally all interrupt bits are ored together and the result is output (inverted) as INT_n. Masking an interrupt has the effect that this interrupt bit does not contribute to the OR function. If all interrupt bits are masked the INT_n line will become inactive. An interrupt bit is masked if the corresponding mask bit is cleared.

2.10.1 Interrupt Mask Register 0 (IMR0)

Read/write Address 09_H
Value after reset 0000_H

15							8
unused							IRM0(10:8)
7							**0**
IMR0(7:0)							

IMR0(i) i = [0..10]:
0 Interrupt i masked.
1 Interrupt i enabled.

2.10.2 Interrupt Mask Register 1 (IMR1)

Read/write Address $0A_H$
Value after reset 0000_H

15							8
IMR1(15:8)							
7							**0**
IMR1(7:0)							

IMR1(i) i = [0..15]:
0 Interrupt i masked.
1 Interrupt i enabled.

2.11 Interrupt Header Capture Register Upstream (UINTADR)

Read only Address $0B_H$
Value after reset 0000_H

15							8
VCON-ERR	PRTY-ERR	LCI(13:8)					
7							**0**
LCI(7:0)							

VCONERR

1 RAM access to invalid connection detected.

PRTYERR

1 Parity error at upstream RAM detected.

LCI(13:0) This is the LCI after transformation using port numbers (LCIMOD and UTMULT bits).

2.12 Downstream Header Capture 0 (DHCR0)

Read only Address $0C_H$
Value after reset 0000_H

15							8
EMCI(15:8)							
7							**0**
EMCI(7:0)							

EMCI(15:0)

2.13 Downstream Header Capture 1 (DHCR1)

Read only Address $0D_H$
Value after reset 0000_H

15							8
CLP	HK(2:0)			ADI(1:0)		CDP(1:0)	
7							**0**
RMS	unused	HEACAP	PLANE	INV-CONN	RAM-PARER	ADDER	FCS2ER

The least significant 4 bit of this register indicate the type of error occurred. More than one error may occur with one cell.

CLP Cell Loss Priority bit

HK(2:0) Housekeeping bits

ADI(1:0) Address Identifier

CDP(1:0) Cell Delay Priority

RMS Redundant Module Sender

HEACAP Error source:
0 Header capture caused by cell access.
1 Header capture caused by µP access.

PLANE Plane Bit.

INVCONN Invalid connection (VCON=0).

RAMPARER RAM parity error.

ADDER Address error.

FCS2ER FCS2 error.

2.14 High Speed Input Line Status (LINSTAT)

Clear on read Address $0E_H$
Value after reset 0000_H

15							8
SYLOS(7:0)							
7							**0**
ASYN(7:0)							

These bits are set with the first occurrence of the respective event. They must be cleared by the µP by a read access. The bits are set also in the case the respective input is disabled.

SYLOS(7:0) Each of the 8 bits represents one of the 8 input lines.
SYLOS(3:0) represents the 4 input lines of plane 0 and SYLOS(7:4) of plane 1.

1 This input line is in the state SYLOS of the cell synchronization algorithm (see page 30 and **Table 3**)

ASYN(7:0) Each of the 8 bits represents one of the 8 input lines.
ASYN(3:0) represents the 4 input lines of plane 0 and ASYN(7:4) of plane 1.

1 This input line is in the state ASYN of the cell synchronization algorithm, i.e. it is asynchronous (see page 30 and **Table 3**)

2.15 FCS1+FCS2 Error Counter Register (FECR)

Clear on read Address $0F_H$
Value after reset 0000_H

15							8
FEC1(7:0)							
7							**0**
FEC0(7:0)							

These counters are incremented each time a FCS error is detected, either in the internal cell header (FCS1) or cell payload (FCS2). They are cleared by a µP read access of FEC.

FEC1(7:0) Error counter FCS1+FCS2 errors plane 1.

FEC0(7:0) Error counter FCS1+FCS2 errors plane 0.

Note: These counters do not stop at 255, but continue at 0 with the next error. Hence the microprocessor should read FECR frequently enough to avoid multiple overruns.

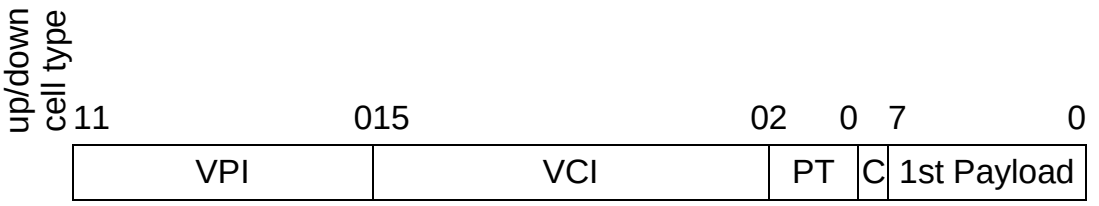
2.16 Cell Type Recognition Register/Mask Register (CTRxyz, CTMxyz)

Read/write Address 10_H to 27_H
Value after reset 0000_H

The 24 registers are used for detecting special ATM cells, for up- and downstream side . It is possible to compare the passing ATM cells with two pre-programmed pattern with an associated mask register set to mask each individual bit of the pattern. The pattern includes the 4 header octets plus the first payload octet.

Each comparision bit has an associated mask bit. If the mask bit is set to ’1’ the corresponding bit of cell filter register is don’t care for cell type recognition.

All special cell detectors are located close to the UTOPIA interfaces and are comparing cells with UTOPIA cell format.



U 1	CTM01U	CTM00U	CTM02U*
U 1	CTR01U	CTR00U	CTR02U**
U 2	CTM11U	CTM10U	CTM12U*
U 2	CTR11U	CTR10U	CTR12U**
D 1	CTM01D	CTM00D	CTM02D*
D 1	CTR01D	CTR00D	CTR02D**
D 2	CTM11D	CTM10D	CTM12D*
D 2	CTR11D	CTR10D	CTR12D**

15 015 015 0

CTRxyz, CTMxyz Meaning of the indices x, y, z:

- x Fill 0 (=cell type 1) or 1 (=cell type 2).
- y Count 0..2.
- z Up or down.

*Only the 8 MSBs of the CTMx2z registers define the pattern to be compared and the corresponding mask bits. The lower 8 bit (bit 7 to 0) are don´t care. These bits are unused, i.e. not represented by flip-flops. They always read as 0.

**In the CTRx2z registers the 2 LSBs are used to select the action upon a matching pattern. The bits 7 to 2 are unused, i.e. not represented by flip-flops. They always read as 0.

Bit 1, 0 of CTRx2z Used for function select:

- 00 Ignore, i.e. cell is forwarded normally.
- 01 Discard, i.e. cell is discarded.
- 10 Extract, i.e. cell is forwarded to the receive buffer.
- 11 Monitor, i.e. cell is forwarded normally and copied to the receive buffer.

2.17 Multicast RAM Part Offset Register (MCOF)

Read/write Address 28_H
Value after reset 0060_H

15	8
unused	

7	0
unused	MCIPOI(6:0)

MCIPOI(6:0) Defines start address of multicast pointer range in external downstream memory in steps of 1024. Default 96K, i.e. MCOF(6:0)=60_H.

2.18 Queue Length Register High/Low Priority (QLEN)

Read/write Address 29_H
Value after reset $C080_H$

15	8
QLEN-ITP	LPRIOLIM(6:0)

7	0
MAXQLEN(7:0)	

QLENITP Queue length ITP queue:
0 Length 0 (no ITP queue, used also for overflow test).
1 Length 32, default.

LPRIOLIM(6:0) Low priority limit. If higher values than the maximum queue length are programmed the low priority interrupt never occurs. Default length 64 (100 0000).

MAXQLEN(7:0) Maximum queue length in steps of 2. If higher values than the physical queue size are programmed the ASP uses the physical queue sizes for the queue length. Physical queue size = 292 for queue 0, 256 for all other queues. Default length 256 (1000 0000).

2.19 Internal Pointer RAM Location (MCRANGE)

Read/write Address $2A_H$
Value after reset 0018_H

15							8
unused							OVSEL
7							**0**
unused				INTPOIRAM(4:0)			

OVSEL — Selects which overflow reports the queue number in the PHY-IND(4:0) bits of the ISR1 register:

- 0 The queue number of the QEVNT interrupt is signalled (queue overflow).
- 1 The queue number of the TQOV interrupt is signalled (threshold overflow).

INTPOIRAM(4:0) — Defines the start address of the internal pointer RAM in steps of 1024. Default 16K, i.e. MCRANGE(4:0) = 10000.

2.20 TXR Queue Select Register (TXQSEL)

Read/write Address $2B_H$
Value after reset 0000_H

15	14	13	12	11	10	9	8
unused							

7	6	5	4	3	2	1	0
unused			QSELDN(4:0)				

QSELDN(4:0) Selects queue for downstream cell insertion:

00000	Queue 0
00001	Queue 1
....	....
10111	Queue 23
11000	ITP/RSATM queue
11001	Cell not sent, command bit reset.
....	....
11111	Cell not sent, command bit reset.

2.21 Upstream RAM Data Registers (URAM0L..URAM2H)

Read/write Address $2C_H$...31_H
Value after reset 0000_H (for all)

These registers specify the data to be transferred to the upstream external connection RAM or contain the data of an entry after transfer of data from the external RAM into the register set. Register URADR specifies the address of the entry to be written or read. Four types of transfer can be specified with the URAMACC(1:0) bits of CMR.

2.21.1 General Mapping Registers to Dwords

Dword	31 ... 23	15 ... 7 ... 0
2	Register URAM2H / Address 31_H	Register URAM2L / Address 30_H
1	Register URAM1H / Address $2F_H$	Register URAM1L / Address $2E_H$
0	Register URAM0H / Address $2D_H$	Register URAM0L / Address $2C_H$

2.21.2 Upstream RAM Dword Contents

Dword	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 ... 7 ... 0
2	RA(31:0)																
1	Pf	SSN (3:0)				ADI (1:0)		CDP (1:0)		EN 0,1		20	19	18	Res (1:0)		EMCI(15:0)
0	Pv	res													V		SN(15:0)

2.21.2.1 Upstream RAM : Dword0

Pv — Varying parity bit.
This bit is set to **odd** parity with every write access. It protects **address and content** of dword 0 and is also checked at each read access. This bit is always generated by the ASP when writing an entry, be it initiated by the microprocessor or by a cell access. If it's initiated by the microprocessor then the Pv has to be generated in following way:

0 Pv is generated correctly.
1 Pv is falsified by inversion.

res(13:0) Reserved bits.

V Valid connection.
0 Cell is discarded with interrupt.
1 Cell is forwarded.

SN(15:0) Sequence number.

2.21.2.2 Upstream RAM : Dword1

Pf Fixed parity bit.
This bit covers the two words with offset 1 and 2 of the entry. It is set in such a way that the number of ’1s’ in both words is **odd**. This parity bit is always generated by the ASP when writing an entry. If it is initiated by the microprocessor then the Pv has to be generated in the following way:
if bit URAM1H(15) = ’0’ then Pf is generated correctly
if bit URAM1H(15) = ’1’ then Pf is falsified by inversion

SSN(3:0) Switching stage number.

ADI(1:0) Address identifier.

CDP(1:0) Cell delay priority.

EN0 Enable bit for plane 0.

EN1 Enable bit for plane 1.

Bit 20 iCLP
Cell loss priority internal. If clen=1 this bit is copied to the iCLPclpi field of the internal cell.

*Note: The clp bit of the external cell is always copied (saved) to the clp bit of the internal cell **before** this copying procedure.*

Bit 19 CLEN
Enable bit for iCLP.
1 The iCLP bit is copied to the iCLP field of the internal cell.

Bit 18 RMR (Redundant Module Receiver)

Res(1:0) Reserved bits.
They are written to the cell.

EMCI(15:0) Egress or multicast identifier.
This field is used at the downstream side of the ASP to address the external RAM.

Note: The maximum length of EMCI is 16 bit. The user must clear the unused bits in the upstream external RAM entries accordingly.

2.21.2.3 Upstream RAM : Dword2

RA(31:0) Routing address.

2.22 Address for Upstream RAM Entry (URADR)

Read/write Address 32_H
Value after reset 0000_H

15							8
RAMSEL	URAMADR(14:8)						
7							**0**
URAMADR(7:0)							

Specifies the base address of an entry for all transfers to or from the upstream external connection RAM.

RAMSEL Used for RAM0/1 selection.

URAMADR(14:0)

2.23 Address for Downstream RAM Entry (DRADR)

Read/write Address 33_H
Value after reset 0000_H

15							8
RAMADD(15:8)							
7							**0**
RAMADD(7:0)							

RAMADD(15:0) Physical RAM address (bit 16 contained in bit DRAMSEL of register CMR).

2.24 Downstream RAM Data Registers (DRAM0L..DRAM2H)

Read/write Address 34_H...39_H
Value after reset 0000_H (for all)

These registers specify the data to be transferred to the external downstream connection RAM or contain the data of an entry after transfer of data from the external RAM into the register set. Register DRADR specifies the address of the entry to be written or read. Three types of transfer can be specified with the DRAMACC(1:0) bits of CMR.

2.24.1 General Mapping to Dwords

Dword	31 23	15 7 0
2	Register DRAM2H / Address39_H	Register DRAM2L / Address 38_H
1	Register DRAM1H / Address 37_H	Register DRAM1L / Address 36_H
0	Register DRAM0H / Address 35_H	Register DRAM0L / Address 34_H

2.24.2 Downstream RAM Dword Contents : Point-to-Point Connection

Dword	31							23								15								7							0
2	PV2	unused						26	25	24	unused					21	q1	q0	z(2:0)					15	14	c1(2:0)				c0(2:0)				d1(3:0)				d0(3:0)			
1	PV1	fe		29	a		sc1(5:0)									sc0(5:0)								sl(15:0)																		
0	Pf	don't care														BLCI(13:0)															QN(4:0)					pn(2:0)			-	V	1	-

2.24.2.1 Downstream RAM : Dword0

Pf — Fixed parity bit (odd parity bit).
Is calculated by ASP during µP write access and is checked each time the ASP reads an entry. It protects address and content of dword 0, the base entry. To force a parity error the generated parity bit can be inverted by setting the MSB of DRAM0H to '1'.

Note: Odd parity means that the parity bit is set in such a way that the number of '1' incl. Parity in the covered bits is odd.

BLCI(13:0) — For point-to-point connections only.

QN(4:0) — For point-to-point connections only.

pn(2:0) — Paddack-Portnumber.

V — VCON-Identifier.

Bit 1 — PRI
Traffic Priority:
0 High priority.
1 Low priority.

2.24.2.2 Downstream RAM : Dword1

PV1 — Variable parity bit (odd parity bit). This bit covers the dwords with the offset +1 of the entry, **odd** parity. This bit is re-calculated each time the ASP writes an entry (only write3). Both µP and cell initiated accesses generate a correct parity bit. These generated parity bit (Pv1) can be inverted when the MSB of DRAM1H for Pv1 is high. If a parity error is detected an interrupt bit is set and normally the cell is discarded. If TSTPERR='0' the discard function is disabled.

Note: Odd parity means that the parity bit is set in such a way that the number of '1' incl. Parity in the covered bits is odd.

fe — Control bit of cell acceptance in case of fcs2:

0 Cell discard.

Bit 29 — lrms
RMS of the last accepted cell.

a — Active plane bit.

sc1(5:0) — 6 LSBs of Sequence Number of the last accepted cell from plane 1.

sc0(5:0) — 6 LSBs of Sequence Number of the last accepted cell from plane 0.

sl(15:0) — Sequence number of the last accepted cell.

2.24.2.3 Downstream RAM : Dword2

PV2 — Variable parity bit (odd parity bit). This bit covers the dwords with the offset +2 of the entry, **odd** parity. This bit is re-calculated each time the ASP writes an entry (only write3). Both µP and cell initiated accesses generate a correct parity bit. These generated parity bit (Pv2) can be inverted when the MSB of DRAM2H for Pv2 is high. If a parity error is detected an interrupt bit is set and normally the cell is discarded. If TSTPERR='0' the discard function is disabled.

Note: Odd parity means that the parity bit is set in such a way that the number of '1' incl. Parity in the covered bits is odd.

Bit 26	cspmen Enable of Conditional Single Plane Mode.
Bit 25	lraen Enable of local Single Plane Mode (Plane lra).
Bit 24	lra Active plane bit for the local Single Plane Mode.
Bit 21	lrpcen Enable for the Accept Algorithm: 0 Local disable.
q1	Quality Bit for the Plane 1.
q0	Quality Bit for the Plane 0.
z(2:0)	Weight for the Dead Plane Counter (default: 6) d0/d1 of not active plane (p-1) is incremented by 1 for every 2^z cells arrived from the actual plane p.
Bit 15	lps1 Indication bit for an arrived cell from plane 1 after a LPS-Switching.
Bit 14	lps0 Indication bit for an arrived cell from plane 1 after a LPS-Switching.
c1(2:0)	Condition Monitor Plane 1.
c0(2:0)	Condition Monitor Plane 0.
d1(3:0)	Dead Plane Counter Plane 1.
d0(3:0)	Dead Plane Counter Plane 0.

2.24.3 Downstream RAM Dword Contents : Point-to-Multipoint Connection

For pointer entries it is recommended to use the write access with one dword only. For read accesses always 3 dwords are transferred but the offset +1 and +2 dwords should be ignored.

Dword	31 … 23	15 … 7 … 0
2	16 bit pointer n+5	16 bit pointer n+4
1	16 bit pointer n+3	16 bit pointer n+2
0	16 bit pointer n+1	16 bit pointer n

Dword	31	30	29	28	27	26	25	24	23 … 22	21	20	19	18 … 16	15	14	13 … 11	10 … 8	7 … 4	3 … 0
2	PV2	unused				26	25	24	unused	21	q1	q0	z(2:0)	15	14	c1(2:0)	c0(2:0)	d1(3:0)	d0(3:0)
1	PV1	fe	29	a	sc1(5:0)					sc0(5:0)				sl(15:0)					
0	Pf	port bitmap(23:0)															pn(2:0)	V	1

2.24.3.1 Downstream RAM : Dword0

Pf — Fixed parity bit (odd parity bit).
Is calculated by ASP during µP write access and is checked each time the ASP reads an entry. It protects address and content of dword 0, the base entry. To force a parity error the generated parity bit can be inverted by setting the MSB of DRAM0H to ’1’.

Note: Odd parity means that the parity bit is set in such a way that the number of ’1’ incl. Parity in the covered bits is odd.

port bitmap(23:0) — For point-to-multipoint connections only.

pn(2:0) Paddack-Portnumber.

V VCON-Identifier.

Bit 1 PRI
Traffic Priority:
0 High priority.
1 Low priority.

Note: Dword1 and Dword2 are equal to Dword1 and Dword2 of section "Downstream RAM Dword Contents : Point-to-Point Connection" on page 68.

2.25 Pointer RAM Address (PRAMADR)

Read/write Address $3A_H$
Value after reset 0000_H

15							8
unused							RAMPOIADD(9:8)
7							**0**
RAMPOIADD(7:0)							

RAMPOIADD(9:0) RAM Address.

2.26 Pointer RAM Pointer +E-Bit Entry (PRAMPT)

Read/write Address $3B_H$
Value after reset 0000_H

15	8
unused	RAMPOI(10:8)

7	0
RAMPOI(7:1)	RAMEBIT

RAMPOI(9:0) Pointer of RAM entry.

RAMEBIT E-bit of RAM entry:
1 Indicates that this is the last entry of a logical multicast list.

2.27 Pointer RAM LCI Entry (PRAMLCI)

Read/write Address $3C_H$
Value after reset 0000_H

15	8
unused	LCI(13:8)

7	0
LCI(7:0)	

LCI(13:0) LCI(13:0) of outgoing cell.

2.28 RPC Algorithm Register (RPCALG)

Read/write Address $3D_H$
Value after reset 4003_H

15							8
RLPS-ACT(1)	RPCEN	rAEN	rA	CS-PAUSE	rYg	rXg	rY(2)
7							**0**
rY(1:0)		rX(1:0)		RLPSEN	RLPS-ACT(0)	RLPS1	RLPS0

RLPSACT(1) LPS active status MSB.

RPCEN Global enable of RPC algorithm:
0 Disabled
1 Enabled

rAEN Enable global single plane mode with active plane rA:
0 Disabled
1 Enabled

rA Active plane bit for conditional/global single plane mode:
0 Plane 0
1 Plane 1

CSPAUSE Affect only on conditional/global single plane mode: transmission pause:
1 Discard all cells if CONFDN(15) is enabled.

rYg Selects value of rY:
0 Used hardwired default rY=4.
1 Use Bit 8...6 of RPCALG.

rXg Selects value of rX:
0 Used hardwired default rX=2.
1 Use Bit 5,4 of RPCALG.

rY(2:0) Weight of correct sequence numbers (range: 0..6, value of 7 leads to default rY=4).

rX(1:0) Weight of sequence number error in the condition monitor.

RLPSEN LPS enable bit

RLPSACT(0) LPS active status LSB.

RLPS1 Indicates that the PSI cell has been received on plane1.

RLPS0 Indicates that the PSI cell has been received on plane0

2.29 Cell Header for Upstream Insertion (TXR0..2)

Read/write Address 40_H...42_H
Value after reset 0000_H (for all)

Addr.	Name	15			8	7		0
40	TXR0	LCI(11:4)				LCI(3:0)	VCI(15:12)	
41	TXR1	VCI(11:4)				VCI(3:0)	PT(2:0)	CLP
42	TXR2	LCI (13:12)	HK(2:0)	PN(2:0)		00_H(FCS1)[1)]		

[1)] If 01_H then FCS1 are falsified for test purposes in upstream direction only.

2.30 Cell Header for Downstream Insertion (TXR0..2)

Read/write Address 40_H...42_H
Value after reset 0000_H (for all)

Addr.	Name	15				8	7			0
40	TXR0	CLP	HK(2:0)	ADI(1:0)	PN(2:1)	PN (0)	MCCNT(4:0)			LCI (13:12)
41	TXR1	LCI(11:4)					LCI(3:0)	VCI(15:12)		
42	TXR2	VCI(11:4)					VCI(3:0)	PT(2:0)		iCLP

2.31 Cell Payload (TXR3..27)

Read/write Address 43_H...$5B_H$
Value after reset 0000_H (for all)

Addr.	Name	15 8	7 0
43	TXR3	Payload octet 0	Payload octet 1
44	TXR4	Payload octet 2	Payload octet 3
45	TXR5	Payload octet 4	Payload octet 5
46	TXR6	Payload octet 6	Payload octet 7
47	TXR7	Payload octet 8	Payload octet 9
48	TXR8	Payload octet 10	Payload octet 11
49	TXR9	Payload octet 12	Payload octet 13
4A	TXR10	Payload octet 14	Payload octet 15
4B	TXR11	Payload octet 16	Payload octet 17
4C	TXR12	Payload octet 18	Payload octet 19
4D	TXR13	Payload octet 20	Payload octet 21
4E	TXR14	Payload octet 22	Payload octet 23
4F	TXR15	Payload octet 24	Payload octet 25
50	TXR16	Payload octet 26	Payload octet 27
51	TXR17	Payload octet 28	Payload octet 29
52	TXR18	Payload octet 30	Payload octet 31
53	TXR19	Payload octet 32	Payload octet 33
54	TXR20	Payload octet 34	Payload octet 35
55	TXR21	Payload octet 36	Payload octet 37
56	TXR22	Payload octet 38	Payload octet 39
57	TXR23	Payload octet 40	Payload octet 41
58	TXR24	Payload octet 42	Payload octet 43
59	TXR25	Payload octet 44	Payload octet 45
5A	TXR26	Payload octet 46	Payload octet 47
5B	TXR27	00_H (FCS2)[1)]	00_H

[1)] If 01_H then FCS2 are falsified for test purposes in upstream direction only.

2.32 Utopia Configuration Register 0 (CONUT0)

Read/write Address $5C_H$
Value after reset 0000_H

15					8
unused	UTQLEN(6:0)				

7					0
unused	UTCEL-DISC	UTP-BUSW	UTPRT-DISC	UTPRTY	UTCONFIG(1:0)

UTQLEN(6:0) Queue size for downstream UTOPIA buffer.

UTCELDISC

1 Enable cell discard with start of cell error upstream.

UTPBUSW 8 or 16 bit mode at up- and downstream interface:

0 8-bit
1 16-bit

UTPRTDISC

1 Discard cells with false parity upstream.

UTPRTY

0 No parity check at upstream UTOPIA interface.

UTCONFIG(1:0) Port mode at up- and downstream UTOPIA interface:

00 4x6 port
01 3x8 port
10 2x12 port
11 Level 1 mode.

2.33 Utopia Configuration Register 1 (CONUT1)

Read/write Address $5D_H$
Value after reset 0000_H

15							8
PHYEN(15:8)							
7							**0**
PHYEN(7:0)							

PHYEN(15:0) Bit mapped enable signals for ports 15..0 up- and downstream:
1 Port enabled.

2.34 Utopia Configuration Register 2 (CONUT2)

Read/write Address $5E_H$
Value after reset 0000_H

15							8
unused							
7							**0**
PHYEN(23:16)							

PHYEN(23:16) Bit mapped enable signals for ports 23..16 up- and downstream:
1 Port enabled.

2.35 Downstream Test Connection Registers (DITC1L..DITC2H)

Read/write Address 60_H...63_H
Value after reset 0000_H (for all)

These registers contain the sequence entries for the internal test channel ITC. These cells are defined with HK=001 and have no connection identifier EMCI or LCI. The base entry (offset 0) of the entry has fixed values and is not programmable.

2.35.1 General Mapping Registers to Dwords

Dword	31 ... 23	15 ... 7 ... 0
1	Register DITC2H / Address 63	Register DITC2L / Address 62
0	Register DITC1H / Address 61	Register DITC1L / Address 60

2.35.2 Downstream Test Connection Dword Contents

Dword	31				23					15					7	0
1	31			26	25	24		21	q1	q0	z(2:0)	15	14	c1(2:0)	c0(2:0)	d1(3:0)	d0(3:0)
0	31	fe	29	a	sc1(5:0)			sc0(5:0)				sl(15:0)					

Note: The Dword0 and Dword1 have the same mapping as the Dword1 and Dword2 of section "Downstream RAM Dword Contents : Point-to-Point Connection" on page 68. Additionally the 31-st bit of Dword0 and Dword1 are don't care.

2.36 Upstream Test Connection Registers (UITC0L..UITC2H)

Read/write Address 64_H...69_H
Value after reset 0000_H (for all)

These registers contain the sequence entries for the internal upstream test channel UITC. These cells are defined with HK=001.

2.36.1 General Mapping Registers to Dwords

Dword	31 ... 23	15 ... 7 ... 0
2	Register UITC2H / Address 69_H	Register UITC2L / Address 68_H
1	Register UITC1H / Address 67_H	Register UITC1L / Address 66_H
0	Register UITC0H / Address 65_H	Register UITC0L / Address 64_H

2.36.2 Upstream Test Connection Dword Contents

Dword	31	30 ... 24	23 ... 16	15	14	13	12	11	10 ... 8	7 ... 0
2	RA(31:0)									
1	Pf	SSN (3:0)	ADI (1:0)	CDP (1:0)	EN 0,1	20	19	18	Res (1:0)	EMCI(15:0)
0	Pv	res						V		SN(15:0)

Note: The Dword0, Dword1 and Dword2 have the same mapping as the Dword0, Dword1 and Dword2 of section “Upstream RAM Dword Contents” on page 64. Additionally the 31-st bit of Dword0, Dword1 and Dword2 are don’t care.

2.37 Test Register 0 (TSTR0)

Read/write Address $6A_H$
Value after reset 0079_H

(write access to this register is only accepted if bit TSTEN in register CONGEN is set.)

15							8
unused						TST_CONDERR	TSTMC
7							**0**
TST_DISCONDU_PCNT	DCHK16	DCHK15	TSTADR	TST-CONN	TSTFCS2	RS	TST-PERR

TST_CONDERR Test condition error (downstream):
- 0 (Default) Test disabled.
- 1 Single SN error causes immediately bad condition and bad quality (c(p)=0, q(p)=0).

TSTMC Test multicast error condition (downstream):
- 0 (Default) Error condition disabled.
- 1 Error condition enabled, Phy RAM address will be forced automatically to '$17FFF_H$' (MCOF must have default value) and MCCOUNT in DSB will be forced to '1F'. Therefore ISR0(9) will be set.

TST_DISCONDU_PCNT Disable condition monitor upcount (downstream):
- 0 (Default) Condition monitor upcount enabled.
- 1 Condition monitor upcount disabled.

DCHK16 Disable overflow check of (addr > 2^{16}-1):
- 0 Check enabled.
- 1 (Default) Check disabled.

DCHK15 Disable overflow check of addr > 2^{15}-1:
- 0 Check enabled.
- 1 (Default) Check disabled.

TSTADR Disable cell discard on address range errors:
- 0 Accept cells independent of address range error.
- 1 (Default) Discard cells on address range error.

TSTCONN

0 Accept cells independent on VCON.
1 (Default) Discard cells if VCON=0.

TSTFCS2 Test mode for FCS2:

0 (Default) Disabling global cell discard in case of FCS2. Cell will be discarded if fe='0' otherwise cell will be accepted; fe-bit is bit 30 of dword1 of external RAM entry.
1 Cell discard in case of FCS2 error independent on fe-bit.

RS Sequence number size:

0 (Default) 16 bit
1 9 bit

TSTPERR Cell discard on RAM parity error downstream:

0 Do not discard cells on RAM parity error downstream.
1 (Default) Discard cells on RAM parity error downstream.

2.38 Test Register 1 (TSTR1)

Read/write Address $6B_H$
Value after reset 0002_H

(write access to this register is only accepted if bit TSTEN in register CONGEN is set.)

15					8
unused				UT_SRES	reserved (3)
7					**0**
reserved(2:0)	RXR_REPEAT	DIS_UTTXDMS	FCS2CNTDIS	FCS1DISCARD	TSTU-PER

UT_SRES Software reset for utopia interface.

RXR_REPEAT

1 Resets the RXR readpointer to the begin of the cell which is currently read out.

DIS_UTTXDMS Disabling cell stream to Utopia transmit interface. Should be set in loop mode to avoid backpressure because of utopia buffer overflow.

FCS2CNTDIS

1 Switch off generation of FCS2 count (downstream).

FCS1DISCARD

1 Switch on cell discarded at FCS1 errors (downstream).

TSTUPER

1 Switch on cell discarded on RAM parity error upstream.

2.39 Test Register 2 (TSTR2)

Read/write Address $6C_H$
Value after reset $00A0_H$

For test only. Don't write to this register.

2.40 Version Register Low (VERL)

Read only Address $6E_H$
Value after reset 4083_H

2.41 Version Register High (VERH)

Read only Address $6F_H$
Value after reset 1003_H

2.42 RAM BIST Done Bits 0 (RBDONE0)

Clear on write Address 70_H
Value after reset 0000_H

For test only. Don't write to this register.

2.43 RAM BIST Done Bits 1 (RBDONE1)

Clear on write Address 71_H
Value after reset 0000_H

For test only. Don't write to this register.

2.44 RAM BIST ERRN Bits 0 (RBERRN0)

Clear on write Address 72_H
Value after reset $7FFF_H$

For test only. Don't write to this register.

2.45 RAM BIST ERRN Bits 1 (RBERRN1)

Clear on write Address 73_H
Value after reset $00FF_H$

For test only. Don’t write to this register.

3 Operation

This chapter describes how to operate the ASP in some example configurations.

3.1 Access to Downstream External RAM

The microprocessor access depends on the setting of MCOF.

3.2 Connection Handling

As described in **Chapter 1.7**, page 17 header translation occurs in the ASP for both upstream and downstream direction. At the downstream side header translation is more complicated as it must support also spatial and logical multicast.

A special case occurs if a normal point-to-point connection is extended to a multicast connection. This happens e.g. if two persons in a phone conversation decide to add a third party. Obviously they want such an extension to be without service interuption, i.e. without lost cells. Further parties might be added and dropped, it is also possible that the initiating party the call leaves the conference and the others continue talking. The implication of these cases to the ASP is described below.

Starting point is **Figure 18**, derived from **Figure 11** with a point-to-point connection set-up. The ECI is chosen identical to the LCIa of the connection. The multicast range in the downstream external connection RAM as well as the internal translation table are unused. Assuming that LCIa is destined to PHY 0 the PN number in the sequence entry is coded with 0 0000_b.

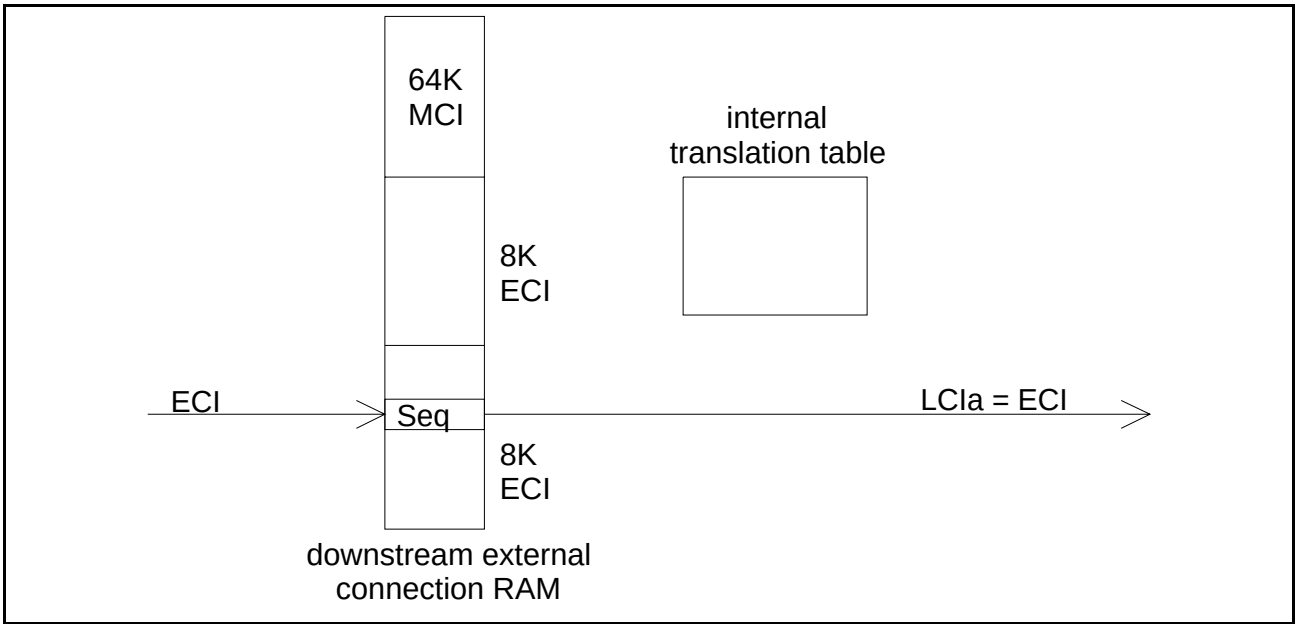


Figure 18 Point-to-Point Connection

To add a third party, i.e. a second branch of the ATM cell stream several steps are required:

1. A free MCI must be found for the whole system and all ASMs and ASPs in the system configured accordingly.
2. A free range of PN entries must be found in the internal translation table. PN is the number of PHYs connected to the switch port.
3. The multicast connection is set-up in both external RAM and internal table so that the original connection gets the same LCIa than before.
4. For the new branch a free LCIb must be found on the egress switch port and set-up in the other devices (ALP, AOP, ABM).
5. Now the switchover is done by re-programming the header translation of the ASP on the ingress switch port. Cell sequence is preserved as the multicast cells follow the same path as the point-to-point cells before. The new sequence entry is configured as for an initial connection set-up.

Figure 19 shows the new configuration together with the „old“ entry (in gray) for the point-to-point connection. Note that the former ECI value can not be used for other connections with the assumption that LCI=ECI.

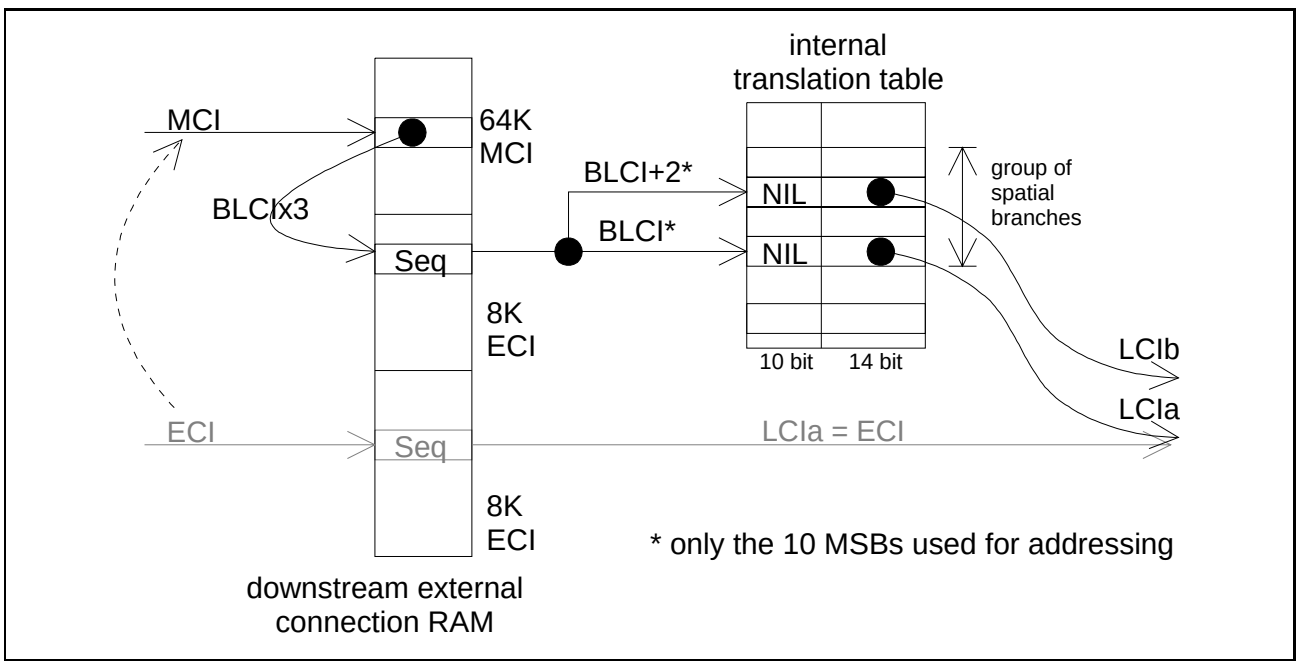


Figure 19 Extension to a Third Party

Only the 10 MSBs of the BLCI+PN vector are used for addressing the internal translation table; the MSBs are used for localization of the table within the BLCI range (**see Section 1.7.3**, page 22).

In this example the two receivers of the multicast connection are connected to the PHYs 0 and 2. The bit map in the sequence entry thus has only two bits set: 0000 0000 0000 0000 0000 0101. The other PHYs are not addressed by this multicast connection and therefore other address values than BLCI and BLCI+2 will not occur. The „NIL“ pointers in the internal translation table indicate that no further logical multicast

branch is defined. A NIL pointer is programmed by setting the end-bit (E-bit) of the logical entry to one.

In the next step a logical branch is added:

Logical multicast means that the third branch is at the same PHY than one of the existing branches, in this case on PHY 0. The cells of this connection are replicated twice to PHY 0, with two different LCIs. The steps to set-up the logical branch are:

1. A free LCIc must be found on the egress switch port and set-up in the other devices (ALP, AOP, ABM).
2. A free entry for logical multicast branches must be found in the internal translation table.
3. The entry for the additional branch is established with the new LCIc and the NIL pointer.
4. The final set-up of the new branch is done by overwriting the NIL pointer of the BLCI base entry with the pointer to the new entry.

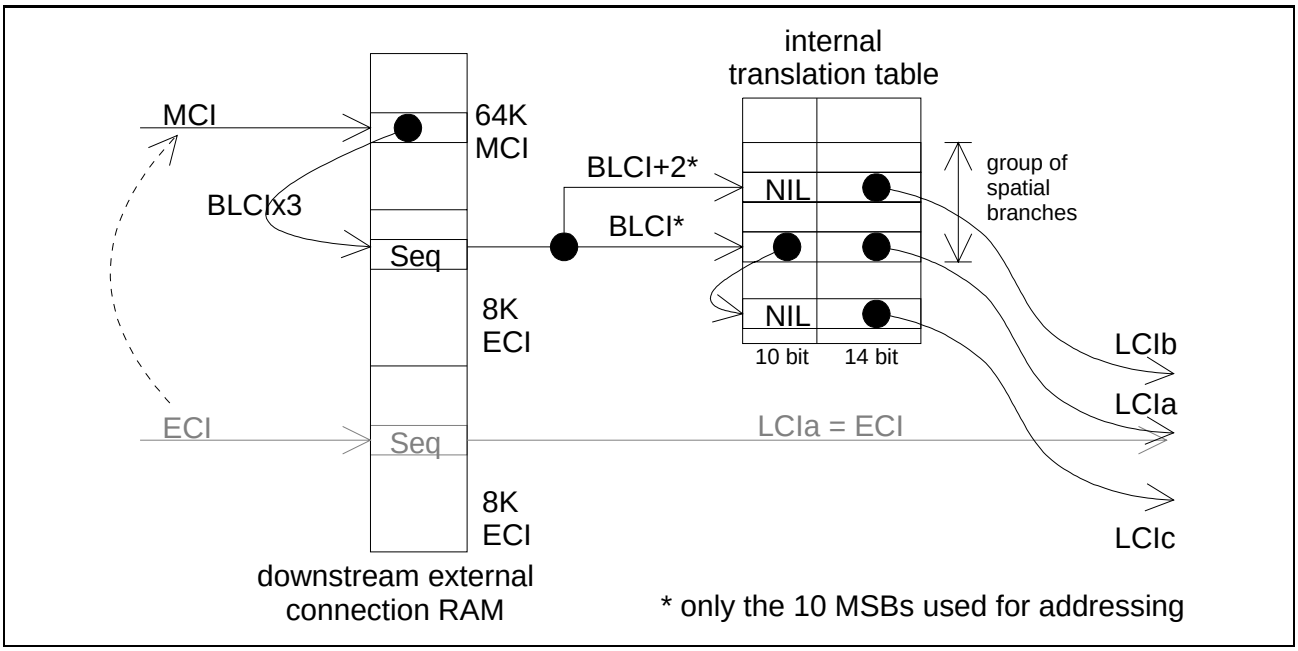


Figure 20 Extension to a Further, Logical Multicast Branch

Finally the originating connection denoted by LCIa could be removed with the following procedure:

1. The entry of LCIc is moved to the BLCI base entry, overwriting the former LCIa entry. The logical multicast chain now stops here due to the NIL pointer.

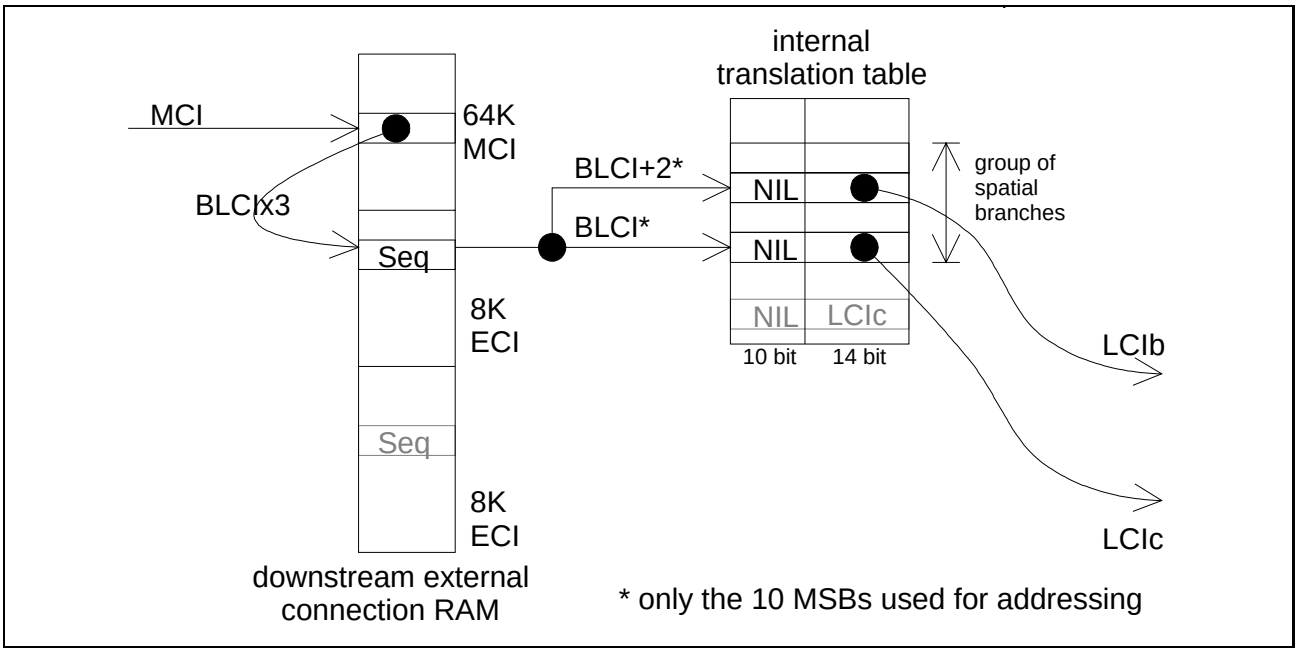


Figure 21 Original Receiver of Multi-Party Call Removed

4 Interfaces

4.1 UTOPIA Interface

The ASP has one UTOPIA receive interface and one UTOPIA transmit interface both with master capability (ATM layer side). The interfaces are compliant to the UTOPIA Level 1 and 2 specification [**5, 6**], i.e.:

- bus width is selectable either 8 or 16 bit
- frequency 19... 52 MHz
- support of single-PHY or multi-PHY configurations
- support of direct status polling option of UTOPIA Level 2 specification

The UTOPIA interface has a 8-bit and a 16-bit option. The 16-bit option has 54 octet and is shown in **Figure 22** for the standardized format and in **Figure 23** for the proprietary format. The 8-bit format has 53 octet by omitting the UDF2 octet.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	UDF1								UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Figure 22 Standardized UTOPIA Cell Format (16-bit)
All Fields According to Standards, Unused Octets Shaded

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	LCI(13:12)		HK(2:0)			PN(2:0)			UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Figure 23 Proprietary UTOPIA Cell Format (16-bit)

- with PN(2:0) = port number for PXB 4220 IWE8
  HK(2:0) = housekeeping bits
  LCI(13:0) = Logical Channel Indicator
  all other fields according to standards, unused octets shaded

Both receive and transmit side operate with one common clock which may be completely independent from the core clock. The UTOPIA clock frequency must be less than or equal to the system clock.

In multi-PHY configuration the ASP polls the PHYs at both interfaces independently in 3 selectable modes. In all modes the polling cycle is identical: the address lines apply the addresses between 0 and 11 to the PHYs and these respond by assigning the respective CLAVx signal.

The direct status polling option allows the simultaneous polling of up to 4 groups of PHYs by using 4 CLAVx/$\overline{\text{ENx}}$ signal pairs. In each of the 12 polling cycles up to 4 PHYs may respond to the same address. Therefore the ASP adds different offset values to the PHY numbers in order to get unique internal port numbers. The offset values for all CLAVx/$\overline{\text{ENx}}$ pairs and modes are shown in **Table 6**.

Table 6 UTOPIA Polling Modes. The Numbers Indicate the Offset which is Added to the PHY Number.

	Mode 2 x 12	**Mode 3 x 8**	**Mode 4 x 6**
$\overline{\text{EN0}}$ / CLAV0	0	0	0
$\overline{\text{EN1}}$ / CLAV1	12	8	6
$\overline{\text{EN2}}$ / CLAV2	do not connect	16	12
$\overline{\text{EN3}}$ / CLAV3	do not connect	do not connect	18

It is the users responsibility to program the PHY numbers to avoid ambiguous port numbers.

If less or equal than 12 PHYs are to be polled, mode 2 x 12 should be used with only the CLAV0/$\overline{\text{EN0}}$ pair connected.

Examples:

1. One PHY device, e.g. a 622 Mbit/s PHY: 16-bit bus width, address lines unconnected, RxCLAV0/$\overline{\text{RxEN0}}$ and TxCLAV0/$\overline{\text{TxEN0}}$ signal pairs connected, all other CLAVx/$\overline{\text{ENx}}$ pairs unconnected.
2. 4 PHY devices 155.52 Mbit/s PHYs: 16-bit bus width, address lines unconnected, all 4 CLAVx/$\overline{\text{ENx}}$ pairs connected, one to each PHY device
3. 4 PHY devices of 6-fold 25.6 Mbit/s PHYs: 16-bit bus width, address and all 4 CLAVx/$\overline{\text{ENx}}$ pairs connected, one to each PHY device
4. 4 PXB 4220 IWE8s: 8-bit bus width, address bus unconnected, all 4 CLAVx/$\overline{\text{ENx}}$ pairs connected, one to each IWE8

Normally the ASP is not directly connected to the PHYs, but to ALP, AOP or ABM. To be independent on the configuration of PHYs it is recommended to chose in all cases the '2 x 12' option for the UTOPIA interface, as this saves 8 interconnection lines (see the example in **Figure 24**): RxCLAV(3:2), $\overline{\text{RxEN(3:2)}}$, TxCLAV(3:2) and $\overline{\text{TxEN(3:2)}}$ remain unconnected.

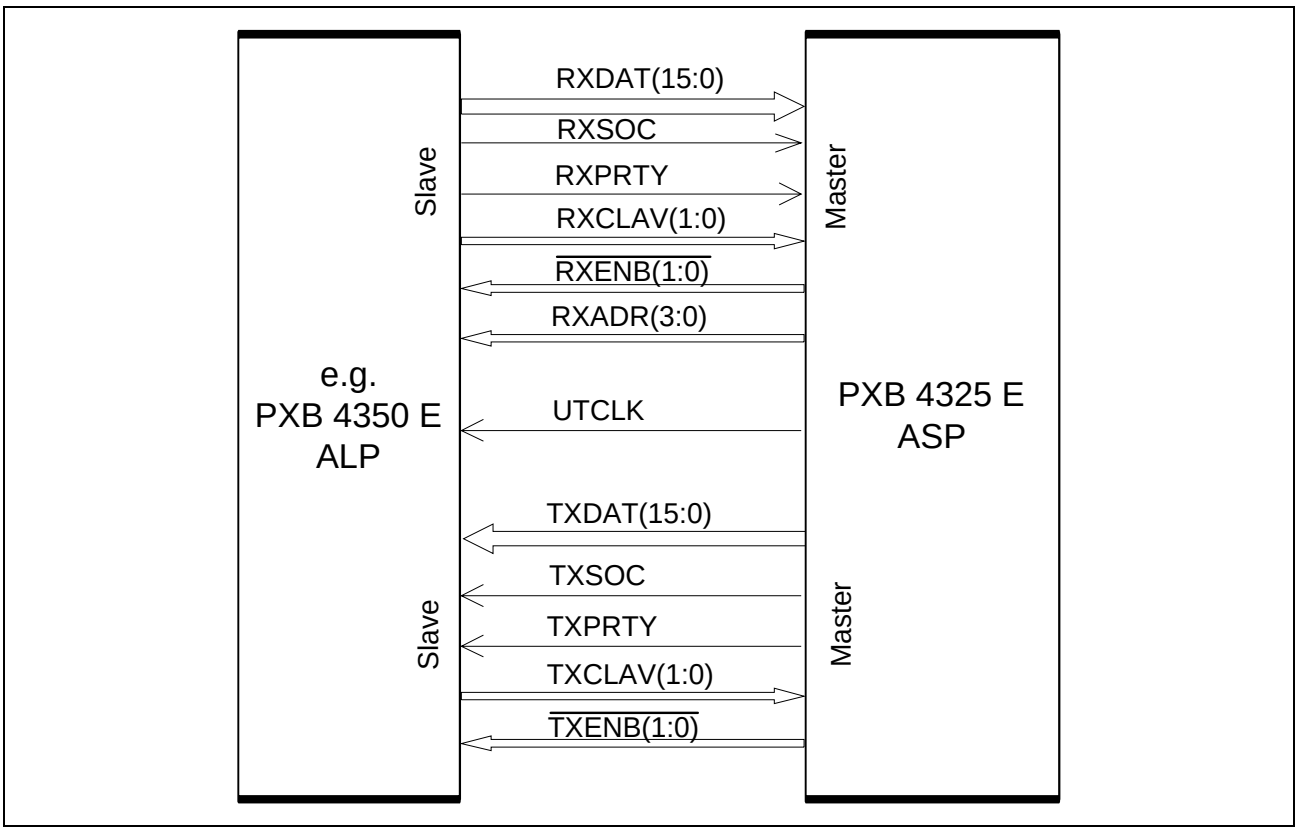


Figure 24 UTOPIA Interface Example

4.2 High Speed Interface

This interface consists of 2 bundles of up to 4 serial, differential outputs, 2 bundles of up to 4 serial, differential inputs and a differential clock input. In non-redundant systems one of the input and output bundles could be omitted. A common differential clock input of up to 207.36 MHz is provided as transmit clock and as reference clock for the phase adaptation circuits. All high speed pins use LVDS [**7, 8**] levels.

Depending on the required throughput a bundle of 1, 2 or 4 lines can be defined. Unused output differential pairs can be individually switched off to output a constant level. This measure saves power and reduces the jitter on the active outputs.

The input phase adaptations are always running and the synchronisation status of the input lines can always be detected. The input cell stream for plane 0 and 1 can be enabled individually.

Figure 25 shows the signals of the high speed interface. Each high speed signal is a pair of differential lines, e.g. D0O(1) and $\overline{\text{D0O(1)}}$. The electrical levels used are LVDS [**7, 8**]. This standard uses terminated transmission lines of 50W. The LVDS pins need the reference voltage at input VREF and the precision resistor at pin RCAL.

The lines of a bundle must always be connected to one single device on both sides, e.g. from an ASP to a ASM. Also the bundling restrictions of the ASM must be taken into account, that 4-bundles can only be connected at input pins 0-3, 4-7, 8-11, ... Bundles between different ASPs are possible and the connection from the output to the input of one ASP.

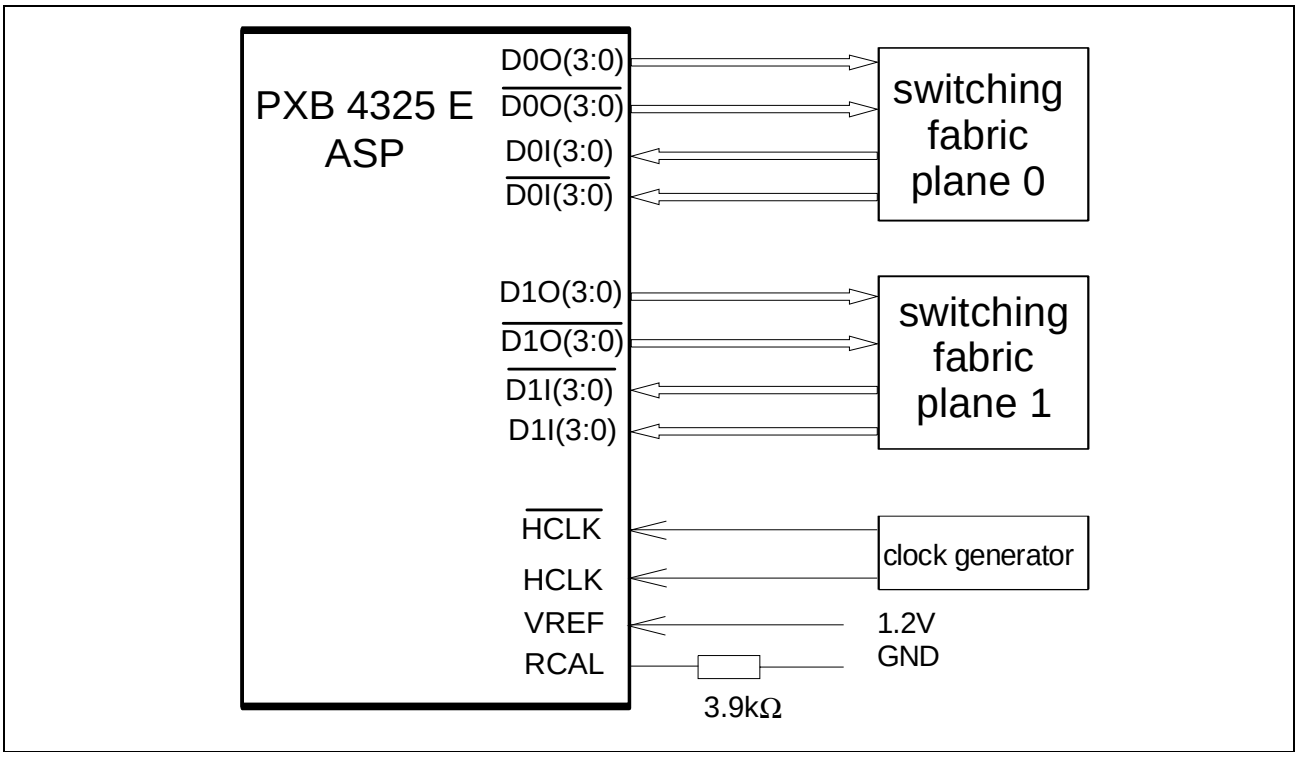


Figure 25 High Speed Interface

The SLIF cell format is shown in **Figure 26** together with the description of the fields.

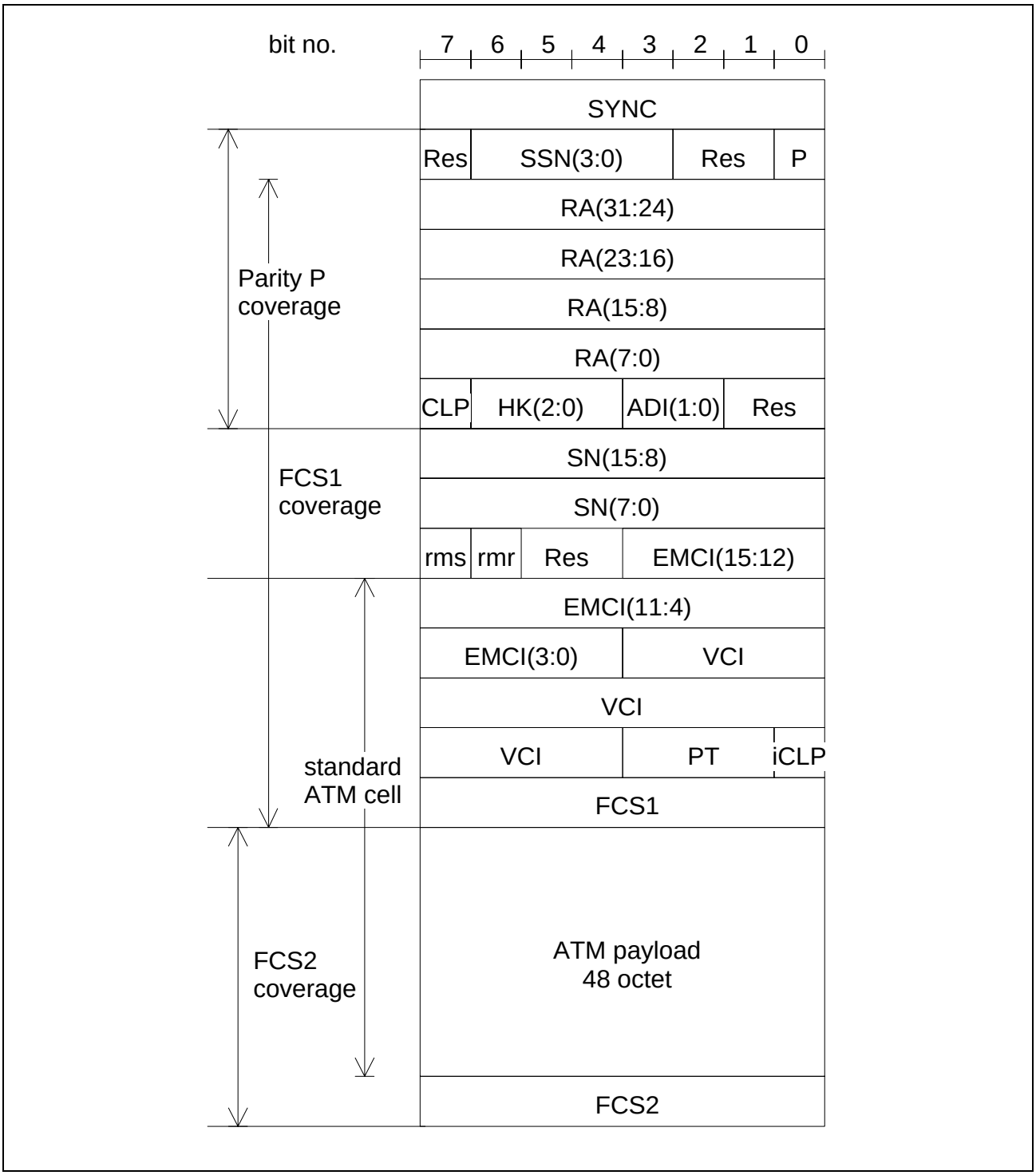


Figure 26 SLIF Cell Format

- PT = payload type bits of standardized ATM cell
- CLP = cell loss priority of standardized ATM cell
- iCLP = internal loss priority bit
- SSN = switching stage number, directs test cells to selected ASMs
- RA = routing address for switching fabric
- P = parity over 6 routing octets
- Res = reserved bits, currently unused
- ADI = address identifier, distinguishes between point-to-point and multicast
- HK = housekeeping bits, denote internal cell type
- SN = sequence number of cell, to be incremented per connection
- rmr = redundant module receiver, used to select redundant output LICs (**see Chapter 1.13**, page 29)
- rms = redundant module sender, used to distinguish redundant input LICs
- VCI = virtual channel identifier of standardized ATM cell
- LCI = logical channel identifier, see **Chapter 1.7**, page 17
- EMCI = egress or multicast connection identifier
- FCS1 = frame check sequence, checksum over 13 header octets
- FCS2 = frame check sequence, checksum over 48 payload octets

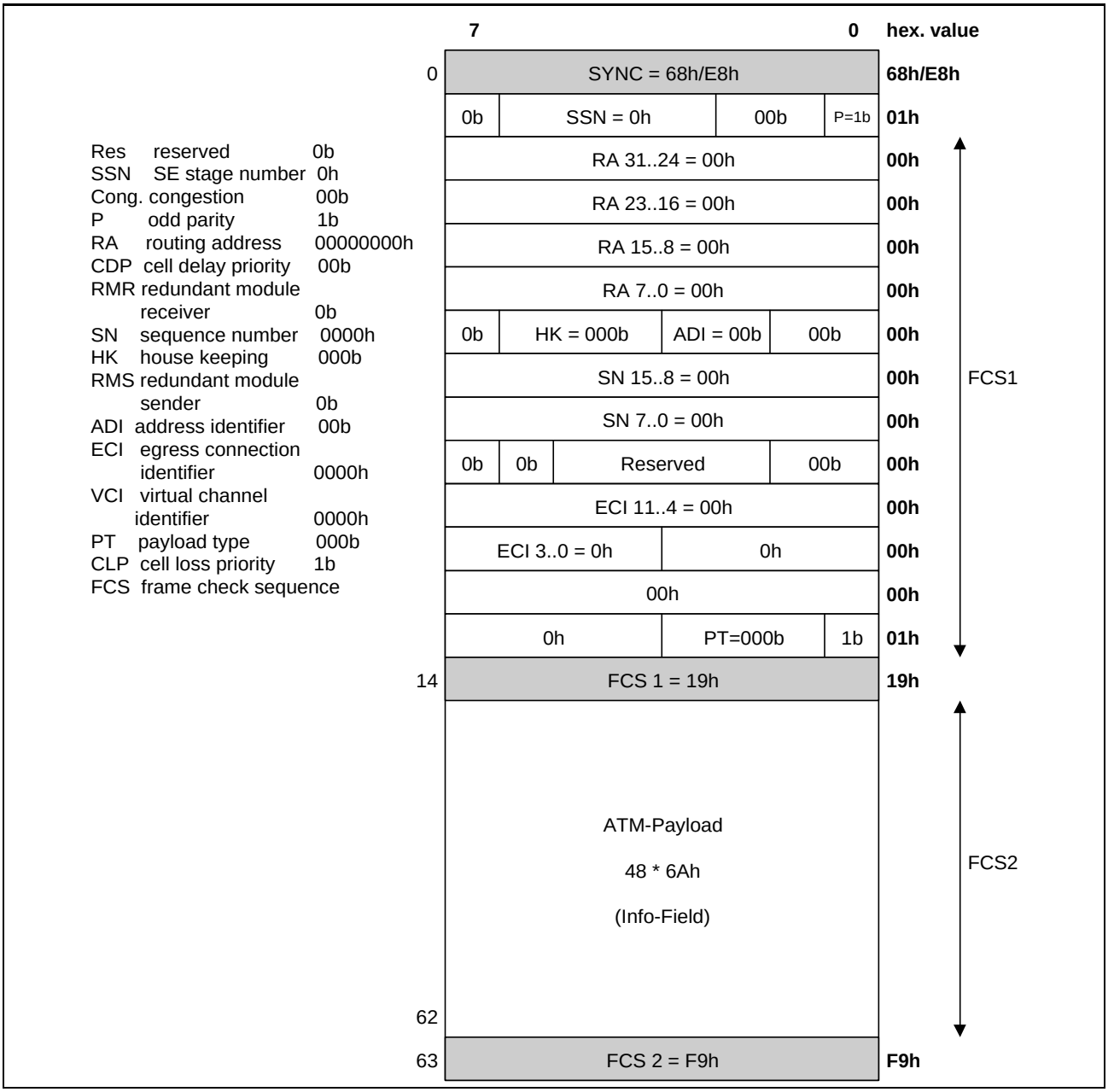


Figure 27 ATM IDLE cell format

4.3 Upstream RAM Interface

This is a 32-bit synchronous static RAM interface. Depending on the required number of connections on the switch ports one or two 1 M RAM chips of 32 K x 32 bit or one 2 M RAM chip of 64 K x 32 bit can be connected:

- one 1 M RAM chip of 32 K x 32 bit usable LCIs: 0..10921
- two 1 M RAM chips of 32 K x 32 bit usable LCIs: 0..10921, 10923..21844

Note: In the case of 2 RAM chips of 32 K x 32 bit the LCI value 10922 is unusable.

For each cell coming either from UTOPIA receive interface or from the transmit buffer the respective entry is accessed. 3 double words are read and in case the cell is accepted one double word is written back. It contains the sequence number.

The upstream external RAM is connected as shown in **Figure 28**. If two RAM chips are used the chip enable lines $\overline{\text{RCEU(1:0)}}$ and the status control lines $\overline{\text{RSCU(1:0)}}$ are connected separately to each RAM chip. All other lines are connected to both RAM chips in parallel.

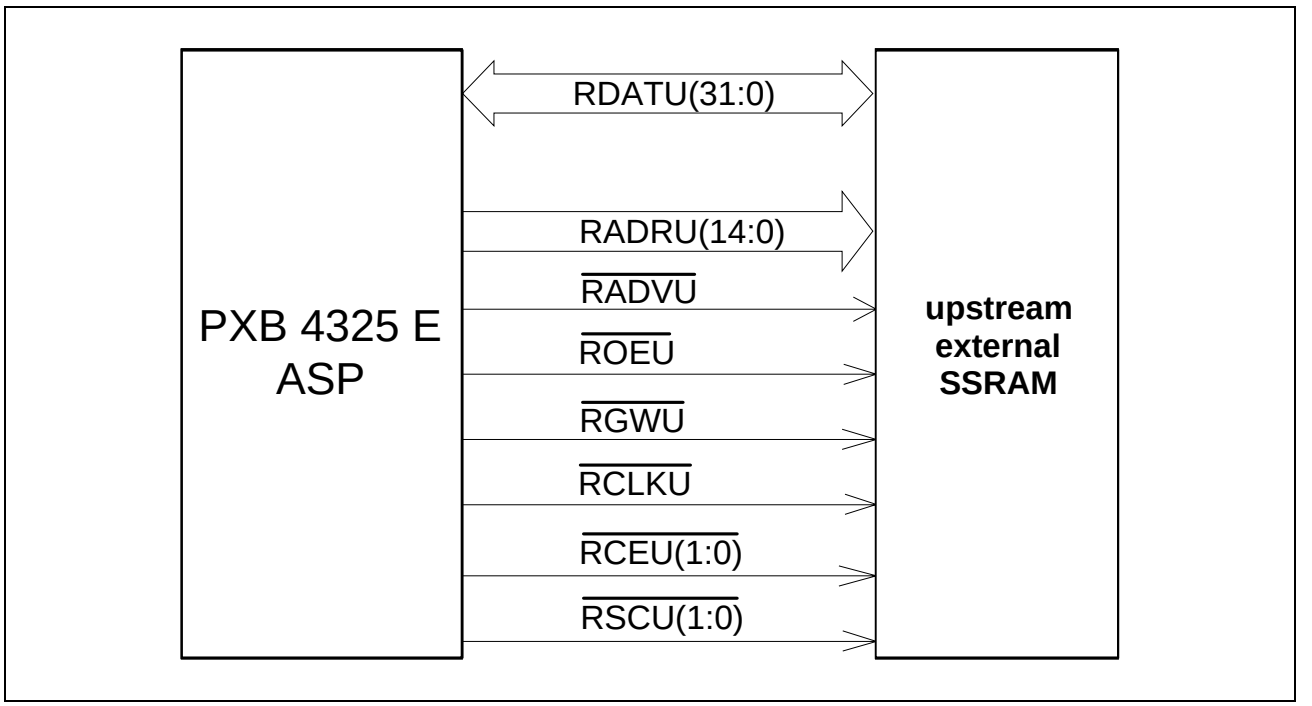


Figure 28 Upstream RAM Interface

4.4 Downstream RAM Interface

This is a 32-bit synchronous static RAM interface. Depending on the required number of connections on the switch ports and the number of multicast connections in the system the following configurations are possible:

- one 1 M RAM chip of 32 K x 32 bit

- two 1 M RAM chips of 32 K x 32 bit
- four 1 M RAM chips of 32 K x 32 bit

For example 2 Mbit RAM connected to the ASP allow the support of 16 K connections on the switch port and 32 K multicast connections in the whole switch.

The downstream external RAM is connected as shown in **Figure 29**.

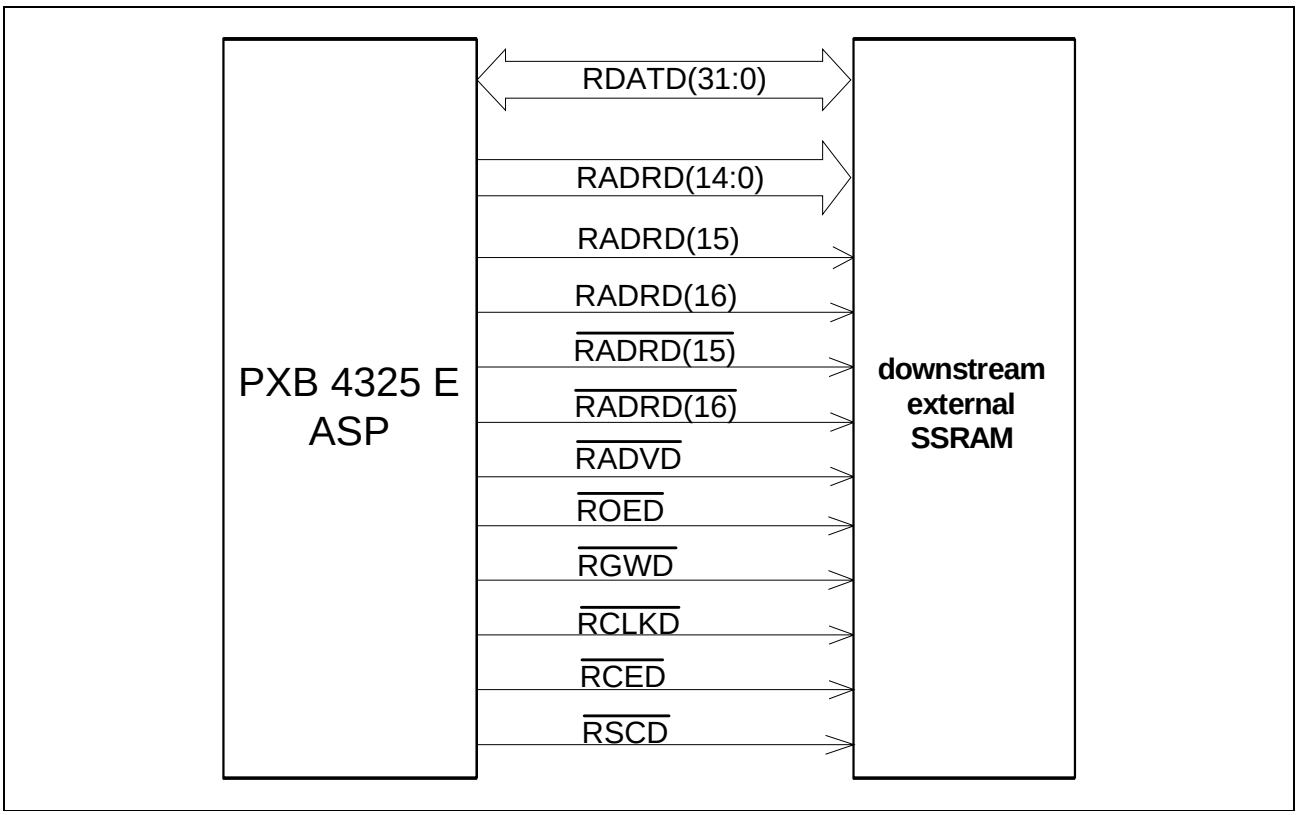


Figure 29 Downstream External RAM

The downstream external RAM is accessed simultaneously by cells incoming from up to 8 high speed inputs with up to 207.36 Mbit/s each.

The memory space of the downstream connection RAM is divided into two parts:

- the lower part contains up to 32 K ECI entries containing 3 double words per connection
- the higher part contains up to 64 K MCI entries containing pointers to the ECI memory part

Size and partition of the two parts is programmable. Range check functions are provided if by error accesses outside a given range occur. **Figure 30** shows the maximum possible memory size and the segmentation into different parts. The lower 96 K addresses are used for 32 K connection entries of 3 double words each. This part of the memory is addressed with:

- ECI x 3.

The upper 32K address range is used for 64K multicast pointers, as each address contains two pointers of 16-bit. This range is addressed with

- MCI / 2 + MCOF

with the MultiCast OFfset MCOF defining the start address of the MCI range; it is programmable in steps of 1024.

Figure 30 shows the structure of the dowstream external RAM in case of maximum size of 4 Mbit.

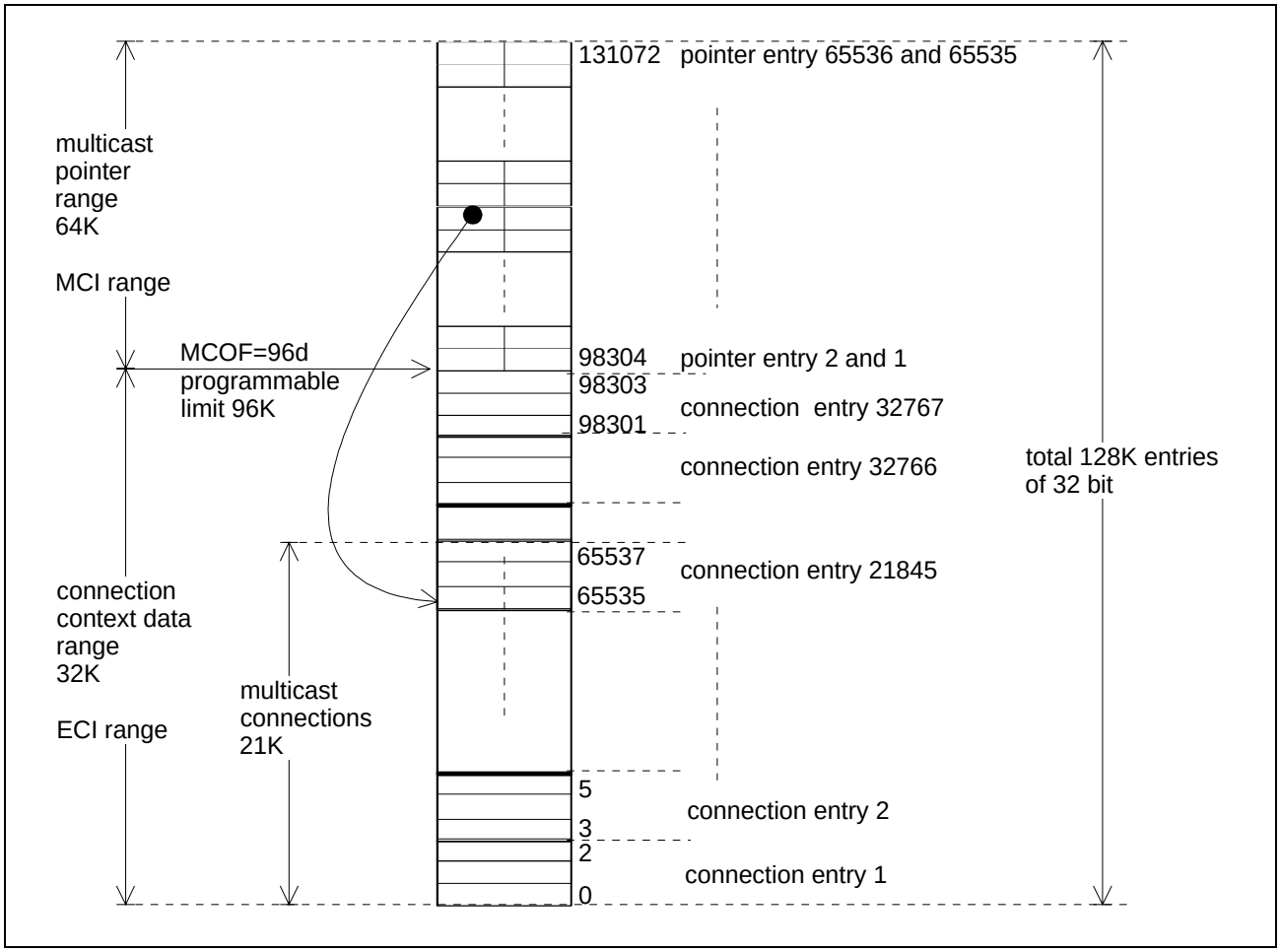


Figure 30 Downstream External Memory Structure

If only 2 Mbit RAM are connected to the ASP the maximum range of connections on the switch port of 16 K is possible. The corresponding entries use 16 K x 3 = 48 K entries with the remaining upper 16 K usable for 32 K multicast connections. The same range of multicast identifiers must be provided for all ASPs and for all ASMs of the switch.

4.5 Communication Channel / RSATM Interface

This interface consists of 4 pins as shown in **Figure 31**; 2 lines for serial data input and output plus 2 bi-directional control lines. Data format on this interface is the 64 octet SLIF format.

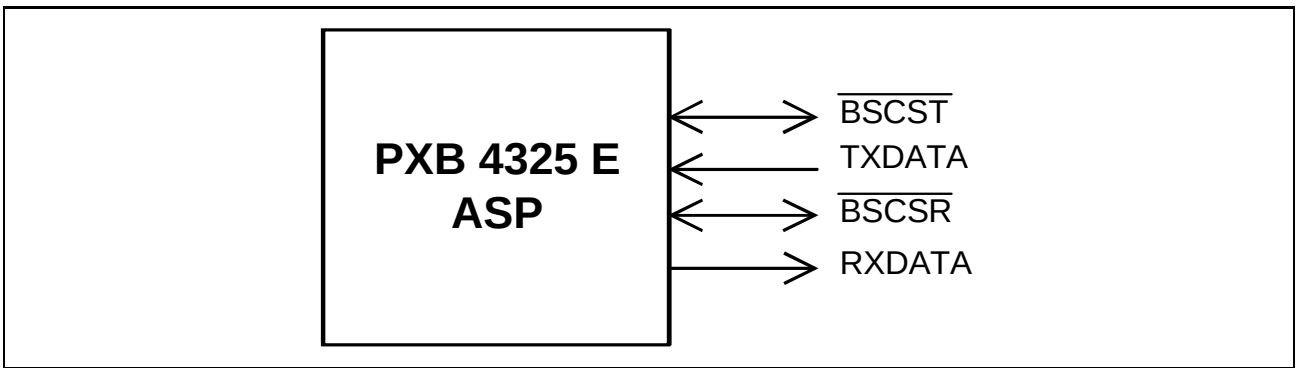


Figure 31 RSATM Interface

The input cells must have the complete internal header and trailer, as the cell is directly forwarded by the ASP to the high speed interface. Only the values of the Sync octet and the two FCS octets are calculated by the ASP. The output cells have most of the internal header fields filled with dummy octets as shown in **Figure 32**. In this figure the following abbreviations are used:

- PT = payload type bits of standardized ATM cell
- BIP-8 = bit interleaved parity, odd parity bit over whole cell
- CLP = cell loss priority of standardized ATM cell
- iCLP = internal loss priority bit
- SSN = switching stage number, used by ASM only
- RA = routing address, used by ASM only
- Res = reserved bits, currently unused
- ADI = address identifier, distinguishes between point-to-point and multicast
- HK = housekeeping bits, denote internal cell type
- SN = sequence number of cell, to be incremented per connection
- rmr = redundant module receiver, used to select redundant output LICs (**see Chapter 1.13**, page 29)
- rms = redundant module sender, used to distinguish redundant input LICs
- VCI = virtual channel identifier of standardized ATM cell
- LCI = logical channel identifier, see **Chapter 1.7**, page 17
- EMCI = egress or multicast connection identifier, for RSATM only ECI possible

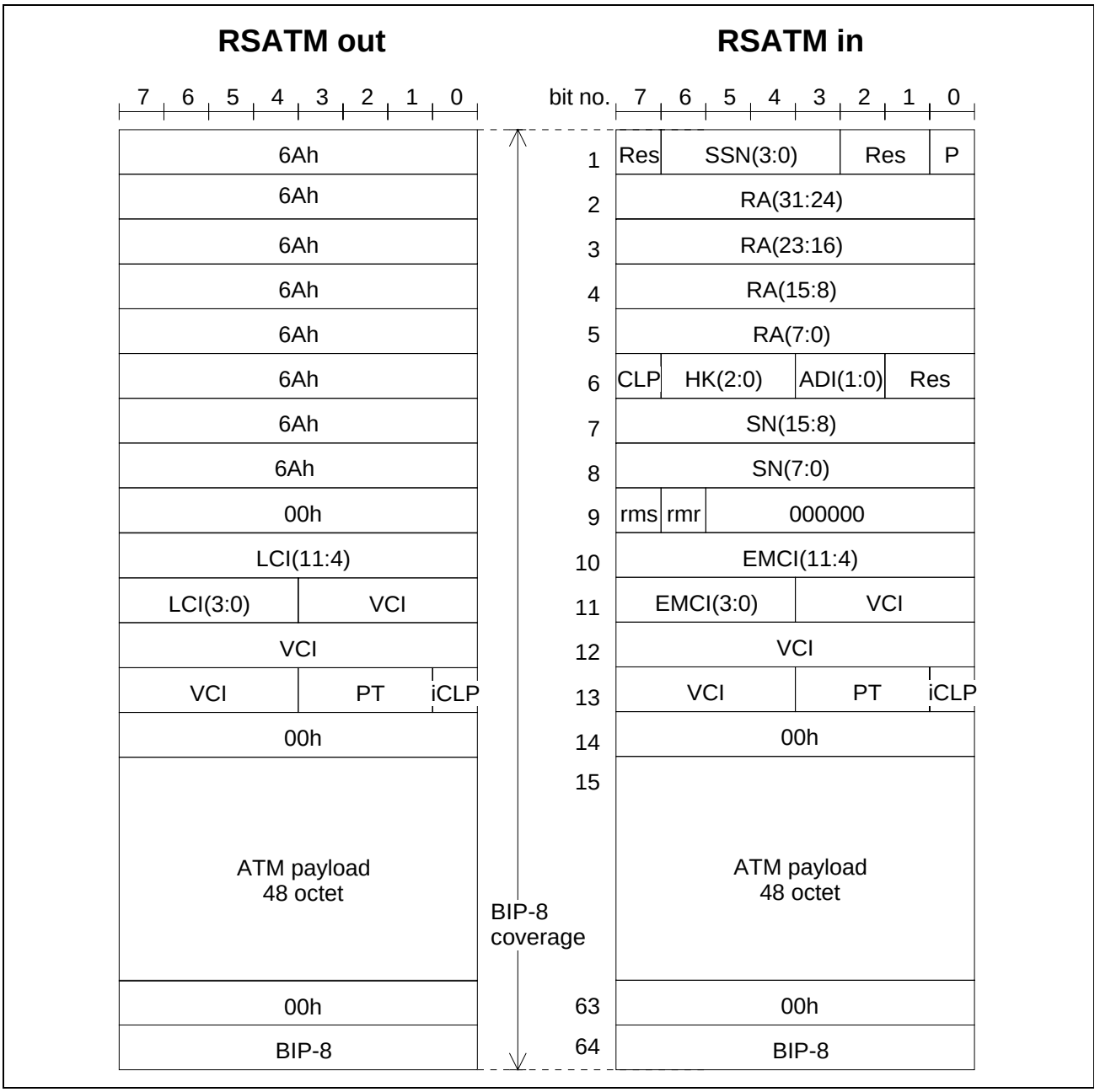


Figure 32 Cell Formats at RSATM Interface

4.6 JTAG Interface

This interface is realized according to the standard.

The 32 bit boundary scan ID is equal to register contents VERH and VERL:
ID = 10034083_H

which is Version=1_H, Device Code = 0034_H and Manufacturer Code = 083_H (including the fixed LSB bit).

4.7 Pin Definitions and Functions

The following explanations applies for all Pins of a field in the table respectively:

- Pins with a [1)] attached are connected with an internal pull up resistor.
- Pins with a [2)] attached are connected with an internal pull down resistor.
- Pins with a [3)] attached are 5V compatible.

Pin No.	Symbol	Input (I) Output (O)	Function
General (3 pins)			
C4	$\overline{\text{RESET}}$	I	Chip reset
U26	SYSCLK	I	Core operating clock
V24	UTCLK	I	UTOPIA clock
UTOPIA Receive Interface, Master Mode (30 pins)			
AD26, AC25, AC24, AC26, AB25, AB23, AB24, AB26, AA25, Y23, AA24, AA26, Y25, Y26, Y24, W25 [2)]	RXDAT (15:0)	I	Data bus
AD21, AE23, AC22, AF23	RXADR (3:0)	O	Receive PHY address
AD25 [2)]	RXPRTY	I	Odd parity of RXDAT(15:0) from PHY side
AF21, AD20, AE22, AF22	$\overline{\text{RXENB}}$ (3:0)	O	Enable signals to PHY groups
AE24, AD23, AF24, AE26 [2)]	RXCLAV (3:0)	I	Cell available signals from PHY groups
AD22 [2)]	RXSOC	I	Start of cell signal

Pin No.	Symbol	Input (I) Output (O)	Function
Utopia Transmit Interface, Master Mode (30 pins)			
R25, R26, T24, P25, R23, P26, R24, N25, N23, N26, P24, M25, N24, M26, L25, M24	TXDAT (15:0)	O	Data bus
U25, U23, T25, U24	TXADR (3:0)	O	Transmit PHY address
T26	TXPRTY	O	Odd parity to PHY side
W26, W24, V25, V26	$\overline{\text{TXENB}}$ (3:0)	O	Enable signals to PHY groups
L26, M23, K25, L24 [2]	TXCLAV (3:0)	I	Cell available signals from PHY groups
V23 [2]	TXSOC	O	Start of cell signal
Microprocessor Interface (28 pins)			
G23, F26, G24, E25, E26, F24, D25, E23, D26, E24, C25, D24, C26, A25, B24, A24	MPDAT (15:0)	I/O	µP data bus
H26, H25, J26, K24, J25, K23, K26	MPADR (7:1)	I	µP address bus
H23	$\overline{\text{MPWR}}$	I	µP write enable
G26	$\overline{\text{MPRD}}$	I	µP read enable
G25	$\overline{\text{MPCS}}$	I	µP chip select. A pull-up resistor to V_{DD} is recommended.

Pin No.	Symbol	Input (I) Output (O)	Function
F25	$\overline{\text{MPINT}}$	O	Interrupt request; open drain. A pull-up resistor to V_{DD} is recommended.
H24	$\overline{\text{MPRDY}}$	O	Ready output for read and write access. A pull-up resistor to V_{DD} is recommended.

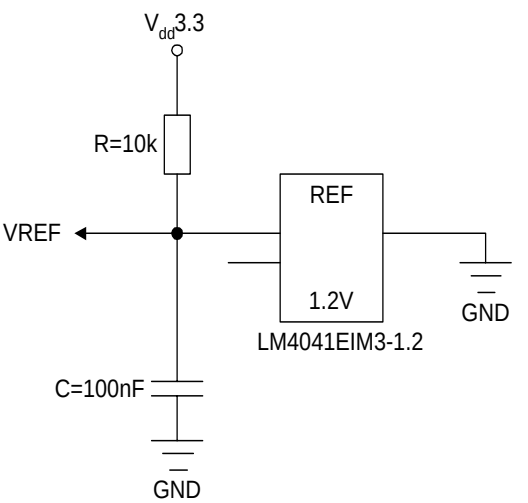
Upstream Connection RAM Interface (55 pins)

AD11, AE13, AC12, AF13, AD12, AE14, AC14, AF14, AD13, AE15, AD14, AF15, AE16, AD15, AF16, AC15, AE17, AD16, AF17, AC17, AE18, AD17, AF18, AE19, AF19, AD18, AE20, AC19, AF20, AD19, AE21, AC20	RDATU (31:0)	I/O	Upstream RAM data bus
AC9, AE8, AD7, AF7, AF12, AE12, AF11, AD8, AF8, AF5, AE6, AC7, AD6, AF6, AE7	RADRU (14:0)	O	Upstream RAM address bus
AD10	$\overline{\text{RADVU}}$	O	Upstream RAM advance input
AC10	$\overline{\text{ROEU}}$	O	Upstream RAM output enable
AF10	$\overline{\text{RGWU}}$	O	Upstream RAM global write
AE10	RCLKU	O	Upstream RAM clock
AE9	$\overline{\text{RCEU0}}$	O	Upstream RAM chip enable for RAM 0
AD9	$\overline{\text{RSCU0}}$	O	Upstream RAM status controller for RAM 0

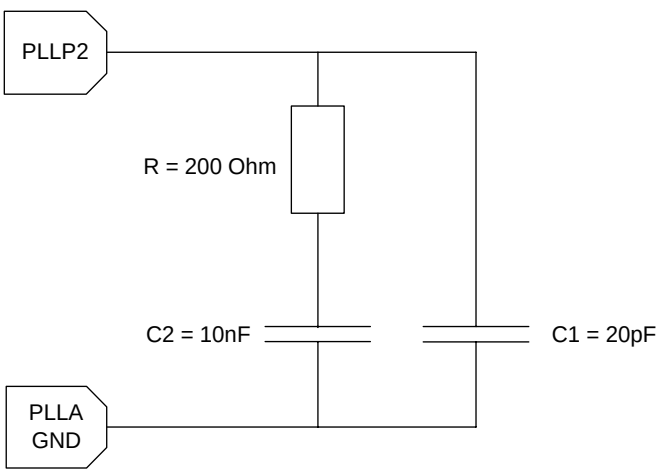
Pin No.	Symbol	Input (I) Output (O)	Function
AF9	$\overline{\text{RCEU1}}$	O	Upstream RAM chip enable for RAM 1
AE11	$\overline{\text{RSCU1}}$	O	Upstream RAM status controller for RAM 1

Downstream Connection RAM Interface (57 pins)

C15, B13, D13, A13, C14, B12, C13, A12, B11, C12, A11, D12, B10, C11, A10, D10, B9, C10, A9, B8, A8, C9, B7, D8, A7, C8, B6, D7, A6, C7, B5, A5	RDATD (31:0)	I/O	Downstream RAM data bus
A19, D18, B19, C20, A20, A14, D15, B18, C19, A22, B21, D20, C21, A21, B20	RADRD (14:0)	O	Downstream RAM address
B14	$\overline{\text{RADVD}}$	O	Downstream RAM advance input
B15, A16, C17, B16	$\overline{\text{ROED}}$ (3:0)	O	Downstream RAM output enable
D17	$\overline{\text{RGWD}}$	O	Downstream RAM global write
C22	RCLKD	O	Downstream RAM clock
A17, C18, B17, A18	RCED (3:0)	O	Downstream RAM chip enable all RAM chips.
C16	$\overline{\text{RSCD}}$	O	Downstream RAM status controller for all RAM chips.
A15	$\overline{\text{RSPD}}$	O	Downstream RAM status processor signal for all RAM chips.

Pin No.	Symbol	Input (I) Output (O)	Function
High Speed Interface, LVDS Levels (36 pins)			
M2 [3]	HCLK	I	High speed clock input, non-inverting.
L1 [3]	$\overline{\text{HCLK}}$	I	High speed clock input, inverting.
W1, U3, R3, R2 [3]	D0O(3:0)	O	Serial data out, plane 0, non-inverting.
Y2, V2, R4, P1 [3]	$\overline{\text{D0O}}$(3:0)	O	Serial data out, plane 0, inverting.
W3, V1, U2, T2 [3]	D1O(3:0)	O	Serial data out, plane 1, non-inverting.
W4, W2, T3, R1 [3]	$\overline{\text{D1O}}$(3:0)	O	Serial data out, plane 1, inverting.
G2, H2, J2, L2 [3]	D0IN(3:0)	I	Serial data in, plane 0, non-inverting.
F1, G1, H1, K1 [3]	$\overline{\text{D0IN}}$(3:0)	I	Serial data in, plane 0, inverting.
C2, D2, E2, F2 [3]	D1IN(3:0)	I	Serial data in, plane 1, non-inverting.
B1, C1, D1, E1 [3]	$\overline{\text{D1IN}}$(3:0)	I	Serial data in, plane 1 inverting.
N1	RCAL	O	Calibration resistor output, 3,9 kΩ to GND
P2	VREF	I	Reference voltage input, 1.23 V: 

Pin No.	Symbol	Input (I) Output (O)	Function
RSATM Interface (5 pins)			
B22	TXDATA	I	Serial data input
A23	$\overline{\text{BSCST}}$	I/O	Bi-directional control signal for transmit.
C23	RXDATA	O	Serial data output
B23	$\overline{\text{BSCSR}}$	I/O	Bi-directional control signal for receive.
D22	RSCLK	I	RSATM clock input
JTAG Interface (5 pins)			
B4 [1)]	TDI	I	Test data input; this pin has an internal pull-up resistor and need not to be connected for normal operation.
A3 [1)]	TCK	I	Test clock; this pin has an internal pull-up resistor and need not to be connected for normal operation.
D5 [1)]	TMS	I	Test mode select this pin has an internal pull-up resistor and need not to be connected for normal operation.
C6	TDO	O	Test data output; need not to be connected for normal operation.
A4 [1)]	$\overline{\text{TRST}}$	I	Test data reset this pin has an internal pull-down resistor and need not to be connected for normal operation. If connected it must be driven to V_L for normal operation.

Pin No.	Symbol	Input (I) Output (O)	Function
Test Interface (16 pins)			
C5 [1]	$\overline{\text{OUTTRI}}$	I	If low switches all output pins and bi-directional pins of the chip into tristate mode. A pull-up resistor to V_{DD} is recommended for normal operation.
B3 [1]	$\overline{\text{UTTRI}}$	I	If low switches all output pins of the UTOPIA interface into tristate mode. A Pull-Up resistor to V_{DD3} is recommended for normal operation.
M4	PLLVDD		Supply pin, connect to 3.3 V
M1	PLLVSS		Supply pin, connect to GND.
L3	PLLP2	I/O	Must be connected to RC-circuit: 
N2	PLLAGND	O	Connect to PLLP2 RC-circuit. Never connect to V_{SS}.
AA3, AB1, AB2 [2]	TMPA(2:0)	I	Device test pins. Can be left open or connected to GND.
Y4 [2]	TCKPA	I	Device test pin. Can be left open or connected to GND.
AA1 [1]	ENPA	I	Device test pin. Do not connect.
Y3	IDDT	I	Device test pin. Connect to GND.
AB4 [2]	TSCANEN	I	Device test pin. Can be left open or connected to GND.

Pin No.	Symbol	Input (I) Output (O)	Function
AC1 [2)]	TSCANM	I	Device test pin. Can be left open or connected to GND.
AC2 [2)]	TSCANR	I	Device test pin. Can be left open or connected to GND.
AD1	NTOUT	O	Device test pin. Do not connect.
AC3, AD5, AC5, AE5, AF4, AD4, AE4, AF3, AE3, AF2	TOUT(9:0)	O	Device test pins. Do not connect.

Supply (pins)

D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21	VDD	I	3.3V supply pins.
A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D19, D23, H4, J23, N4, P23, V4, W23, AC4, AC8, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26	VSS	I	GND pins.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Storage temperature	T_{stg}	- 65 to 125	°C
Voltage on any pin with respect to ground	V_S	- 0.4 to V_{DD} + 0.4	V
Input voltage	V_{in}	-0.5 to V_{CC}+0.5	V
Input / output current	I	-20 to +20	mA
Continuous output current		-25 to +25	mA
Power dissipation	P	3.5	W

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

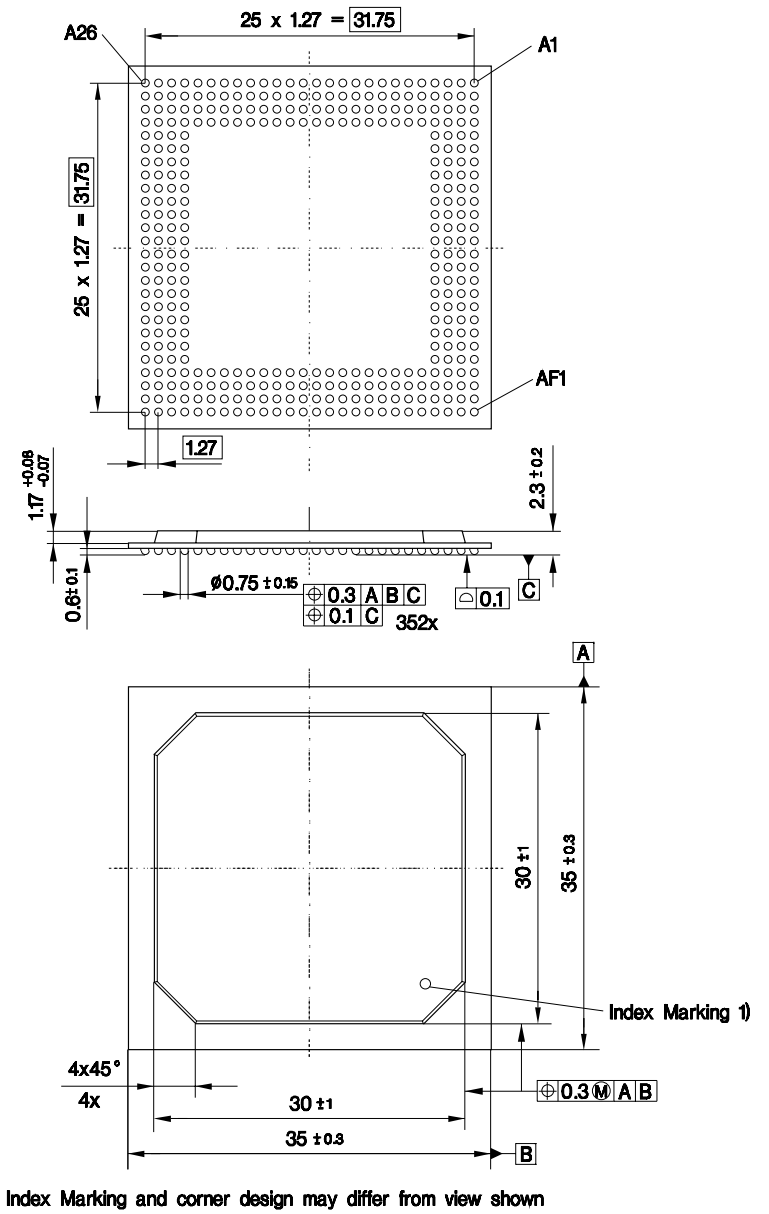
5.2 Operating Conditions

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_{CC}	3.135 to 3.465	V
Digital ground	GND	0	V
Ambient temperature under bias[1)]	T_A	0 to 70	°C
Junction temperature	T_J	max. 100	°C

1) (Extended temperature range -40°C to 80°C upon request)

6 Package Outlines

P-BGA-352-2
(Plastic Ball Grid Array Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Table 7 Thermal Resistance

Parameter	Symbol	Limit Values	Unit
Junction to case	R_{thJC}	3.0	K/W
Junction to ambient air without air flow	R_{thJA}	16.9	K/W
Junction to ambient air with air flow 1.0 m/s	R_{thJA}	14.7	K/W
Junction to ambient air with air flow 2.0 m/s	R_{thJA}	13.7	K/W
Junction to ambient air with air flow 3.0 m/s	R_{thJA}	12.8	K/W

7 Overview Lists

7.1 References

5. UTOPIA Level 1 Specification Version 2.01, March 21, 1994, ATM Forum
6. UTOPIA Level 2 Specification Version 1.0, June 1995, ATM Forum
7. IEEE 1596.3 Standard for Low-Voltage Differential Signals for SCI, Draft 1.3, Nov. 95
8. TIA/EIA PN-3357 (Draft) Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits
9. PXB 4310 E ASM Preliminary Data Sheet, 8/95
10. Traffic Studies of a Multiplexer in an ATM Network and Applications to the future Broadband ISDN', D. Lampe, International Journal of Digital and Analog Cabled Systems, Vol.2, 237-245, 1989

7.2 Acronyms

- ABM = PXB 4330 E ATM Buffer Manager
- ADI = Address Identifier of SLIF cell format
- ALP = PXB 4350 E ATM Layer Processor
- AOP = PXB 4340 E ATM OAM Processor
- AR = Address Reduction
- ARC = Address Reduction Circuit
- ASF = Atm Switching Fabric
- ASM = PXB 4310 E Atm Switching Matrix
- BIP-8 = Bit Interleaved Parity, odd parity bit over whole cell at RSATM interface
- BLCI = Base-LCI
- byte = octet = 8 bit
- CAME = Content Addressable Memory Element PXB 4360 H
- CLP = Cell Loss Priority of standardized ATM cell
- double word = 32 bit
- EMCI = Egress or Multicast Connection Identifier
- FCS = Frame Check Sequence
- HK = HouseKeeping bits of SLIF cell format
- HT = Header Translation
- I/O = Input / Output
- iCLP = internal Cell Loss Priority bit
- ITU-T = International Telecommunications Union - Telecommunications standardization sector
- IWE8 = PXB 4220 InterWorking Element for 8 channels
- LCI = Logical Connection Identifier
- LIC = Line Interface Card or Line Interface Circuit
- LPS = Line Protection Switching
- LSB = Least Significant Bit
- LVDS = Low Voltage Differential Signaling

- MCI = MultiCast Identifier
- PSI = Protection Switch Identifier (special internal ATM cell)
- PT = Payload Type bits of standardized ATM cell
- RA = Routing Address of SLIF cell format
- Res = Reserved bits in SLIF cell format
- rmr = Redundant Module Receiver bit of SLIF cell format
- rms = Redundant Module Sender of SLIF cell format
- RSATM = Reduced Speed ATM (internal communication interface)
- SLIF = Switch Link InterFace
- SN = Sequence Number of SLIF cell format
- SSN = Switching Stage Number of SLIF cell format
- SSRAM = Synchronous Static RAM
- tbd = to be defined
- TM = Traffic Management
- UTOPIA = Universal Test and OPeration Interface for Atm
- VCI = virtual channel identifier of standardized ATM cell
- word = 16 bit