SIEMENS

ICs for Communications

ATM OAM Processor
AOP

PXB 4340 Version 1.1

Product Overview 04.97

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1 Introduction

1.1 ATM Layer Chip Set Overview

The PXB 4340 AOP is a member of the Siemens ATM layer chip set. It consists of the five chips

- PXB 4310 ATM Switching Matrix ASM
- PXB 4325 ATM Switching Preprocessor ASP
- PXB 4330 ATM Buffer Manager ABM
- PXB 4340 ATM OAM Processor AOP
- PXB 4350 ATM Layer Processor ALP.

These chips form a complete chip set to build an ATM switch. A generic ATM switch consists of a switching fabric and switch ports as shown in **figure 1**.

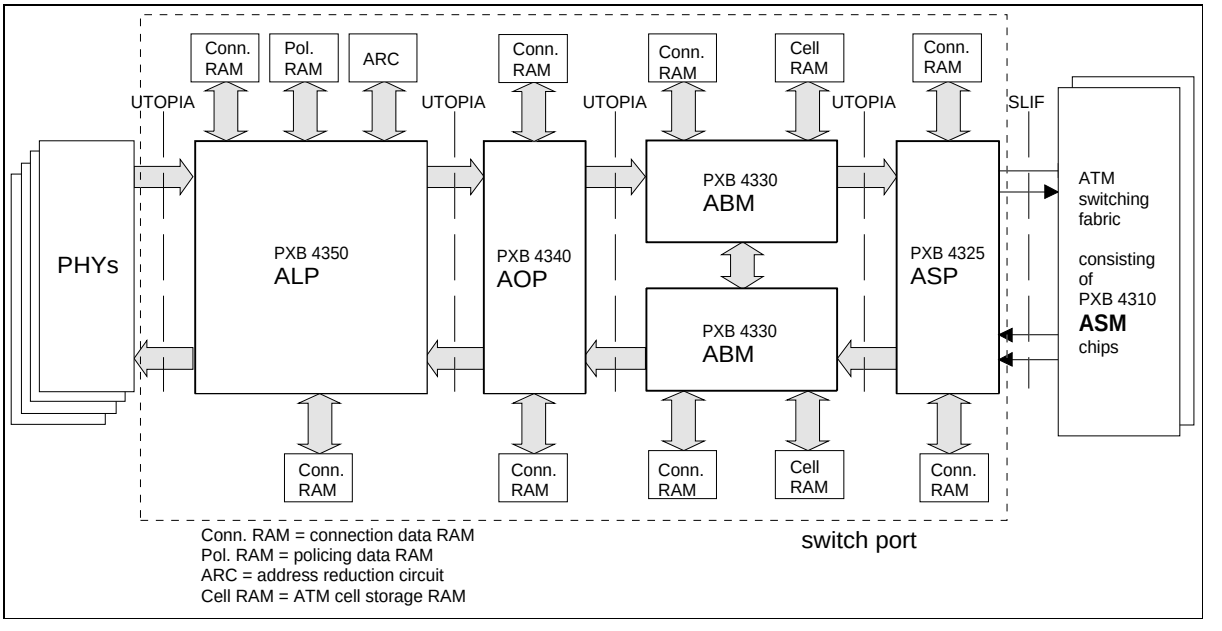

Figure 1
ATM Switch basic Configuration

In the Siemens ATM layer chip set the switching fabric only does cell routing using the PXB 4310 ASM, which can be used stand alone or in arrays to scale switching fabric throughput from 2.5 Gbit/s up to more than 40 Gbit/s. All other ATM layer functions are performed on the switch ports: policing, header translation and cell counting by the PXB 4350 ALP, OAM functions by the PXB 4340 AOP and traffic management by the PXB 4330 ABM. The PXB 4325 ASP is the access device to the switching fabric and adds/removes the routing header. It also supports redundant switching fabrics and does multicast.

Only two interfaces are used for data transfer: the industry standard UTOPIA [**1, 2**] Level 2 multi-PHY interfaces and the proprietary Switch Link InterFace SLIF. This is a serial, differential high speed link using LVDS [**3**] levels.

For low end applications a single board switch with 622 Mbit/s throughput can be built with only one PXB 4350 ALP, one PXB 4340 AOP and one PXB 4330 ABM. Such a mini-switch (**figure 2**) is basically one switch port stand alone, without switching network access via the PXB 4325 ASP. It could also be a multiplexer connecting many subscriber lines to one access line.

If the full OAM functionality is not needed the PXB 4340 AOP chip could be omitted. Minimum OAM and multicast functionality is also built into the PXB 4350 ALP. The Address Reduction Circuit ARC could be omitted if the built-in address reduction is sufficient. If the ABM is not needed some glue logic is required to loop the UTOPIA interface of the PXB 4340 AOP and to do some minimum LCI translation.

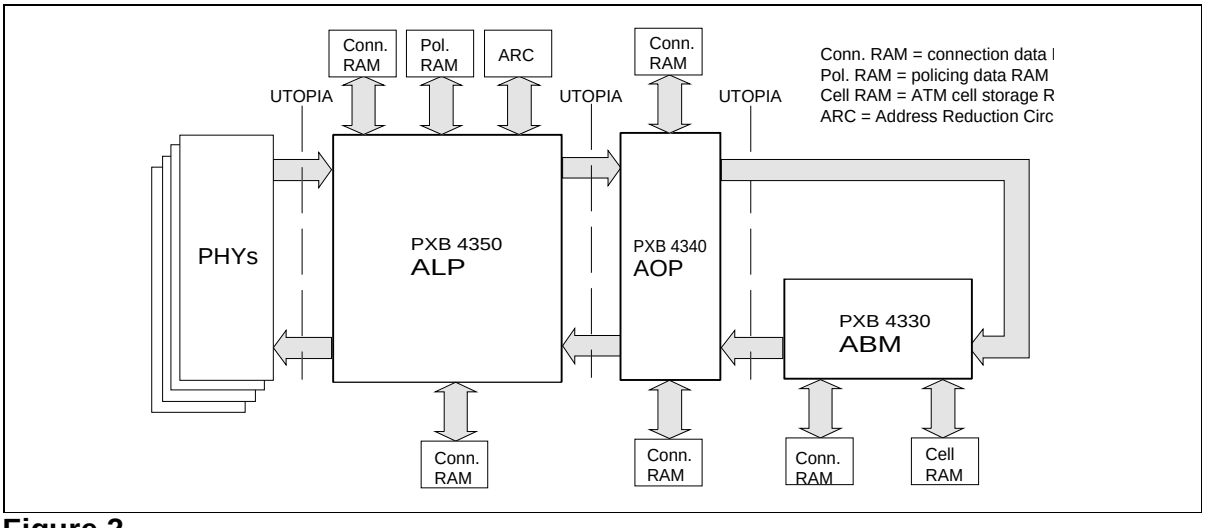

Figure 2
Mini Switch with 622 Mbit/s Throughput

Apart from the two applications of **figure 1** and **2**, many other combinations of the chip set are possible in designing ATM switches. Functionality is selectable in many combinations due to the modular function split of the chip set. Address reduction, multicast, policing, redundant switching network and other functions can be implemented by appropriate chip combinations. The number of supported connections scales with the size of the external connection RAMs. The policing data RAM can be omitted if this function is not required.

Thus functionality and size of an ATM switch can be tailored exactly to what the respective application requires, without carrying the overhead of unnecessary functions.

1.2 Nomenclature

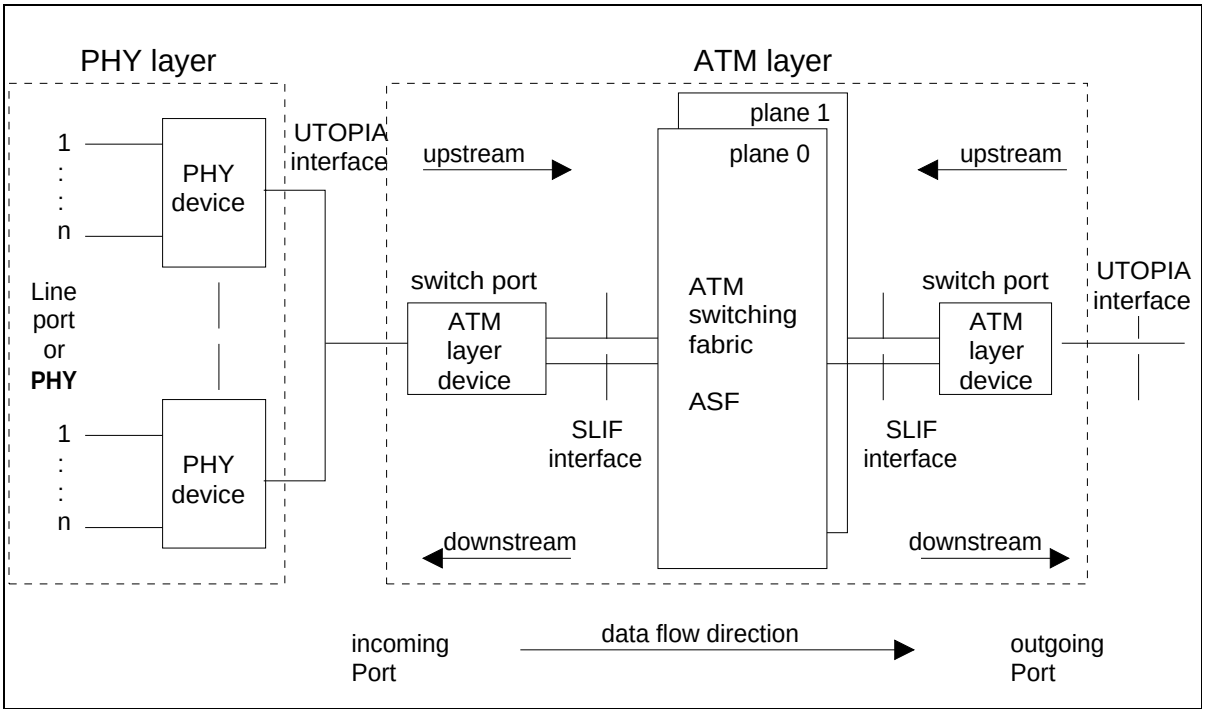

Figure 3: Nomenclature

- PHY = line port.
- PHY device = a component (chip) containing the PMD (physical media dependent) and TC (transmission convergence) sublayers of one or several line ports. Both PMD and TC together form the Physical or PHY layer. For the interface between PHY and ATM layer the UTOPIA interface is used.
- UTOPIA = Universal Test and OPerations Interface for ATM, defined by the ATM Forum in [**1**] and [**2**].
- Switch port = in the Siemens ATM switching strategy performs all ATM layer functions except routing.
- ATM layer device = combinations of the chips PXB 4350 ALP, PXB 4340 AOP, PXB 4330 ABM and PXB 4325 ASP as shown e.g. in **figure 1**. They perform the ATM layer functions as header translation, policing, OAM, traffic management etc. and are interconnected with the UTOPIA interface.
- ATM switching fabric ASF = array of PXB 4310 ASM chips, does space switching of ATM cells (routing); including the buffering of cells for cell level congestion.
- Planes 0 and 1 = two redundant switching fabrics, which should be identical.
- Incoming / outgoing port = refers to a connection with the data flow direction as shown in **figure 3**.
- Upstream / downstream = refers to the ATM switching network; the direction towards the ASF is upstream, coming from the ASF is downstream.

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1.3 Features

Performance

- Performance up to STM-4/OC-12 equivalent ATM layer processing
- Throughput up to 687 Mbit/s bi-directional
- Up to 16384 connections in both directions (VPC/ VCC)
- Temperature range from 0°C to 70°C

- Multiport UTOPIA Level 2 interface in up- and downstream direction according to ATM Forum, UTOPIA Level 1 and 2 specifications [**1, 2**]
- 16-bit microprocessor interface, e.g. 386EX
- Cell insert/extract function
- 32 cell Fifo buffer at UTOPIA upstream receive interface
- 96 cell shared buffer for up to 24 PHYs at UTOPIA downstream transmit interface
- Boundary scan support according to JTAG [**4**]
- Internal data stream loop at ATM and at PHY side

External RAMs

- Two external SSRAMs for connection related data, one for upstream and one for downstream direction, 2 x 4 Mbit for 16K connections
- DMA for fast data transfer between external RAM and microprocessor
- All entries parity protected
- Usable as extended microprocessor memory

OAM Functions

- OAM Levels and Flows (F4/F5) according to ITU-T/I.610 [**6**] and Bellcore GR-1248 [**7**]
- All OAM cell types hard-wired
- Generation, discard, extraction and insertion of OAM cells

Type	Ordering Code	Package
PXB 4340	Q67001-H9310	BGA-352

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- Programmable OAM cell types for future standardization

AIS/RDI/CC Functions

- AIS/RDI/CC function for all connections permanently active
- Automatic generation of VP/VC-AIS cells at line failures
- Automatic generation of VC-AIS cells for all VCCs of a VPC at the endpoint including automatic backward emission of VP-RDI cells
- Automatic generation of VP/VC-CC cells at ATM layer failures
- Optional internal CC function for switch test (proprietary)
- Programmable guard times and cell insertion intervals
- Support of CC activation/deactivation cells

Loopback

- Automatic loop of cells for all connections with LB ID inversion
- Programmable Port ID for on the fly comparison with Location ID or Source ID of LB cells
- Insertion/extraction of LB cells via microprocessor

Performance Monitoring

- 128 simultaneous PM generation/ evaluation processors shared for up- and down-stream direction
- Full HW evaluation of FM cells and generation of BR cells
- Full HW support of data collection according to Bellcore GR-1248 for 128 connections
- Support of PM activation/deactivation cells
- Support of simultaneous PM flows of F4 and F5 level
- Support of adjacent PM segments in one PXB 4340 AOP

Technology

- BGA-352 package
- Expected power dissipation 2.2 W

OAM Functions which are not supported

- Combined Monitoring and Reporting OAM cells for performance monitoring
- Time stamp in Forward Monitoring OAM cells
- Defect type and defect location fields in AIS/RDI cells
- Simultaneous generation of end-to-end and segment FM cells

1.4 Logic Symbol

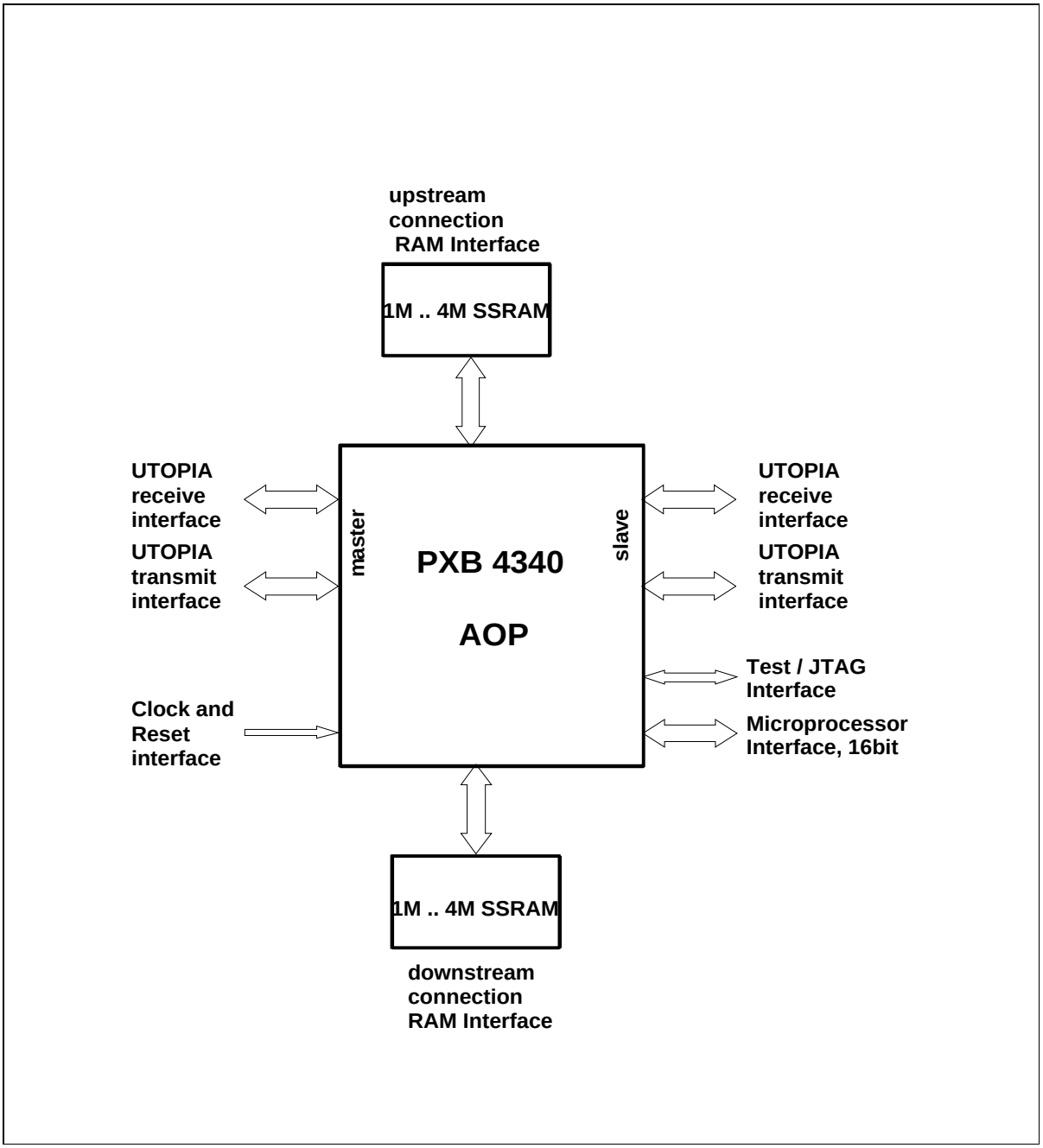

Figure 4
Logic Symbol

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1.5 System Integration

The PXB 4340 AOP is located at the ports of a switch so that each ATM cell passes two PXB 4340 AOP devices, one at the ingress port and one at the egress port.

The PXB 4340 AOP assumes that all connections are set-up bi-directional with the same Local Connection Identifier LCI in both directions. In the Siemens ATM chip set environment (**see figures 1, 2 and figure 5**) the LCI is provided by the PXB 4350 ALP and contains VPI, VCI and PHY information. The PXB 4340 AOP uses pointers to define a connection as VPC or VCC (**see figure 12**); the PHY number is not evaluated. If the PXB 4340 AOP is not used together with the PXB 4350 ALP it can operate on VPI or VCI identifiers only. In these cases the OAM functionality is reduced accordingly.

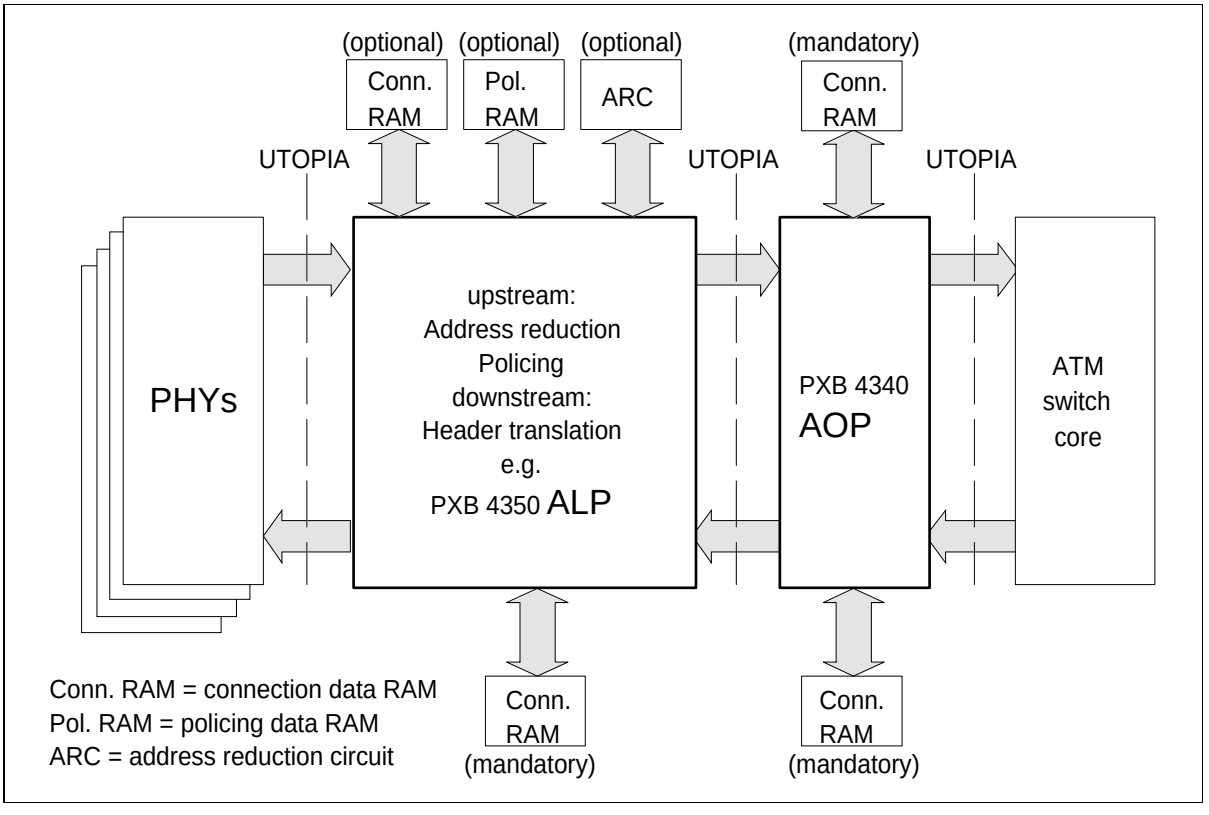

Figure 5: Location of PXB 4340 AOP on a Switch Port

1.6 System Control Overview

In large switches there are typically two control levels, the central system controller and peripheral controllers as shown in **figure 6**. Throughout this document the peripheral controllers are referenced as „microprocessor“.

The peripheral controllers are located on the line cards where they control all components. Typical tasks are initialization, board self test, maintenance, connection handling etc. The peripheral controller knows about the HW configuration of the line card and con-

verts messages from the system controller (e.g. connection set-up) into register accesses.

The system controller does operation and maintenance of the whole switch running high level SW for signalling and network management.

Two groups of connections are terminated at the system controller:

- Signalling connections from all subscribers/terminals
- Control connections to all peripheral controllers

In **figure 12** only the control connections are shown.

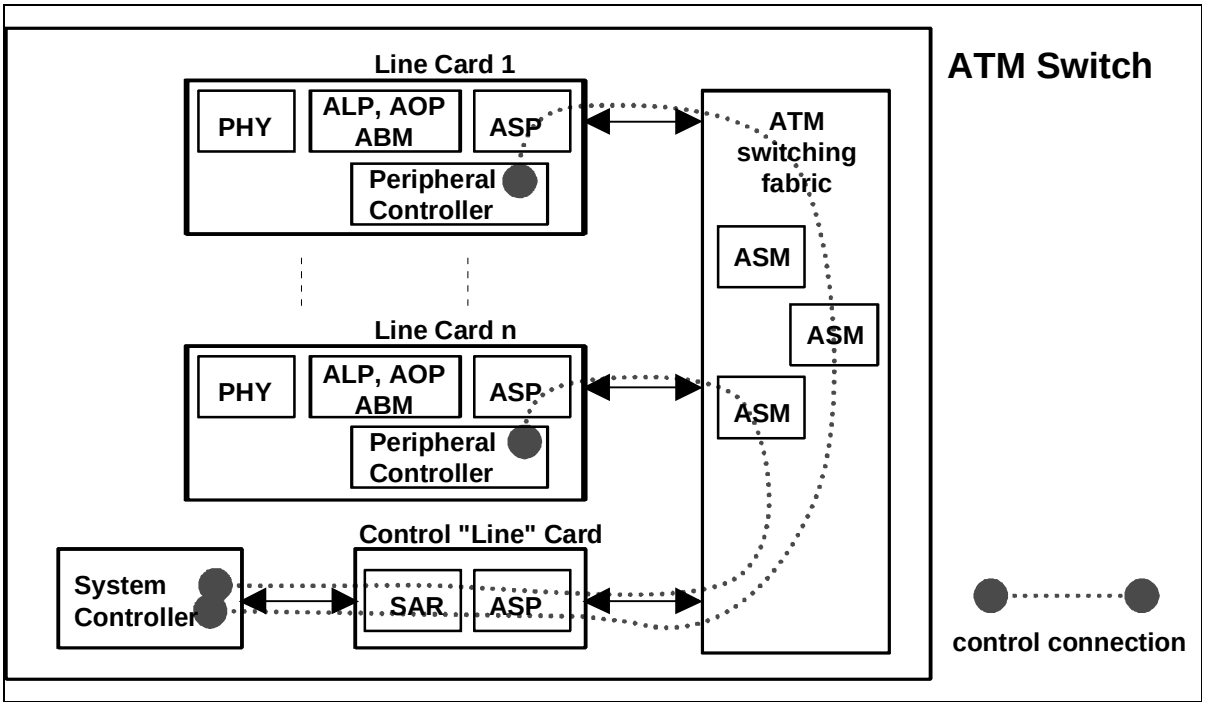

Figure 6: Switch Control Example

The Siemens ATM switching solution offers an embedded control channel using the data links inside the switch. PXB 4310 ASM and PXB 4325 ASP extract and insert the cells of the control channel via the Reduced Speed ATM (RSATM) interface. The termination of the control connections on the line cards is done by the peripheral controller, whereas the other end of the connection could be terminated by a Segmentation and Reassembly device as e.g. the PXB 4110 SARE. The system controller can terminate not only control connections, but also signalling connections to/from the subscribers/terminals, as both use AAL5.

1.7 Application Scenarios

In this section a switch with one incoming and one outgoing port is represented by the symbol shown in **figure 7**.

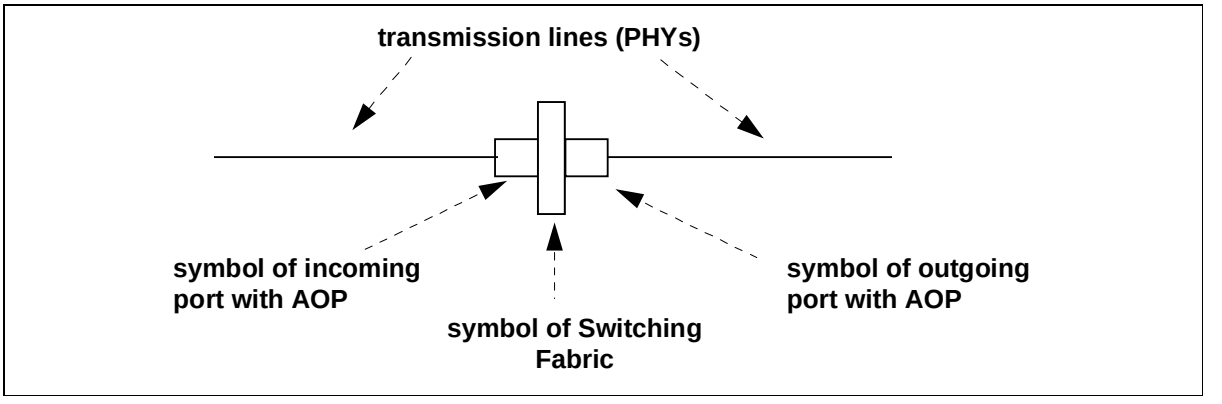

Figure 7: Symbol for Switch with AOPs

The PXB 4340 AOP can be configured according to its location in the network as shown in the following examples.

Within a pure ATM network VPCs may be originated or terminated. In addition VP segments can be originated or terminated as shown in **figure 8**.

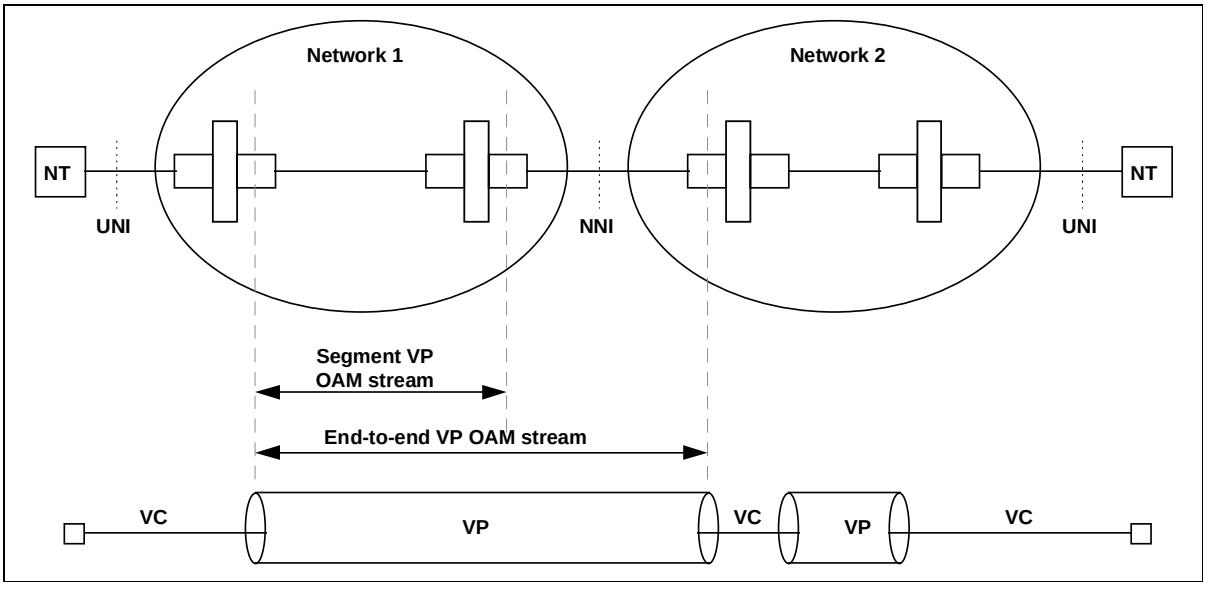

Figure 8: VP Level OAM Functions

As VPCs are always terminated at an ingress port and originated at an egress port, the functionality of the PXB 4340 AOP is restricted accordingly. For example it is not possible to terminate VP-AIS cells at the egress port of a switch. **Table 3** shows an overview over all possible layer points.

VCCs are not originated or terminated within a pure ATM network, but only VC segments (**figure 9**).

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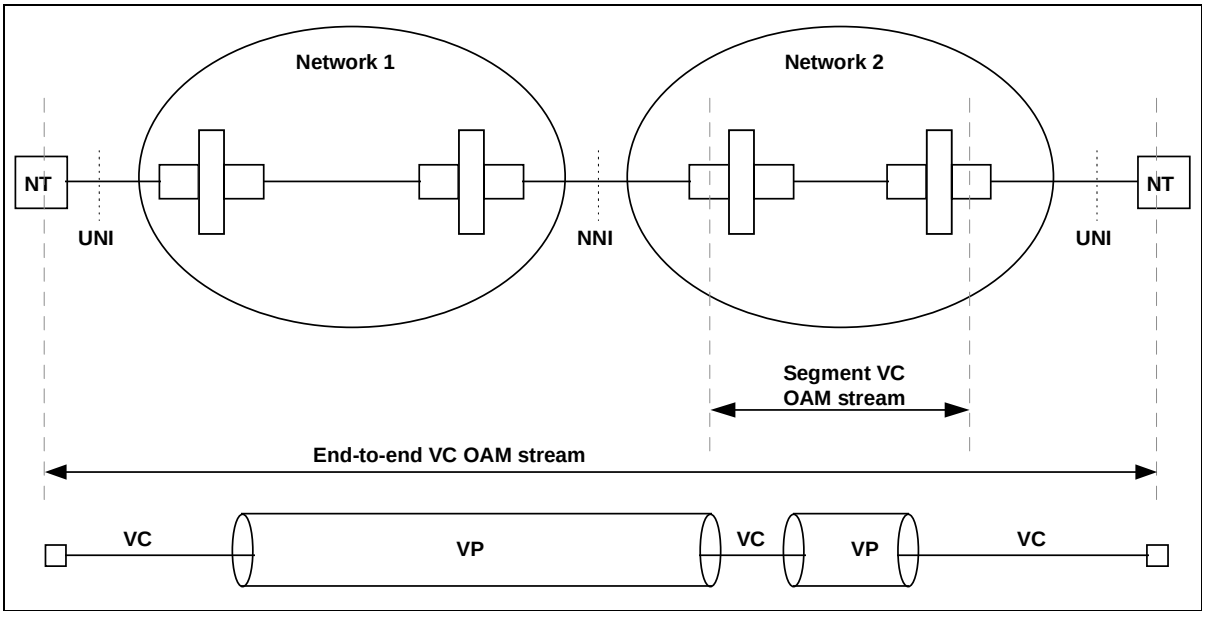


Figure 9: VC Level OAM Functions

In a heterogeneous network containing ATM and non-ATM interfaces VCC origination or termination occurs at the AAL function, as e.g. Circuit Emulation Service (CES) with AAL1 or Segmentation and Reassembly (SAR) with AAL5 as shown in **figure 10**.

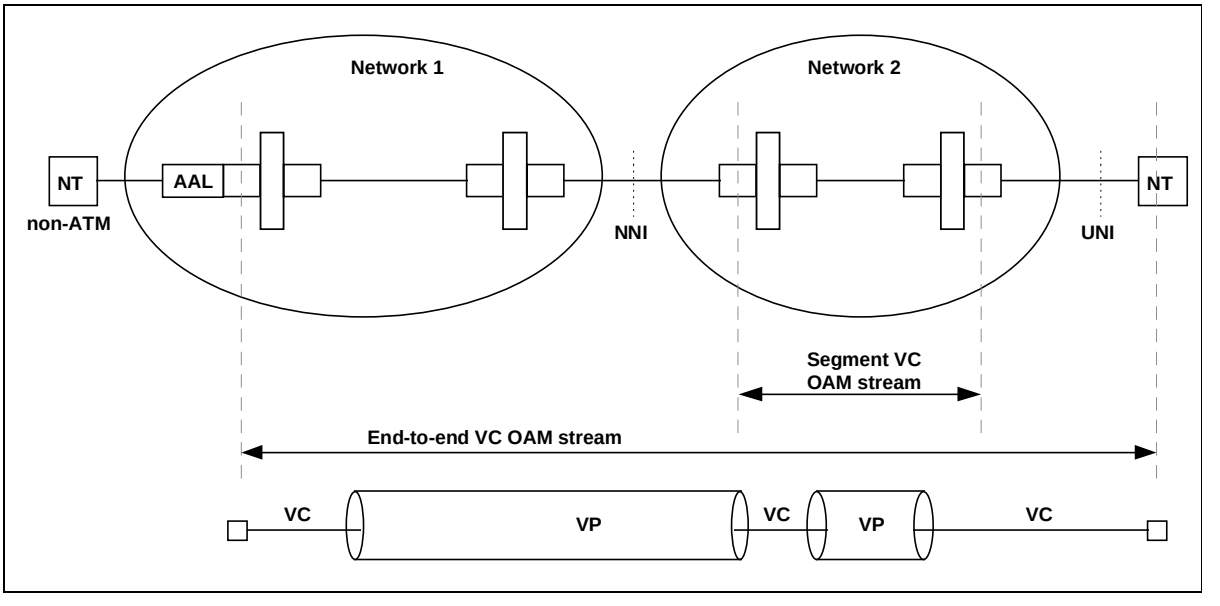


Figure 10: VC Endpoint inside the Network

The PXB 4340 AOP in downstream direction terminates the OAM cell stream just before the AAL device which terminates the ATM connections.

2 Functional Description

2.1 Overview

The PXB 4340 AOP provides full standardized OAM functionality of the ATM layer in one device, covering the functions Fault Management (AIS, RDI, CC, LB) and Performance Monitoring (FM flow, BR flow, Data Collection). It has STM-4/OC-12 equivalent throughput in upstream and downstream direction.

The AIS, RDI, CC mechanism can be applied to a range of up to 16K (=16384) connections. Performance Monitoring can be done for 128 connections simultaneously with each connection selectable from up- or downstream direction. Loopback functionality can be applied to the full range of up to 16K connections.

Data cells are transferred via industry standard Level 2, single-port/ multi-port UTOPIA interfaces based on cell level handshake. They can be adjusted for 8-bit or 16-bit data transfer. The ATM side UTOPIA interface is operating in slave mode, the PHY side UTOPIA interface in master mode. The PHY number of a cell is transported transparently through the chip, i.e. a cell input at an UTOPIA receive interface with the PHY number P is output at the corresponding UTOPIA transmit interface with the same PHY number P. Note that the PHY number is not the UTOPIA address, but contains address and handshake line pair information (**see section 4.1**)

Two 32 bit external SSRAM blocks are provided for OAM data storage for each connection. Their size is depending on the number of supported connections.

Chip control is performed by a standard 16-bit asynchronous microprocessor interface (e.g. for 80386EX). The microprocessor can access the external RAMs any time during operation. This is necessary for connection set up/release, data read/modify/write and configuration adjustment. The external RAM is not memory mapped into the microprocessor address range. Accesses occur via a transfer register set using transfer commands or via DMA.

All functions are supported to a great extent in HW, so that SW effort is minimized.

2.2 Throughput

Data throughput is depending on the chip operating clock SYSCLK, which is used for the chip core and the external SSRAMs. The PXB 4340 AOP needs 32 cycles of the SYSCLK to process one ATM cell. Thus in 32 cycles 64 octet are transported through the chip for 53 octet ATM cell, giving a penalty of 53/64. Hence the ATM cell throughput is:

ATM cell throughput[Mbit/s] = SYSCLK[MHz] x 16 x 53/64 = SYSCLK[MHz] x 13.25

For the frequency 51.84 MHz the throughput is 686.88 Mbit/s. The 51.84 MHz are easy to generate, as this is 1/3 of 155.52 MHz, the ubiquitous SDH/SONET frequency.

The clock of the UTOPIA interfaces is independent on SYSCLK. It should be less or equal to SYSCLK frequency. This is not a restriction, as the transfer time for a cell at the UTOPIA interface is only 27 clock cycles.

2.3 Cell Handling

Each cell entering the PXB 4340 AOP via the upstream/downstream receive UTOPIA interface is identified as user cell or as OAM cell. The chip recognizes all standardized OAM cells and has two programmable comparators for possible new OAM cell types. Data stored on a connection basis in the external RAMs determines if a connection is enabled and which layer point is configured (see **table 3** for all possible configurations). Accordingly the respective function is performed.

- For example a VP-AIS cell would be ignored at a VP segment endpoint.
- As an other example a user cell belonging to a VPC for which end-to-end performance monitoring is enabled is counted and its checksum (BIP-16) added to the checksum in the AOP located at the VP endpoint.

In the respective OAM processing block new status information is calculated, for example alarm indication bits, BIP-16 checksums, cell counts etc.

Whereas user cells are never modified and are always forwarded, OAM cells can be

- generated and inserted into the cell stream in up- or downstream direction
- extracted from the cell stream and discarded or dropped to the receive buffer
- forwarded with or without modification
- looped with modification.

For OAM cell generation the PXB 4340 AOP uses the configuration bits of the respective connection to determine the OAM cell type: F4 or F5 and segment or end-to-end.

When detecting OAM cells the PXB 4340 AOP recognizes F4 or F5 OAM cells for end-to-end or segment. According to the configuration the required actions are performed.

2.4 Cell Buffering and OAM Cell Insertion

The PXB 3440 AOP has four cell buffers located close to the two UTOPIA interfaces in each direction (**figure 11**):

- UTOPIA upstream receive interface: 32 cells, single queue
- UTOPIA upstream transmit interface: 4 cells, single queue
- UTOPIA downstream receive interface: 4 cells, single queue
- UTOPIA downstream transmit interface: 96 cells, shared buffer with 24 queues.

The 4-cell buffers cope with the UTOPIA slave handshake at the upstream transmit and downstream receive interface.

The upstream receive buffer of 32 cells stores incoming user cells during the insertion of OAM cells. OAM cells can be generated or looped from the opposite direction. The PXB 4340 AOP uses forced insertion for all OAM cells. Forced insertion is disabled beyond a buffer filling level which is programmable separately for up- and downstream direction. The OAM cells to be inserted are lost in this state.

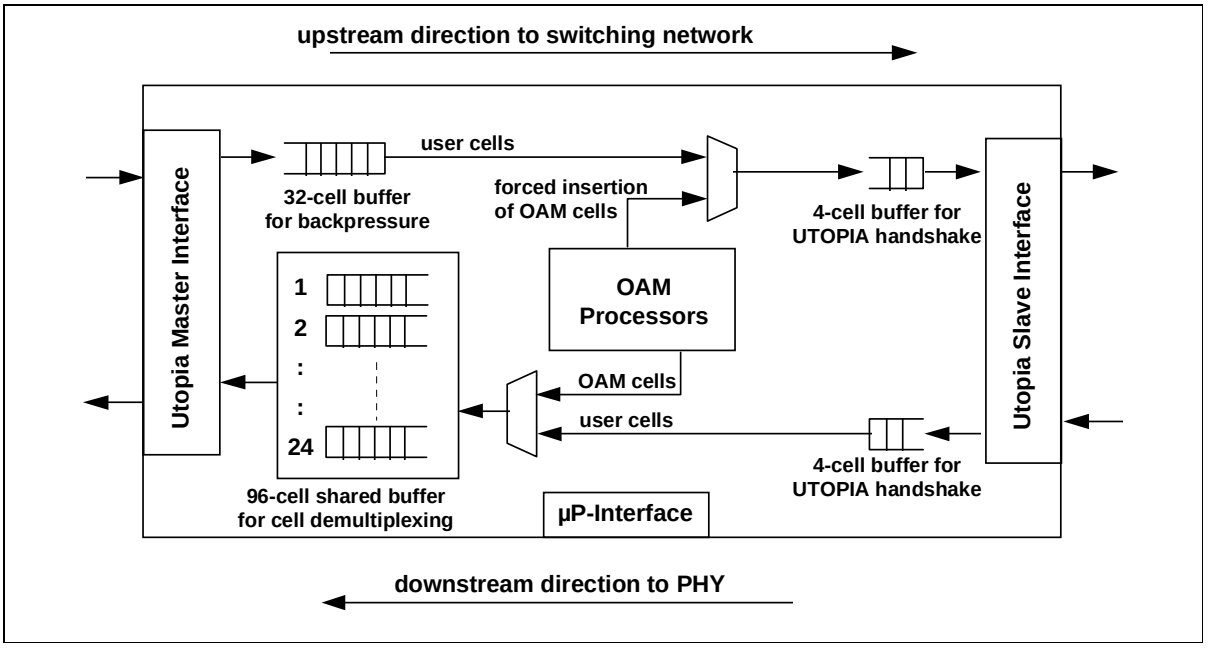


Figure 11: Cell Buffers in PXB 4340 AOP

The downstream transmit buffer also does forced OAM cell insertion by back-pressuring user cells to the downstream receive interface and possibly to the previous chip. It is realized as shared buffer of up to 24 queues, associated to the respective PHYs. The back-pressured user cells then are released in bursts of up to 687 Mbit/s. These bursts must be stored by the downstream transmit buffer and released to the PHYs according to their respective speed. The downstream transmit buffer has 2 thresholds for each queue:

- the UTOPIA backpressure threshold:
  beyond this threshold the backpressure signal is given to the downstream receive interface for this PHY
- the OAM cell insertion threshold:
  beyond this threshold the insertion of OAM cells is disabled. As with the upstream receive buffer in this state OAM cells which are to be inserted are lost.

The two thresholds are identical for all queues. The UTOPIA backpressure threshold should be programmed to a value lower than the OAM cell insertion threshold, this difference guarantees a cell storage space for OAM cells.

The ATM cell load should be selected by the user in a way that the probability to lose OAM cells is almost zero (e.g. 10^{-11}). This is done by reserving bandwidth for the inserted OAM cells. OAM cell bandwidth is mainly depending on the selected PM block size (128, 256, 512, 1024). In worst case, when F4 and F5 level PM cell streams are generated, the overhead is still less than 2%.

Lost OAM cells do not lead to system malfunction. If e.g. a FM cell is lost the PM processor continues to count user cells and BIP-16 checksums. The correct values will be sent out with the next block. Thus block size would be e.g. 256 instead of 128 in case of a lost

cell. The insertion of AIS/RDI/CC cells will only be temporarily halted during the (very unlikely) case of buffer overflow. A LB cell to be looped, however, will be lost. Here only the repeat function would help.

2.5 Addressing of external RAMs

The external RAMs for the storage of connection related OAM data are symmetrical in up- and downstream direction. Also the addressing is symmetrical as the LCI values for forward and backward connection are identical. Note that according to the standards each ATM connection is set-up bi-directional, but not necessarily with the same bit rate in both directions.

Both external RAMs are divided into a F4 and a F5 OAM table. Each connection entry has 4 dwords. With the LCI of the cell first the VC-specific table is addressed. Therein a F4 pointer is contained pointing to a VP-specific entry. There are two cases, both depicted in the circle of **figure 12**:

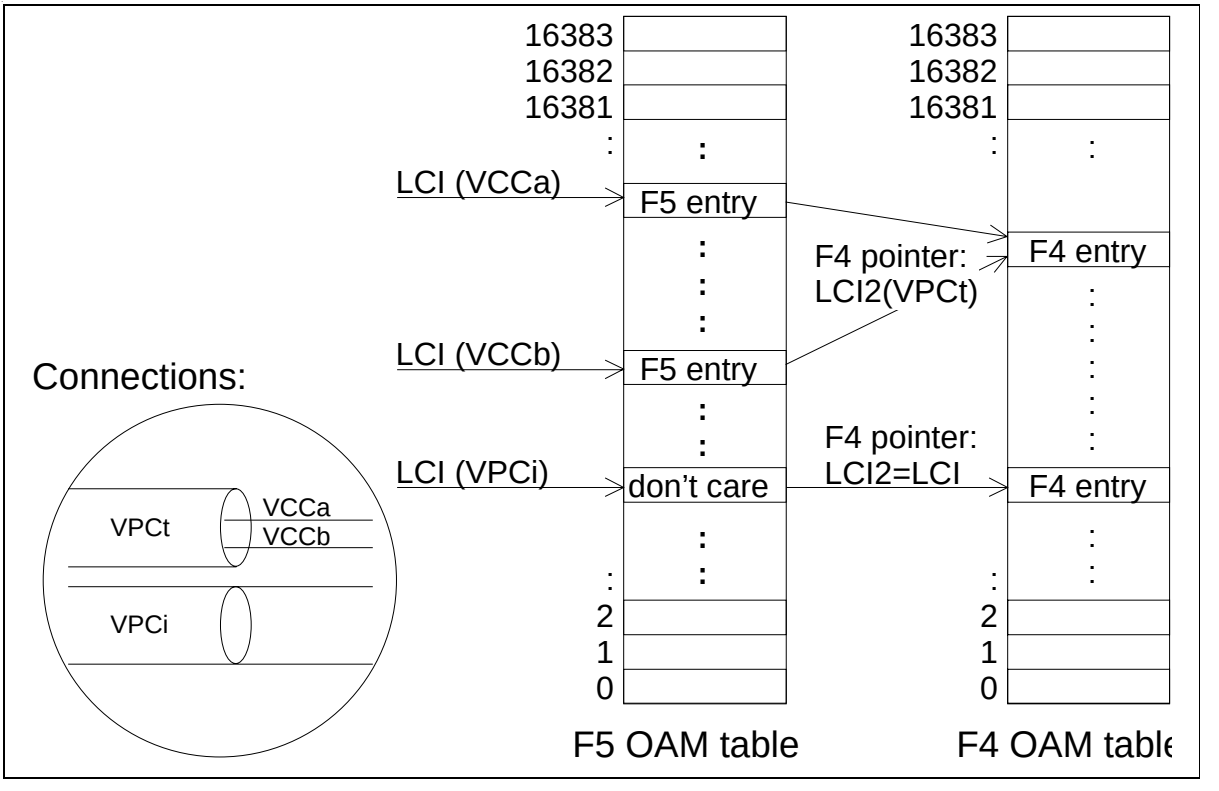


Figure 12: Pointer Structure of up- and downstream OAM Tables

1. A VPC intermediate point
   In this case the F5 entry is don't care, except the pointer to the VP-specific entry. See e.g. VPC_i in **figure 12**. The VP-specific entry contains the OAM data for the VPC.

2. A terminated VPC decomposed into VCCs
   In this case each VCC has a F5 entry with identical F4 pointers pointing all to the same F4 entry. See e.g. VCC_a and VCC_b of VPC_t in **figure 12**.

2.6 OAM Functions Overview

There are two groups of applications for OAM functions: alarms and measurements. Alarm functions inform user and network operator about network failures. These include the OAM functions

- Alarm Indication Signal AIS
- Remote Defect Indication RDI
- Continuity Check CC.

AIS and RDI are used to convey transmission line failure information to subscriber and network operator; CC detects ATM layer failures.

As failure events are unpredictable the alarm supervising HW is always running. When a failure occurs the notification process automatically starts.

Measurements are initiated for diagnosis purpose by the network operator. Therefore these functions need not be permanently active for all connections. The respective OAM functions are:

- Loopback LB
- Performance Monitoring PM

LB checks the connectivity of a connection by sending a single cell which is looped back at predefined points. LB is used e.g. immediately after connection set-up or periodically to check all permanent connections of a network using end-to-end or segment LB. A network operator could also use intra-domain LB to localize a failed link. Another option for loopback are subscriber initiated loops either end-to-end to the partner or access line LB to the first node in the network.

PM is a more precise tool than LB. It checks not only the connectivity, but the real performance of a connection in terms of bit failures and cell losses. As it requires complex HW support and SW performance PM will not be activated permanently for all connections. E.g. VPCs or permanent VCCs could be monitored if a subscriber pays for this service. Also a network operator would use PM to check the quality of a connection if a subscriber complains it.

2.7 Alarm OAM Functions (AIS/RDI/CC)

There are two types of failures detected by the alarm functions: transmission line failures and ATM layer failures. Transmission line failures are e.g. line brakes, failures of lasers or failures of reception diodes. Typical ATM layer failures are the misrouting of cells in the switching fabric or a falsified entry in a routing table. All the cells of a connection are then forwarded to a wrong destination.

2.7.1 Transmission Line Failures (AIS/RDI)

Transmission line failures are recognized by the receiving PHY and conveyed to the PXB 4340 AOP by the on-board control processor. It is sufficient to set one single bit for the respective PHY to initiate the periodic insertion of AIS cells for all affected connections. The PXB 4340 AOP automatically inserts VP-AIS cells for VPCs and VC-AIS cells for VCCs. **Figure 13** shows that this case occurs at the incoming port of a switch.

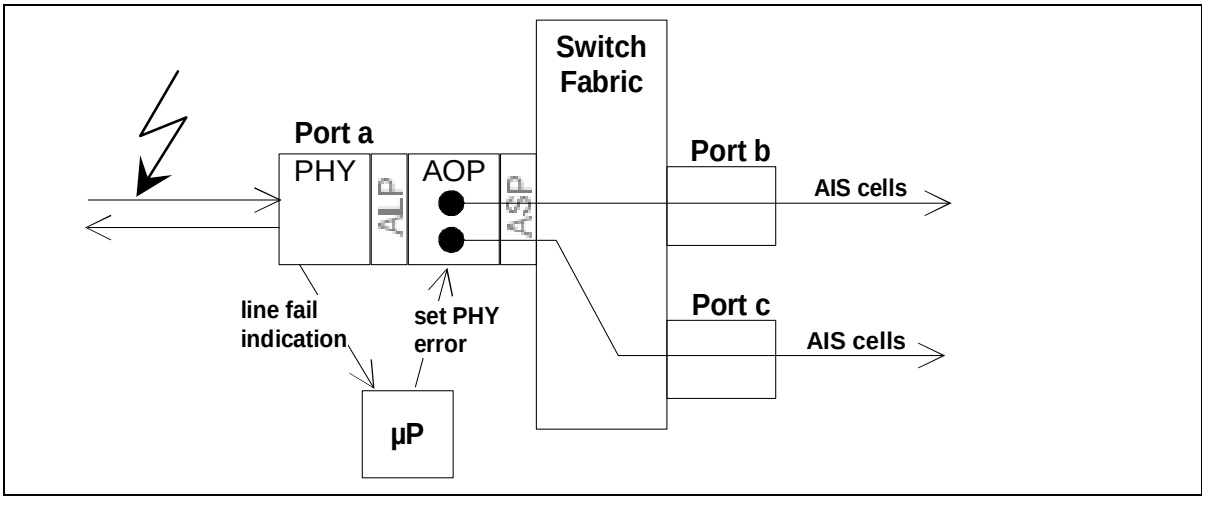


Figure 13
Example for Line Failure Notification via AIS cells

VC-AIS cells travel up to the endpoint of the connection, which normally is the user terminal. Thus within a very short delay time - determined by the control processor's response time, the PXB 4340 AOP insertion delay and the cell transfer time - the user is informed about the failure.

The PXB 4340 AOP insertion delay is determined by the scan mechanism used for all alarm functions: a HW mechanism triggered by the microprocessor scans through all connections within about 0.5 s and a repetition interval of nominally 0.5 s. If the scan mechanism has passed a connection entry just before an AIS condition became true the maximum waiting time for the next scan access is about 0.5 s.

VP-AIS cells travel up to the VP endpoint which normally is within the network. Moreover, at the VP endpoint - which is at the incoming port of a switch - the VCCs contained in this VPC are distributed in various directions. Each VCC must be informed about the failure.

The PXB 4340 AOP automatically performs the following actions when receiving VP-AIS cells at a VP endpoint:

- discard of VP-AIS cells
- declaration of AIS/RDI **defect** states and insertion of the following cell types after at most 0.5 s with a period of 1 s::
  a) VP-RDI cells in backward direction. This measure informs the origin of the VPC

about the failure. RDI makes sense in the cases where the failure of the line affects only one direction. The automatic RDI generation in backward direction assumes bi-directional connections with the same identifier (LCI) in both directions.
b) VC-AIS cells in forward direction for each VCC of this VPC. This measure informs all users sharing this VPC about the failure in the network.

- Declaration of AIS/RDI **failure** states after 3.5 s persistence of AIS defect state. The cell insertions continue unaffected.

Both forward and backward cell insertions are initiated by the scan mechansim (**see section 2.15**). All delay times given are default values, recommended by I.610 [**6**]. The PXB 4340 AOP allows to program these values in multiples of the scan frequency which in turn is given by the microprocessor.

2.7.2 ATM Layer Failures (CC)

The mechanism to detect failures like misrouting is the Continuity Check (CC). Its idea is to insert dummy cells in a connection if it is inactive, i.e. if the user is not sending data cells. The dummy cells are called CC OAM cells and are inserted at the originating end-point of a connection after a 1-second absence of user cells. The repetition interval is one second. At the connection/segment endpoint the CC cells are discarded. If no user or OAM cells are received within 3.5 seconds the Loss of Continuity (LOC) defect state is declared. Like AIS state LOC causes the automatic insertion of VP-AIS or VC-AIS cells for the affected connections.

Figure 14 shows an example for the operation of CC: two VCCs entering a switch at ports a and b should both be forwarded to port c. Due to misrouting within the switching fabric the cells of VCCb are forwarded to an unconnected switch output, where they are lost without being notified. The CC detection function at port c, however, detects the absence of user cells after the 3.5 s time-out and inserts VC-AIS cells for the connection b.

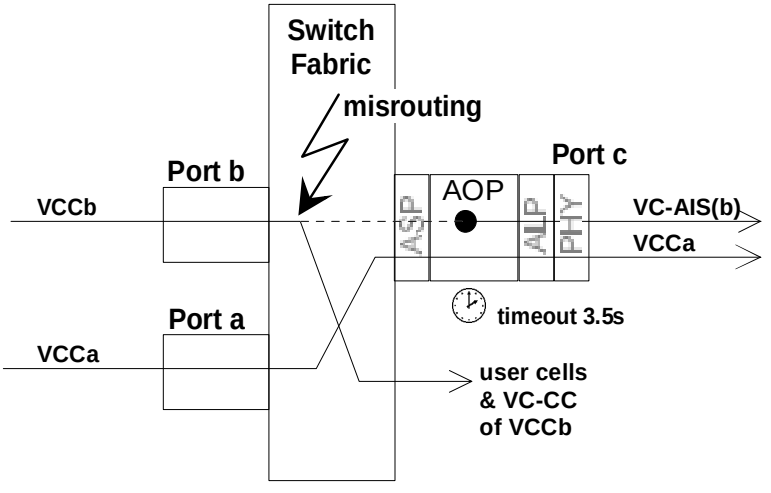


Figure 14: Example for Misrouting Failure Detection

The PXB 4340 AOP supports the CC function for all 16384 connections in both up- and downstream direction. Setting one bit in the respective connection RAM is sufficient to activate the origination or the termination of a CC flow. All other actions are automatic:

At the CC origination point:

- continuous supervision of user cell stream
- periodic insertion of CC cells in 1 s intervals after 3.5 s time-out

At the CC termination point:

- discard of CC cells
- declaration of LOC **defect** state and insertion of AIS cells in 1 s intervals after 3.5 s absence of user or OAM cells
- declaration of LOC **failure** state if LOC defect state persists for 2.5 s.

The LOC failure state is notified to the control processor, while still AIS cells are automatically generated. This additional filtering according to the standards avoids frequent notifications to the microprocessor due to sporadic errors.

All cell insertions are initiated by the scan mechansim (**see section 2.15**). The delay times given are default values, recommended by I.610 [**6**]. The PXB 4340 AOP allows to program these values in multiples of the scan frequency which in turn is given by the microprocessor.

To further limit the load for the microprocessor the DMA function is provided which transfers relevant status bits for all connections to the control processor memory in the background (**see chapter 2.15**).

The insertion of AIS cells occurs as in the AIS state (**chapter 2.7.1**), i.e. with periodic insertion of VP-AIS or VC-AIS cells and VP-RDI cells in backward direction. No additional AIS cells are inserted if AIS and LOC state are declared simultaneously.

Additionally to the standardized CC an Internal Continuity Check ICC is provided as proprietary function. It uses CC cells with a specially marked header (**see section 7.2.4**) between incoming to outgoing port. These cells never leave a switch. ICC is intended for connection supervision within a switch.

2.8 Network Connectivity Check (LB)

2.8.1 General

The loopback (LB) OAM function is intended for checking the connectivity of a virtual connection by sending a single LB cell along the connection. The LB cell is extracted at well defined points of the network and sent back to the source via the backward connection. Note that each ATM connection has an associated connection in backward direction with the same connection identifiers.

There are three possibilities for specifying the loopback point of an LB cell:

1. End-to-end LB cells: these cells are looped at the endpoint of a connection. For a VCC this is normally the sink terminal, but can also be an AAL device within a network, e.g.

a CES interworking chip like the PXB 4220 IWE8, where the ATM connection ends and the conversion to time slots occurs. For VPCs the endpoint normally is within the ATM network.

2. Segment LB cells: these cells are looped at segment endpoints which are typically at boundaries between network operators. Segment LB cells thus are used to check the connectivity with an operators network. If an operator switches a VPC from one port to another, VP segment LB cells are used for connectivity check, if a VCC is switched VC segment LB cells will be used.
3. The third option for LB cells are intra-network LB cells. These are used on F4 and F5 level to check the connectivity within an operators network from node to node. These cells carry the 16-octet location identifier and the 16-octet source identifier. In forward direction the location ID is compared with the port identifier programmed into the PXB 4340 AOP devices. In backward direction the source identifier is compared with the port ID. Forward and backward direction LB cells are distinguished by the LB indication bit (LSB of LB indication octet).

2.8.2 LB Support

The PXB 4340 AOP supports LB in two ways:

- Cell insertion and extraction buffers
- Detection and loop of LB cells at loopback point with inversion of LB indication bit
- Setting of consistency flag at loopback point
- Detection and extraction of LB cells back at the originating point.

Cell insertion and extraction functions are described in **section 2.15.1**.

Loop of LB cells with reset of the LB indication bit in the cell is done without microprocessor interaction at the respective segment or connection end points. The VPC consistency flag indicates the availability of the VPC to the microprocessor at the loopback port.

Note that the automatic loop function assumes identical connection identifiers for both forward and backward connections.

2.9 Connection Quality Measurement (PM)

2.9.1 General

The PM function is split into three different parts:

- PM generation
- PM analysis and loop
- PM data collection.

PM generation and analysis use the same PM processor circuits in the PXB 4340 AOP. In total 128 PM processor circuits are shared by up- and downstream direction. For PM data collection 128 circuits are provided, which are independent of the PM processor circuits. Both PM and data collection processors have their respective entries in the internal PM/data collection RAMs.

The assignment of PM and data collection processors to connections of up- or downstream direction is arbitrary. VPCs and VCCs can be assigned by programming pointers in the F4 and F5 entries, respectively (**see figure 12**).

2.9.2 Example

A typical PM scenario is shown in **figure 15** for the case of VP end-to-end monitoring. Two nodes are involved, Node a where the VPC_{a-b} is originated and Node b where VPC_{a-b} is terminated. In backward direction the associated VPC_{b-a} is originated in Node b and terminated in Node a. Origination of a VPC is always at an outgoing port of a node and termination at an incoming port. Hence the Originating End Point OEP of VPC_{a-b} is located in the downstream part of the PXB 4340 AOP in Node a, and the Terminating End Point TEP of VPC_{a-b} is located in the upstream part of the PXB 4340 AOP in Node b. For VPC_{b-a} the situation is mirrored according to **figure 15**.

Note that between Nodes a and b a number of intermediate nodes can be located. All PXB 4340 AOP chips on these nodes must be configured either as Originating or Terminating Segment Points (OSP, TSP) or as Intermediate Points (IP).

One of the 128 PM processors in the PXB 4340 AOP upstream part of Node a is configured in generate mode, i.e. it monitors all user cells of VPC_{a-b}, computes PM data and inserts it after blocks of user cells into the cell stream as Forward Monitoring (FM) cells.

At the terminating PXB 4340 AOP one of the 128 PM processors is configured in analyze mode, i.e. it monitors all user cells of VPC_{a-b}, computes PM data and compares it with the PM data contained in the FM cells. The FM cells are extracted from the cell stream, converted into Backward Reporting (BR) cells and re-inserted in backward direction in VPC_{b-a}. The conversion into BR cells includes the calculation of the differences between measured PM data and the PM data contained in the FM cells. The differences are written into the BR cells.

Back at the originating Node a, the BR cells are discarded after evaluation.

Note that the re-insertion of BR cells in backward direction assumes the same identifier (LCI) of the backward direction connection.

2.9.3 PM Data Collection

Independent on the FM/BR cell mechanism is the data collection procedure. It uses one of the 128 data collection processors contained in the PXB 4340 AOP. Each of them can evaluate the BR data flow from upstream or downstream direction. Data collection can be done at any node along the way of the BR cells. In the example of **figure 15** Nodes a or b could be selected for data collection. The PXB 4340 AOP uses either the BR cells incoming from the UTOPIA interface or the locally looped BR cells for data collection.

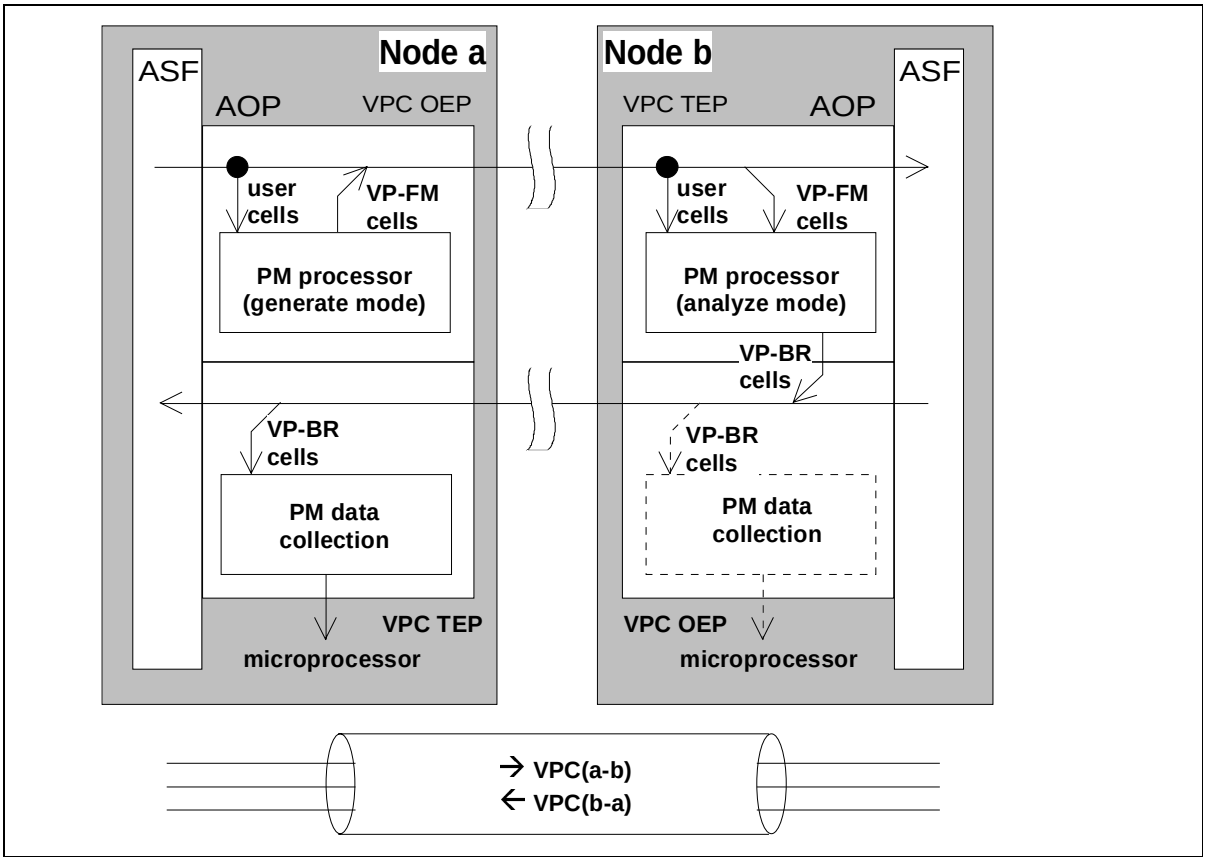


Figure 15: PM Configuration Example

2.9.4 Simultaneous PM flows

The PXB 4340 AOP contains 128 PM processors which may be used to generate a FM flow or to terminate a FM flow. Terminating a FM flow means analyzing and loop of the FM cells as BR cells. During one cell cycle two PM processors can be executed, one on F4 and one on F5 level.

It may happen that a user cell belongs to a VCC for which F5 segment PM is done. E.g. in the example of **figure 15** Node b could be a VCC Originating Segment Point (OSP) in addition to the VPC TEP. Then the arrival of a VCC user cell triggers two PM processors in the upstream part of the PXB 4340 AOP.

In the case of F4 and F5 segments e.g. the downstream part of a PXB 4340 AOP could be configured as VPC OSP and VCC OSP (**refer to table 3**). In this case a user cell not only triggers two PM processors simultaneously, but might also complete two PM blocks. Then two FM cells have to be generated simultaneously. In this case the PXB 4340 AOP first inserts the VP-FM cell and then the VC-FM cell.

2.9.5 Adjacent PM Segments

The arbitrary assignment of PM processors to connections also allows e.g. to terminate a Segment PM flow and generate a new Segment PM flow for the same connection within one PXB 4340 AOP as shown in **figure 16**.

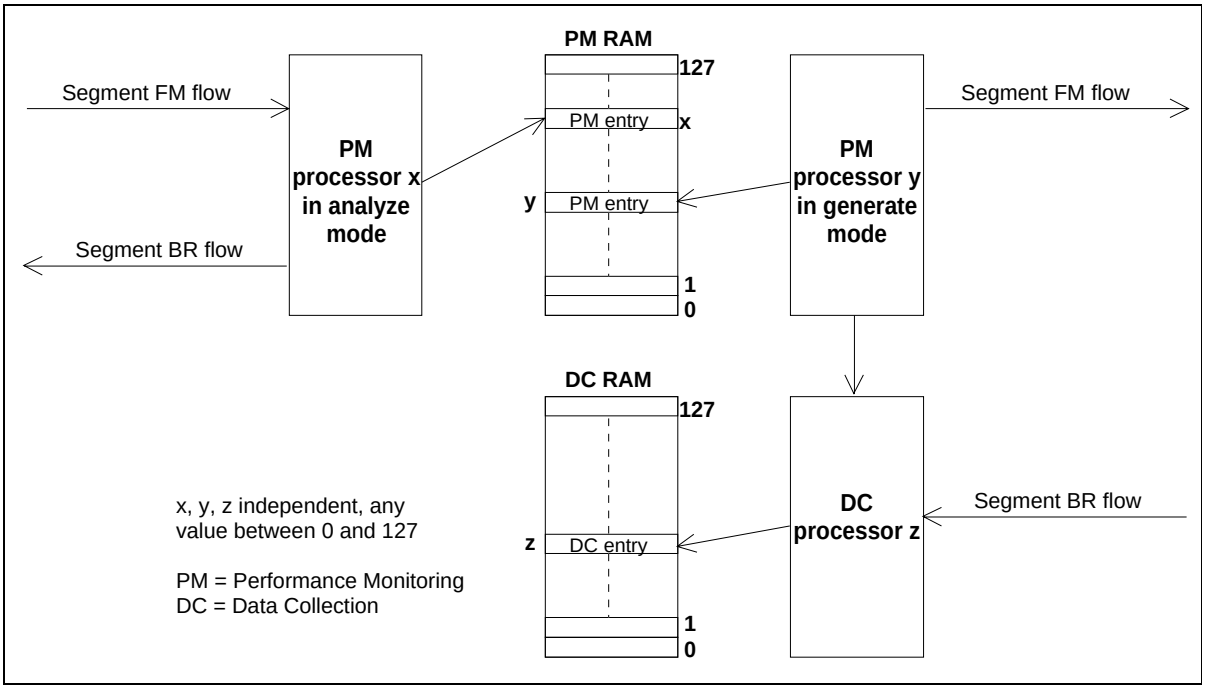


Figure 16: Example for adjacent PM Segments

2.10 Activation and Deactivation Cells

These cell types are generated by the microprocessor and transmitted via the cell insertion function (**section 2.15.1**) of the PXB 4340 AOP.

The detection and extraction of activation/deactivation cells is done automatically at the respective segment or end-to-end points if the PXB 4340 AOP is configured correctly and the function is enabled (which is possible per connection). Extracted cells are stored in the receive buffer (**section 2.15.1**).

2.11 Interactions between OAM Functions

The PXB 4340 AOP does failure propagation automatically, e.g. a received VP-AIS cell automatically leads to the generation of VC-AIS and VP-RDI cells at the VP endpoint. Also the generation of AIS/RDI as a consequence of LOC state is done automatically. Failure propagation from degraded performance, detected with the PM function, to AIS/RDI insertion, however is not done automatically, but must be initiated by the microprocessor.

To enforce VP-level AIS/RDI insertion command bits are available per connection. If enabled the PXB 4340 AOP automatically inserts VC-AIS cells for all VCCs of a VPC.

2.12 Cell Filters

The PXB 4340 AOP provides two types of cell filters:

- filters for special OAM cells
- filters for general purpose ATM cells

For both filter types two filters are provided.

2.12.1 Special OAM Cell Filters

For these filters only the first payload byte of the desired OAM cell (OAM type and function type field) has to be programmed. The other criteria of OAM cells, VCI or PT coding are hard-wired in the chip. All OAM cells, F4 and F5, segment and end-to-end are detected. The filters are working for up- and downstream direction. For each filter the action upon the detection of an OAM cell of the programmed type can be programmed:

- ignore cell (default)
- discard cell
- extract to receive buffer
- copy to receive buffer and forward.

Applications for this filter function are e.g. proprietary OAM functions using the standardized System OAM cell coding or the treatment of future OAM cell types.

2.12.2 General purpose Cell Filters

These filters consist of 3 programmable words for the comparison of all 5 cell header bytes plus the first payload byte. The UTOPIA cell format described in **section 4.1** is compared. Each bit can be individually masked with the mask pattern defined in 3 programmable mask registers. A masked bit matches always when the pattern is compared to the ATM cells. Cells from both up- and downstream direction are compared. Upon match the following actions can be selected:

- ignore cell (default)
- discard cell
- extract to receive buffer
- copy to receive buffer and forward.

See **section 2.15.1** for the receive buffer description.

In addition to the these actions the match signals of both comparators and for up- and downstream direction are output at four pins as a short pulse. The pulses can be further processed by external logic. This feature could be used for measurements.

Other applications for the general purpose cell filters are e.g. communication channels within a switch or the filtering of RM cells.

2.13 Microprocessor Control

A 16-bit microprocessor interface for embedded controllers like e.g. the 386EX is provided for configuration and operation of the PXB 4340 AOP. 8 address lines allow to address 172 registers (non-contiguous addresses). Interrupts are provided for the notification of unexpected events. DMA support is provided for fast data transfer to and from the external RAMs.

2.14 Access to internal and external RAMs

The microprocessor can not access these RAMs directly, but uses a transfer register set. It consists of three blocks:

- read register block
- write register block
- mask register block.

In addition an address register specifying the entry to be accessed and a command register to specify the RAM and to start the transfer are defined. The PXB 4340 AOP uses one single access type, the read-modify-write transfer, where the old data is transferred from the specified RAM entry to the Read Transfer Registers and the contents of the Write Transfer Registers are written to the RAM entry for those bits which are unmasked.

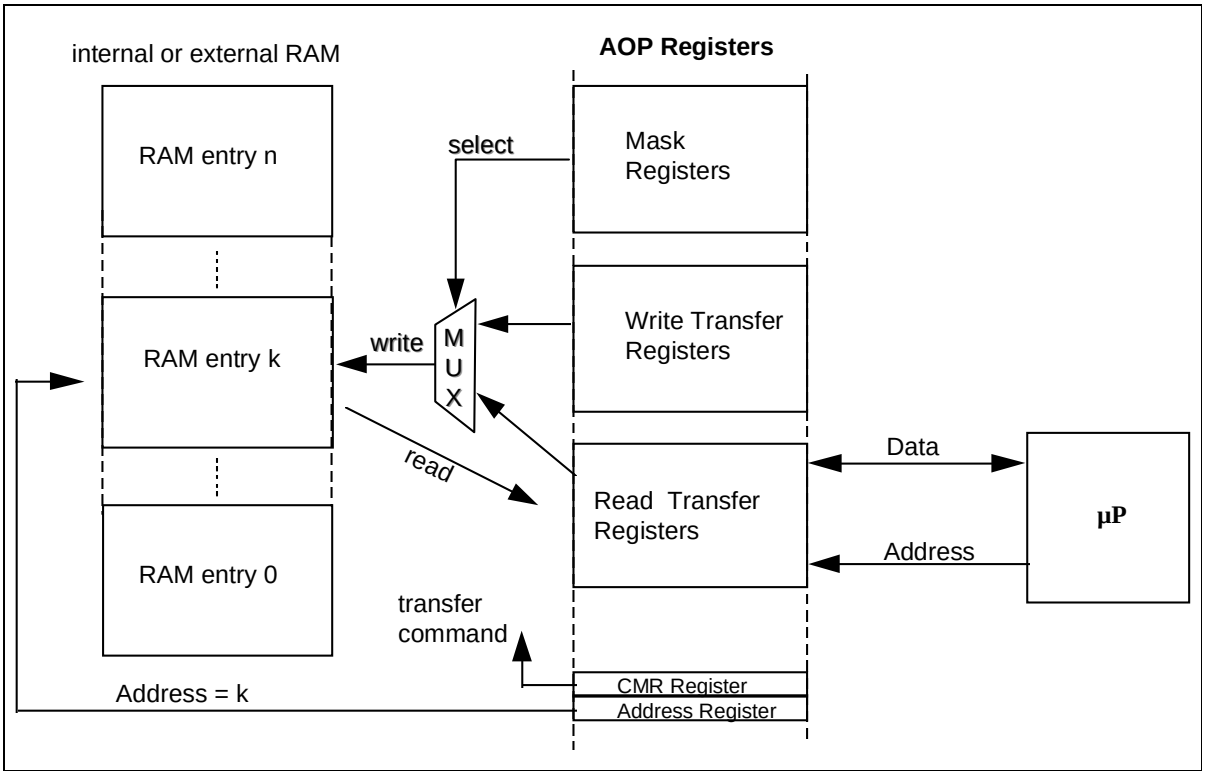


Figure 17: Access to internal or external RAMs

In addition to the read-modify-write access executed upon microprocessor command for a single entry, there are two other access types to the external RAM:

- the access initiated by the passing ATM cell
- the scan access with or without DMA.

2.15 Scan Mechanism with optional DMA

This mechanism has to be triggered by the microprocessor. It is recommended to trigger it in a 500 ms time frame, as all time-out values are determined based on this time interval. During a scan all entries of the external RAMs are accessed sequentially using the read-modify-write access described in **section 2.14**. The scan is programmed in such a way that it covers in a little less than 500 ms all used RAM entries.

In each scan access counters for time-out values are updated and the necessary actions taken (e.g. after 3.5 s transition from defect to failure state). Additionally together with the scan a specified part of the RAM entries can be transferred via DMA to the microprocessor main memory. Also if desired write and mask register blocks can be used to clear part of the bits of each entry. This last feature is used in the compressed DMA mode:

In compressed DMA mode 32 pre-defined bits are transferred from each entry in up- and downstream external RAM. These bits contain the condensed status information from the respective connection. Also the status transition bits are available. These must be reset with each scan, which is achieved with appropriate settings of write and mask register blocks.

For the DMA a 16 dword fifo is provided on-chip. The DMA request pin of the PXB 4340 AOP is asserted when the fifo is occupied and deasserted when it is empty.

2.15.1 Receive and Transmit Buffer

The PXB 4340 AOP provides a 12-cell receive buffer and a 1-cell transmit buffer. They are used for insertion and extraction of LB cells, activation and deactivation cells and special cells defined with the cell filters (**see section 2.12**).

The buffers are realized differently. The transmit buffer consists of 27 words, directly addressable by the microprocessor for read and write. When the cell is assembled it can be inserted by setting a command bit. The command bit is reset after complete insertion of the cell into the data stream. The insertion direction, up- or downstream can be selected and also if the CRC-10 should be computed automatically by the chip or not.

The receive buffer is realized as fifo with word-wise access via a single register. A cell is read with 27 consecutive read accesses to this register. Reception of a cell is signalled to the microprocessor via an interrupt bit. The interrupt bit is reset by the chip automatically after the last read access if no more cell is in the buffer. The receive buffer collects cells from up- and downstream direction, they are distinguished with a bit in the UDF2 octet. Cell format for both receive and transmit buffer is the 16-bit UTOPIA format as described in **section 4.1**.

3 Operation

This section describes the actions to be done by the microprocessor. For this purpose the following network scenario is assumed (see also **figures 8, 9 and 10** for reference):

- The OAM functions AIS/RDI/CC are always enabled for all connections (although the PXB 4340 AOP also supports enabling on a per-connection basis). Activating the CC function by default avoids use of CC activation/deactivation cells.
- For all timeout values the recommended values of the standard [**6**] are used.
- Performance monitoring is always initiated by the generating port (**see figure 15**) using PM activation cells. The respective endpoint loops a cell with 'activation request confirmed' back if a PM processor is available. If all 128 PM processors are in use the 'activation request denied' cell is sent back. The deactivation cell is always confirmed.
- PM data collection is always done on the port where the FM cells are generated, i.e. the BR cells are evaluated and discarded there (the PXB 4340 AOP supports PM data collection on any point along the backward PM cell path).
- Segment borders are fixed to transmission lines (although the PXB 4340 AOP supports the per-connection definition of segment points).
- At originating segment points AIS/RDI monitoring for VPCs is enabled, i.e. at the entrance of the network of an operator it is detected if a VPC is received fault-free or not. The availability of the VPCs is also checked at the terminating segment points with AIS/RDI monitoring. So the network operator knows at any time the availability of his VPCs. Monitoring is not activated for VCCs, as these are set-up only temporary.

All these assumptions facilitate OAM management by reducing the number of parameters to be handled.

3.1 Initialization and Test

These are the actions to be performed after reset to prepare the PXB 4340 AOP for operation.

- Check reset values of all registers
- Set HW configuration (RAM type, UTOPIA configuration)
- Initialize internal and external RAMs
  For this purpose the DMA feature of the chip could be used.
- Test parity detectors
- Check data path (via adjacent ATM devices)

3.2 Configuration

The following parameters must be known by the microprocessor for the operation of the PXB 4340 AOP:

- Number of PHYs
- Edge-of-the-network or intra-network point for each PHY
- Switch Port ID for intra-network Loopback
- Number of supported connections

- Thresholds for PM data collection values
- Use of internal CC function or not.

3.3 Setup/ Cleardown of Connections

For a connection setup the following parameters are required:

- Local connection identifier LCI
- VPC or VCC
- If VCC the LCI2 value of the associated VP-entry (VP-pointer)
- VCC endpoint indication (at AAL function)
- PHY number

All further programming is done using the edge-of-the-network or intra-network configuration of the PHY (for the abbreviations see **table 3**):

- In case of a VCC the upstream part of the PXB 4340 AOP is configured as VP-TEP and the downstream part as VP-OEP. If in addition the PHY is configured as edge of a network the upstream part is configured as VC-OSP and the downstream part as VC-TSP.
- In case of a VPC without a segment border both up- and downstream parts are configured as intermediate point (VP-IP). If the PHY is configured as edge of the network the upstream part is configured as VP-OSP and the downstream part as VP-TSP.

Note: If a PHY is at the edge of a network its transmission line is connected to the network of another operator. Hence all segment streams are terminated before the ATM cells leave the node (non-overlapping mode).

- At OEPs the CC flow generation is enabled (VPC or VCC, segment or end-to-end).

3.4 Enable/ Disable of PM

This command is issued by the microprocessor either on request from the system controller or in the course of a activation/deactivation cell received for this connection. The following parameters are needed:

- LCI of the connection or LCI2 of the VP-pointer
- Block size 128, 256, 512 or 1024
- Mode select:
  1) generate and collect data or
  2) analyze and loop.

3.5 Normal Operation

3.5.1 Scan Process Trigger

In fault free state the main task of the microprocessor is to trigger the scan function in 500 ms intervals. This is done by setting one single bit in a register. An internal logic checks all entries of both up- and downstream external RAMs. According to the actual

state of the connection (AIS state, PHY failure, CC state etc.) and the programmed time-out values the respective state transitions are performed. In addition an interrupt bit is set if any state transition occurred. The microprocessor informs the network management upper layer SW about transitions from defect to failures and transitions back to fault-free state. According to the standards transitions to defect states are not reported.

It is recommended to activate the compressed DMA function with the scan, which transfers the status dword of all connections from both up- and downstream external RAM to the microprocessor memory. The status dword contains:

- VP/VC AIS/RDI/LOC defect/failure state
- transition events between these states and fault-free state
- error indication bits
- direction bit

It is also recommended to program the scan in a way that the transition event bits are cleared after read with the same scan/DMA process (**see figure 17**).

Scan and DMA completion is indicated by flags. With one 32-bit dword transferred per connection and per direction, in total up to 32 K dwords have been transferred to the micrprocessor memory.

3.5.2 PM Threshold Check

Also in normal operation the local controller checks all data collection entries, compares the values with the given thresholds and if these are exceeded

- Activate AIS/RDI insertion
- Inform network management

Optionally records of the e.g. last 15 minutes could be collected.

3.6 Events

Events are unpredictable for the peripheral controller. These may be interrupts from the HW or command messages received from the system controller (**see figure 6**).

3.6.1 Transmission Line Failure

Such failures are e.g. line breaks or transmitter/receiver failure. They are detected by the PHY device and usually signalled to the local controller by interrupt. If the failure is confirmed the local controller

- sets the corresponding PHY error bit in a PXB 4340 AOP register

to signal the failure to the ATM layer. All ensuing actions as generation of VP-AIS or VC-AIS cells in forward direction as well as the insertion of VP-RDI or VC-RDI cells in backward direction are done automatically by the scan mechanism.

3.6.2 LB Cell Transmission/ Reception

The transmission of a LB cell is usually initiated by the system controller. The parameters

- LCI
- segment or end-to-end or intra-domain LB
- the Location identifier in case of intra-domain LB

must be given by the system controller. Note that in case of a segment or end-to-end LB the location and source ID are set to all ones. The microprocessor assembles the LB cell and transmits it via the PXB 4340 AOP. A timer is started for timeout supervision.

Prior to transmission the LB State bit is set for this connection. This bit causes the returning LB cell to be copied to the receive buffer. If it is not set the backward LB cell is discarded without notice. By comparing the correlation tag the peripheral controller makes sure that the cell was the one sent out before.

Note: The correlation tag is not generated by the PXB 4340 AOP. It is recommended to generate a random number by the peripheral controller.

3.6.3 PM Activation/ Deactivation Cell Transmission

The request to do performance monitoring over a given VPC or VCC connection or segment is initiated by the system controller and sent to the originating point microprocessor. The parameters

- LCI or LCI2 (for F4 PM)
- Block size (128, 256, 512, 1024)

must be given. Similar to the LB procedure the microprocessor generates an appropriate activation cell for either segment or end-to-end, depending on the given configuration. After reception of the confirmation cell (**section 2.10**) the FM generation processor is assigned as well as a data collection processor in the opposite direction. There are two restrictions to be checked:

- there are at most 128 processors for FM generation or analysis and 128 processors for data collection
- not more than 2 processors can be invoked for one user cell, one for F4 and one for F5 (**section 2.9**).

3.6.4 PM Activation/ Deactivation Cell Reception

An activation/ deactivation cell may be received at any time at the receive buffer of the PXB 4340 AOP. In such a case the peripheral controller looks for a free PM processor and assigns it to the connection. The PM processor is initialized in analyzing mode. Then a confirmation cell is sent back to the originating port. The PM endpoint is now ready for reception of the first FM cell.

4 Interfaces

4.1 UTOPIA Interfaces

The PXB 4340 AOP has one UTOPIA receive interface and one UTOPIA transmit interface with master capability at the PHY side and one receive and transmit interface with slave capability at the ATM side (**figure 18**). The interfaces are compliant to the UTOPIA Level 1 and 2 specification [**1, 2**], i.e.:

- bus width is selectable either 8 or 16 bit
- frequency 19... 52 MHz
- support of single-PHY or multi-PHY configurations
- support of direct status polling option of UTOPIA Level 2 specification

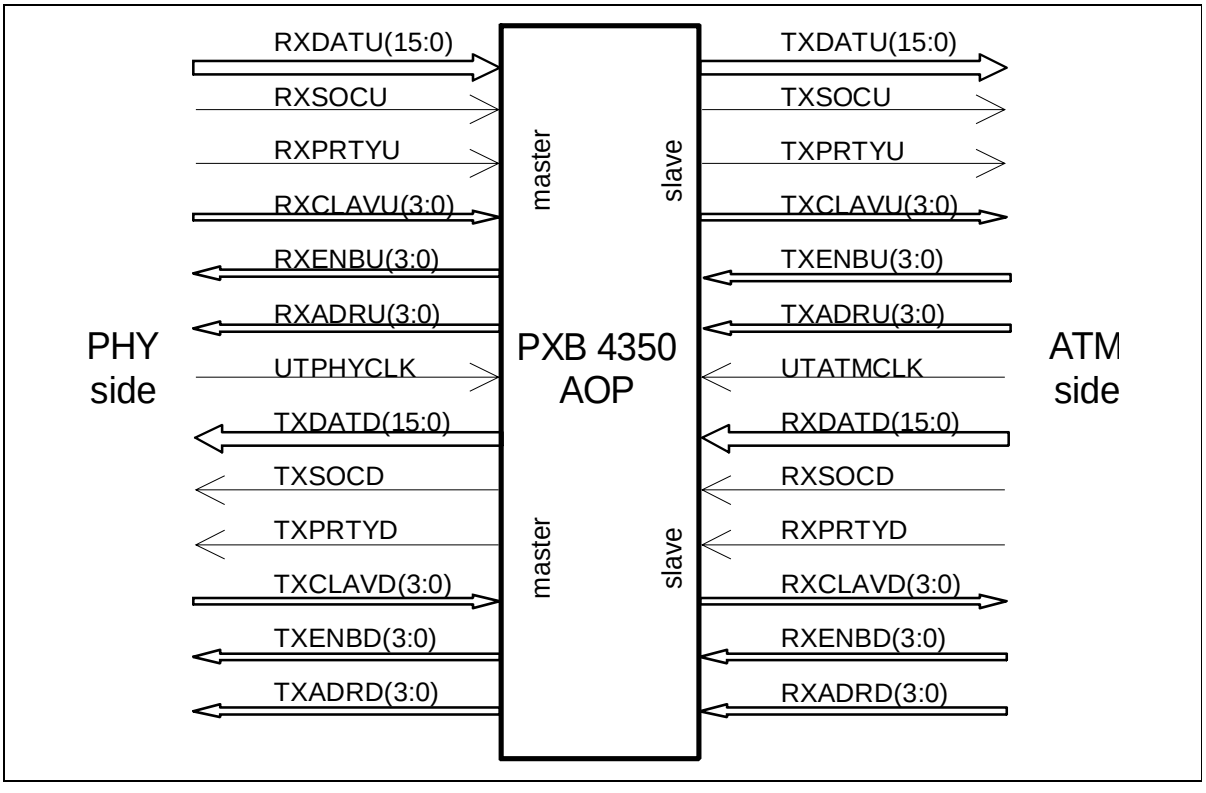


Figure 18: UTOPIA Interfaces

Receive and transmit side of ATM and PHY side UTOPIA interface operate each from one clock which may be completely independent from the main chip clock SYSCLK. The UTOPIA clock frequency must be less than or equal to the main chip clock SYSCLK.

The UTOPIA interface has a 8-bit and a 16-bit option. The 16-bit option has the 54 octet cell format shown in **figure 19** for the standardized format and in **figure 20** for the proprietary format. The 8-bit format has 53 octet without the UDF2 octet. ATM side and PHY side UTOPIA interface can be configured independently in 8-bit or 16-bit mode.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	UDF1								UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Figure 19: Standardized UTOPIA cell format (16-bit)
all fields according to standards, unused octets shaded

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	LCI(13:12)		HK(2:0)			PN(2:0)			UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
:	:								:							
26	Payload Octet 47								Payload Octet 48							
word																

Figure 20: Proprietary UTOPIA cell format (16-bit)

- with PN(2:0) = port number for PXB 4220 IWE8 (don't care for PXB 4340 AOP)
  HK(2:0) = housekeeping bits (only for Internal Continuity Check ICC)
  LCI(13:0) = Logical Channel Indicator
  all other fields according to standards, unused octets shaded.

4.1.1 UTOPIA Multi-PHY support

To support multi-PHY configurations with and without use of the UTOPIA PHY address the Siemens ATM switching chip set supports the Direct Status Polling option of the UTOPIA Level 2 standard [**2**]. It allows the simultaneous polling of up to 4 groups of PHYs by using 4 CLAVx/$\overline{\text{ENx}}$ signal pairs (x=0..3).

During the transfer of a cell the master UTOPIA interface polls 12 PHY addresses. The 27 clock cycles time for the transfer of a cell in 16-bit UTOPIA format allows to poll 12 PHY addresses and to select one of them for the next cell transfer. Receive and transmit UTOPIA interfaces always poll separately. To allow the support of more than 12 PHYs 4 pairs of CLAVx/$\overline{\text{ENx}}$ lines are provided in all Siemens ATM switching chips with UTOPIA

interfaces. However, although 48 PHYs could be polled by this configuration only up to 24 PHY are supported.

Note: the number of line interfaces (PHYs) to be supported by an ATM layer chip is depending basically on the number of its queues. The term 'PHY device', however, denotes 'PHY chips', which may contain more than one PHY. For electrical load considerations the number of PHY devices is important, as the standard requires that for 25 MHz clock minimum 8 PHY devices must be driven, for 50 MHz minimum 4 PHY devices.

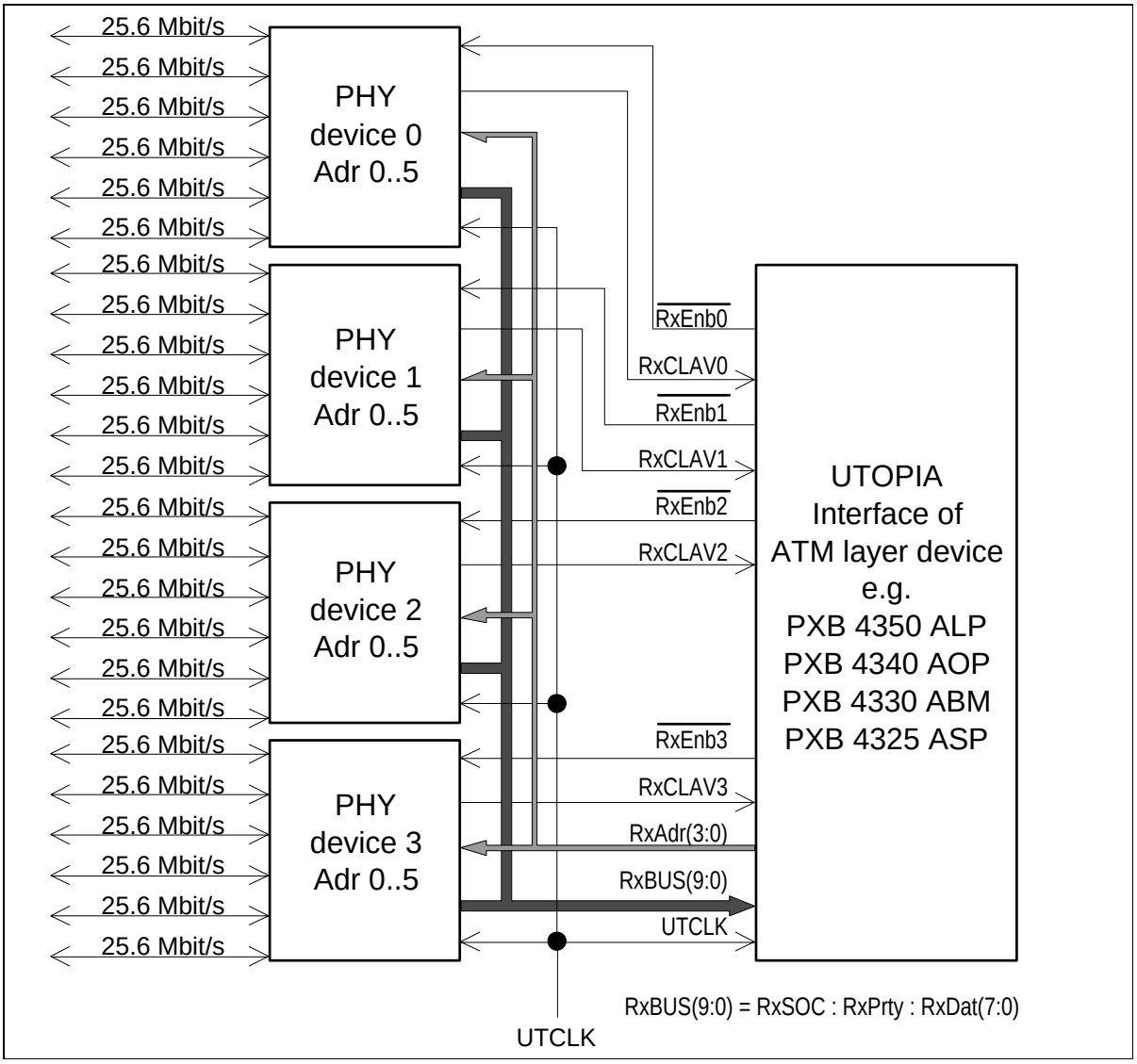


Figure 21: Upstream receive UTOPIA example for 4 x 6 PHYs

The 4 CLAVx/$\overline{\text{ENx}}$ lines are connected one-to-one to different PHY devices, as shown e.g. in the example of **figure 21** for the upstream receive side of an ATM layer chip con-

nected to 4 PHY devices, each containing 6 PHYs of 25.6 Mbit/s. In this example the maximum number of 24 PHYs is connected.

In the example of **figure 21** the PXB 4340 AOP gets 4 CLAVx signals with each polled address. All PHY devices have the addresses 0..5 assigned to their PHYs. The upper 6 addresses always deliver CLAVx=0 when polled. In order to distinguish the PHYs the UTOPIA interface of the PXB 4340 AOP adds offset numbers 6, 12 and 18 to the PHY numbers from PHY device 1, 2 and 3, respectively. Then within the ATM layer device the PHY numbers range from 0..23 without ambiguity.

Two other multi-PHY modes with UTOPIA addresses are selectable. One additional mode is provided, for connecting Level 1 PHY chips without address inputs. All modes are summarized in **table 1**.

Table 1: UTOPIA polling modes.
The numbers indicate the offset which is added to the PHY number.

	Mode 2 x 12	Mode 3 x 8	Mode 4 x 6	Level 1 Mode
$\overline{EN0}$ / CLAV0	0	0	0	0
$\overline{EN1}$ / CLAV1	12	8	6	0
$\overline{EN2}$ / CLAV2	do not connect	16	12	0
$\overline{EN3}$ / CLAV3	do not connect	do not connect	18	0

- In Level 1 mode the PHY numbers are identical to the CLAV/$\overline{EN}$ group: 0, 1, 2, 3.
- It is the users responsibility to program the PHY numbers in a way that ambiguous PHY numbers inside the ATM layer device are avoided.
- The mode selection can be done independently for the PHY side and the ATM side UTOPIA interface.
- If less or equal than 12 PHYs are to be polled, mode 2 x 12 should be used with only the CLAV0/$\overline{EN0}$ pair connected. This minimizes the interconnection lines between the chips.

Examples:

1. One PHY device, e.g. a 622 Mbit/s PHY: 16-bit bus width, address lines unconnected, RxCLAV0/$\overline{RxEN0}$ and TxCLAV0/$\overline{TxEN0}$ signal pairs connected, all other CLAVx/$\overline{ENx}$ pairs unconnected.
2. 4 PHY devices 155.52 Mbit/s PHYs: 16-bit bus width, address lines unconnected, all 4 CLAVx/$\overline{ENx}$ pairs connected, one to each PHY device
3. 4 PHY devices of 6-fold 25.6 Mbit/s PHYs: 16-bit bus width, address and all 4 CLAVx/$\overline{ENx}$ pairs connected, one to each PHY device (**see figure 21**)
4. 4 PXB 4220 IWE8s: 8-bit bus width, address bus unconnected, all 4 CLAVx/$\overline{ENx}$ pairs connected, one to each IWE8 (this mode requires the PXB 4350 ALP).

4.2 RAM Interfaces

The PXB 4340 AOP uses external, synchronous, static RAM (SSRAM) for the storage of connection related OAM data. Two identical SSRAM interfaces are provided, one for each direction. The SSRAM chips are operated with the system clock of up to 52 MHz.

All memory entries are protected with a parity bit at the MSB location.

Size of the SSRAM is depending on the number of supported connection: 8 dwords of 32-bit are required per connection. Using SSRAM devices of 1 M or 2 M size, i.e. 32 K x 32 bit and 64 K x 32 bit, respectively, the possible memory configurations are:

- 2 x 2 Mbit or 4 x 1 Mbit SSRAM for 16384 conections
- 1 x 2 Mbit or 2 x 1 Mbit SSRAM for 8192 connections
- 1 x 1 Mbit SSRAM for 4096 connections

These figures are per direction. Both up- and downstream external memory should always be configured symmetrical. The selection 1 Mbit or 2 Mbit SSRAM chips is done via register bits. **Figure 22** shows an example of maximum RAM size with 1 Mbit devices.

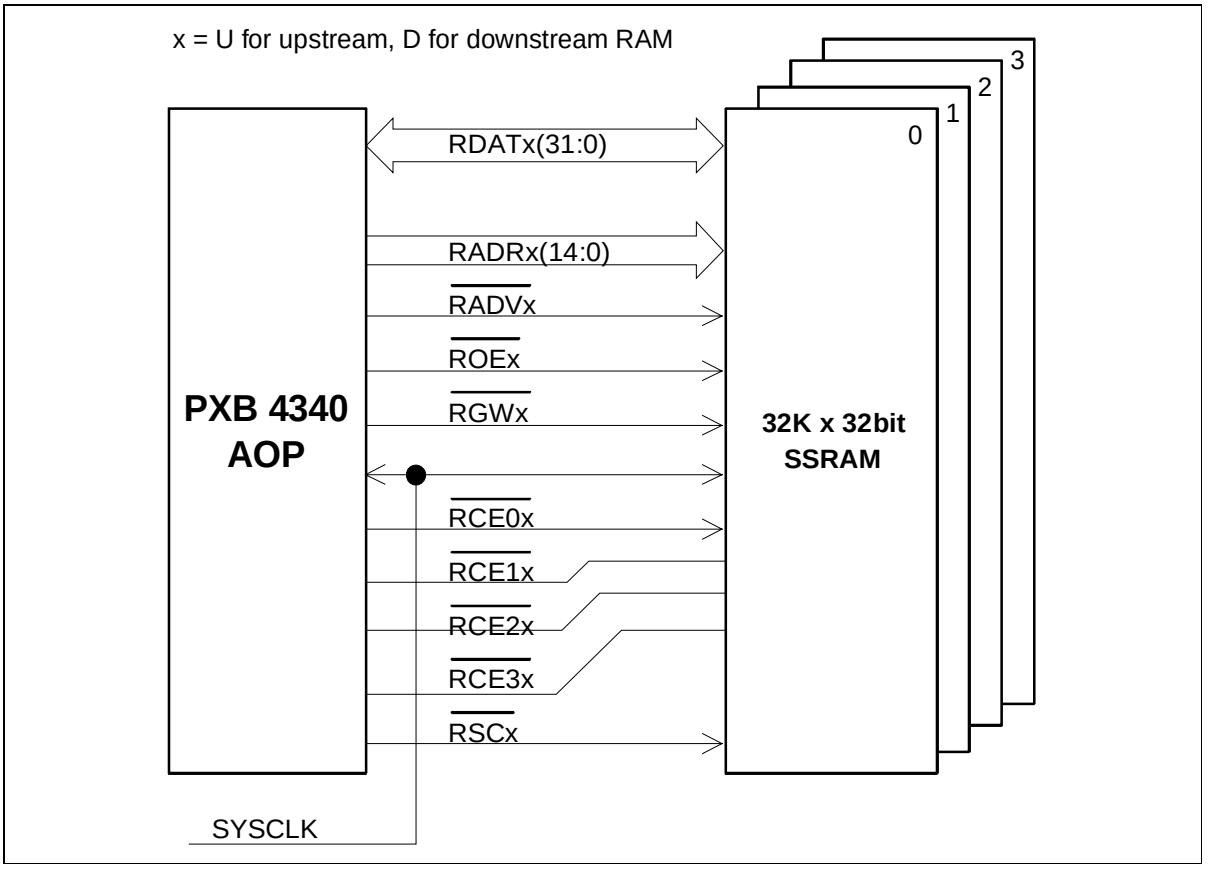


Figure 22: Upstream or downstream RAM Interface using 1 Mbit RAMs

Timing of the synchronous RAM interfaces is simplified, as all signals are referenced to the rising edge of SYSCLK. In **figure 23** it can be seen that all signals output by the PXB 4340 AOP have identical delay times with reference to the clock. Due to concurrent propagation delays the signals may be slightly before (T+) or after (T-) the rising edge. This is also true for the data when writing to the RAM. When reading from the RAM the PXB 4340 samples the data after the access time within the window to the data hold time of the next riding clock edge.

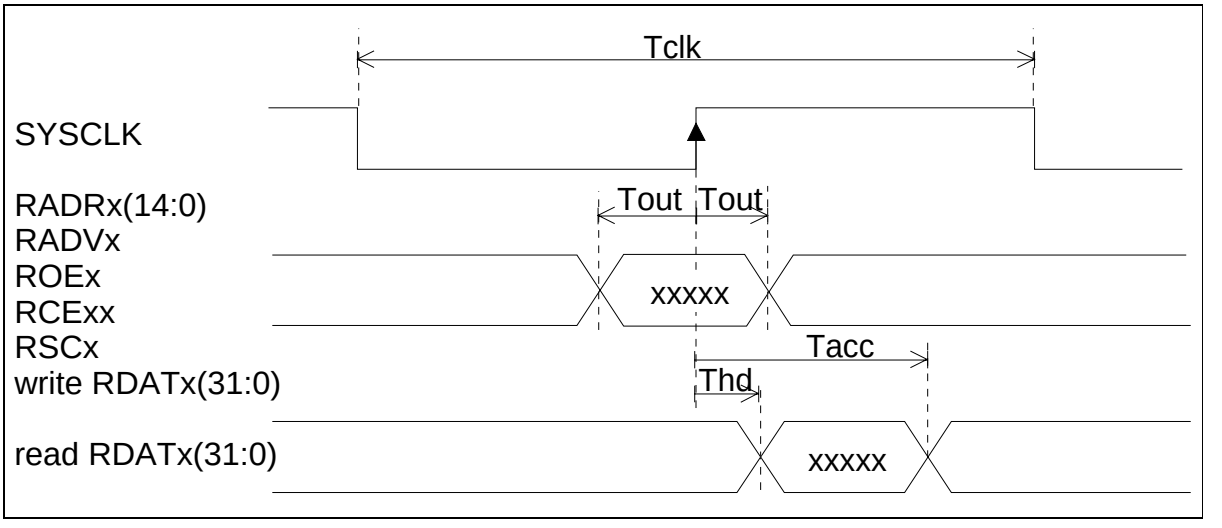


Figure 23: Timing of external RAM

Table 2:

Description	Symbol	Minimum	Maximum
Clock to output signal[1] time	T_{out}	- 2.5 ns	0.5ns
Clock cycle time	T_{clk}	19.2 ns	
Data access time	T_{acc}	8 ns	
Data guaranteed after next clock edge	T_{hd}		2 ns

1) Applies to RADRx(14:0), RADVx, ROEx, RCExx, RSCx, RDATx(31:0) in write access

4.3 Microprocessor Interface

The PXB 4340 AOP has a 16-bit microprocessor interface for control and operation. It is identical for all devices of the Siemens ATM switching chip set (the PXB 4310 ASM uses only a 8-bit data bus). A possible microprocessor could be the 386EX embedded controller as shown in **figure 24**.

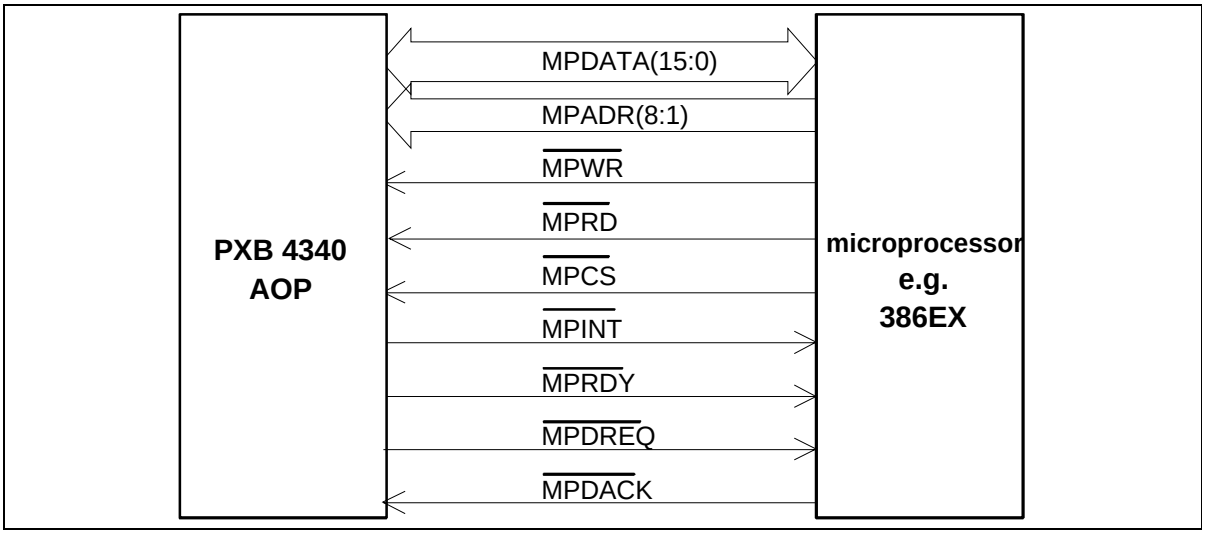


Figure 24: Microprocessor Interface

The interface is operating completely asynchronous to the system clock SysClk.

4.4 JTAG Interface

This interface contains the boundary scan of all signal pins according to the standard [**4**]. It consists of the pins shown in **figure 25**.

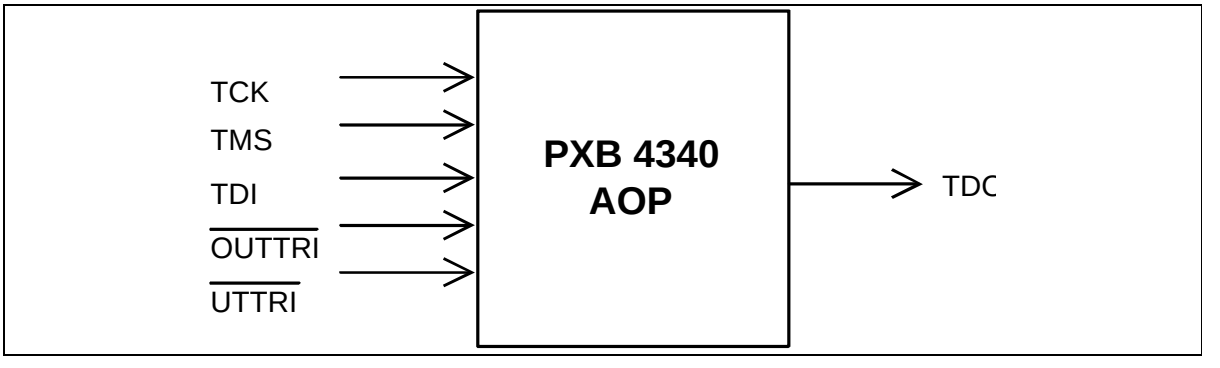


Figure 25: JTAG Interface

In addition to the standard boundary scan pins the pins are provided for board test:

- $\overline{\text{OUTTRI}}$: if this pin is low all other signal pins of the device are put into high impedance mode
- $\overline{\text{UTTRI}}$: if this pin is low all pins of both UTOPIA interfaces are put into high impedance mode.

4.5 Clock Supply

The PXB 4340 AOP's core is operated with a main chip clock SYSCLK, which has a frequency between 25 and 51.84 MHz as shown in **figure 26**. The two UTOPIA interfaces

have different clocks, one for the PHY side interface (**towards the ALP in figure 26**) and one for the ATM side interface (**towards ABM/ASP in figure 26**). Both UTOPIA clocks may be independent (asynchronous) on each other and also asynchronous the System Clock. The only restriction is that their frequency be less or equal than the System Clock. Otherwise the UTOPIA handshake might not work properly.

A further asynchronous interface is the microprocessor interface. Its speed is limited to less or equal to SYSCLK/2.

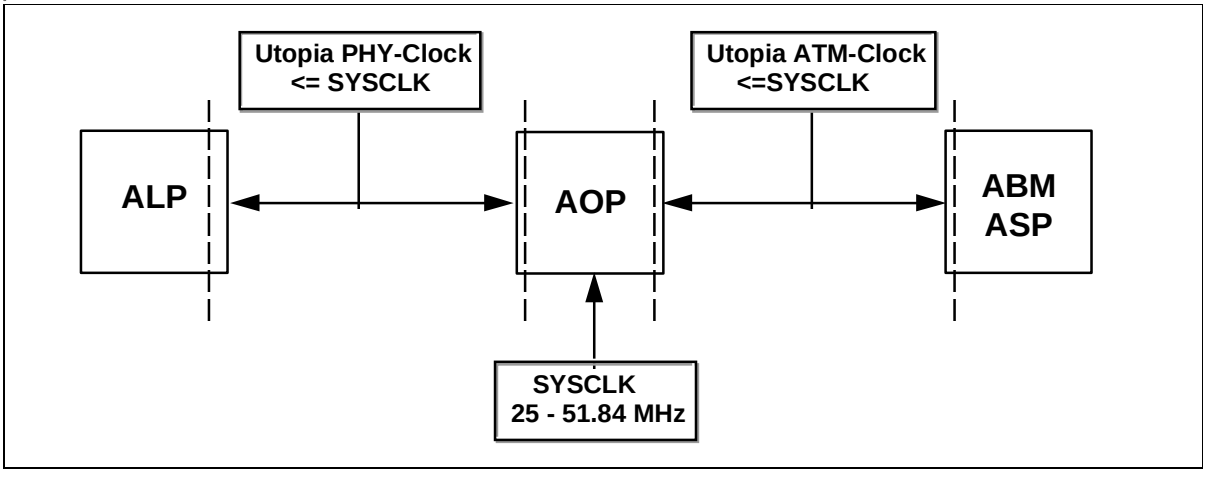


Figure 26: Clock Concept

4.6 Pin Definitions and Functions

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Clock and Reset (4 pins)			
	$\overline{\text{RESET}}$	I	Chip reset
	SYSCLK	I	Main chip clock
	UTPHY-CLK	I	UTOPIA clock at PHY side (master)
	UTATM-CLK	I	UTOPIA clock at ATM side (slave)
Utopia-Interface (receive upstream master)			
	RXDATU (15:0)	I	Receive data bus from PHY side
	RXADRU (3:0)	O	Address outputs to PHY side
	RXPRTYU	I	Odd parity of RXDATU(15:0) from PHY side
	$\overline{\text{RXENBU}}$ (3:0)	O	Enable signal to PHY side
	RXCLAVU (3:0)	I	Cell available signal from PHY side
	RXSOCU	I	Start of cell signal from PHY side
Utopia-Interface (transmit downstream master)			
	TXDATD (15:0)	O	Transmit data bus to PHY side
	TXADRD (3:0)	O	Address to PHY side
	TXPRTYD	O	Odd parity to PHY side
	$\overline{\text{TXENBD}}$ (3:0)	O	Enable signal to PHY side

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
	TXCLAVD (3:0)	I	Cell available signal from PHY side
	TXSOCD	O	Start of cell signal to PHY side
Utopia-Interface (receive downstream slave)			
	RXDATD (15:0)	I	Receive data bus from ATM side
	RXADRD (3:0)	I	Address from ATM side
	RXPRTYD	I	Odd parity of RXDATD(15:0) from ATM side
	$\overline{\text{RXENBD}}$(3:0)	I	Enable signals from ATM side
	RXCLAVD (3:0)	O	Cell available signal to ATM side
	RXSOCD	I	Start of cell signal from ATM side
Utopia-Interface (transmit upstream slave)			
	TXDATU (15:0)	O	Transmit data bus to ATM side
	TXADRU (3:0)	I	Address from ATM side
	TXPRTY	O	Odd parity of RXDATU(15:0) to ATM side
	$\overline{\text{TXENBU}}$ (3:0)	I	Enable signal from ATM side
	TXCLAVU (3:0)	O	Cell available signal to ATM side
	TXSOCU	O	Start of cell signal to ATM side
Microprocessor Interface			
	MPDATA (15:0)	I/O	Microprocessor data bus

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
	MPADR (8:1)	I	Address from microprocessor
	$\overline{\text{MPWR}}$	I	Write enable from microprocessor
	$\overline{\text{MPRD}}$	I	Read enable from microprocessor
	$\overline{\text{MPCS}}$	I	Chip select from microprocessor
	$\overline{\text{MPDACK}}$	I	DMA acknowledge from microprocessor
	$\overline{\text{MPINT}}$	O	Interrupt request to microprocessor
	$\overline{\text{MPDREQ}}$	O	DMA request to microprocessor
	MPRDY	O	Ready output to microprocessor for read and write accesses

Connection Data SSRAM Upstream

	RDATU (31:0)	I/O	Databus of Upstream Connection RAM
	RADRU (14:0)	O	Addressbus of Upstream Connection RAM
	$\overline{\text{RADVU}}$	O	Address Advance Input
	$\overline{\text{ROEU}}$	O	Output Enable
	$\overline{\text{RGWU}}$	O	Global Write
	$\overline{\text{RCE0U}}$	O	Chip Enable RAM 0
	$\overline{\text{RCE1U}}$	O	Chip Enable RAM 1
	$\overline{\text{RCE2U}}$	O	Chip Enable RAM 2
	$\overline{\text{RCE3U}}$	O	Chip Enable RAM 3
	$\overline{\text{RSCU}}$	O	Status Controller RAM

Connection Data SSRAM Downstream

	RDATU (31:0)	I/O	Databus of Downstream Connection RAM
	RADRD (14:0)	O	Address bus of Downstream Connection RAM
	$\overline{\text{RADVD}}$	O	Address Advance Input

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
	$\overline{\text{ROED}}$	O	Output Enable
	$\overline{\text{RGWD}}$	O	Global Write
	$\overline{\text{RCE0D}}$	O	Chip Enable RAM 0
	$\overline{\text{RCE1D}}$	O	Chip Enable RAM 1
	$\overline{\text{RCE2D}}$	O	Chip Enable RAM 2
	$\overline{\text{RCE3D}}$	O	Chip Enable RAM 3
	$\overline{\text{RSCD}}$	O	Status Controller
Detector Interface			
	FPCT1D	O	Detector output 1 downstream
	FPCT2D	O	Detector output 2 downstream
	FPCT1U	O	Detector output 1 upstream
	FPCT2U	O	Detector output 2 upstream
Test/JTAG Boundary Scan			
	TDI	I	Test data input
	TCK	I	Test clock
	TMS	I	Test mode select
	$\overline{\text{TRST}}$	I	TAP Controller Reset
	TDO	O	Test data output
	$\overline{\text{OUTTRI}}$	I	Puts all outputs except TDO into tristate mode
	$\overline{\text{UTTRI}}$	I	Puts all UTOPIA outputs into tristate mode
Additional Testpins			
	STEST	I	For test only, don’t connect
	AOPIIDD	I	Has to be connected to ground
	NDTRO	O	For test only, don’t connect
	TSTBUSI (3:0)	I	Testbus in For test only, don’t connect

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
	TSTBUSO (3:0)	O	Testbus out For test only, don’t connect
Supply			
	VDD		Chip 3.3 V supply
	VSS		Chip ground

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Input voltage	V_{in}	-0.5 to V_{CC} +0.5	V
Input / output current	I	-20 to +20	mA
Continuous output current		-25 to +25	mA
Power dissipation	P	3.5	W

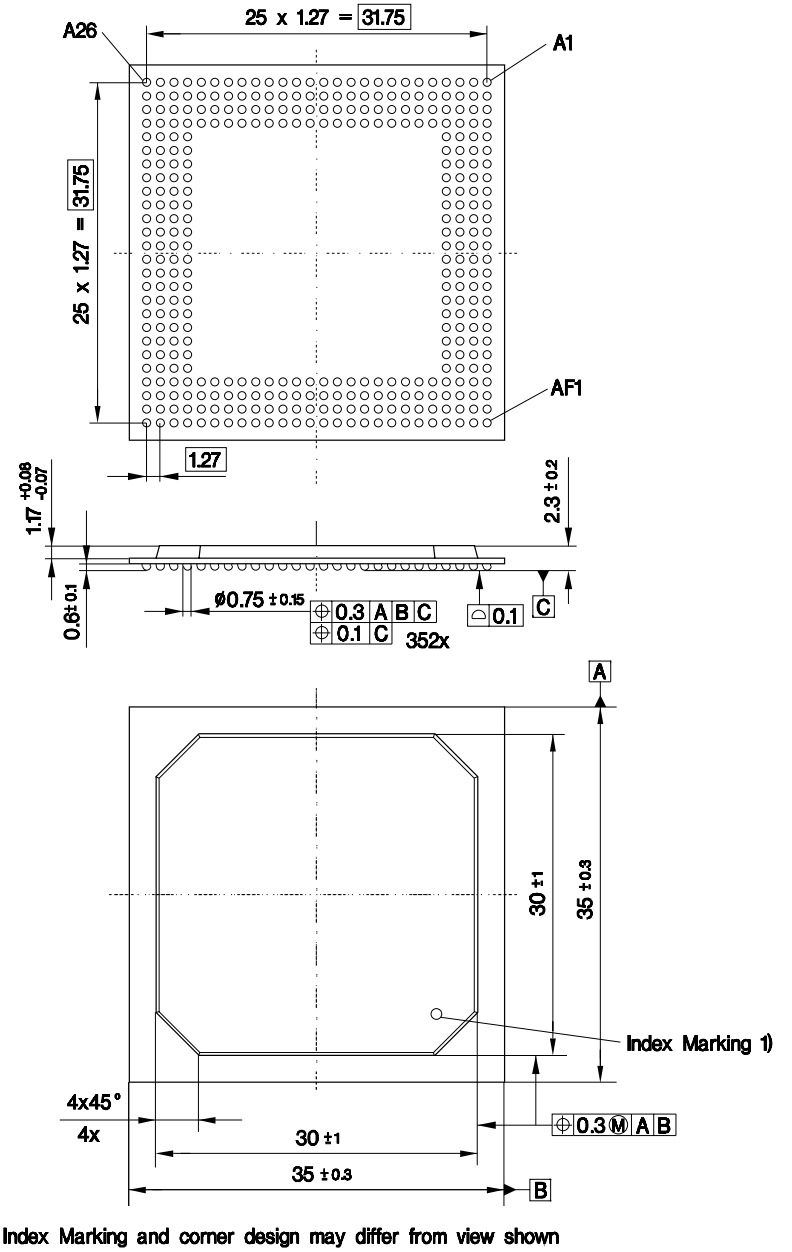
Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Operating Conditions

Parameter	Symbol	Limit Values	Unit
Supply voltage	VCC	3.135 to 3.465	V
Digital ground	GND	0	V
Ambient temperature under bias	TA	0 to 70	°C
Junction temperature	TJ	max. 100	°C

6 Package Outlines

BGA-352
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

7 Overview Lists

7.1 Layer Point Configurations

The following layer points are defined for both F4 and F5 OAM flows:

- OEP = Originating End Point (end-to-end OAM cell flow)
- TEP = Terminating End Point (end-to-end cell flow)
- OSP = Originating Segment Point (segment cell flow)
- TSP = Terminating Segment Point (segment cell flow)
- IP = Intermediate Point (no origination or termination of OAM flows).

The following table gives an overview over all layer points that can be configured in up- and downstream direction of the PXB 4340 AOP:

Table 3: Layer Point Configurations

ATM Layer flow	ATM Layer Point VPC	ATM Layer Point VCC	up	down
F4	VPC IP		yes	yes
F4	VPC TSP		yes	yes
F4	VPC OSP		yes	yes
F4	VPC TSP & VPC OSP		yes	yes
F5		VCC IP	yes	yes
F5		VCC OSP	yes	yes
F5		VCC TSP	yes	yes
F5		VCC OSP & VCC TSP	yes	yes
F4 & F5*	VPC TEP	VCC IP	yes	no
F4 & F5*	VPC TEP	VCC OSP	yes	no
F4 & F5*	VPC TEP	VCC TSP	yes	no
F4 & F5*	VPC TEP	VCC OSP & VCC TSP	yes	no
F4 & F5*	VPC TEP & VPC TSP	VCC IP	yes	no
F4 & F5*	VPC TEP & VPC TSP	VCC OSP	yes	no
F4 & F5*	VPC TEP & VPC TSP	VCC TSP	yes	no
F4 & F5*	VPC TEP & VPC TSP	VCC OSP & VCC TSP	yes	no
F5		VCC OEP	yes	no
F5		VCC OEP & VCC OSP	yes	no
F4 & F5*	VPC OEP	VCC IP	no	yes
F4 & F5*	VPC OEP	VCC OSP	no	yes
F4 & F5*	VPC OEP	VCC TSP	no	yes
F4 & F5*	VPC OEP	VCC OSP & VCC TSP	no	yes
F4 & F5*	VPC OEP & VPC OSP	VCC IP	no	yes

F4 & F5*	VPC OEP & VPC OSP	VCC OSP	no	yes
F4 & F5*	VPC OEP & VPC OSP	VCC TSP	no	yes
F4 & F5*	VPC OEP & VPC OSP	VCC OSP & VCC TSP	no	yes
F5		VCC TEP	no	yes
F5		VCC TEP & VCC TSP	no	yes

* It is also possible to configure a VP without any VCs

7.2 OAM Cell Formats

7.2.1 OAM Cell Header Coding

	VCI	PTI	HK*
F4 Segment flow	0003_H	don't care for Rx 000 for Tx	111
F4 End-to-end flow	0004_H	don't care for Rx 000 for Tx	111
F4 Internal Flow (for ICC)*	0003_H	don't care for Rx 000 for Tx	100
F5 Segment flow	don't care for Rx $FFFF_H$ for Tx	100	111
F5 End-to-end flow	don't care for Rx $FFFF_H$ for Tx	101	111
F5 Internal Flow (for ICC)*	don't care for Rx $FFFF_H$ for Tx	100	100

* Proprietary functions, use optional

7.2.2 AIS Cell

Payload byte	Generated AIS Cell			
0..3	10_H	$6A_H$	$6A_H$	$6A_H$
4..7	$6A_H$	$6A_H$	$6A_H$	$6A_H$
8..11	$6A_H$	$6A_H$	$6A_H$	$6A_H$
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received AIS Cell			
0..3	10_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

7.2.3 RDI Cell

Payload byte	Generated RDI Cell			
0..3	11_H	$6A_H$	$6A_H$	$6A_H$
4..7	$6A_H$	$6A_H$	$6A_H$	$6A_H$
8..11	$6A_H$	$6A_H$	$6A_H$	$6A_H$
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received RDI Cell			
0..3	11_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

7.2.4 CC Cell

Payload byte	Generated CC Cell			
0..3	14_H	$6A_H$	$6A_H$	$6A_H$
4..7	$6A_H$	$6A_H$	$6A_H$	$6A_H$
8..11	$6A_H$	$6A_H$	$6A_H$	$6A_H$
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	Received CC Cell			
0..3	14_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

7.2.5 LB Cell

Payload byte	Generated LB Cell at originating point			
0..3	TMR1L(15:8)	TMR1L(7:0)	TMR2H(15:8)	TMR2H(7:0)
4..7	TMR2L(15:8)	TMR2L(7:0)	TMR3H(15:8)	TMR3H(7:0)
8..11	TMR3L(15:8)	TMR3L(7:0)	TMR4H(15:8)	TMR4H(7:0)
12..15	TMR4L(15:8)	TMR4L(7:0)	TMR5H(15:8)	TMR5H(7:0)
16..19	TMR5L(15:8)	TMR5L(7:0)	TMR6H(15:8)	TMR6H(7:0)
20..23	TMR6L(15:8)	TMR6L(7:0)	TMR7H(15:8)	TMR7H(7:0)
24..27	TMR7L(15:8)	TMR7L(7:0)	TMR8H(15:8)	TMR8H(7:0)
28...31	TMR8L(15:8)	TMR8L(7:0)	TMR9H(15:8)	TMR9H(7:0)
32..35	TMR9L(15:8)	TMR9L(7:0)	TMR10H(15:8)	TMR10H(7:0)
36..39	TMR10L(15:8)	TMR10L(7:0)	TMR11H(15:8)	TMR11H(7:0)
40..43	TMR11L(15:8)	TMR11L(7:0)	TMR12H(15:8)	TMR12H(7:0)
44..47	TMR12L(15:8)	TMR12L(7:0)	000000 : CRC-10(9:0)	

TMRxx = Registers for Insertion Buffer access

Payload byte	Received Location Cell at loopback and at terminating point			
0..3	18_H	LB_IND		
4..7			Location ID #15	Location ID #14
8..11	Location ID #13	Location ID #12	Location ID #11	Location ID #10
12..15	Location ID #9	Location ID #8	Location ID #7	Location ID #6
16..19	Location ID #5	Location ID #4	Location ID #3	Location ID #2
20..23	Location ID #1	Location ID #0	Source ID #15	Source ID #14
24..27	Source ID #13	Source ID #12	Source ID #11	Source ID #10
28...31	Source ID #9	Source ID #8	Source ID #7	Source ID #6
32..35	Source ID #5	Source ID #4	Source ID #3	Source ID #2
36..39	Source ID #1	Source ID #0		
40..43				
44..47			xxxxxx : CRC-10(9:0)	

Payload byte	Generated LB Cell at loopback point			
0..3	18_H	LB_IND		
4..7				
8..11				
12..15				
16..19				
20..23		**byte 2..45 and byte 46(7:2)**		

24..27		**are copied from received**		
28...31		**LB cell**		
32..35				
36..39				
40..43				
44..47			000000 : CRC-10(9:0)	

7.2.6 FM Cell

Payload byte	**Generated FM Cell**			
0..3	20_H	MCSN	TUC_{0+1}(15:8)	TUC_{0+1}(7:0)
4..7	BEDC(15:8)	BEDC(7:0)	TUC_0(15:8)	TUC_0(7:0)
8..11	FF_H	FF_H	FF_H	FF_H
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$6A_H$	$6A_H$	$6A_H$
44..47	$6A_H$	$6A_H$	000000 : CRC-10(9:0)	

Payload byte	**Received FM Cell**			
0..3	20_H	MCSN	TUC_{0+1}(15:8)	TUC_{0+1}(7:0)
4..7	BEDC(15:8)	BEDC(7:0)	TUC_0(15:8)	TUC_0(7:0)
8..11				
12..15				
16..19				
20..23		**byte 8..45 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

7.2.7 BR Cell

Payload byte	Generated BR Cell			
0..3	21_H	MCSN	TUC_{0+1}(15:8)*	TUC_{0+1}(7:0)*
4..7	BEDC(15:8)	BEDC(7:0)	TUC_0(15:8)*	TUC_0(7:0)*
8..11	FF_H	FF_H	FF_H	FF_H
12..15	$6A_H$	$6A_H$	$6A_H$	$6A_H$
16..19	$6A_H$	$6A_H$	$6A_H$	$6A_H$
20..23	$6A_H$	$6A_H$	$6A_H$	$6A_H$
24..27	$6A_H$	$6A_H$	$6A_H$	$6A_H$
28...31	$6A_H$	$6A_H$	$6A_H$	$6A_H$
32..35	$6A_H$	$6A_H$	$6A_H$	$6A_H$
36..39	$6A_H$	$6A_H$	$6A_H$	$6A_H$
40..43	$6A_H$	$TRCC_0$(15:8)	$TRCC_0$(7:0)	BLER
44..47	$TRCC_{0+1}$(15:8)	$TRCC_{0+1}$(7:0)	000000 : CRC-10(9:0)	

* TUC_0 and TUC_{0+1} are copied from the received FM cell

Payload byte	Received BR Cell			
0..3	21_H	MCSN	TUC_{0+1}(15:8)	TUC_{0+1}(7:0))
4..7			TUC_0(15:8)	TUC_0(7:0))
8..11				
12..15				
16..19		**byte 4, 5 and**		
20..23		**byte 8..40 and**		
24..27		**byte 46(7:2)**		
28...31		**don't care**		
32..35				
36..39				
40..43		$TRCC_0$(15:8)	$TRCC_0$(7:0)	BLER
44..47	$TRCC_{0+1}$(15:8)	$TRCC_{0+1}$(7:0)	xxxxxx : CRC-10(9:0)	

7.2.8 PM/CC Activation/deactivation Cell

Payload byte	Generated PM/CC activation/deactivation Cell			
0..3	TMR1L(15:8)	TMR1L(7:0)	TMR2H(15:8)	TMR2H(7:0)
4..7	TMR2L(15:8)	TMR2L(7:0)	TMR3H(15:8)	TMR3H(7:0)
8..11	TMR3L(15:8)	TMR3L(7:0)	TMR4H(15:8)	TMR4H(7:0)
12..15	TMR4L(15:8)	TMR4L(7:0)	TMR5H(15:8)	TMR5H(7:0)
16..19	TMR5L(15:8)	TMR5L(7:0)	TMR6H(15:8)	TMR6H(7:0)
20..23	TMR6L(15:8)	TMR6L(7:0)	TMR7H(15:8)	TMR7H(7:0)
24..27	TMR7L(15:8)	TMR7L(7:0)	TMR8H(15:8)	TMR8H(7:0)
28...31	TMR8L(15:8)	TMR8L(7:0)	TMR9H(15:8)	TMR9H(7:0)
32..35	TMR9L(15:8)	TMR9L(7:0)	TMR10H(15:8)	TMR10H(7:0)
36..39	TMR10L(15:8)	TMR10L(7:0)	TMR11H(15:8)	TMR11H(7:0)
40..43	TMR11L(15:8)	TMR11L(7:0)	TMR12H(15:8)	TMR12H(7:0)
44..47	TMR12L(15:8)	TMR12L(7:0)	000000 : CRC-10(9:0)	

TMRxx = Registers for Insertion Buffer access

Payload byte	Received activation/deactivation PM Cell at terminating point			
0..3	80_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and byte 46(7:2)**		
24..27		**are don't care**		
28...31				
32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

Payload byte	Received activation/deactivation CC Cell at terminating point			
0..3	81_H			
4..7				
8..11				
12..15				
16..19				
20..23		**byte 1..45 and byte 46(7:2)**		
24..27		**are don't care**		
28...31				

32..35				
36..39				
40..43				
44..47			xxxxxx : CRC-10(9:0)	

7.3 References

1. UTOPIA Level 1 Specification Version 2.01, March 21, 1994, ATM Forum
2. UTOPIA Level 2 Specification Version 1.0, June 1995, ATM Forum
3. IEEE 1596.3 Standard for Low-Voltage Differential Signals for SCI, Draft 1.3, Nov. 95
4. Joint Test Action Group JTAG standard IEEE Std. 1149.1
5. 'ATM Networks: Concepts, Protocols, Applications', Händel, Schröder, Huber, Addison-Wesley, 1994, ISBN 0-201-42274-3
6. ITU-T Recommendation I.610 „B-ISDN Operation and Maintenance Principles and Functions", 11/94
7. Bellcore TA-NWT 1248 CORE „Generic Requirements for Operations of ATM Network Elements"

7.4 Acronyms

- ABM = PXB 4330 ATM Buffer Manager
- AIS = Alarm Indication Signal (OAM function)
- ALP = PXB 4350 ATM Layer Processor
- AOP = PXB 4340 ATM OAM Processor
- ASF = ATM Switching Fabric
- ASM = PXB 4310 ATM Switching Matrix
- BIP-16 = Bit Interleaved Parity, 16 bit
- BR = Backward Reporting (PM function)
- byte = octet = 8 bit
- CC = Continuity Check (OAM function)
- CLP = Cell Loss Priority of standardized ATM cell
- double word = 32 bit
- FM = Forward Monitoring (PM cell type)
- HK = HouseKeeping bits of UDF1 field in UTOPIA cell format
- HT = Header Translation
- I/O = Input / Output
- ICC = Internal Continuity Check (proprietary OAM function)
- ITU-T = International Telecommunications Union - Telecommunications standardization sector
- IWE8 = PXB 4220 InterWorking Element for 8 channels
- LB = Loopback (OAM function)
- LCI = Local Connection Identifier

- LIC = Line Interface Card or Line Interface Circuit
- LOC = Loss Of Continuity (OAM state)
- LPS = Line Protection Switching
- LSB = Least Significant Bit
- LVDS = Low Voltage Differential Signaling
- octet = byte = 8 bit
- OAM = Operation And Maintenance
- PM = Performance Monitoring (OAM function)
- PTI = Payload Type Indication field of standardized ATM cell
- RDI = Remote Defect Indication (OAM function)
- SLIF = Switch Link InterFace
- SSRAM = Synchronous Static RAM
- tbd = to be defined
- TM = Traffic Management
- UTOPIA = Universal Test and OPeration Interface for ATM
- VC- = Virtual Channel specific
- VCC = Virtual Channel Connection
- VCI = Virtual Channel Identifier of standardized ATM cell
- VP- = Virtual Path specific
- VPC = Virtual Path Connection
- VPI = Virtual Path Identifier of standardized ATM cell
- word = 16 bit