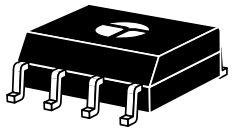
# ULTRA LOW CAPACITANCE TVS ARRAY

## APPLICATIONS

- ✓ Hand Held Electronics
- ✓ Sense & Control Circuits
- ✓ FireWire
- ✓ Ethernet - 10/100 Base T



SO-8 PACKAGE

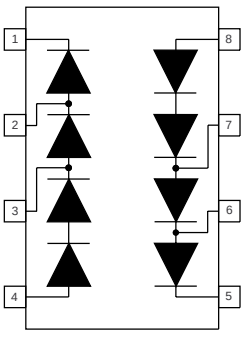
## IEC COMPATIBILITY (EN61000-4)

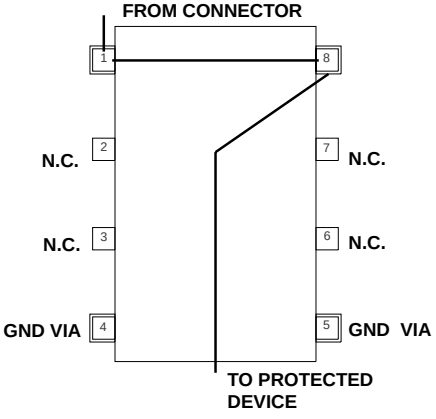
- ✓ 61000-4-2 (ESD): Air - 15kv, Contact - 8kv
- ✓ 61000-4-4 (EFT): 40A - 5/50ns

## FEATURES

- ✓ Suitable for Low Capacitance High Speed $V^2D$ Protection
- ✓ 500 Watts Peak Pulse Power Dissipation per Line (8/20 μs)
- ✓ Bidirectional Configuration
- ✓ ESD Protection > 40 kilovolts
- ✓ Ultra Low Capacitance < 1.25 pF @ 0V, 1 MHz
- ✓ Standard SO-8 Package
- ✓ Low Clamping Voltage < 5 Volts
- ✓ UL 94V-0 Flammability Classification

## CIRCUIT DIAGRAM & PCB LAYOUT RECOMMENDATION



# DEVICE CHARACTERISTICS

| MECHANICAL CHARACTERISTICS | | MAXIMUM RATINGS | |
|---|---|---|---|
| **PACKAGE** | Molded SO-8 Surface Mount | **$P_{PP}$ @ 25°C (SEE FIGURE 1)** | 500 Watts, 8/20 µs Waveshape |
| **PACKAGING** | 12 mm Tape per EIA 481-1 | **OPERATING & STORAGE TEMPERATURE** | -55° to +150°C |
| **APPROX. WEIGHT** | 0.1 grams | **REPETITION RATE (DUTY CYCLE)** | 0.01% |
| **DEVICE MARKINGS** | Logo & Marking Code | **$T_{CLAMPING}$ (0 VOLTS TO $V_{(BR)}$ MIN.)** | Bidirectional: $< 1 \times 10^{-9}$ seconds |
| **MISCELLANEOUS** | Pin 1 Indicated by Dot on Top of Package | | |

**ELECTRICAL CHARACTERISTICS** @ 25° C Ambient Temperature

| PROTEK PART NUMBER | DEVICE MARKING CODE | RATED STAND-OFF VOLTAGE $V_{WM}$ VOLTS | BREAKDOWN VOLTAGE (NOTE 2) @ 1 mA $V_{(BR)}$ VOLTS | MAXIMUM REVERSE LEAKAGE CURRENT @ $V_{WM}$ $I_D$ (NOTE 2) µA | MAXIMUM CLAMPING VOLTAGE (See Fig. 2) (NOTE 2) @ 8/20 µs $V_C$ @ $I_{PP}$ | WORKING INVERSE BLOCKING VOLTAGE (NOTE 3) $V_{WIB}$ VOLTS | MAXIMUM CAPACITANCE (NOTE 1) @ 0V, 1 MHz C pF | INVERSE BLOCKING LEAKAGE CURRENT @ $V_{WIB}$ $I_R$ (NOTE 3) µA |
|---|---|---|---|---|---|---|---|---|
| PLC496 | VEC | 1.0 | 2.5 | 20 | 10.0V @ 50A | 75 | 1.25 | 1.0 |

**Note 1:** Capacitance from pin 1 to pin 4 < 1.25 pF, capacitance from pin 8 to pin 5 < 1.25pF.
**Note 2:** Apply positive voltage from pin 4 to pin 1 & pin 8 to pin 5.
**Note 3:** Apply positive voltage from pin 1 to pin 4 & pin 5 to pin 8.

**FIGURE 1**
**PEAK PULSE POWER VS PULSE TIME**

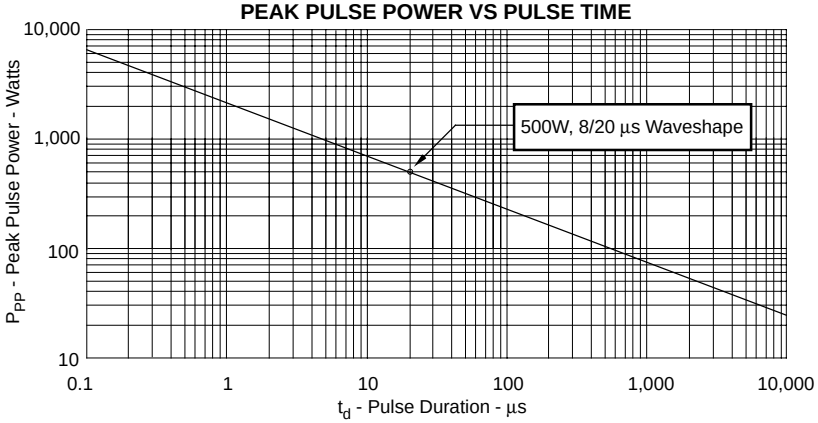
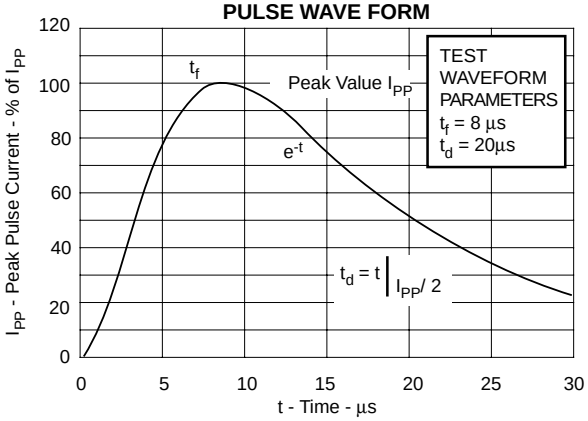



**FIGURE 2**
**PULSE WAVE FORM**



# DEVICE CHARACTERISTICS

**FIGURE 3**
**POWER DERATING CURVE**

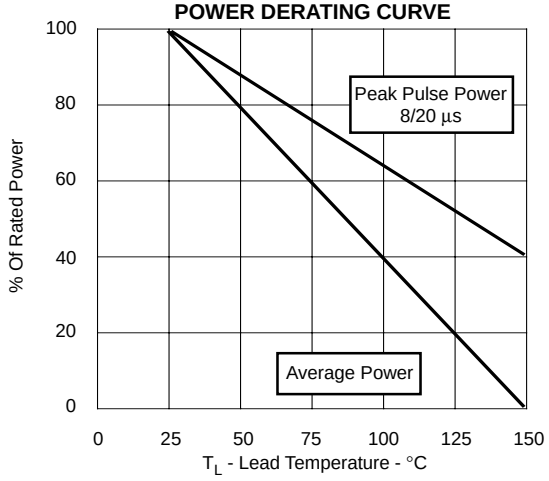
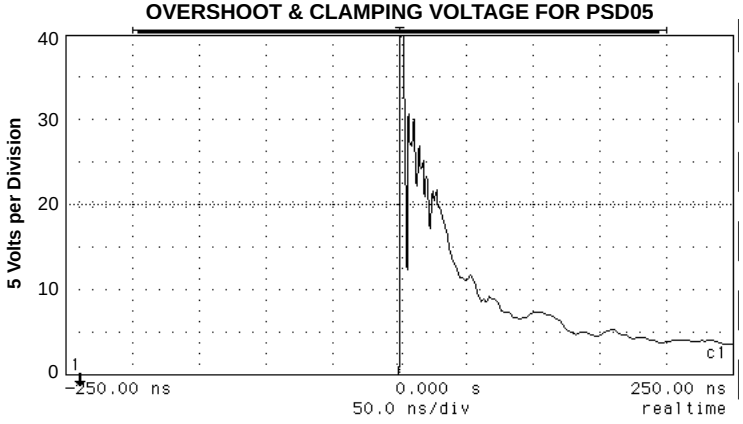



**FIGURE 4**
**OVERSHOOT & CLAMPING VOLTAGE FOR PSD05**




**ESD Test Pulse: 5 kilovolt, 1/30ns (waveshape)**

# DEVICE SPECIFIC APPLICATION NOTE

The PLC496 is an ultra low capacitance, bidirectional, TVS array designed to protect I/O or high-speed data lines from the effects of ESD or EFT. In addition, this series has a surge capability of 500 Watts $P_{PP}$ line for an 8/20 µs waveshape and offers ESD protection > 25kV.

The PLC496 is ideal for use in protecting and maintaining signal integrity in I/O and sensor circuit applications. When a transient occurs, the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. For most applications, ESD is considered a common mode (line-to-ground) transient event and EFT is considered a differential mode (line-to-line) transient event.

The PLC496 is designed to protect one bidirectional line where the normal signal voltage is both positive and negaitve. Figure 1 shows a typical differential mode (line-to-line) I/O port protection circuit application. Pins 1, 4, 5 and 8 are connected to the data lines. Pins 2, 3, 7 and 6 are not connected.

In addition, the PLC496 can provide protection for sensor circuit applications. Figure 2, a typical common mode (line-to-ground) sensor circuit application, shows pins 1 and 8 of each TVS device connected to the line and pins 4 and 5 connected to ground.

**Circuit Board Layout Recommendations**

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

✓ The PLC496 should be placed near the input terminals or connectors. By placing the TVS close to the connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

✓ The path length between the TVS device and the protected line should be minimized.

✓ All conductive loops including power and ground loops should be minimized.

✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.

✓ Ground planes should be used whenever possible. Ground vias are recommended for multilayer PCBs.

Figure 1. Typical Differential Mode I/O Port Protection Circuit

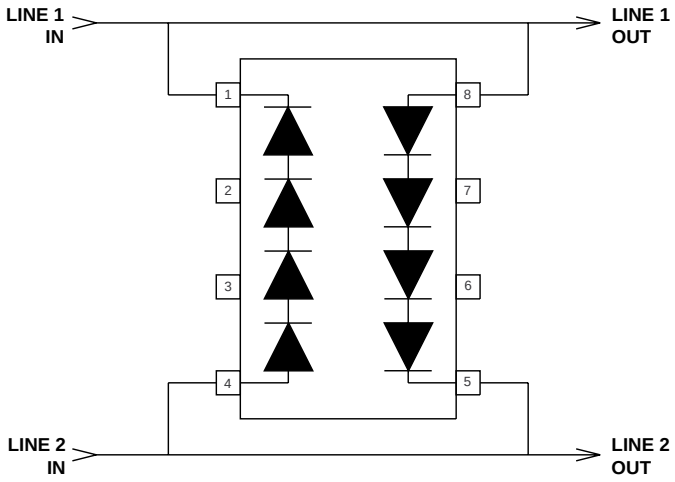
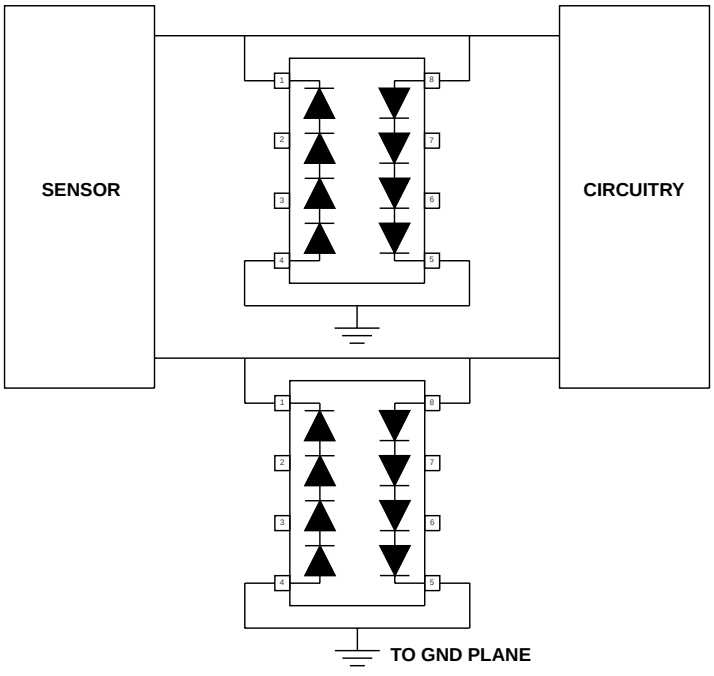
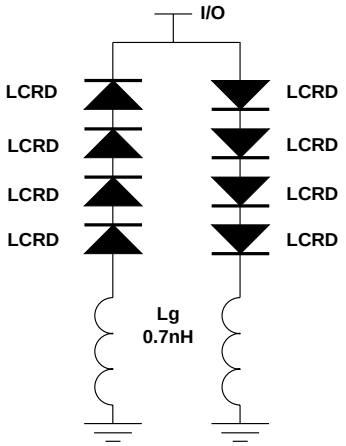



Figure 2. Typical Common-Mode Sensor Protection Circuit



# SPICE MODEL & PARAMETERS

**FIGURE 1**
**SPICE MODEL FOR PLC496**



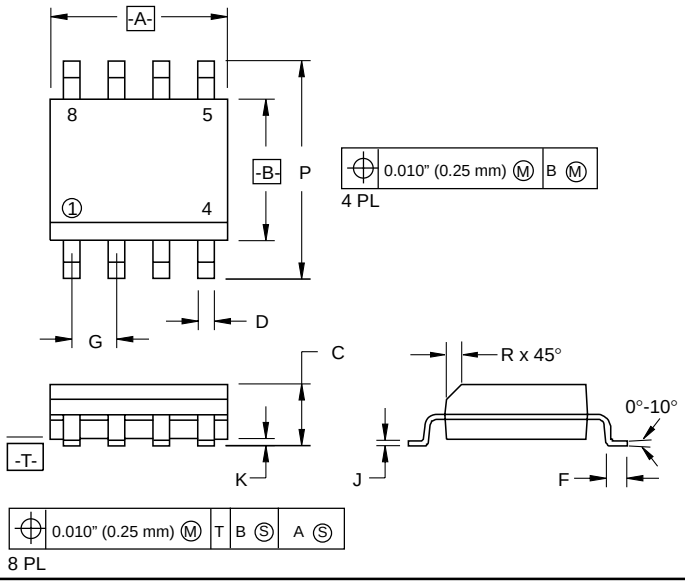

**LCRD:** **LOW CAPACITANCE RECTIFIER DIODE**
**Lg:** **LEAD INDUCTANCE**

TABLE 1 - SPICE PARAMETERS

| PARAMETER | UNIT | LCRD |
|---|---|---|
| BV | V | 200 |
| IBV | µA | 0.01 |
| Cjo | pF | 5 |
| Is | A | $10E^{-14}$ |
| Vj | V | 0.6 |
| M | - | 0.33 |
| N | - | 1 |
| Rs | Ohms | 0.31 |
| TT | µs | 1 |
| EG | eV | 1.11 |

# PACKAGE OUTLINES & DIMENSIONS

## SO-8 PACKAGE OUTLINE




## SO-8 PACKAGE DIMENSIONS

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.196 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.250 | 0.016 | 0.049 |
| G | 1.27 BSC | 1.27 BSC | 0.05 BSC | 0.05 BSC |
| J | 0.18 | 0.25 | 0.007 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.008 |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

**NOTES:**
1. - T - = Seating Plane
2. Dimension “A” is Datum.
3. Dimension “A” and “B” do not include mold protusion.
4. Maximum mold protusion is 0.15” (0.006 mm) per side.
5. Dimensioning and tolerances per ANSI Y14.5M, 1982.

## SO-8 MOUNTING PAD