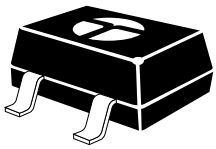
PROTEK DEVICES®
.....Engineered solutions for the transient environment

PLC497

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Low Voltage Wireless Equipment
- ✓ Sense & Control Circuits
- ✓ FireWire
- ✓ Ethernet - 10/100 Base T



SOT-23 PACKAGE

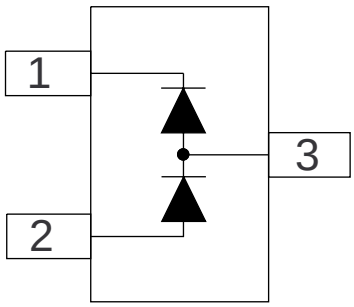
IEC COMPATIBILITY (EN61000-4)

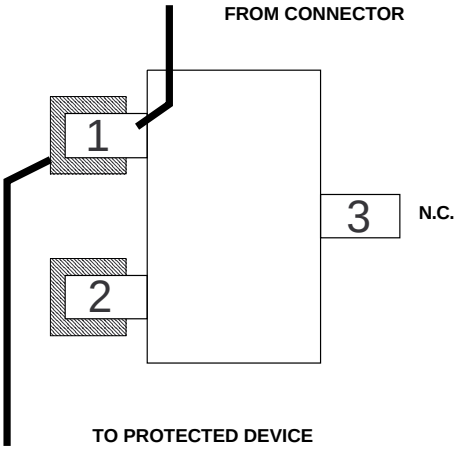
- ✓ 61000-4-2 (ESD): Air - 15kv, Contact - 8kv
- ✓ 61000-4-4 (EFT): 40A - 5/50ns

FEATURES

- ✓ Suitable for Low Capacitance High Speed V^2D Protection
- ✓ 250 Watts Peak Pulse Power Dissipation per Line (8/20 μs)
- ✓ Unidirectional Configuration
- ✓ ESD Protection > 25 kilovolts
- ✓ Ultra Low Capacitance < 2.5 pF @ 0V, 1 MHz
- ✓ Standard SOT-23 Package
- ✓ Low Clamping Voltage < 5 Volts
- ✓ UL 94V-0 Flammability Classification

CIRCUIT DIAGRAM & PCB LAYOUT RECOMMENDATION





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DEVICE CHARACTERISTICS

MECHANICAL CHARACTERISTICS		MAXIMUM RATINGS	
PACKAGE	Molded SOT-23 Surface Mount	**P_{PP} @ 25°C (SEE FIGURE 1)**	250 Watts, 8/20 µs Waveshape
PACKAGING	8 mm Tape per EIA 481-1	**OPERATING & STORAGE TEMPERATURE**	-55°C to +150°C

ELECTRICAL CHARACTERISTICS @ 25° C Ambient Temperature

PROTEK	DEVICE	RATED STAND-OFF VOLTAGE (NOTE 3)	BREAKDOWN VOLTAGE (NOTE 3)	MAXIMUM REVERSE LEAKAGE CURRENT	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	WORKING INVERSE BLOCKING VOLTAGE	MAXIMUM CAPACITANCE (See Note 1)	INVERSE BLOCKING LEAKAGE CURRENT
PLC497	**LC**	**1.0**	**1.3**	**20**	**5.0V @ 50A**	**75**	**2.5**	**1.0**

Note 1: Capacitance from Pin 1 to Pin 2 = 2.5 pF.
Note 2: Apply positive voltage from pin 1 to pin 2
Note 3: Apply positive voltage from pin 2 to pin 1

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

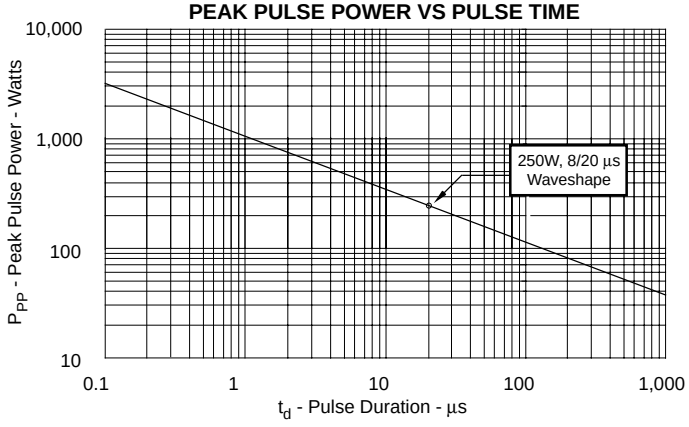
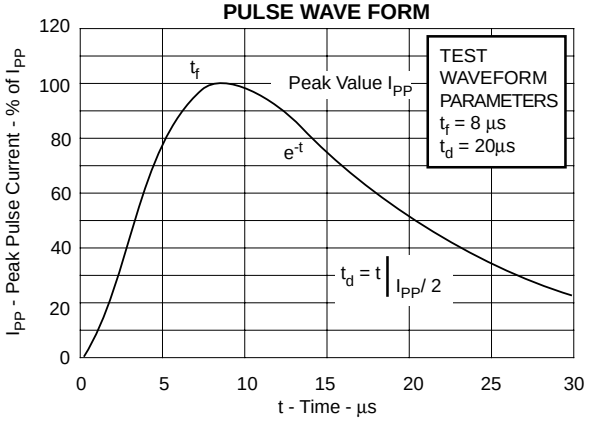


FIGURE 2
PULSE WAVE FORM



DEVICE CHARACTERISTICS

FIGURE 3
POWER DERATING CURVE

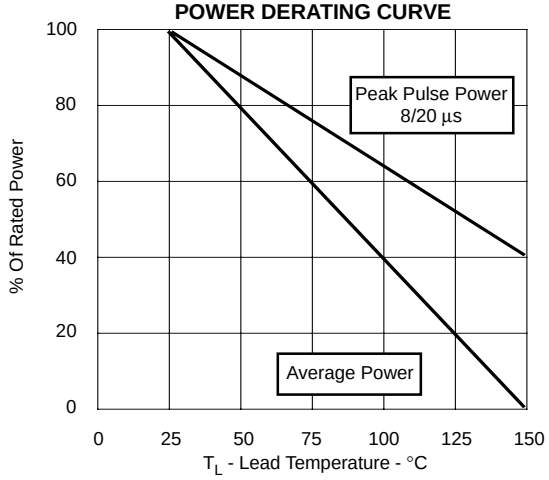
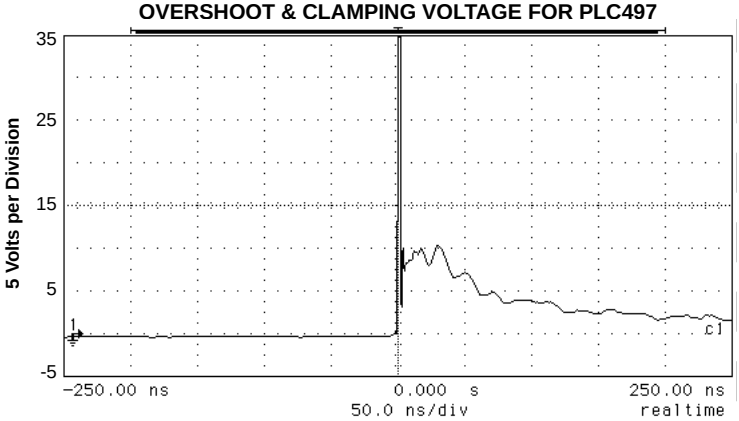
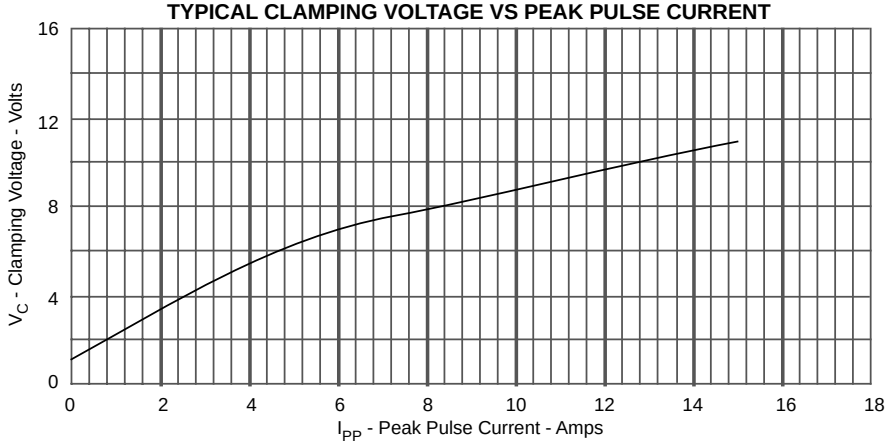


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PLC497



ESD Test Pulse: 25 kilovolt, 1/30ns (waveshape)

FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT



DEVICE SPECIFIC APPLICATION NOTE

The PLC497 is an ultra low capacitance, unidirectional, TVS array designed to protect I/O or high-speed data lines from the effects of ESD or EFT. In addition, this series has a surge capability of 250 Watts P_{PP} line for an 8/20 μs waveshape and offers ESD protection > 25kV.

The PLC497 is ideal for use in protecting and maintaining signal integrity in I/O and sensor circuit applications. When a transient occurs, the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. For most applications, ESD is considered a common mode (line-to-ground) transient event and EFT is considered a differential mode (line-to-line) transient event.

The PLC497 is designed to protect one unidirectional line. Figure 1 shows a typical differential mode (line-to-line) I/O port protection circuit application. Pins 1 and 2 are connected to the data lines. Pin 3 is not connected. To achieve bidirectional protection, two PLC497 units are placed in parallel with opposing polarities within the circuit layout.

In addition, the PLC497 can provide protection for sensor circuit applications. Figure 2, a typical common mode (line-to-ground) sensor circuit application, shows two TVS devices with pins 1 connected to the line, pins 2 connected to ground and pins three unconnected.. To acheive bidirectional protection in this application, a second pair of TVS devices is added in parallel with opposing polarities where pins 2 are connected to the line, pins 1 connected to ground and pins three unconnected.

Circuit Board Layout Recommendations

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

✓ The PLC497 should be placed near the input terminals or connectors. By placing the TVS close to the connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

✓ The path length between the TVS device and the protected line should be minimized.

✓ All conductive loops including power and ground loops should be minimized.

✓ The transient current return path to ground should be kept as short as possible to reduce parasiticinductance.

✓ Ground planes should be used whenever possible. Ground vias are recommended for multilayer PCBs.

Figure 1. Typical Differential-Mode I/O Port Protection Circuit

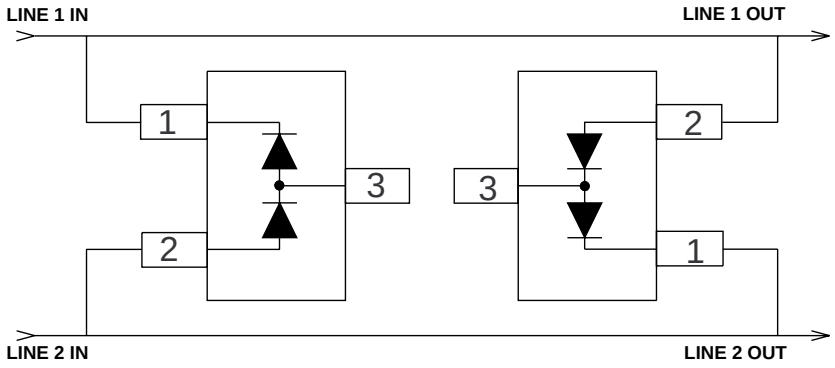


Figure 2. Typical Common-Mode Sensor Protection Circuit

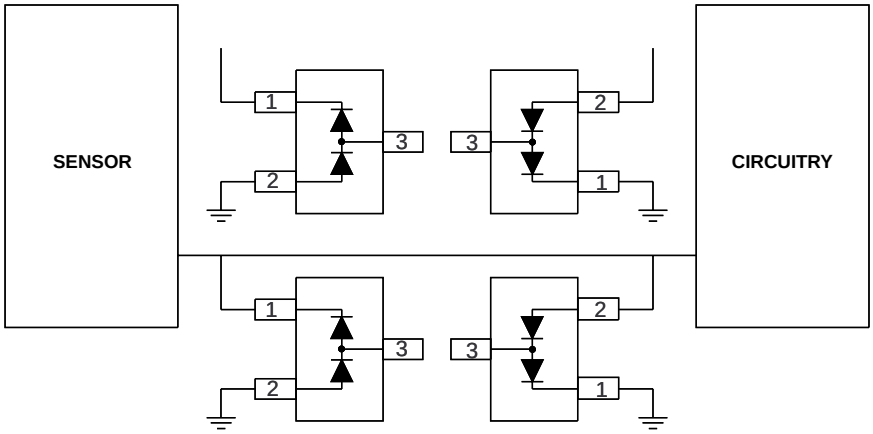
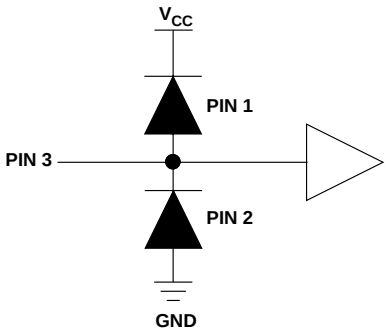
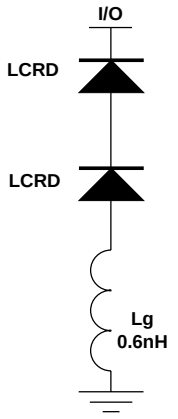


Figure 3. Steering Diode Array Circuit Schematic



SPICE MODEL & PARAMETERS

FIGURE 1
SPICE MODEL FOR PLC497



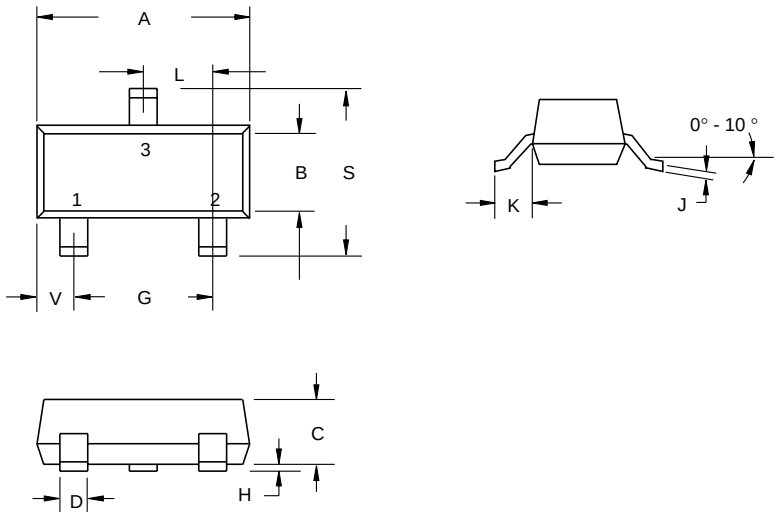
LCRD: **LOW CAPACITANCE RECTIFIER DIODE**
Lg: **LEAD INDUCTANCE**

TABLE 1 - SPICE PARAMETERS

PARAMETER	UNIT	LCRD
BV	V	200
IBV	µA	0.01
Cjo	pF	5
Is	A	$10E^{-14}$
Vj	V	0.6
M	-	0.33
N	-	1
Rs	Ohms	0.31
TT	µs	1
EG	eV	1.11

PACKAGE OUTLINES & DIMENSIONS

SOT-23 PACKAGE OUTLINE

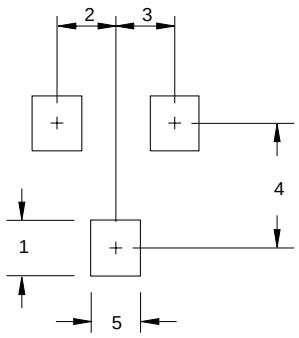


SOT-23 PACKAGE DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

NOTES:
1. Dimensioning and tolerance per ANSI Y 14.5M, 1985.
2. Controlling Dimension: Inches
3. Maximum lead thickness includes lead finish thickness.
4. Minimum lead thickness is the minimum thickness of the base material.
4. Pin 3 is the cathode (Unidirectional only).

SOLDER PAD LAYOUT



DIM	TYPICAL	
	Millimeters	Inches
1	0.85	0.033
2	0.95	0.037
3	0.95	0.037
4	2.00	0.079
5	0.85	0.033