Features

- **PC603e™ Microprocessor (Embedded PowerPC™ Core) at 100 - 200 MHz**
  - **140 MIPS at 100 MHz (Dhrystone 2.1)**
  - **280 MIPS at 200 MHz (Dhrystone 2.1)**
  - **High-performance, Superscalar Microprocessor**
  - **Disable CPU Mode**
  - **Improved Low-power Core**
  - **16-Kbyte Data and 16-Kbyte Instruction Cache, Four-way Set Associative**
  - **Memory Management Unit**
  - **No Floating Point Unit**
  - **Common On-chip Processor (COP)**
- **System Integration Unit (SIU)**
  - **Memory Controller, Including Two Dedicated SDRAM Machines**
  - **PCI up to 66 MHz (Available in Subsequent Versions)**
  - **Hardware Bus Monitor and Software Watchdog Timer**
  - **IEEE 1149.1 JTAG Test Access Port**
- **High-performance Communications Processor Module (CPM) with Operating Frequency up to 166 MHz**
  - **PowerPC and CPM May Run at Different Frequencies**
  - **Supports Serial Bit Rates up to 710 Mbps at 133 MHz**
  - **Parallel I/O Registers**
  - **On-board 24 KBytes of Dual-port RAM**
  - **Two Multi-channel Controllers (MCCs) Each Supporting 128 Full-duplex, 64-Kbps, HDLC Lines**
  - **Virtual DMA Functionality**
- **Two Bus Architectures: One 64-bit PowerPC and One 32-bit Local Bus (or PCI on PC8265)**
- **Two UTOPIA Level-2 Master/Slave Ports, Both with Multi-PHY Support. One Can Support 8/16 bit Data**
- **Three MIL Interfaces**
- **Eight TDM Interfaces (T1/E1), Two TDM Ports Can Be Glueless to T3/E3**
- **Power Consumption: 2.5W at 133 MHz**

Description

The PC8260 PowerQUICC II™ is a versatile communications processor that integrates on one chip, a high-performance PowerPC (PC603e) RISC microprocessor, a highly flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PC603e microprocessor, specifically referred to later in this document as the EC603e, with 16 Kbytes of instruction cache and 16 Kbytes of data cache and no floating-point unit (FPU). The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system, a 60x-to-PCI bus bridge (available in future revisions) and many other peripherals, making this device a complete system on a chip.

The communications processor module (CPM) includes all the peripherals found in the PC860, with the addition of three high-performance communication channels that support new emerging protocols (for example, 155-Mbps ATM and Fast Ethernet).

Equipped with dedicated hardware, the PC8260 can handle up to 256 full-duplex, time-division, multiplexed logical channels.

PowerPC-based Communications Processors

PC8260 PowerQUICC II™

Rev. 2131A–08/01

Screening
Quality
Packaging

This product is manufactured in full compliance with:

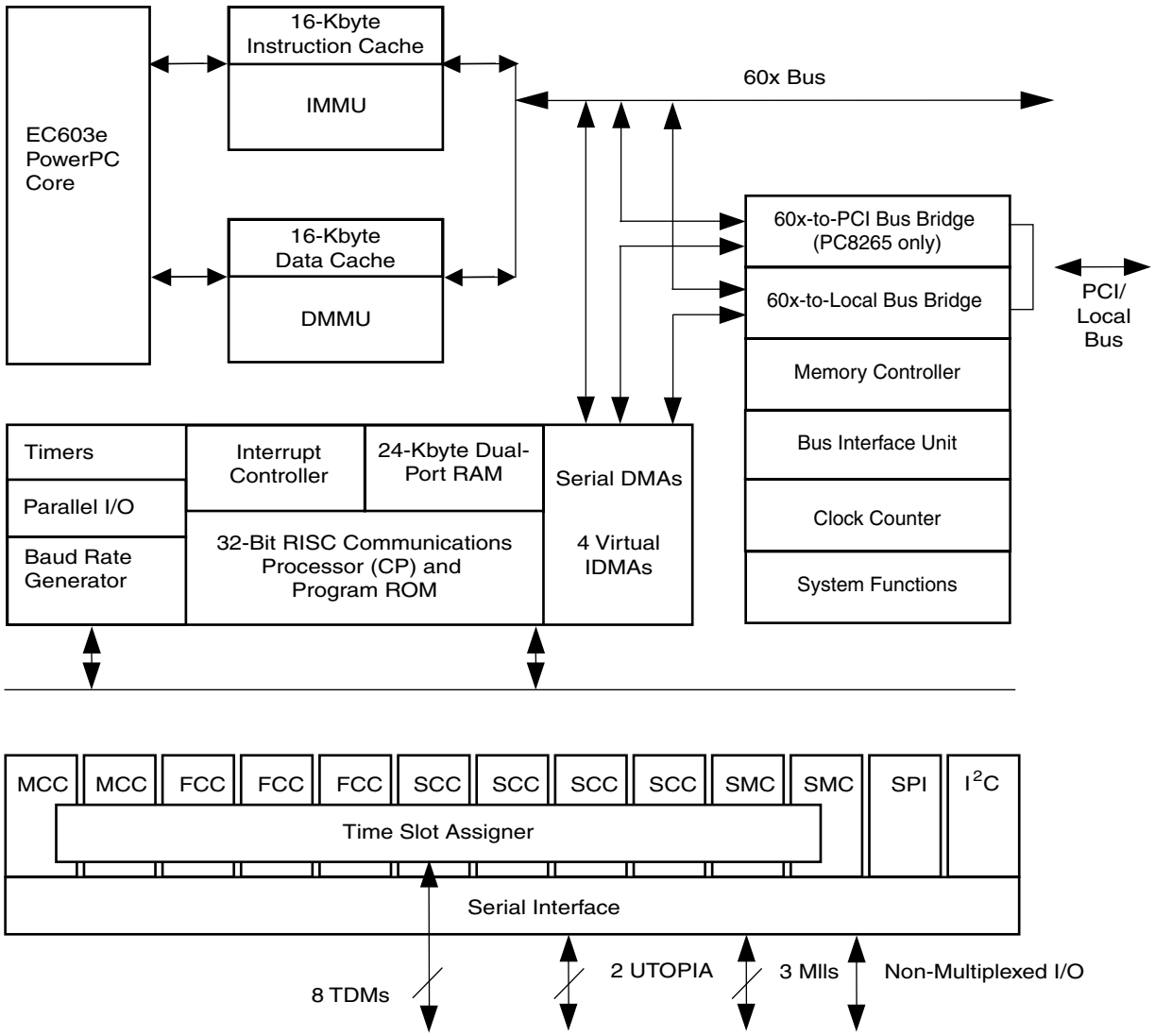
- Upscreening based upon Atmel standards.
- Full military temperature range (T_J = -55°C, T_J = +125°C)
- Industrial temperature range (T_J = -40°C, T_J = +110°C)
- Core power supply:
  2.5V ± 5% (L-Spec for 200 MHz)
  2.50V to 2.75V (R-Spec for 250 MHz) (tbc)
- I/O power supply: 3.0V to 3.6V
- 480-ball Tape Ball Grid Array package (TBGA 37.5 mm x 37.5 mm)

PC8260 Architecture General Overview

The PC8260 has two external buses to accommodate bandwidth requirements from the high-speed system core and the very fast communications channels. The device is composed of the following three major functional blocks:

- A 64-bit PowerPC core derived from the EC603e with MMUs and caches.
- A system interface unit (SIU).
- A communications processor module (CPM). Both the system core and the CPM have an internal PLL, which allows independent optimization of the frequencies at which they run. The system core and CPM are both connected to the 60x bus.

Figure 1. PC8260 Block Diagram



EC603e Core

The EC603e core is derived from the PowerPC603e microprocessor without the floating-point unit and with power management modifications.The core is a high-performance low-power implementation of the PowerPC family of reduced instruction set computer (RISC) microprocessors. The EC603e core implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits. The EC603e cache provides snooping to ensure data coherency with other masters. This helps ensure coherency between the CPM and system core.

The core includes 16 Kbytes of instruction cache and 16 Kbytes of data cache. It has a 64-bit split-transaction external data bus which is connected directly to the external PC8260 pins.

The EC603e core has an internal common on-chip (COP) debug processor. This processor allows access to internal scan chains for debugging purposes. It is also used as a serial connection to the core for emulator support.

The EC603e core performance for the SPEC 95 benchmark for integer operations ranges between 4.4 and 5.1 at 200 MHz. In Dhrystone 2.1 MIPS, the EC603e is 280 MIPS at 200 MHz (compared to 86 MIPS of the PC860 at 66 MHz).

The EC603e core can be disabled. In this mode, the PC8260 functions as a slave peripheral to an external core or to another PC8260 device with its core enabled.

System Interface Unit (SIU)

The SIU consists of the following:

- A 60x-compatible parallel system bus configurable to 64-bit data width. The PC8260 supports 64-, 32-, 16-, and 8-bit port sizes.The PC8260 internal arbiter arbitrates between internal components that can access the bus (system core, PCI bridge, CPM, and one external master). This arbiter can be disabled, and an external arbiter can be used if necessary.
- A local (32-bit data, 32-bit internal and 18-bit external address) bus. This bus is used to enhance the operation of the very high-speed communication controllers. Without requiring extensive manipulation by the core, the bus can be used to store connection tables for ATM or buffer descriptors (BDs) for the communication channels or raw data that is transmitted between channels. The local bus is synchronous to the 60x bus and runs at the same frequency.
- The local bus can be configured as a 32-bit data and up to 66 MHz PCI (version 2.1) bus. In PCI mode the bus can be programmed as a host or as an agent. The PCI bus can be configured to run synchronously or asynchronously to the 60x bus. The PC8260 has an internal PCI bridge with an efficient 60x-to-PCI DMA for memory block transfers.
- Applications that require both the local bus and PCI bus need to connect an external PCI bridge.
- A memory controller supporting 12 memory banks that can be allocated for either the system or the local bus. The memory controller is an enhanced version of the PC8260 memory controller. It supports three user-programmable machines. Besides supporting all PC8260 features, the memory controller also supports SDRAM with page mode and address data pipeline
- Supports JTAG controller IEEE 1149.1 test access port (TAP).
- A bus monitor that prevents 60x bus lock-ups, a real-time clock, a periodic interrupt timer, and other system functions useful in embedded applications.
- Glueless interface to L2 cache and 4-/16-K-entry CAM.

Communication Processor Module (CPM)

The CPM contains features that allow the PC8260 to excel in a variety of applications targeted mainly for networking and telecommunication markets.

The CPM is a superset of the PC8260 PowerQUICC CPM, with enhancements on the CP performance and additional hardware and microcode routines that support high bit rate protocols like ATM (up to 155 Mbps full-duplex) and Fast Ethernet (100 Mbps full-duplex).

The following list summarizes the major features of the CPM:

- The communications processor (CP) is an embedded 32-bit RISC controller residing on a separate bus (CPM local bus) from the 60x bus (used by the system core). With this separate bus, the CP does not affect the performance of the PowerPC core. The CP handles the lower layer tasks and DMA control activities, leaving the PowerPC core free to handle higher layer activities. The CP has an instruction set optimized for communications, but can also be used for general-purpose applications, relieving the system core of small often repeated tasks.
- Two serial DMAs (SDMAs) that can do simultaneous transfers, optimized for burst transfers to the 60x bus and to the local bus.
- Three full-duplex, serial fast communications controllers (FCCs) supporting ATM (155 Mbps) protocol through UTOPIA2 interface (there are two UTOPIA interfaces on the PC8260), IEEE 802.3 and Fast Ethernet protocols, HDLC up to E3 rates (45 Mbps) and totally transparent operation. Each FCC can be configured to transmit fully transparent and receive HDLC, or vice-versa.
- Two multichannel controllers (MCCs) that can handle an aggregate of 256 x 64 Kbps HDLC or transparent channels, multiplexed on up to eight TDM interfaces. The MCC also supports super-channels of rates higher than 64 Kbps and subchanneling of the 64-Kbps channels.
- Four full-duplex serial communications controllers (SCCs) supporting IEEE802.3/Ethernet, high-level synchronous data link control, HDLC, local talk, UART, synchronous UART, BISYNC and transparent.
- Two full-duplex serial management controllers (SMC) supporting GCI, UART, and transparent operations.
- Serial peripheral interface (SPI) and I^2C bus controllers.
- Time-slot assigner (TSA) that supports multiplexing of data from any of the four SCCs, three FCCs, and two SMCs.

Software Compatibility Issues

As much as possible, the PC8260 CPM features were made similar to those of the previous devices (PC860). The code ports easily from previous devices to the PC8260, except for new protocols supported by the PC8260.

Although many registers are new, most registers retain the old status and event bits, so an understanding of the programming models of the 68360, PC860, or PC850 is helpful. Note that the PC8260 initialization code requires changes from the PC8260 initialization code.

Differences Between PC860 and PC8260

The following PC860 features are not included in the PC8260:

- On-chip crystal oscillators (must use external oscillator)
- 4 MHz oscillator (input clock must be at the bus speed)
- Low power (standby) modes
- Battery-backup real-time clock (must use external battery-backup clock)
- BDM (COP offers most of the same functionality)
- True little endian mode (except the PCI bus)
- PCMCIA interface
- Infrared (IR) port
- QMC protocol in SCC (256 HDLC channels are supported by the MCCs)
- Multiply and accumulate (MAC) block in the CPM
- Centronics port (PIP)
- Asynchronous HDLC protocol (optional RAM microcode)
- Pulse-width modulated outputs
- SCC Ethernet controller option to sample 1 byte from the parallel port when a receive frame is complete.
- Parallel CAM interface for SCC (Ethernet)

Serial Protocol Table

Table 1 summarizes available protocols for each serial port.

Table 1. PC8260 Serial Protocols

	Port			
Protocol	**FCC**	**SCC**	**MCC**	**SMC**
ATM (Utopia)	x			
100BaseT	x			
10BaseT	x	x		
HDLC	x	x	x	
HDLC_BUS		x		
Transparent	x	x	x	x
UART		x		x
DPLL		x		
Multichannel			x	

Pin Assignment

Table 2 shows the pinout of the PC8260.

Table 2. Pinout

Pin Name	Ball
$\overline{BR}$	W5
$\overline{BG}$	F4
$\overline{ABB}$/IRQ2	E2
$\overline{TS}$	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5

Table 2. Pinout (Continued)

Pin Name	Ball
A31	R4
TTO	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
TBST	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
AACK	F3
ARTRY	E1
DBG	V1
$\overline{\text{DBB}}$/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11

Table 2. Pinout (Continued)

Pin Name	Ball
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A187
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18

Table 2. Pinout (Continued)

Pin Name	Ball
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DPO/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
IRQ1/DP1/$\overline{\text{EXT\_BG2}}$	A22
IRQ2/DP2/TLBISYNC/EXT_$\overline{\text{DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSEO	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20
$\overline{\text{PSDVAL}}$	V3
$\overline{\text{TA}}$	C22
$\overline{\text{TEA}}$	V5
$\overline{\text{GBL}}$/IRQ1	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	U3
$\overline{\text{L2\_HIT}}$/IRQ4	Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	U4
$\overline{\text{CPU\_DBG}}$	R2
$\overline{\text{CPU\_BR}}$	Y3
$\overline{\text{CS0}}$	F25
$\overline{\text{CS1}}$	C29
$\overline{\text{CS2}}$	E27
$\overline{\text{CS3}}$	E28
$\overline{\text{CS4}}$	F26
$\overline{\text{CS5}}$	F27
$\overline{\text{CS6}}$	F28
$\overline{\text{CS7}}$	G25
$\overline{\text{CS8}}$	D29
$\overline{\text{CS9}}$	E29
$\overline{\text{CS10}}$/$\overline{\text{BCTL1}}$	F29

Table 2. Pinout (Continued)

Pin Name	Ball
$\overline{\text{CS11}}$/APO	G28
BADDR27	T5
BADDR28	U1
ALE	T2
$\overline{\text{BCTL0}}$	A27
$\overline{\text{PWE0}}$/PSDQM0/PBS0	C25
$\overline{\text{PWE1}}$/PSDDQM1/PBS1	E24
$\overline{\text{PWE2}}$/PSDDQM2/PBS2	D24
$\overline{\text{PWE3}}$/PSDDQM3/PBS3	C24
$\overline{\text{PWE4}}$/PSDDQM4/PBS4	B26
$\overline{\text{PWE5}}$PSDDQM5/PBS5	A26
$\overline{\text{PWE6}}$/PSDDQM6/PBS6	B25
$\overline{\text{PWE7}}$/PSDDQM7/PBS7	A25
PSDA10/PGL0	E23
$\overline{\text{PSDWE}}$/PGPL1	B24
$\overline{\text{POE}}$/$\overline{\text{OSDRAS}}$/PGPL2	A24
$\overline{\text{PSDCAS}}$/PGPL3	B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22
$\overline{\text{LWE0}}$/LSDDQM0/LBS0	H28
$\overline{\text{LWE1}}$/LSDDQM1/LBS1	H27
$\overline{\text{LWE2}}$/LSDDQM2/LBS2	H26
$\overline{\text{LWE3}}$/LSDDQM3/LBS3	G29
LSDA10/LGPL0	D27
$\overline{\text{LSDWE}}$/LGPL1	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2	E26
$\overline{\text{LSDCAS}}$/LGPL3	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5	B27
$\overline{\text{LWR}}$	D28
L_A14	N27
L_A15/$\overline{\text{SMI}}$	T29
L_A16	R27
L_A17/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18	R29
L_A19	R28

Table 2. Pinout (Continued)

Pin Name	Ball
L_A20	W20
L_A21	P28
L_A22	N26
L_A23	AA27
L_A24	P29
L_A25	AA26
L_A26	N25
L_A27	AA25
L_A28/$\overline{\text{CORE\_SRESET}}$	AB29
L_A29	AB28
L_A30	P25
L_A31	AB27
LCL_D0	H29
LCL_D1	J29
LCL_D2	J28
LCL_D3	J27
LCL_D4	J26
LCL_D5	J25
LCL_D6	K25
LCL_D7	L29
LCL_D8	L27
LCL_D9	L26
LCL_D10	L25
LCL_D11	M29
LCL_D12	M28
LCL_D13	M27
LCL_D14	M26
LCL_D15	N29
LCL_D16	T25
LCL_D17	U27
LCL_D18	U26
LCL_D19	U25
LCL_D20	V29
LCL_D21	V28
LCL_D22	V27
LCL_D23	V26

Table 2. Pinout (Continued)

Pin Name	Ball
LCL_D24	W27
LCL_D25	W26
LCL_D26	W25
LCL_D27	Y29
LCL_D28	Y28
LCL_D29	Y25
LCL_D30	AA29
LCL_D31	AA28
LCL_DP0	L28
LCL_DP1	N28
LCL_DP2	T28
LCL_DP3	W28
$\overline{\text{IRQ0}}$/NMI_OUT	W28
$\overline{\text{IRQ7}}$INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
$\overline{\text{TRIS}}$	AB4
$\overline{\text{PORESET}}$	AG6
$\overline{\text{HRESET}}$	AH5
$\overline{\text{SRESET}}$	AF6
$\overline{\text{QREQ}}$	AA3
$\overline{\text{RSTCONF}}$	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ/FCC2_UTM_TXADDRS	AC29
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29
PA4/$\overline{\text{REJECT2}}$/FCC2/RXADDR1/$\overline{\text{DONE4}}$	AG28
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26

Table 2. Pinout (Continued)

Pin Name	Ball
PA6/L1RSYNCA1	AE24
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25
PA8/SMRSXD2/L1RXD0A1/L1RXDA1	AF23
PA6/L1RSYNCA1	AE24
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23
PA9/SMTXD2/L1TXD0A1	AH23
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7
PA28/$\overline{\text{FCC1\_UTM\_RXENB}}$/$\overline{\text{FCC1\_UTS\_RXENB}}$/FCC1_MII_TX_EN	AD5
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	AD3
PA31/$\overline{\text{FCC1\_UTM\_TXENB}}$/$\overline{\text{FCC1\_UTS\_TXENB}}$/FCC1_MII_COL	AB5
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24

Table 2. Pinout (Continued)

Pin Name	Ball
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22
PB13/FCC3_MII_COL/$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21
PB14/FCC3_MIL_TX_EN/RXD3/L1RXDC1	AG20
PB15/FCC3_MIL_TX_ER/RXD2/L1TXDC1	AF19
PB14/FCC3_MIL_RX_ER/L1CLKOA1/CLK18	AJ18
PB17FCC3_MIL_RX_DV/L1RQA1/CLK17	AJ17
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/ L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_L1RXD1A1/L1RXDD2	AH16
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1RXDD2	AE15
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/ L1RSYNCB2/FCC2_MII_TX_EN	AE2
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/1RXDB2	AC5
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29
PC2/$\overline{\text{FCC3\_CD}}$/FCC2_UT8_TXD3/$\overline{\text{DONE2}}$	AE29
PC3/$\overline{\text{FCC3\_CTS}}$/FCC2_UT8_TXD2/$\overline{\text{DACk2}}$/$\overline{\text{CTS4}}$	AE27
PC4/$\overline{\text{FCC2\_UTM\_RXENB}}$/$\overline{\text{FCC2\_UTS\_RXENB}}$/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24
PC6/$\overline{\text{FCC1\_CD}}$/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26
PC7/$\overline{\text{FCC1\_CTS}}$/$\overline{\text{L1RQC1}}$/ FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/FCC1_UTM_TSCLAV1	AJ25
PC8/$\overline{\text{CD4}}$/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22
PC9/$\overline{\text{CTS4}}$/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21
PC10/$\overline{\text{CD3}}$/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AE20
PC11/$\overline{\text{CTS3}}$/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19

Table 2. Pinout (Continued)

Pin Name	Ball
PC12/$\overline{\text{CD2}}$/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18
PC13/$\overline{\text{CTS2}}$/SLSN2/$\overline{\text{L1RQD1}}$/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18
PC14/$\overline{\text{CD1}}$/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16
PC16/CLK16/TIN3	AF15
PC17/CLK15/TIN4/BRGO8	AJ15
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14
PC19/CLK13/BRGO7	AG13
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12
PC21/CLK11/BTGO6	AJ11
PC22/CLK10/$\overline{\text{DONE1}}$	AG10
PC23/CLK9/BRGO*5*/$\overline{\text{DACK1}}$	AE10
PC24/FCC2_UT8_TXD3/CLK8/$\overline{\text{TOUT4}}$	AF9
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1
PC31/CLK1/BRGO1	AD1
PD4/BRGO8/L1TSYNCD1/L1GNTD1/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/FCC1_TXCLAV2	AF28
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23
PD12/SI1_L1ST2/L1RXDB1	AG23
PD13/SI1_L1ST1/L1RTDB1	AJ22
PD14/FCC1_UT16_RXD0/L1CLKOC2/L2CSCL	AE20
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/ SPICLK	AF16

Table 2. Pinout (Continued)

Pin Name	Ball
PD19/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_ TXCLAV3/SPISEL/BRGO1	AH15
PD20/$\overline{\text{RTS4}}$/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4
PD29/RTS1/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2	AG1
PD30/$\overline{\text{FCC2\_UTM\_TXENB}}$/$\overline{\text{FCC2\_UTS\_TXENB}}$/TXD1	AD4
PD31/RXD1	AD2
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
THERMAL0 (thermal ball)	AA1
THERMAL1 (thermal ball)	AG4
SPARE1	AE11
SPARE4	UF
SPARE5	AF25
SPARE6	V4

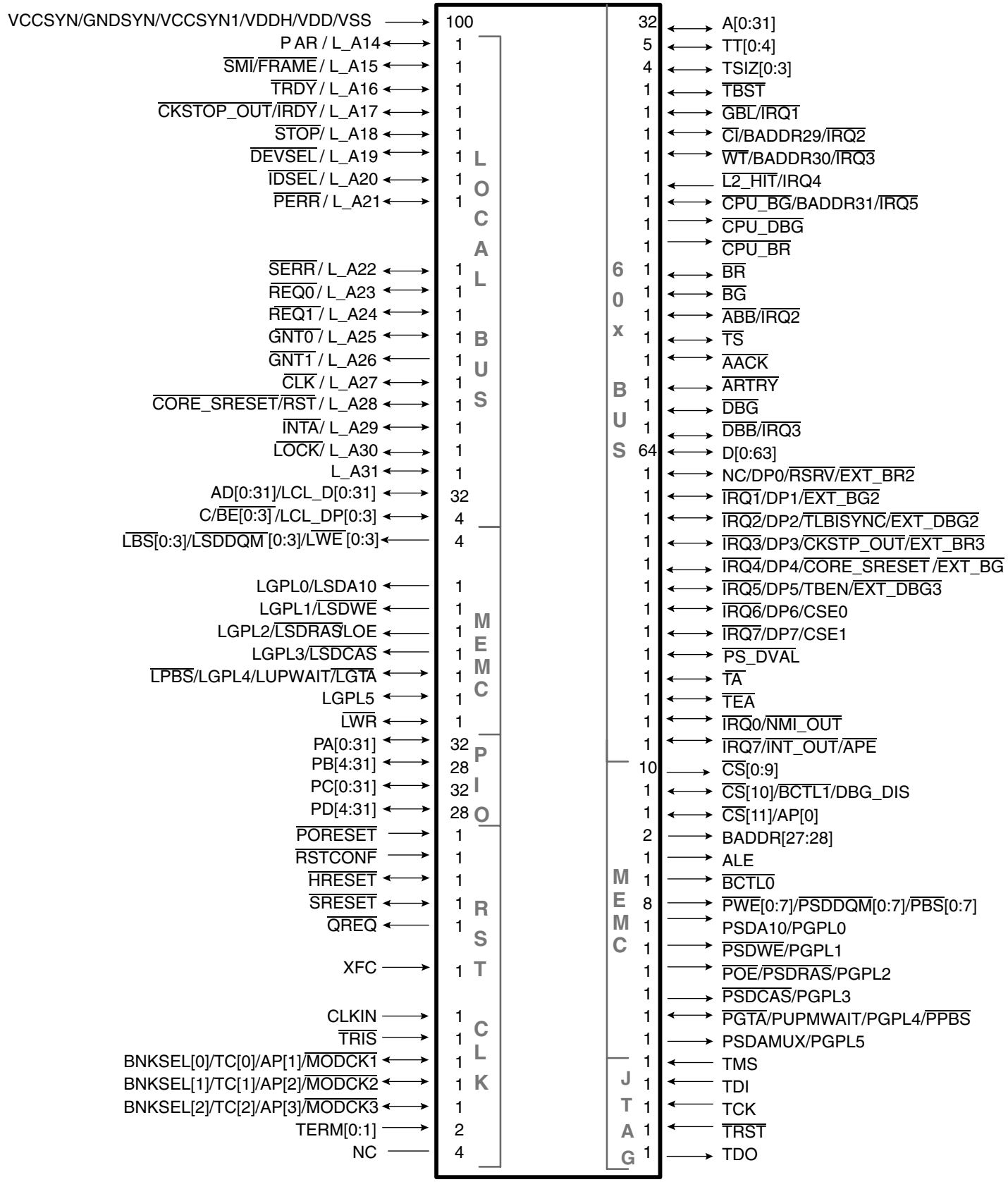
Table 2. Pinout (Continued)

Pin Name	Ball
I/O Power	AG21,AG14, AG8, AJ1, AJ2, AH1, AH2,AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7,C14,C16,C20,C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5

Note: Symbol Legend:

$\overline{\text{Overline}}$: Signals with overlines, such as $\overline{\text{TA}}$, are active low
UTM: Indicates that a signal is part of the UTOPIA master interface
UTS: Indicates that a signal is part of the UTOPIA slave interface
2UT8: Indicates that a signal is part of the 8-bit UTOPIA interface
UT16: Indicates that a signal is part of the 16-bit UTOPIA interface
MII: Indicates that a signal is part of the media independent interface

Figure 2. PowerQUICC II External Signals



Signal Descriptions

The PowerQUICC II system bus signals consist of all the lines that interface with the external bus. Many of these lines perform different functions, depending on how the user assigns them. Each signal's pin number can be found in Table 3.

Table 3. External Signals

Pin	Signal Name	Type	Description
$\overline{BR}$	60x Bus Request	I/O	This is an output when an external arbiter is used and an input when an internal arbiter is used. As an output, the PowerQUICC II asserts this pin to request ownership of the 60x bus. As an input, an external master should assert this pin to request 60x bus ownership from the internal arbiter.
$\overline{BG}$	60x BusGrant	I/O	This is an output when an internal arbiter is used and an input when an internal arbiter is used. As an output, the PowerQUICC II asserts this pin to grant 60x bus ownership to an external bus master. As an input, an external arbiter should assert this pin to grant 60x bus ownership to the PowerQUICC II.
$\overline{ABB}$ $\overline{IRQ2}$	60x Address Bus Busy	I/O	As an output the PowerQUICC II asserts this pin for the duration of the address bus tenure. Following an $\overline{AACK}$, which terminates the address bus tenure, the PowerQUICC II negates $\overline{ABB}$ for a fraction of a bus cycle and than stops driving this pin. As an input, the PowerQUICC II will not assume 60x bus ownership, as long as it senses this pin is asserted by an external 60x bus master.
	Interrupt Request 2	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{TS}$	T-S 60x Bus Transfer Start	I/O	Assertion of this pin signals the beginning of a new address bus tenure. The PowerQUICC II asserts this signal when one of its internal 60x bus masters (core, dma, PCI bridge) begins an address tenure. When the PowerQUICC II senses this pin being asserted by an external 60x bus master, it will respond to the address bus tenure as required (snoop if enabled, access internal PowerQUICC II resources and memory controller support).
A[0:31]	60x Address Bus	I/O	When the PowerQUICC II is in the external master bus mode, these pins function as the 60x address bus. The PowerQUICC II drives the address of its internal 60x bus masters and will respond to addresses generated by external 60x bus masters. When the PowerQUICC II is in the internal master bus mode, these pins are used as address lines connected to memory devices and controlled by the PowerQUICC II's memory controller.
TT[0:4]	60x Bus Transfer Type	I/O	The 60x bus master drives these pins during the address tenure to specify the type of the transaction.
$\overline{TBST}$	60x Bus Transfer Burst	I/O	The 60x bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers 4 double words).
TSIZ[0:3]	60x Transfer Size	I/O	The 60x bus master drives these pins with a value indicating the amount of bytes transferred in the current transaction.
$\overline{AACK}$	60x Address Acknowledge	I/O	A 60x bus slave asserts this signal to indicate that it has identified the address tenure. Assertion of this signal terminates the address tenure.
$\overline{ARTRY}$	60x Address Retry	I/O	Assertion of this signal indicates that the bus transaction should be retried by the 60x bus master. The PowerQUICC II asserts this signal to enforce data coherency with its internal cache and to prevent deadlock situations.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
$\overline{\text{DBG}}$	60x Data Bus Grant	I/O	This is an output when an internal arbiter is used and an input when an external arbiter is used. As an output, the PowerQUICC II asserts this pin to grant 60x data bus ownership to an external bus master. As an input, the external arbiter should assert this pin to grant 60x data bus ownership to the PowerQUICC II.
$\overline{\text{DBB}}$ $\overline{\text{IRQ3}}$	60x Data Bus Busy	I/O	As an output the PowerQUICC II asserts this pin for the duration of the data bus tenure. Following a $\overline{\text{TA}}$, which terminates the data bus tenure, the PowerQUICC II negates $\overline{\text{DBB}}$ for a fraction of a bus cycle and then stops driving this pin. As an input, the PowerQUICC II will not assume 60x data bus ownership, as long as it senses this pin is asserted by an external 60x bus master.
	Interrupt Request 3	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
D[0:63]	60x Data Bus	I/O	In write transactions, the 60x bus master drives the valid data on this bus. In read transactions, the 60x slave drives the valid data on this bus.
DP[0] $\overline{\text{RSRV}}$ $\overline{\text{EXT\_BR2}}$	60x Data Parity 0	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 0 pin should provide odd parity (odd number of 1's) on the group of signals that include data parity 0 and D[0:7].
	Reservation	O	The value driven on this output pin represents the state of the coherency bit in the reservation address register that is used by the lwarx and stwcx. instructions.
	External Bus Request 2	I	An external master should assert this pin to request 60xbus ownership from the internal arbiter.
$\overline{\text{IRQ1}}$ DP[1] $\overline{\text{EXT\_BG2}}$	Interrupt Request 1	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 1	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 1 pin should provide odd parity (odd number of 1's) on the group of signals that includes data parity 1 and D[8:15].
	External Bus Grant 2	O	The PowerQUICC II asserts this pin to grant 60x bus ownership to an external bus master.
$\overline{\text{IRQ2}}$ DP[2] $\overline{\text{TLBISYNC}}$ $\overline{\text{EXT\_DBG2}}$	Interrupt Request 2	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 2	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 2 pin should provide odd parity (odd number of 1's) on the group of signals that includes data parity 2 and S[16:23].
	TLB Sync:	I	This input pin can be used to synchronize 60x core instruction execution to hardware indications. Asserting this pin will force the core to stop instruction execution following a tlbsinc instruction execution. The core resumes instruction execution once this pin is negated.
	External Data Bus Grant 2	O	The PowerQUICC II asserts this pin to grant 60x data bus ownership to an external bus master.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
IRQ3 DP[3] CKSTP_OUT EXT_BR3	Interrupt Request 3	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 3	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 3 pin should provide odd parity (odd number of 1's) on the group of signals that includes data parity 3 and D[24:31].
	Checkstop Output	O	Assertion of this pin indicates that the core is in its checkstop mode.
	External Bus Request 3	I	An external master should assert this pin to request 60x bus ownership from the internal arbiter.
IRQ4 DP[4] CORE_SRESET EXT_BG3	Interrupt Request 4	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 4	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 4 pin should provide odd parity (odd number of 1's) on the group of signals that includes data parity 4 and D[32:39].
	Core system reset	I	Asserting this pin will force the core to branch to its reset vector.
	External Bus Grant 3	O	The PowerQUICC II asserts this pin to grant 60x data bus ownership to an external bus master.
IRQ5 DP[5] TBEN EXT_DBG3	Interrupt Request 5	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 5	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 5 pin should provide odd parity (odd number of 1's) on the group of signals that includes data parity 5 and D[40:47].
	Time Base Enable	I	This is a count enable input to the Time Base counter in the core.
	External Bus Grant3	O	The PowerQUICC II asserts this pin to grant 60x data bus ownership to an external bus master.
IRQ6 DP[6] CSE[0]	Interrupt Request 6	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 6	I/O	The 60x agent that drives the data bus, also drives the data parity signals. The value driven on the data parity 6 pin should provide odd parity (odd number of 1's) on the group of signals that include data parity 6 and D[48:55].
	Cache Set Entry 0	O	The cache set entry outputs from the core, represent the cache replacement set element for the current core transaction reloading into, or writing out of, the cache.
IRQ7 DP[7] CSE[1]	Interrupt Request 7	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	60x Data Parity 7	I/O	The 60x master or slave that drives the data bus, also drives the data parity signals. The value driven on the data parity 7pin should provide odd parity (odd number of 1's) on the group of signals that include data parity 7 and D[56:63].
	Cache Set Entry 1	O	The cache set entry outputs from the core, represent the cache replacement set element for the current core transaction reloading into, or writing out of, the cache.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
$\overline{\text{PSDVAL}}$	60x Data Valid	I/O	Assertion of the $\overline{\text{PSDVAL}}$ pin indicates that a data beat is valid on the data bus. The difference between the $\overline{\text{TA}}$ pin and the $\overline{\text{PSDVAL}}$ pin is that the $\overline{\text{TA}}$ pin is asserted to indicate 60x data transfer terminations, while the $\overline{\text{PSDVAL}}$ signal is asserted with each data beat movement. Thus, always when $\overline{\text{TA}}$ is asserted, $\overline{\text{PSDVAL}}$ will be asserted, but, when $\overline{\text{PSDVAL}}$ is asserted, $\overline{\text{TA}}$ is not necessarily asserted. For example, when a double-double word (2x64 bits) transfer is initiated by the SDMA to a memory device that has 32 bits port size, $\overline{\text{PSDVAL}}$ will be asserted 3 times without $\overline{\text{TA}}$ and, finally, both pins will be asserted to terminate the transfer.
$\overline{\text{TA}}$	Transfer Acknowledge	I/O	Assertion of the $\overline{\text{TA}}$ pin indicates that a 60x data beat is valid on the data bus. For 60x single beat transfers, assertion of this pin indicates the termination of the transfer. For 60x burst transfers, this pin will be asserted four times to indicate the transfer of four data beats, with the last assertion indicating the termination of the burst transfer.
$\overline{\text{TEA}}$	Transfer Error Acknowledge	I/O	Assertion of this pin indicates a bus error. 60x masters within the PowerQUICC II monitor the state of this pin. PowerQUICC II's internal bus monitor may assert this pin if it has identified a 60x transfer that is hung.
$\overline{\text{GBL}}$ $\overline{\text{IRQ1}}$	Global	I/O	When a 60x master within the chip initiates a bus transaction it drives this pin. When an external 60x master initiates a bus transaction, it should drive this pin. Assertion of this pin indicates that the transfer is global and it should be snooped by caches in the system. The PowerQUICC II data cache monitors the state of this pin.
	Interrupt Request 1	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{\text{CI}}$ BADDR29 $\overline{\text{IRQ2}}$	Cache Inhibit	O	This pin is an output pin. It is used for L2 cache control. For each BADDR29 PowerQUICC II 60x transaction initiated in the core, the state of this pin indicates if this transaction should be cached or not. Assertion of the CI pin indicates that the transaction should not be cached.
	Burst Address 29	O	There are five burst address output pins. These pins are outputs of the 60x memory controller. These pins are used in external master configuration and are connected directly to memory devices controlled by PowerQUICC II memory controller.
	Interrupt Request 2	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{\text{WT}}$ BADDR30 $\overline{\text{IRQ3}}$	Write Through	O	Output used for L2 cache control. For each core initiated PowerQUICC II 60x transaction, the state of this pin indicates if the transaction should be cached using write-through or copy-back mode. Assertion of $\overline{\text{WT}}$ indicates that the transaction should be cached using the write-through mode.
	Burst Address 30	O	There are five burst address output pins. These pins are outputs of the 60x memory controller. These pins are used in external master configuration and are connected directly to memory devices controlled by PowerQUICC II's memory controller.
	Interrupt Request 3	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
L2_HIT IRQ4	L2 Cache Hit	I	This pin is used for L2 cache control. Assertion of this pin indicates that the 60x transaction will be handled by the L2 cache. In this case, the memory controller will not start an access to the memory it controls.
	Interrupt Request 4	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
CPU_BG BADDR31 IRQ5	CPU BusGrant	O	The value of the60x core bus grant is driven on this pin for the BADDR31 use of an external L2 cache. The driven bus grant is non qualified. that is, in the IRQ5 case of external arbiter, the user should qualify this signal with the bus grant input to the PowerQUICC II before connecting it to the L2 Cache.
	Burst address 31	O	There are five burst address outputs of the 60x memory controller used in the external master configuration and are connected directly to the memory devices controlled by PowerQUICC II's memory controller.
	Interrupt Request 5	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
CPU_DBG	CPU Bus Data Bus Grant	O	The value of the 60x core data bus grant is driven on this pin for the use of an external L2 cache.
CPU_BR	CPU Bus Request	O	The value of the 60x core bus request is driven on this pin for the use of an external L2 cache.
CS[0:9]	Chip Select	O	These are output pins that enable specific memory devices or peripherals connected to PowerQUICC II buses.
CS[10] BCTL1 DBG_DIS	Chip Select	O	This is an output pin that enables specific memory devices or peripherals connected to PowerQUICC II buses.
	Buffer Control 1	O	Output signal whose function is to control buffers on the 60x data bus. This pin will usually be used with BCTL0. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See 6.5.1.8 SIU Module Configuration Register for details.
	Data Bus Grant Disable	O	This is an output when the PowerQUICC II is in external arbiter mode and an input when the PowerQUICC II is in internal arbiter mode. When this pin is asserted, the 60x bus arbiter should negate all of its DBG outputs to prevent data bus contention.
CS[11] AP[0]	Chip Select	O	Output that enables specific memory devices or peripherals connected to PowerQUICC II buses.
	Address Parity 0	I/O	The 60x master that drives the address bus, also drives the address parity signals. The value driven on address parity 0 pin should provide odd parity (odd number of 1's) on the group of signals that includes address parity 0 and A[0: 7].
BADDR[27:28]	Burst Address 27:28	O	There are five burst address output pins. These pins are outputs of the 60x memory controller. Used in external master configuration and connected directly to the memory devices controlled by PowerQUICC II's memory controller.
ALE	Address Latch Enable	O	This output pin controls the external address latch that should be used in external master 60x bus configuration.
BCTLO	Buffer Control 0		An Output whose function is to control buffers on the 60x data bus. This pin will usually be used with BCTL1 that is MUXed on CS10. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See 6.5.1.8 SIU Module Configuration Register for details.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
$\overline{\text{PWE}}[0:7]$ $\overline{\text{PSDDQM}}[0:7]$ $\overline{\text{PBS}}[0:7]$	60x Bus Write Enable	O	Outputs of the 60x bus GPCM, these pins select byte lanes for PSDDQM[0-7] write operations.
	60x Bus SDRAM DQM	O	The DQM pins are outputs of the SDRAM control machine. These pins select specific byte lanes of SRAM devices.
	60x Bus UPM Byte Select	O	The byte select pins are outputs of the UPM in the memory controller. They are used to select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
PSDA10 PGPLO	60x Bus SDRAM A10	O	An output from the 60x bus SDRAM controller, this pin is part of the address when a row address is driven and is part of the command when a column address is driven.
	60x Bus UPM General Purpose Line 0	O	This is one of six general purpose output lines from UPM. The values and timing of this pin are programmed in the UPM;
$\overline{\text{PSDWE}}$ PGPL1	60x Bus SDRAM Write Enable	O	An output from the 60x bus SDRAM controller. This pin should be connected to SRAM's WE input.
	60x Bus UPM General Purpose Line 1	O	This is one of six general purpose output lines from UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{POE}}$ $\overline{\text{PSDRAS}}$ PGPL2	60x Bus Output Enable	O	The output enable pin is an output of the 60x bus GPCM. This pin controls the output buffer of memory devices during read operations.
	60x Bus SDRAM RAS	O	Output from the 60x bus SDRAM controller. This pin should be connected to SDRAM's RAS input.
	60xBus UPM General Purpose Line 2.	O	This is one of six general purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDCAS}}$ PGPL3	60x bus SDRAM CAS	O	Output from the 60x bus SDRAM controller. This pin should be connected to SDRAM's CAS input.
	60x Bus UPM General Purpose line 3	O	This is one of six general purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PGTA}}$ PUPMWAIT PGPL4 $\overline{\text{PPBS}}$	60x GPCM TA	I	This input pin is used for transaction termination during GPCM operation. This pin requires external pull up resistor for proper operation.
	60x Bus UPM Wait	I	This is an input to the UPM. An external device may hold this pin low to force the UPM to wait until the device is ready for the continuation of the operation.
	60x Bus UPM General Purpose Line 4	O	This is one of six general purpose output lines from UPM. The values and timing of this pin are programmed in the UPM.
	60 x Bus Parity Byte Select	O	In systems in which data parity is stored in a separate chip, this output is used as the byte select for that chip.
PSDAMUX PGPL5	60x SDRAM Address Multiplexer	O	This output pin controls the 60x SDRAM address multiplexer when the PowerQUICC II is in external master mode.
	60x Bus General Purpose Line 5	O	This is one of six general purpose output lines from UPM. The values and timing of this pin are programmed in the UPM.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
$\overline{\text{LWE[0:3]}}$ $\overline{\text{LSDDQM[0:3]}}$ $\overline{\text{LBS[0:3]}}$	Local Bus Write Enable	O	The write enable pins are outputs of the Local bus GPCM. These pins select specific byte lanes for write operations.
	Local Bus SDRAM DQM	O	The DQM pins are outputs of the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
	Local Bus UPM byte select	O	The byte select pins are outputs of the UPM in the memory controller. They are used to select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
$\overline{\text{LSDA10}}$ LGPL0	Local Bus SDRAM A10	O	Output from the 60x bus SDRAM controller. This pin is part of the address when a row address is driven and is part of the command when a column address is driven.
	Local Bus UPM General Purpose Line 0	O	This is one of six general purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{LSDWE}}$ LGPL1	Local Bus SDRAM Write Enable	O	Output from the local bus SDRAM controller. This pin should be connected to SDRAM's WE input.
	Local Bus UPM General Purpose Line 1	O	This is one of six general purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{LOE}}$ $\overline{\text{LSDRAS}}$ LGPL2	Local Bus Output Enable	O	The output enable pin is an output of the Local bus GPCM. This pin controls the output buffer of memory devices during read operations.
	Local Bus SDRAM RAS	O	Output from the Local bus SDRAM controller. This pin should be connected to the SDRAM RAS input.
	Local bus UPM General Purpose Line 2	O	This is one of six general purpose output lines from UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{LSDCAS}}$ LGPL3	Local Bus SDRAM CAS	O	Output from the Local bus SDRAM controller. This pin should be connected to SDRAM's CAS input.
	Local Bus UPM General Purpose Line 3	O	This is one of six general purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{LGTA}}$ LUPWAIT LGPL4 $\overline{\text{LPBS}}$	Local Bus GPCM TA	I	This input pin is used for transaction termination during GPCM operation. This pin requires an external pull up resistor for proper operation.
	Local Bus UPM Wait	I	This is an input to the UPM. An external device may hold this pin low to force the UPM to wait until the device is ready for the continuation of the operation.
	Local Bus UPM General Purpose Line 4	O	This is one of six general purpose output lines from UPM. The values and timing of this pin is programmed in the UPM.
	Local Bus Parity Byte Select	O	In systems in which the data parity is stored in a separate chip, this output is used as the byte select for that chip.
$\overline{\text{LGPL5}}$	Local Bus UPM General Purpose Line 5	O	This is one of six general purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{LWR}}$	Local Write	O	The local write pin is an output from the local bus memory controller. It is used to distinguish between read and write transactions.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
L_A14 PCI_PAR	Local Bus Address 14	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Parity	I/O	Assertion of this pin indicates that odd parity is driven across AD[31:0] and C/BE3-C/BE0 during address and data phases. Negation of this pin indicates that even parity is driven across the AD31-AD0 and C/BE3-C/BE0 signals during address and data phases.
L_A15 FRAME SMI	Local Bus Address 15	O	In the local address bus, bit 14 FRAME is most significant and bit 31 is least significant.
	PCI Frame i	I/O	This pin is driven by the PowerQUICC II when its interface is the initiator of a PCI transfer. This pin is asserted to indicate that a PCI transfer is on going.
	System Management Interrupt	I	System management interrupt input to the core.
L-A16 PCI_TRDY	Local Bus Address 16	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Target Ready	I/O	This pin is driven by the PowerQUICC II when its PCI interface is the target of a PCI transfer. Assertion of this pin indicates that the PCI target is ready to send or accept a data beat.
L_A17 PCI_IRDY CKSTP_OUT	Local Bus Address 17	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Initiator Ready	I/O	This pin is driven by the PowerQUICC II when its PCI interface is the initiator of a PC] transfer. Assertion of this pin indicates that the PCI initiator is ready to send or accept a data beat.
	Checkstop Output	O	Assertion of CKSTP_OUT indicates the core is in checkstop mode.
L_A18 PCI_STOP	Local Bus Address 18	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Stop	I/O	This pin is driven by the PowerQUICC II when its PCI interface is the target of a PCI transfer. Assertion of this pin indicates that the PCI target is requesting to stop the PCI transfer.
L_A19 PCI_DEVESEL	Local Bus Address 19	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Device Select	I/O	This pin is driven by the PowerQUICC II when its PCI interface is the target of a PCI transfer. Assertion of this pin indicates that a PCI target has recognized a new PCI transfer with an address that belongs to the PCI target.
L_A20 PCI_IDSEL	Local Bus Address 20	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI ID select	I	Used to select PowerQUICC II's PCI interface during a PCI configuration cycle.
L_A21 PCI_PERR	Local Bus Address 21	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Parity Error	I/O	Assertion of this pin indicates that a parity error was detected during a PCI transfer.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
L_A22 $\overline{\text{PCI\_SERR}}$	Local Bus Address 22	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI System Error	I/O	Assertion of this pin indicates that a PCI system error was detected during a PCI transfer.
L_A23 $\overline{\text{PCI\_REQ0}}$	Local Bus Address 23	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Arbiter Request 0	I/O	When PowerQUICC II's internal PCI arbiter is used, this is an input pin. In this mode assertion of this pin indicates that an external PCI agent is requesting the PCI bus. When an external PCI arbiter is used, this is an output pin. In this mode assertion of this pin indicates that PowerQUICC II's PCI interface is requesting the PCI bus.
L_A24 $\overline{\text{PCI\_REQ1}}$	Local Bus Address 24	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Arbiter Request 1	I	When PowerQUICC II's internal PCI arbiter is used, assertion of this pin indicates that an external PCI agent is requesting the PCI bus.
L_A25 $\overline{\text{PCI\_GNT0}}$	Local Bus Address 25	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Arbiter Grant 0	I/O	When PowerQUICC II's internal PCI arbiter is used, this is an output pin. In this mode, assertion of this pin indicates that an external PCI agent that requested the PCI bus with the REQ0 pin is granted the bus. When an external PCI arbiter is used, this is an input pin. In this mode, assertion of this pin indicates that PowerQUICC II's PCI interface is granted the PCI bus.
L_A26 $\overline{\text{PCI\_GNT1}}$	Local Bus Address 26	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI Arbiter Grant 1	O	When PowerQUICC II's internal PCI arbiter is used, assertion of this pin indicates that the external PCI agent that requested the PCI bus with the REQ1 pin is granted the bus.
L_A27 CLKOUT	Local Bus Address 27	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	Clock Output pin	O	In a PCI system where PC8260's PCI interface is configured to operate from an external PCI clock, the 60x bus clock is driven on CLKOUT. In a PCI system where the PC8260's PCI interface is configured to generate the PCI clock, the PCI clock is driven on CLKOUT. The PCI clock frequency range is 25-66MHz.
L_A28 $\overline{\text{PCI\_RST}}$ $\overline{\text{CORE\_SRESET}}$	Local Bus Address 28	O	In the local address bus bit 14 is most significant and bit 31 is least significant.
	PCI Reset	I/O	When the PC8260 is the host in the PCI system, $\overline{\text{PCI\_RST}}$ is an output. When the PC8260is not the host of the PCI system, $\overline{\text{PCI\_RST}}$ is an input.
	Core System Reset	I	This an input to the core. When this input pin is asserted the core branches to its reset vector.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
L_A29 PCI_INTA	Local Bus Address 29	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	PCI INTA	I/O	When the PowerQUICC II is the host in the PCI system, this pin is an input for delivering PCI interrupts to the host. When the PowerQUICC II is not the host of the PCI system, this pin is an output used by the PowerQUICC II to signal an interrupt to the PCI host.
L_A30	Local Bus Address 30	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
L_A31 DLLSYNC	Local Bus Address 31	O	In the local address bus, bit 14 is most significant and bit 31 is least significant.
	DLL Synchronization	I	DLLSYNC is used to eliminate skew for the clock driven on CLKOUT.
LCL_D[0:31] PCI_AD[0:31]	Local Bus Data	I/O	In the local data bus, bit 0 is most significant and bit 31 is least significant.
	PCI Address Data	I/O	PCI bus address data input/output pins. In the PCI address data bus, bit 31 is most significant and bit 0 is least significant.
LCL_DP[0:3] PCI_C/BE[0:3]	Local Bus Data Parity	I/O	In local bus write operations the PowerQUICC II drives these pins. In local bus read operations the accessed device drives these pins. LCL_DP(0) is driven with a value that gives odd parity with LCL_D(0:7). LCL-DP(1) is driven with a value that gives odd parity with LCL_D(8:15). LCL_DP(2) is driven with a value that gives odd parity with LCL_D(16:23). LCL_DP(3) is driven with a value that gives odd parity with LCL_D(24:31)
	PCP Command/Byte Enable	I/O	The PowerQUICC II drives these pins when it is the initiator of a PCI transfer.
IRQ0 NMI_OUT	Interrupt request 0	I	This input is one of the eight external lines that can request (by means of the NMI-OUT internal interrupt controller) a service routine from the core.
	Non Maskable Interrupt Output	O	This is an output driven from PowerQUICC II's internal interrupt controller. Assertion of this output indicates that an unmasked interrupt is pending in PowerQUICC II's internal interrupt controller.
IRQ7 INT_OUT APE	Interrupt Request 7	I	This input is one of the eight external lines that can request (by means of the internal interrupt controller) a service routine from the core.
	Interrupt Output	O	This is an output driven from PowerQUICC II's internal interrupt controller. Assertion of this output indicates that an unmasked interrupt is pending in PowerQUICC II's internal interrupt controller.
	Address Parity Error	O	This output pin will be asserted when the PowerQUICC II's detects wrong parity driven on its address parity pins by an external master
TRST	Test Reset (JTAG)	I	This is the reset input to PowerQUICC II's JTAG/COP controller.
TCK	Test Clock (JTAG)	I	This pin provides the clock input for PowerQUICC II's JTAG/COP controller.
TMS	Test Mode Select (JTAG)	I	This pin controls the state of PowerQUICC II's JTAG/COP controller.
TDI	Test Data In (JTAG)	I	This pin is the data input to PowerQUICC II's JTAG/COP controller.
TDO	Test Data Out (JTAG)	O	This pin is the data output from PowerQUICC II's JTAG/COP controller.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
$\overline{\text{TRIS}}$	Three State	I	Asserting $\overline{\text{TRIS}}$ forces all other PowerQUICC II's pins to high impedance state.
$\overline{\text{PORESET}}$	Power-on Reset	I	When asserted, this input line causes the PowerQUICC II to enter power-on reset state.
$\overline{\text{HRESET}}$	Hard Reset	I/O	This open drain line, when asserted, causes the PowerQUICC II to enter hard reset state.
$\overline{\text{SRESET}}$	Soft Reset	I/O	This open drain line, when asserted, causes the PowerQUICC II to enter soft reset state.
$\overline{\text{QREQ}}$	Quiescent Request	O	This pin indicates that PowerQUICC II's internal core is about to enter its low power mode. In the PowerQUICC II, this pin will be typically used for debug purposes.
$\overline{\text{RSTCONF}}$	Reset Configuration	I	This input lien is sampled by the PowerQUICC II during the assertion of the HRESET signal. If the line is asserted, the configuration mode is sampled in the form of the hard reset configuration word driven on the data bus. When this line is negated, the default configuration mode is adopted by the PowerQUICC II. Notice that the initial base address of internal registers is determined in this sequence.
MODCK1 AP[1] TC[0] BNKSEL[0]	Clock Mode Input	I	Defines the operating mode of internal clock circuits.
	Address Parity 1	I/O	The 60x master that drives the address bus, also drives the address parity signals. The value driven on the address parity 1 pin should provide odd parity (odd number of 1's) on the group of signals that includes address parity 1 and [A8:15].
	Transfer Code 0	O	The transfer code output pins supply information that can be useful for debug purposes for each of the PowerQUICC II initiated bus transactions.
	Bank Select 0	O	The bank select outputs are used for selecting SDRAM bank when the PowerQUICC II is in 60x compatible bus mode.
MODCK2 AP[2] TC[1] BNKSEL[1]	Clock Mode Input	I	Defines the operating mode of internal clock circuits.
	Address Parity 2	I/O	The 60x master that drives the address bus, also drives the address parity signals. The value driven on the address parity 2 pin should provide odd parity (odd number of 1's) on the group of signals that includes address parity 2 and [A16:23].
	Transfer Code 1	O	The transfer code output pins supply information that can be useful for debug purposes for each of the PowerQUICC II initiated bus transactions.
	Bank Select 1	O	The bank select outputs are used for selecting SDRAM bank when the PowerQUICC II is in 60x compatible bus mode.

Table 3. External Signals (Continued)

Pin	Signal Name	Type	Description
MODCK3 AP[3] TC[2] BNKSEL[2]	Clock Mode Input	I	Defines the operating mode of internal clock circuits.
	Address Parity 3	I/O	The 60x master that drives the address bus, also drives the address parity signals. The value driven on the address parity 3 pin should provide odd parity (odd number of 1's) on the group of signals that includes address parity 3and [A24:314].
	Transfer Code 2	O	The transfer code output pins supply information that can be useful for debug purposes for each of the PowerQUICC II initiated bus transactions.
	Bank Select 2	O	The bank select outputs are used for selecting SDRAM bank when the PowerQUICC II is in 60x compatible bus mode.
XFC	External Filter Capacitance	I	Input connection for an external capacitor filter for PLL circuity.
CLKIN	Clock In	I	Primary clock input to PowerQUICC II's PLL.
PA[0:31]	Port A Bits 0:31	I/O	General Purpose I/O Port
PB[4:31]	Port B Bits 4:31	I/O	General Purpose I/O Port
PC[0:31]	Port C Bits 0:31	I/O	General Purpose I/O Port
PD[4:31]	Port D Bits 4:31	I/O	General Purpose I/O Port
VDD VDDH VCCSYN GNDSYN VCCSYN1	Power Supply Power Supply Power Supply Special Ground Power Supply		Power supply of the internal logic Power supply of the I/O buffers Power supply of the PLL circuity Special ground of the PLL circuity Power supply of the core's PLL circuity

Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.
2. SQ32S0100.0: Quality levels for supplied components.

Requirements

General

The microcircuits are in accordance with the applicable documents and as specified herein.

Terminal Connections

The terminal connections are shown in Table 2 on page 8.

Absolute Maximum Ratings

Table 4. Maximum Ratings

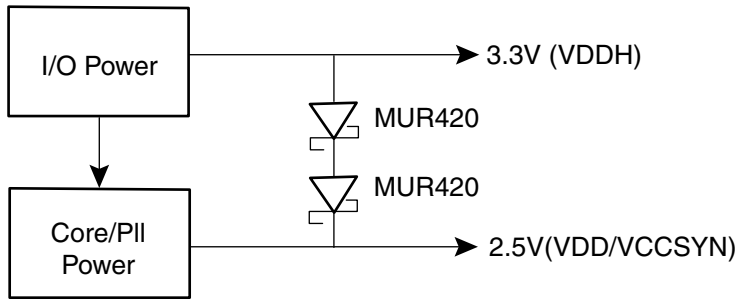
Symbol	Rating	Value	Unit
V_{DD}	Core Supply Voltage	-0.3/2.75	V
V_{CCSYN}	PLL Supply Voltage	-0.3/2.75	V
V_{DDH}	I/O Supply Voltage	-0.3/3.6	V
V_{IN}	Input Voltage	(GND-0.3)/3.6	V
T_{STG}	Storage Temperature Range	-65/+150	°C

Note: Absolute maximum ratings are stress ratings only. Functional operation (see Table on page 34) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

Warning

V_{IN} must not exceed V_{DDH} by more than 2.5V at any time, including during power-on reset. V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 1.6V at any time, including during power-on reset. V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4V at any time, including during power-on reset. It is recommended to use a bootstrap diode between the power rails, as shown in Figure 3.

Figure 3. Bootstrap Diodes for Power-up Sequencing



Select the bootstrap diodes so that a nominal V_{DD}/V_{CCSYN} is sourced from the V_{DDH} power supply until the V_{DD}/V_{CCSYN} power supply becomes active. In Figure 3, two MUR420 Schottky barrier diodes are connected in a series; each has a forward voltage (V_F) of 0.6V at high currents, and so provides a 1.2V drop, maintaining 2.1V on the 2.5V power line. Once the core/PLL power supply stabilizes at 2.5V, the bootstrap diode(s) will be reverse biased with negligible leakage current.

The forward voltage should be effective at the current levels needed by the processor, approximately 2-3 amps. That is, do not use diodes with only a nominal V_F which drops too low at high current.

Recommended Operating Conditions

Table 5. Recommended Operational Voltage Conditions

Symbol	Rating	2.5V Device	Unit
V_{DD}	Core Supply Voltage	2.4 / 2.7	V
V_{CCSYN}	PLL Supply Voltage	2.4 / 2.7	V
V_{DDH}	I/O Supply Voltage	3.15 / 3.465	V
V_{IN}	Input Voltage	GND -0.3 / 3.6	V
T_J	Junction Temperature	-55 / + 125	°C

Note: The recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or $V_{CC)}$.

Table 6. Thermal Characteristics

Symbol	Characteristics	Value	Unit	Air Flow
Θ_{JA}	Thermal Resistance for TBGA	13.5(1)	°C/W	NC(2)
Θ_{JA}		11.0(1)	°C/W	1 m/s
Θ_{JA}		10.8(3)	°C/W	NC
Θ_{JA}		8.5(3)	°C/W	1 m/s

Notes: 1. Assumes a single layer board with no thermal bias
2. Natural convection
3. Assumes a four layer board

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \bullet \Theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C
Q_{JA} = package thermal resistance, junction to ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{DD} \times V_{DD}$ Watts–chip internal power
$P_{I/O}$ = power dissipation on input and output pins–user determined

$$P_{I/O} < 0.3 \bullet P_{INT}$$

Can be neglected for most applications. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K / (T_J + 273\ °C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \Theta \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Layout Practices

Each V_{CC} pin on the PC8260 should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the PC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Electrical Characteristics

DC Electrical Specification

This section describes the DC electrical characteristics for the PC8260. The measurements in Table 7 assume the following system conditions:

T_C = -55°C to +125°C

V_{DD} = 2.0 ± 5% V_{DC}

V_{DDH} = 3.3 ± 5% V_{DC}

GND = 0 V_{DC}

The leakage current is measured for nominal V_{DDH} and V_{DD}, or both. V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by either +5% or -5%).

Table 7. DC Electrical Characteristics

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Voltage, All Inputs Except CLKIN	2.0	3.465	V
V_{IL}	Input Low Voltage	GND	0.8	V
V_{IHC}	CLKIN Input High Voltage	2.4	3.465	V
V_{ILC}	CLKIN Input Low Voltage	GND	0.4	V
I_{IN}	Input Leakage Current, V_{IN}= V_{DDH}		10	µA
I_{OZ}	Hi-Z (off state) Leakage Current, V_{IN} = V_{DDH}		10	µA
I_L	Signal Low Input Current, V_{IL}= 0.8V	TBD	TBD	µA
I_H	Signal High Input Current, V_{IH} = 2.0V	TBD	TBD	µA
V_{OH}	Output High Voltage, I_{OH} = -2 mA Except XFC, and Open Drain Pins	2.4		V

Table 7. DC Electrical Characteristics (Continued)

Symbol	Characteristic	Min	Max	Unit
V_{OL}	I_{OL} = 7.0 mA $\overline{BR}$ $\overline{BG}$ $\overline{ABB}$/$\overline{IRQ2}$ $\overline{TS}$ A[0:31] TT[0:4] TBST TSIZE[0:3] $\overline{AACK}$ $\overline{ARTRY}$ $\overline{DBG}$ $\overline{DBB}$/$\overline{IRQ3}$ D[0:63] DP(0)/$\overline{RSRV}$ DP(1)/$\overline{IRQ1}$ DP(2)/$\overline{TLBISYNC}$/$\overline{IRQ2}$ DP(3)/$\overline{IRQ3}$ DP(4)/$\overline{IRQ4}$ DP(5)/TBEN/$\overline{IRQ5}$ DP(6)/CSE(0)/$\overline{IRQ6}$ DP(7)/CSE(1)/$\overline{IRQ7}$ $\overline{PSDVAL}$ $\overline{TA}$ TEA $\overline{GBL}$/$\overline{IRQ1}$ $\overline{CI}$/BADDR29/$\overline{IRQ2}$ $\overline{WT}$/BADDR30/$\overline{IRQ3}$ $\overline{L2\_HIT}$/$\overline{IRQ4}$ $\overline{CPU\_BG}$/BADDR31/$\overline{IRQ5}$ CPU_DBG CPU_BR $\overline{IRQ0}$/$\overline{NMI\_OUT}$ $\overline{IRQ7}$/$\overline{INT\_OUT}$/$\overline{APE}$ $\overline{PORESET}$ $\overline{SRESET}$ $\overline{RSTCONF}$ $\overline{QREQ}$		0.4	V

Table 7. DC Electrical Characteristics (Continued)

Symbol	Characteristic	Min	Max	Unit
V_{OL}	I_{OL} = 5.3 mA		0.4	V
	$\overline{CS}$[0:9]			
	$\overline{CS}$(10)/$\overline{BCTL1}$			
	$\overline{CS}$(11)/AP(0)			
	BADDR[27–28]			
	ALE			
	$\overline{BCTL0}$			
	$\overline{PWE}$(0:7)/$\overline{PSDDQM}$(0:7)/$\overline{PBS}$(0:7)			
	PSDA10/PGPL0			
	$\overline{PSDWE}$/PGPL1			
	POE/PSDRAS/PGPL2			
	PSDCAS/PGPL3			
	PGTA/PUPMWAIT/PGPL4/PPBS			
	PSDAMUX/PGPL5			
	LWE[0–3]LSDDQM(0:3)/LBS([0–3]			
	LSDA10/LGPL0			
	LSDWE/LGPL1			
	LOE/LSDRAS/LGPL2			
	LSDCAS/LGPL3			
	LGTA/LUPMWAIT/LGPL4/LPBS			
	LGPL5			
	$\overline{LWR}$			
	$\overline{MODCK1}$/$\overline{AP}$(1)/$\overline{TC}$(0)/$\overline{BNKSEL}$(0)			
	MODCK2/AP(2)/TC(1)/BNKSEL(1)			
	MODCK3/AP(3)/TC(2)/BNKSEL(2)			
	I_{OL} = 3.2 mA			
	L_A14			
	L_A15/SMI			
	L_A16			
	L_A17/CKSTP_OUT			
	L_A18			
	L_A19			
	L_A20			
	L_A21			
	L_A22			
	L_A23			
	L_A24			
	L_A25			
	L_A26			
	L_A27			
	L_A28/$\overline{CORE\_SRESET}$			

Table 7. DC Electrical Characteristics (Continued)

Symbol	Characteristic	Min	Max	Unit
VOL	L_A29 L_A30 L_A31 LCL_D(0:31) LCL_DP(0:3) PA[0:31] PB[4:31] PC[0:31] PD[4:31] TDO		0.4	V

AC Electrical Specifications

Included in this section are illustrations and tables of clock diagrams, signals, and CPM outputs and inputs. Note that AC timings are based on a 50 pF load. Typical output buffer impedances are shown in Table 8.

Table 8. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory Controller	40
Parallel I/O	46
PCI	25

Note: These are typical values at 65°C. The impedance may vary by ± 25% with process and temperature.

Although the specifications generally refer to the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 4. FCC External Clock Diagram

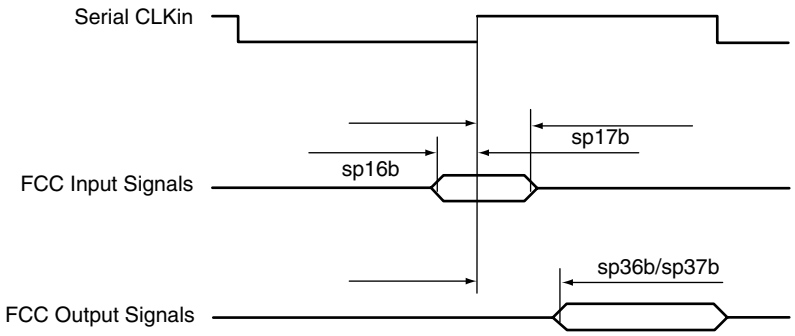


Figure 5. FCC Internal Clock Diagram

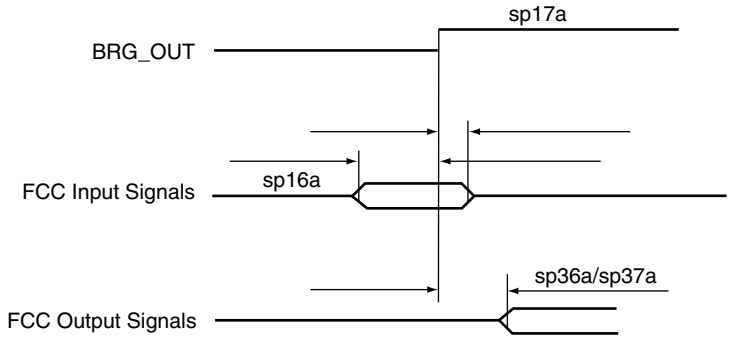


Figure 6. SCC/SMCSPI/I^{2}C External Clock

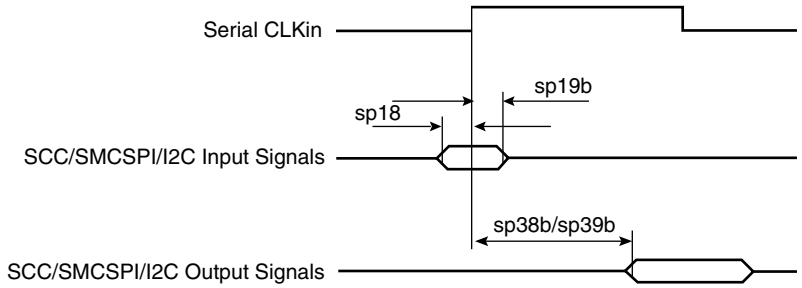


Figure 7. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

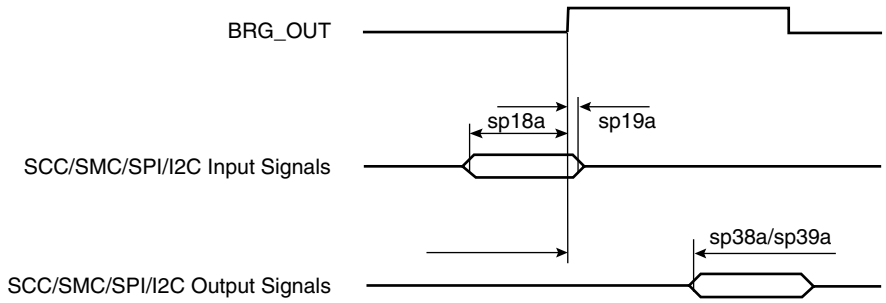


Figure 8. PIO, Timer and DMA Signal Diagram

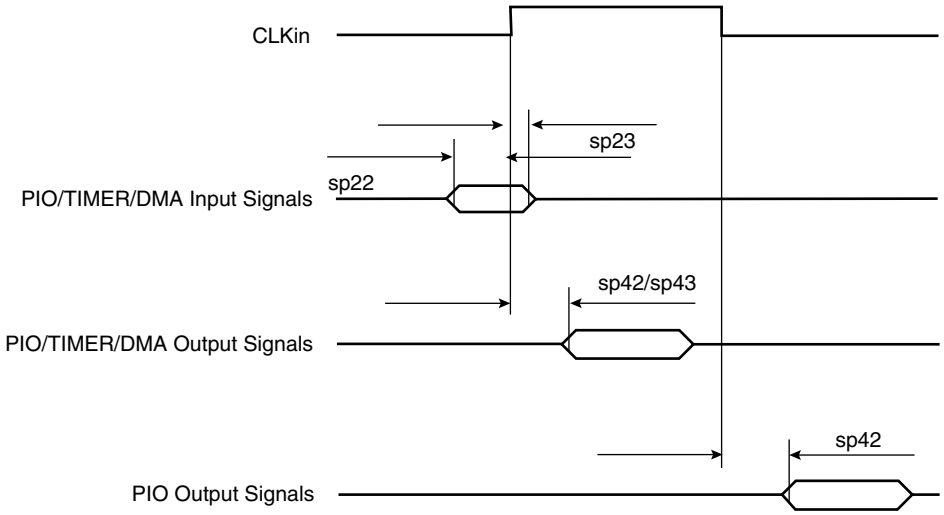


Figure 9. TDM Signal Diagram

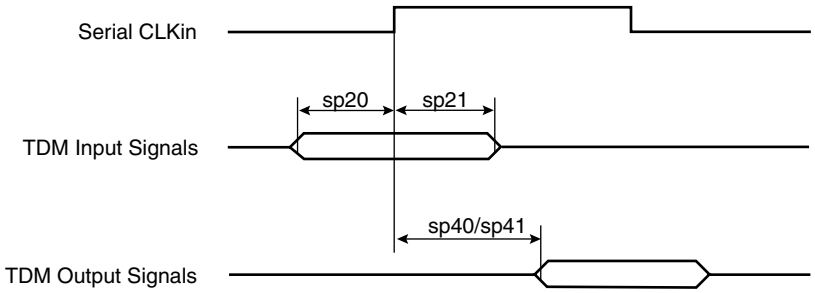


Table 9. AC Characteristics for CPM Outputs

Spec_num	Characteristics	Max Delay (ns)	Min Delay (ns)
sp36a/sp37a	FCC Outputs – Internal clock (NMSI)	6	0
sp36b/sp37b	FCC Outputs – External clock (NMSI)	18	2
sp40/sp41	TDM Outputs	35	5
sp38a/sp39a	SCC/SMC/SPI/I2C Outputs – Internal Clock (NMSI)	20	0
sp38b/sp39b	EX_SCC/SMC/SPI/I2C Outputs – External Clock (NMSI)	30	0
sp42/sp43	PIO/TIMER/DMA Outputs	14	1

Note: Output specifications are measured from the 1.4V level of the rising edge of CLKIN to the TTL level (0.8 or 2.0V) of the signal. Timing is measured at the pin.

Table 10. AC Characteristics for CPM Inputs

Spec_num	Characteristics	Setup (ns)	Hold (ns)
sp16a/sp17a	FCC Inputs – Internal clock (NMSI)	10	0
sp16b/sp17b	FCC Inputs – External clock (NMSI)	5	3
sp20/sp21	TDM Inputs	20	20
sp18a/sp19a	ISCC/SMC/SPI/I2C Inputs – Internal Clock (NMSI)	20	0
sp18b/sp19b	SCC/SMC/SPI/I2C Inputs – External Clock (NMSI)	5	5
sp22/sp23	PIO/TIMER/DMA Outputs	10	3

Note: Input specifications are measured from the TTL level (0.8 or 2.0V) of the signal to the 1.4 level of the rising edge of CLKIN. Timing is measured at the pin.

Figure 10. Interaction of Bus Signals

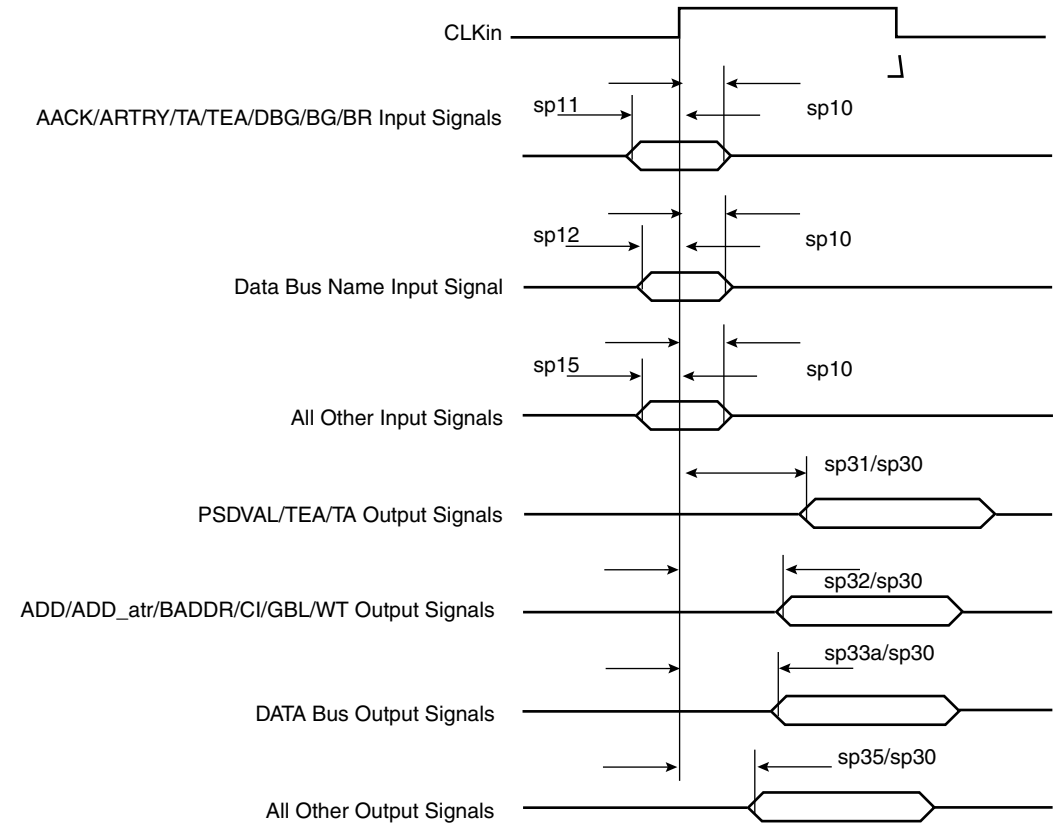


Figure 11. ECC Mode Diagram

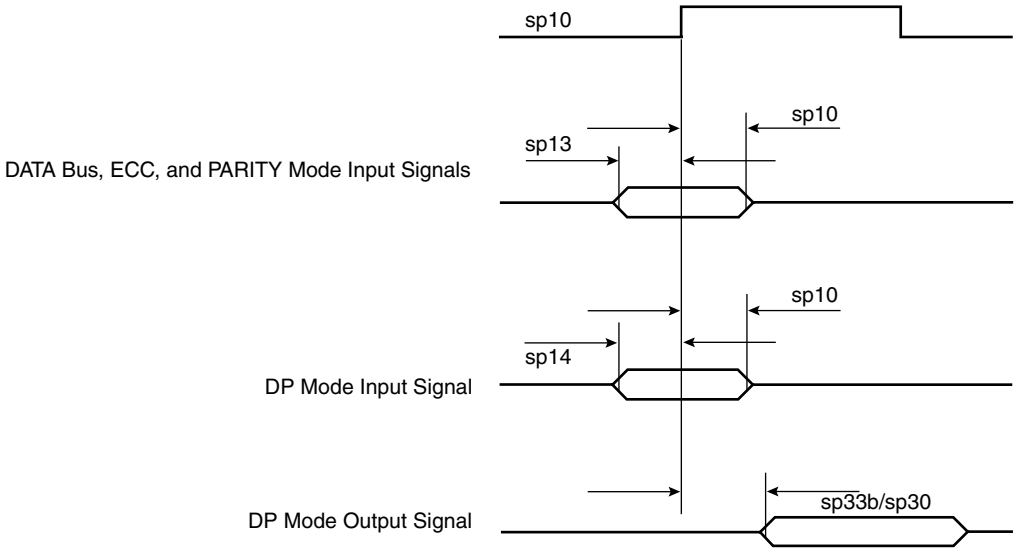


Figure 12. MEMC Mode Diagram

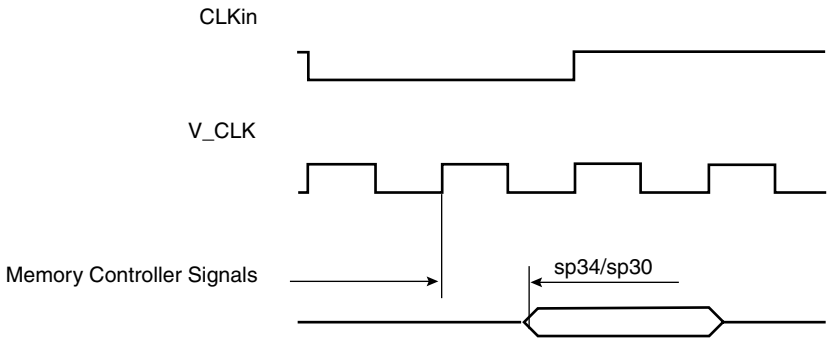
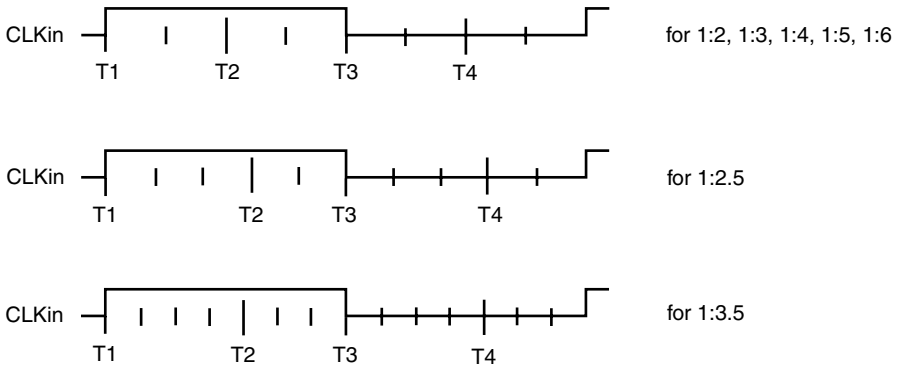


Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Radio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Note: Generally, all PC8260 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of CLKin (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Figure 13. Internal Tick Spacing for Memory Controller Signals



Note: The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming. The AC specifications are relative to the internal tick. Note that SDRAM machine outputs change only on the CLKin's rising edge.

Table 12. AC Characteristics for SIU Inputs

Spec_num	Characteristics	Setup (ns)	Hold (ns)
sp11/sp10	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$	6	1
sp12/sp10	Data Bus in Normal mode	5	1
sp13sp10	Data Bus in ECC and PARITY Modes	8	1
sp14/sp10	DP pins	8	1
sp15/sp10	All Other Pins	5	1

Notes: 1. Input specifications are measured from TTL level (0.8 or 2.0V) of the signal to the 1.4 level of the rising edge of CLKIN.
2. Timings are measured at the pins.

Table 13. AC Characteristics for SIU Outputs

Spec_num	Characteristics	Max Delay (ns)	Min Delay (ns)
sp31/sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	10	1
sp32/sp30	ADD/ADD_atr./BADDR/CIGBL/WT	8	1
sp33a/sp30	Data Bus	8	1
sp33b/sp30	DP	12	1
sp34/sp10	Memc Signals/ALE	6	1
sp35/sp10	All Other Signals	7	1

Notes: 1. Output specifications are measured from the 1.4V level of the rising edge of CLKIN to the TTL level (0.8 or 2.0V) of the signal.
2. Timings are measured at the pin.

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1:3] pins are sampled while HRESET is asserted. Table 14 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin (RSTCONF) and driving four pins on the data bus.

Table 14. Clock Default Modes

MODCK[1–3]	Input Clock Frequency (MH)z	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
000	33	3	100	4	133
001	33	3	100	5	166
010	33	4	133	4	133
011	33	4	133	5	166
100	66	2	133	2.5	166
101	66	2	133	3	200
110	66	2.5	166	2.5	166
111	66	2.5	166	3	200

Table 15. Clock Configuration Modes

MODCK_H–MODCK[1–3]	Input Clock Frequency (MHz)	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
0001_000	33	2	66	4	133
0001_001	33	2	66	5	166
0001_010	33	2	66	6	200
0001_011	33	2	66	7	233
0001_100	33	2	66	8	266
0001_101	33	3	100	4	133
0001_110	33	3	100	5	166
0001_111	33	3	100	6	200
0010_000	33	3	100	7	233
0010_001	33	3	100	8	266
0010_010	33	4	133	4	133
0010_011	33	4	133	5	166
0010_100	33	4	133	6	200
0010_101	33	4	133	7	233
0010_110	33	4	133	8	266

Table 15. Clock Configuration Modes (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency (MHz)	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
0010_111	33	5	166	4	133
0011_000	33	5	166	5	166
0011_001	33	5	166	6	200
0011_010	33	5	166	7	233
0011_011	33	5	166	8	266
0011_100	33	6	200	4	133
0011_101	33	6	200	5	166
0011_110	33	6	200	6	200
0011_111	33	6	200	7	233
0100_000	33	6	200	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66	2	133	2	133
0101_110	66	2	133	2.5	166
0101_111	66	2	133	3	200
0110_000	66	2	133	3.5	233
0110_001	66	2	133	4	266
0110_010	66	2	133	4.5	300
0110_011	66	2.5	166	2	133
0110_100	66	2.5	166	2.5	166

Table 15. Clock Configuration Modes (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency (MHz)	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
0110_101	66	2.5	166	3	200
0110_110	66	2.5	166	3.5	233
0110_111	66	2.5	166	4	266
0111_000	66	2.5	166	4.5	300
0111_001	66	3	200	2	133
0111_010	66	3	200	2.5	166
0110_101	66	2.5	166	3	200
0110_110	66	2.5	166	3.5	233
0110_111	66	2.5	166	4	266
0111_000	66	2.5	166	4.5	300
0111_001	66	3	200	2	133
0111_010	66	3	200	2.5	166
0111_011	66	3	200	3	200
0111_100	66	3	200	3.5	233
0111_101	66	3	200	4	266
0111_110	66	3	200	4.5	300
0111_111	66	3.5	233	2	133
1000_000	66	3.5	233	2.5	166
1000_001	66	3.5	233	3	200
1000_010	66	3.5	233	3.5	233
1000_011	66	3.5	233	4	266
1000_100	66	3.5	233	4.5	300

Notes:
1. This table describes all possible clock configurations when using the hard reset configuration sequence. Note that clock configuration changes only after POR is asserted.
2. Because of speed dependencies, not all of the possible configurations in this table may be applicable.
3. The 66 MHz configurations are required for input clock frequencies higher than 50 MHz. 33 MHz configurations are required for input clock frequencies below 50 MHz.
4. The user should choose the input clock frequency, and the multiplication factor of the CPM so that the frequency of the CPM will be between 50 MHz and 166 MHz for a 2V part, and between 66 MHz and 233 MHz for a 2.5V part.

Status

Table 16. Datasheet Status

Datasheet Status		Validity
Objective Specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Valid before design phase
Target Specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary Specification ∝ Site	This datasheet contains preliminary data. Additional data may be published later. This could include simulation results.	Valid before the characterization phase
Preliminary Specification β Site	This datasheet also contains characterization results.	Valid before the industrialization phase.
Product Specification	This datasheet contains final product specifications.	Valid for production purposes

Limiting Values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

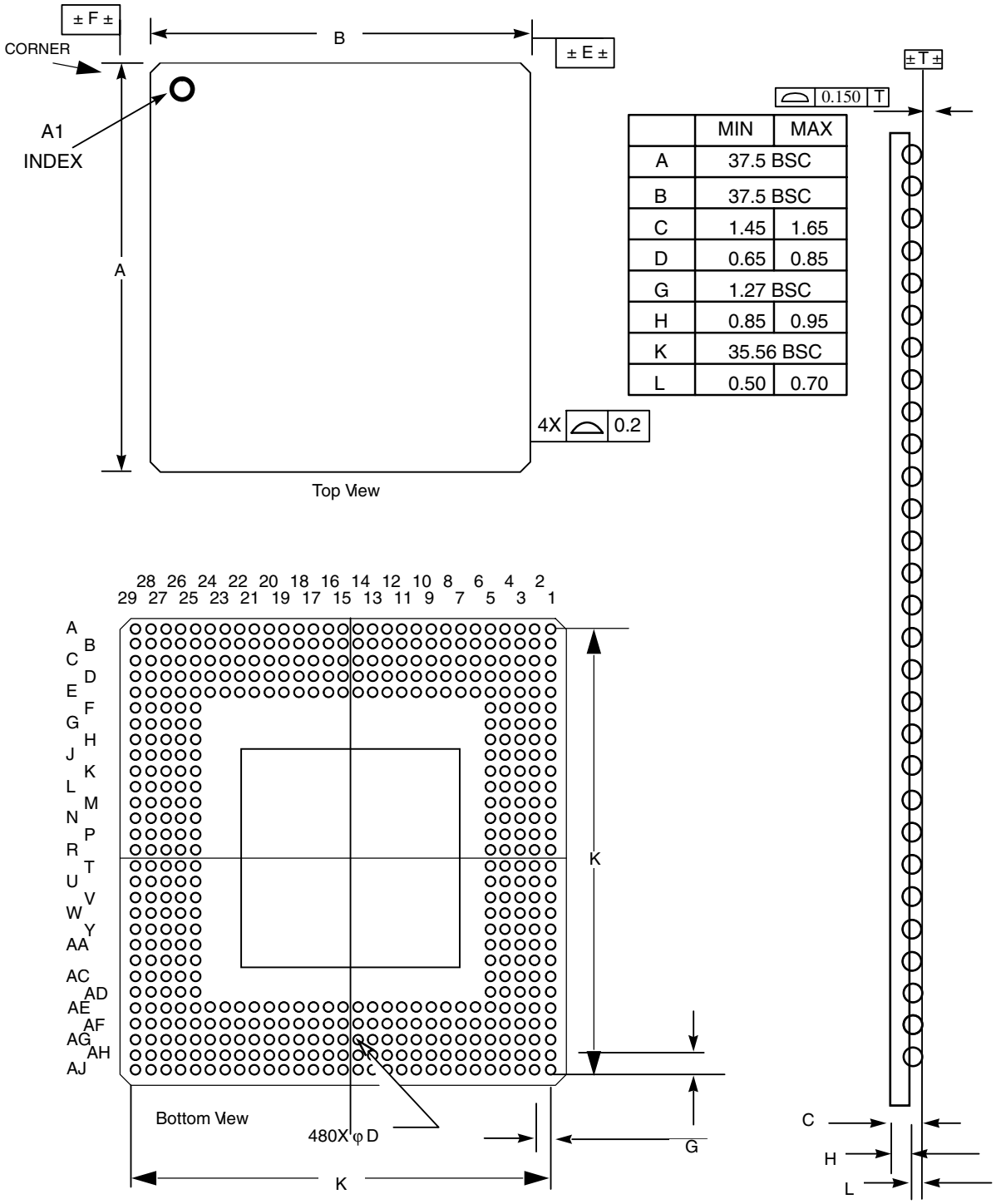
Application Information

Where application information is given, it is advisory and does not form part of the specification.

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. ATMEL-Grenoble customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel-Grenoble for any damages resulting from such improper use or sale.

Package Dimensions TBGA480



	MIN	MAX
A	37.5 BSC	
B	37.5 BSC	
C	1.45	1.65
D	0.65	0.85
G	1.27 BSC	
H	0.85	0.95
K	35.56 BSC	
L	0.50	0.70

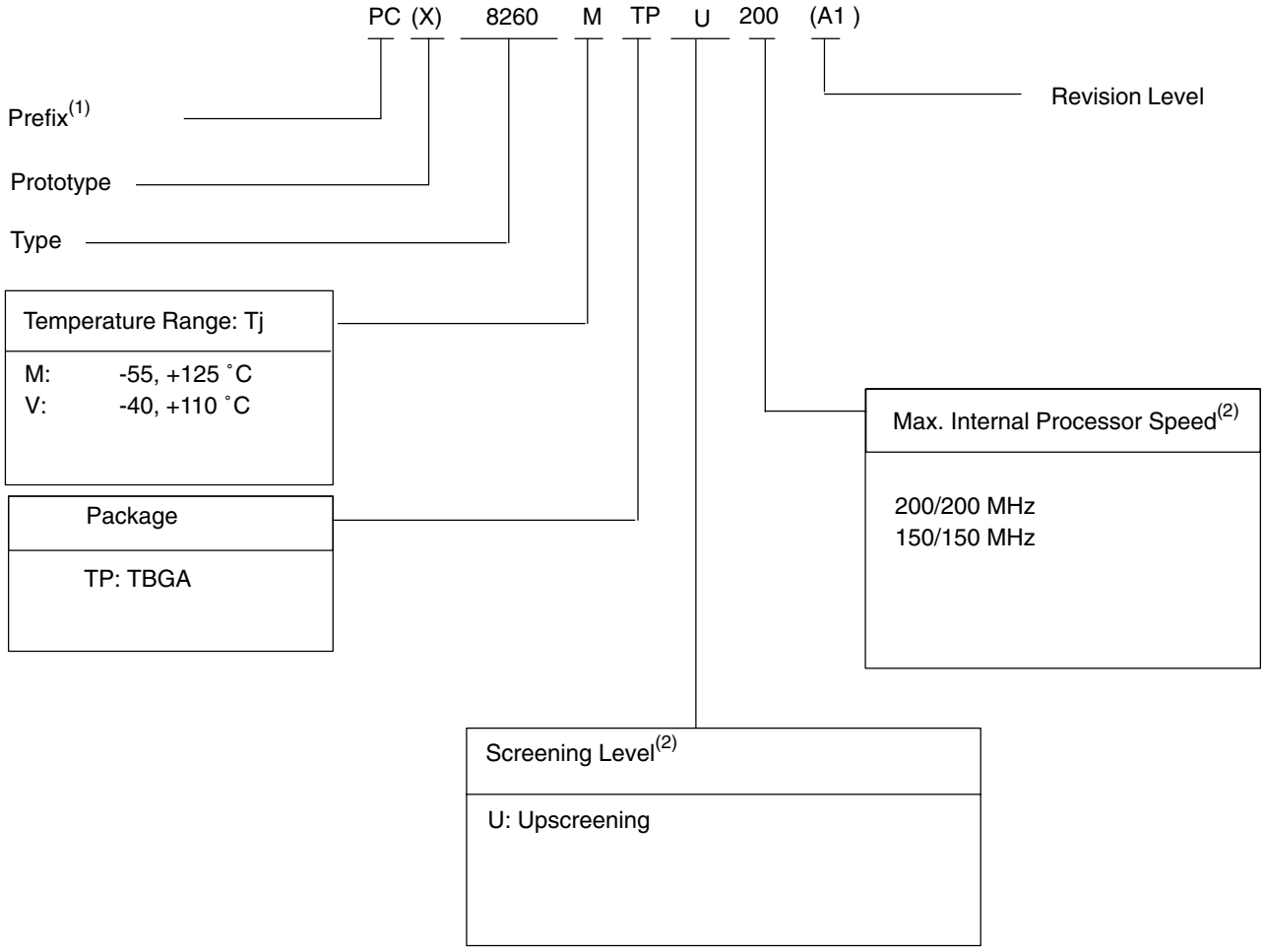
All measurements are in mm.

Notes:

1. Dimensions and tolerancing per asme Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter. Parallel to primary datum A.
4. Primary datum A and the seating plane are defined by the spherical crowns of the solder balls.

Ordering Information

Revision A1



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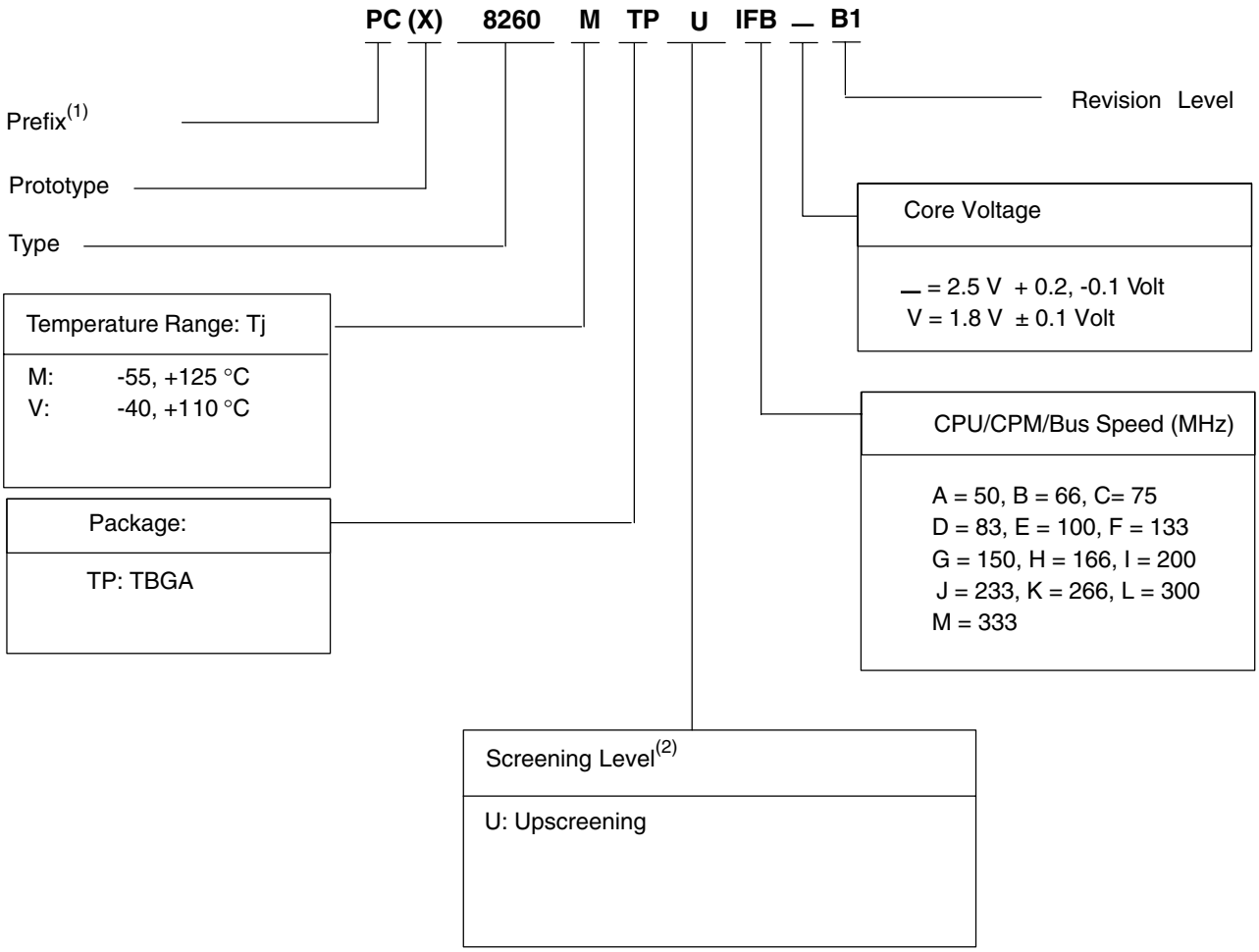
Revision B1 and Above



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