Converting PI6C2310 for 2.5V Outputs

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Introduction

Pericom's versatile PI6C2310 clock driver has a wide operating frequency range: from 10MHz up to 160MHz. It is design to provide necessary PCI & PCIX frequencies with an input of 33.33MHz or 66.67MHz. However, its application is not limited to PCI or PCIX because it can also be used as a generic frequency multiplier and divider. Low jitter, low skew, and low propagation delay characteristics also make it ideal for networking and communication applications.

Unique to the PI6C2310, each bank of two output drivers are powered by a separate V_{CC} pin. Thus each bank interface is independent of the other. OUT0 (pin 21) and OUT1 (pin 20) are powered by V_{CC} pin 22. OUT2 (pin 17) and OUT3 (pin 16) are powered by V_{CC} pin 15. Each output bank can be powered independently. For example, applying 3.3V to pin 22 causes OUT0 and OUT1 to be 3.3V LVCMOS outputs, regardless of the other V_{CC}/AV_{CC}. At the same time, if pin 15 is connected to a 2.5V power supply, OUT2 & OUT3 outputs will be 2.5V LVCMOS compatible.

To connect all PI6C2310 outputs (OUT[0..3]) to a 2.5V interface, both V_{CC} pins (pin 15 and pin 22) should be connected to a 2.5V power source.

Bypass capacitor value:

The value of C1 & C2 bypass capacitors depends on the output loading and edge rate specification.

For example, to drive a 10pF load from 0.4V to 2.4V with 2ns edge rate, the transient current will be:

I = C* (dV/dt)
I = 10pF * (2.4-0.4)V/2ns
I = 10mA per output

For 4 outputs (OUT[0..3]) = 40mA

To tolerate 100mV voltage dip @ a 2ns edge rate, the value of the bypass capacitor is:

C = I * (dt/dV)
C = 40mA * 2ns / 100mV
C = 0.8nF

Thus C1, C3 = 0.001µF (rounded up); C2, C4 are no connect

Note:

1. Other V_{CC}/AV_{CC} (pins 2, 10, and 23) have to be connected to a 3.3V power supply.
2. Tsk and Tskpp between banks will vary from the specification if they are powered differently, i.e. 2.5V & 3.3V.