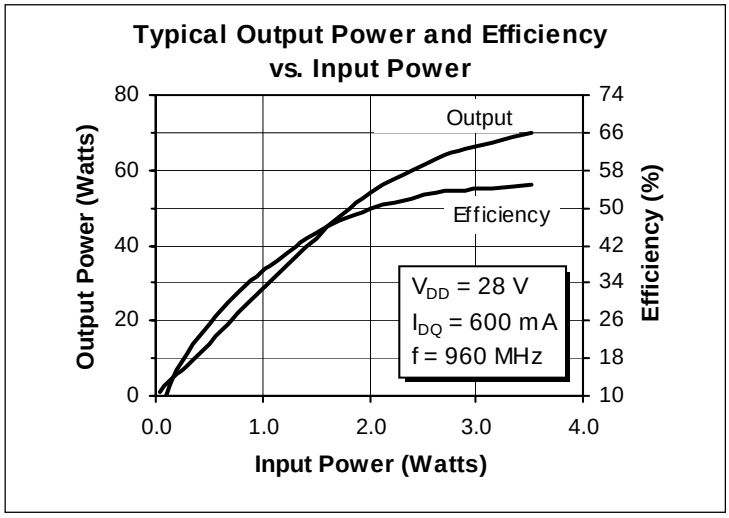
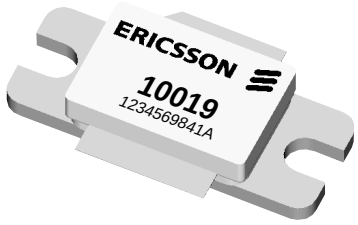
PTF 10019
70 Watts, 860–960 MHz
GOLDMOS Field Effect Transistor

Description

The PTF 10019 is an internally matched, 70–watt *GOLDMOS* FET intended for cellular, GSM and D-AMPS applications from 860 to 960 MHz. This device operates at 50% efficiency with 14.5 dB gain. Nitride surface passivation and full gold metallization ensure excellent device lifetime and reliability.

- ***INTERNALLY MATCHED***
- **Performance at 960 MHz, 28 Volts**
  - Output Power = 70 Watts
  - Power Gain = 14.5 dB Typ
  - Efficiency = 50% Typ
- **Full Gold Metallization**
- **Silicon Nitride Passivated**
- **Excellent Thermal Stability**
- **100% Lot Traceability**





Package 20237

RF Specifications (100% Tested)

Characteristic	Symbol	Min	Typ	Max	Units
Gain (V_{DD} = 28 V, P_{OUT} = 70 W, I_{DQ} = 600 mA, f = 960 MHz)	G_{pe}	13.0	14.5	—	dB
Power Output at 1 dB Compression (V_{DD} = 28 V, I_{DQ} = 600 mA, f = 960 MHz)	P-1dB	70	75	—	Watts
Drain Efficiency (V_{DD} = 28 V, P_{OUT} = 70 W, I_{DQ} = 600 mA, f = 960 MHz)	η	45	50	—	%
Load Mismatch Tolerance (V_{DD} = 28 V, P_{OUT} = 70 W, I_{DQ} = 600 mA, f = 960 MHz —all phase angles at frequency of test)	Y	—	—	10:1	—

All published data at T_{CASE} = 25°C unless otherwise indicated.

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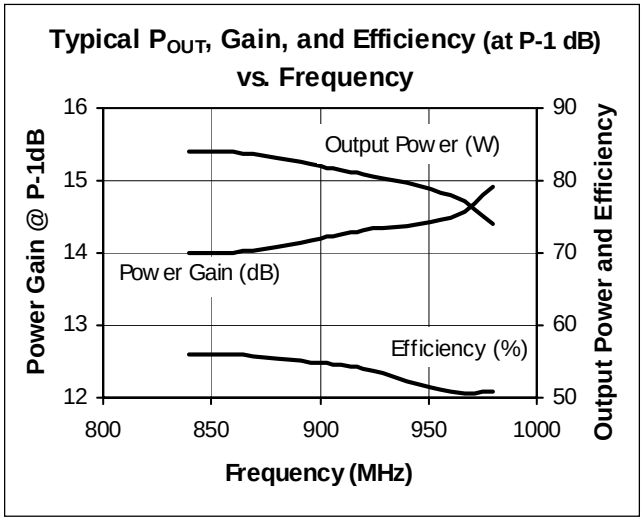
Electrical Characteristics (100% Tested)

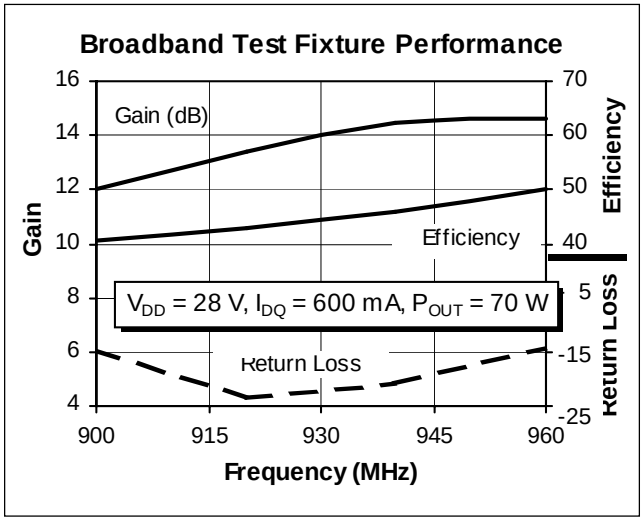
Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 25 mA	$V_{(BR)DSS}$	65	—	—	Volts
Drain-Source Leakage Current	V_{DS} = 26 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	mA
Gate Threshold Voltage	V_{DS} = 10 V, I_D = 75 mA	$V_{GS(th)}$	3.0	—	5.0	Volts
Forward Transconductance	V_{DS} = 10 V, I_D = 3 A	g_{fs}	—	3.0	—	Siemens

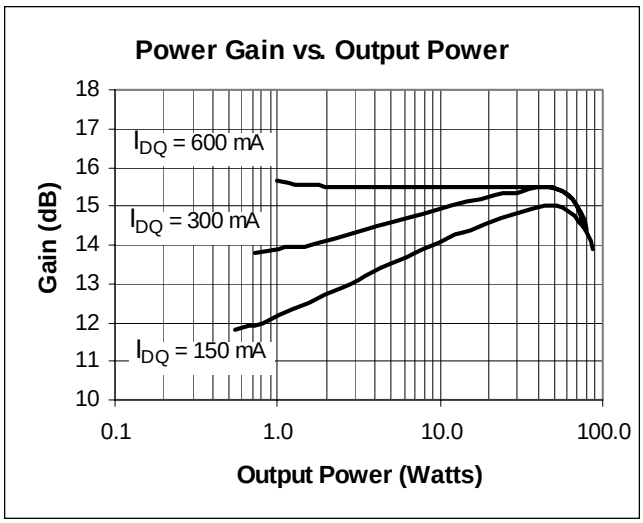
Maximum Ratings

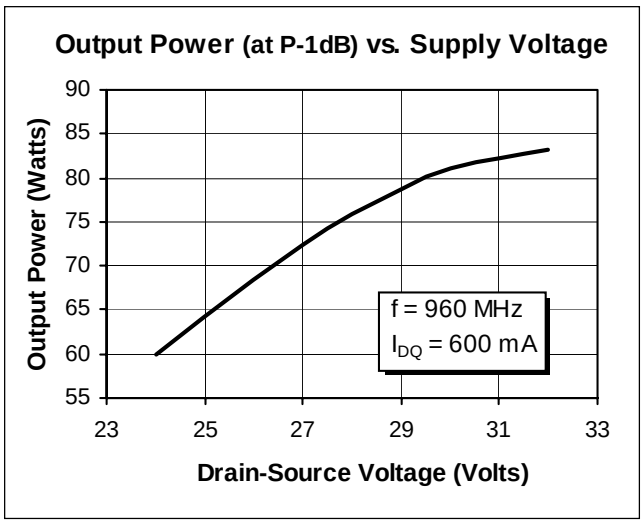
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation Above 25°C derate by	P_D	215 1.25	Watts W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	0.8	°C/W

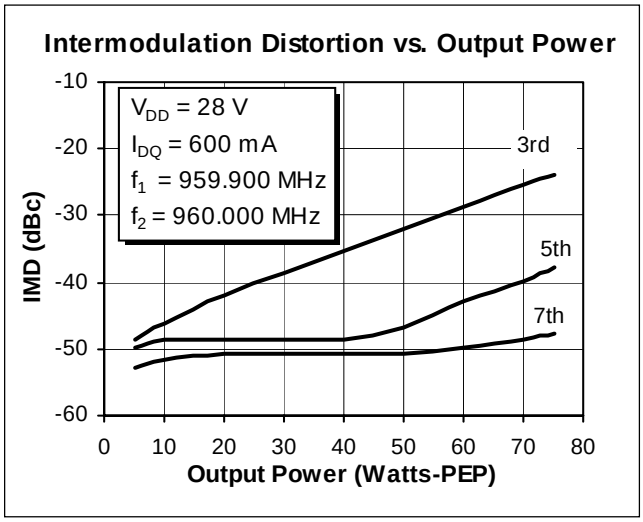
Typical Performance

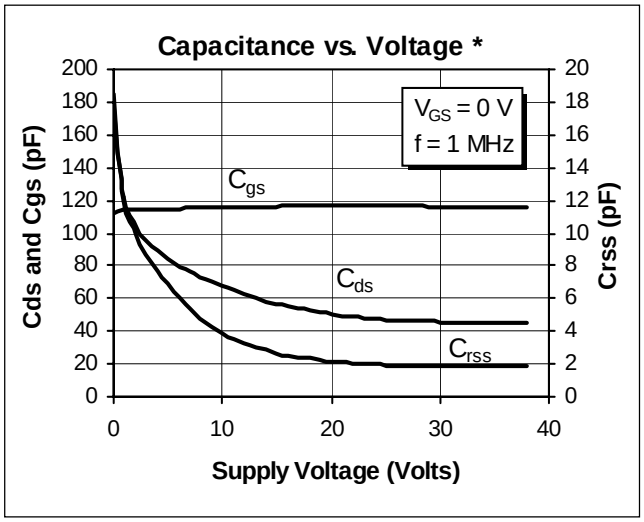




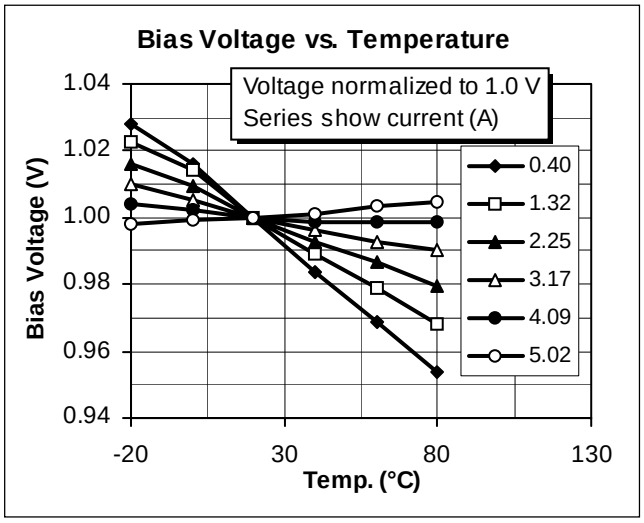






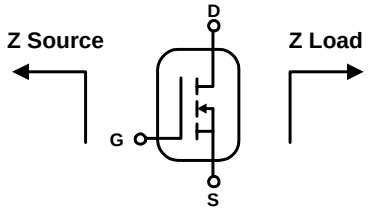


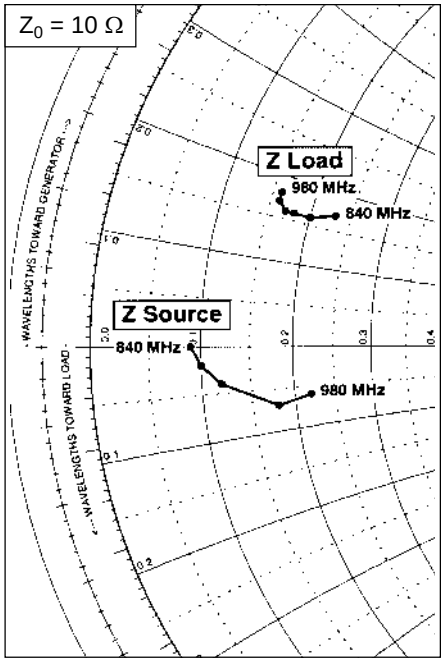
* This part is internally matched. Measurements of the finished product will not yield these figures.



Impedance Data

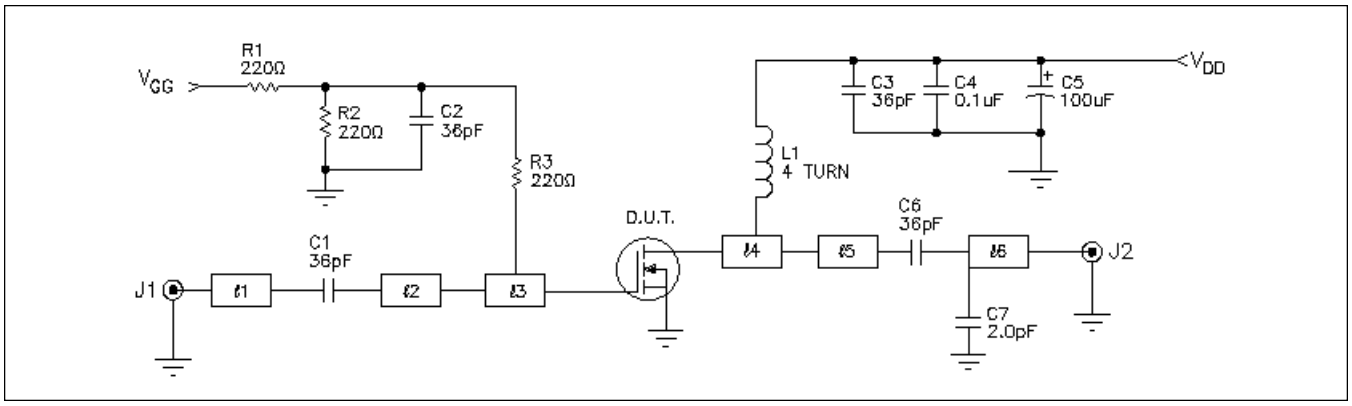
(V_{DD} = 28 V, P_{OUT} = 70 W, I_{DQ} = 600 mA)





Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
840	0.9	0	2.3	1.7
860	1.0	-0.2	2.0	1.6
900	1.2	-0.4	1.8	1.6
920	1.2	-0.4	1.7	1.6
960	1.8	-0.7	1.6	1.7
980	2.2	-0.6	1.6	1.8

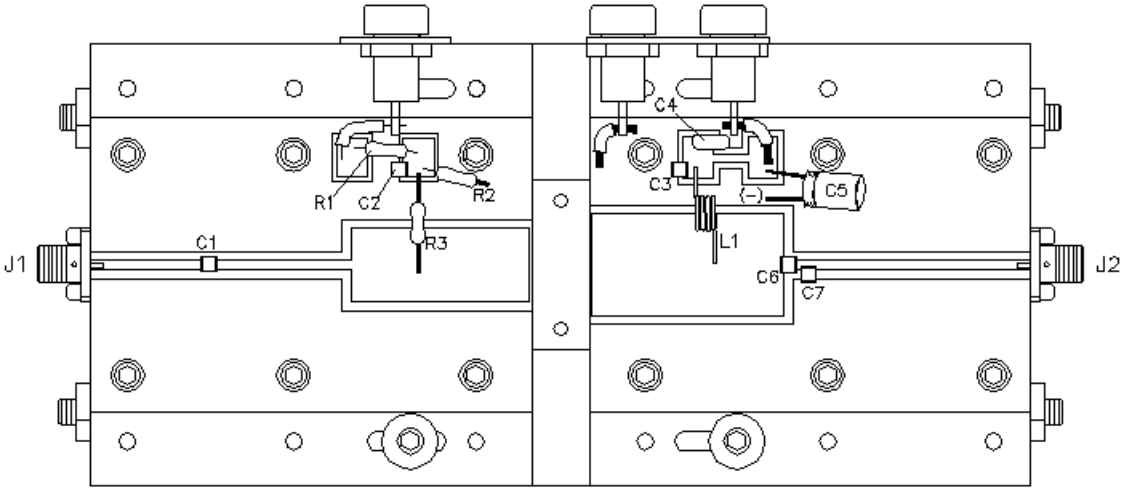
Test Circuit



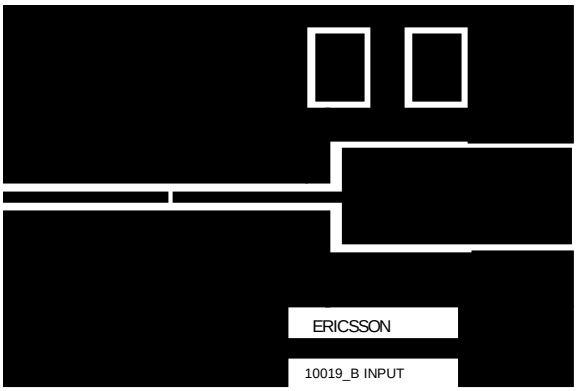
Test Circuit Schematic for f = 960 MHz

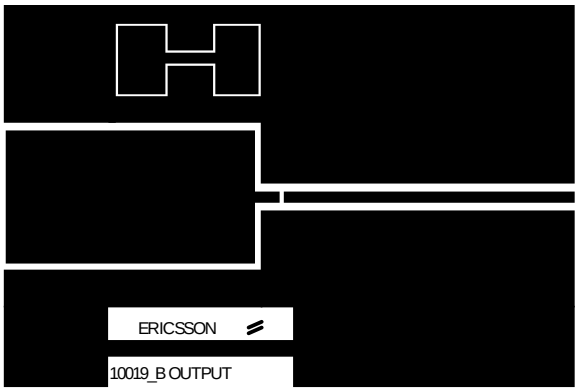
D.U.T.	PTF 10019	LDMOS FET
ℓ1	0.123 λ 960 MHz	Microstrip 50 Ω
ℓ2	0.125 λ 960 MHz	Microstrip 50 Ω
ℓ3	0.186 λ 960 MHz	Microstrip 10 Ω
ℓ4	0.200 λ 960 MHz	Microstrip 7.5 Ω
ℓ5	0.060 λ 960 MHz	Microstrip 50 Ω
ℓ6	0.217 λ 960 MHz	Microstrip 50 Ω

C1, C2, C3, C6	36 pF Chip Cap	ATC 100 B 360
C4	0.1 µF Capacitor	Digi-Key 4525-ND
C5	100 µF, 50 V Electrolytic Capacitor,	Digi-Key P5182-NO
C7	2.0 pF Chip Cap	ATC 100 B 1R7
J1, J2	Female SMA Connectors, Panel Mount	
L1	4 Turn, #20 AWG, .120" I.D.	
R1, R2, R3	220 Ω, 1/4 W Resistor	Digi-Key 220QBK-ND
Circuit Board	.031" Thick, ε_r = 4.0, 2 oz. copper,	AlliedSignal, G200



Components Layout (not to scale)

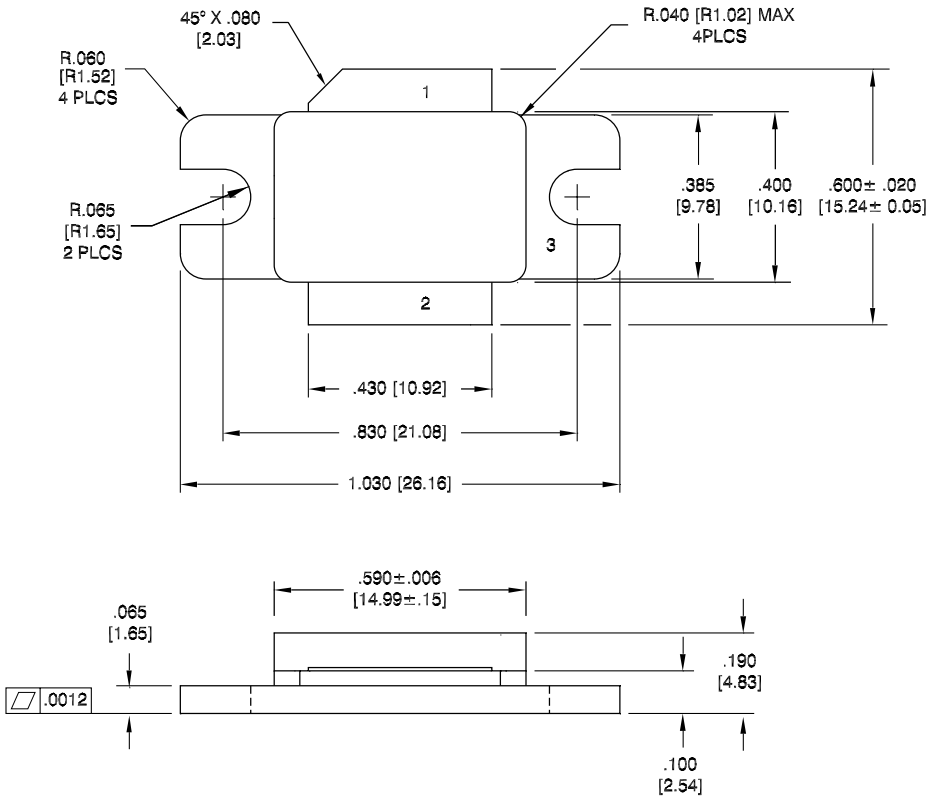




Artwork (not to scale)

Case Outline Specifications

Package 20237



Unless otherwise specified
all tolerances ±0.005" [0.13mm]

Pins: 1.Drain 2.Gate 3.Source
Lead Thickness: 0.005 +0.002/-0.001"
[0.13 +0.05/-0.03mm]

Unless otherwise noted, lids are toleranced with reference to the leads.
Primary dimensions are inches; alternate dimensions are mm.

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