PayloadPlus™/APC UTOPIA Slave Bridge

Introduction

The *PayloadPlus*/ATM port controller (APC) universal test and operations PHY interface for ATM (UTOPIA) slave bridge, also known as the *PayloadPlus* APC wedge (PAW) or the *Atlanta*™ interface device (AID), is based on an OR3T20 optimized reconfigurable cell array (*ORCA*®) FPGA. It provides processor bus interfaces and UTOPIA interfaces to bridge between Agere Systems Inc. APC devices and the Agere Systems *PayloadPlus* network processor chip set.

The bridge provides a plug-in solution to interconnect ATM-layer devices such as the ATM port controller, fast pattern processor (FPP), and route switching processor (RSP).

In addition, the core implements a configuration bus interface providing access to the control and status registers for the UTOPIA interfaces and maps the APC address space for the Agere system interface (ASI) device.

Features

- Two 16-bit, 52 MHz UTOPIA slave ports. Level 2 for the APC and Level 3 for the *PayloadPlus*. Alternatively, the Level 3 UTOPIA ports can be configured as 8-bit, 104 MHz interfaces.
- Both interfaces support multiple physical-layer (MPHY) polling. Port addresses are independently programmable via software registers.
- Cell buffering for three ATM cells in each direction.
- Configuration bus interface provides a host processor access to the bridge and APC register sets via the ASI device.
- Deliverable as a tested bit-stream for ease of use or as HDL code for added flexibility.

Block Diagram

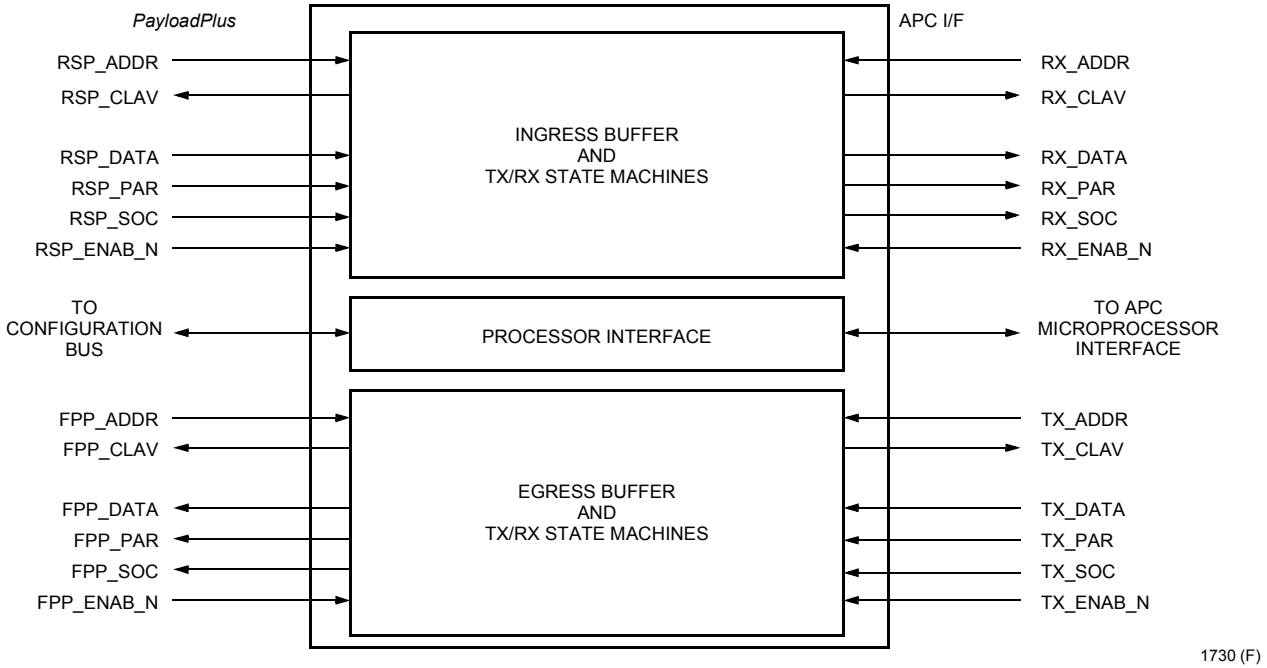

Figure 1. *PayloadPlus*/APC UTOPIA Bridge Block Diagram

Application

Agere Systems' *PayloadPlus* network processor chip set, together with the APC, provides a complete solution to implement multiprotocol OC-12 line cards. The *PayloadPlus*/APC UTOPIA slave bridge provides connectivity between the FPP and RSP UTOPIA interfaces and the APC UTOPIA interface and between the ASI configuration and management bus and the APC processor interface bus.

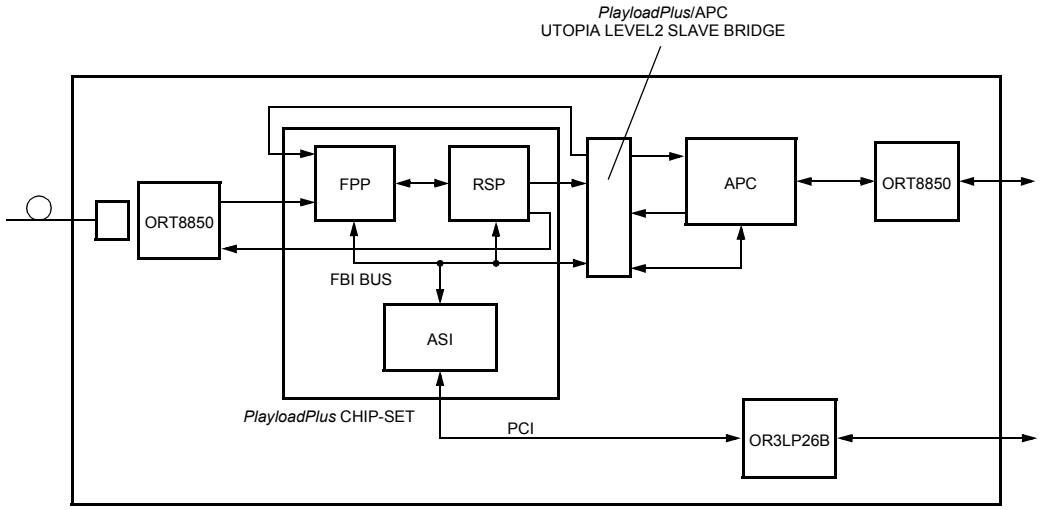

Figure 2. *PayloadPlus*/APC UTOPIA Bridge Application (Multiprotocol OC-12 Port Card)

Processor Interfaces

The *PayloadPlus*/APC bridge and the APC are connected to a host processor PCI bus via the 8-bit configuration bus on the ASI device as shown in Figure 3. Since the APC data bus is 32 bits wide, mirror registers in the *PayloadPlus*/APC bridge are used to adapt the configuration bus to the APC's microprocessor interface.

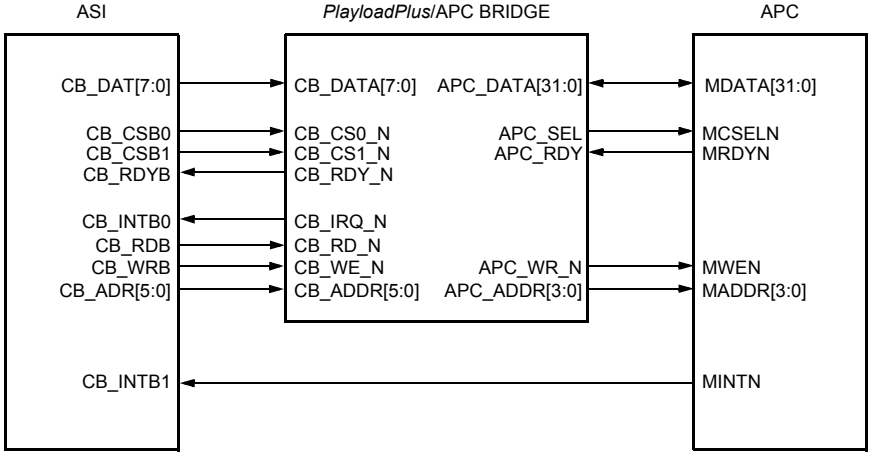

Figure 3. ASI to *PayloadPlus*/APC Bridge and APC Connections

Processor Interfaces (continued)

The configuration bus provides 8-bits for data, 11-bits for addressing (6 address bits are decoded by the *PayloadPlus*/APC bridge), chip enables, and control signals to access registers in the *PayloadPlus*/APC bridge. Figure 4 illustrates a typical write transaction on the configuration bus. The ASI initiates the transaction by asserting a valid address and write enable (CB_WE_N). It then asserts the data, chip select, and data strobe (CB_RD_N). The *PayloadPlus*/APC bridge responds with CB_RDY_N after a delay of 20—40 ns. The ASI takes the data strobe high to initiate the write operation. Shortly thereafter, the chip select, address, and data are deasserted to end the write cycle.

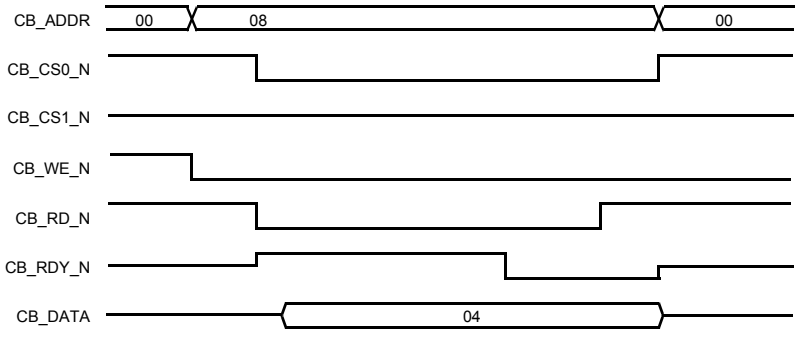

Figure 4. Configuration Bus Write Cycle.

A typical read transaction on the configuration bus is shown in Figure 5. The ASI presents a valid address while the write enable (CB_WE_N) is off (high). It then asserts the appropriate chip select and data strobe (CB_RD_N). The *PayloadPlus*/APC bridge drives the data bus whenever one of its chip selects is low and the write enable is high. Once the data strobe is asserted, it will assert CB_RDY_N after a delay of 20—40 ns. Once the *PayloadPlus*/APC bridge assets CB_RDY_N, the ASI will deassert the data strobe (CB_RD_N) and capture data on its rising edge. It will then deassert the address and chip select to end the read cycle.

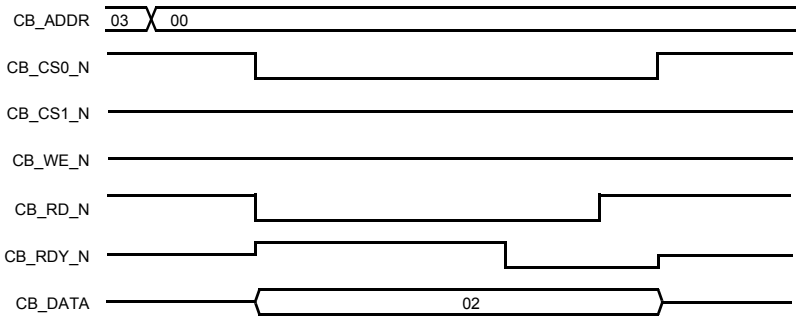

Figure 5. Configuration Bus Read Cycle.

Processor Interfaces (continued)

Figures 4 and 5 represent the configuration bus timing for transactions to any internal register (CS0_N) or to one of the lower three bytes (mirror registers) of the APC (CS1_N). For transactions to the most significant byte (address 0x3) of an APC register (CS1_N), the *PayloadPlus*/APC bridge generates an APC write or read cycle as shown in Figure 6. During an APC write or read cycle, CB_ADDR[5:2] are used as APC_ADDR, CB_WE_N is used as APC_WE_N, and data strobe (CB_RD_N) is used as APC_SEL. Data is passed from the configuration bus to the most significant byte of the APC data bus for write operations or vice-versa for read operations. The lower 24-bits of the APC data bus are driven by the APC mirror registers in the *PayloadPlus*/APC bridge. The ready signal (CB_RDY_N) is controlled by APC_RDY as shown.

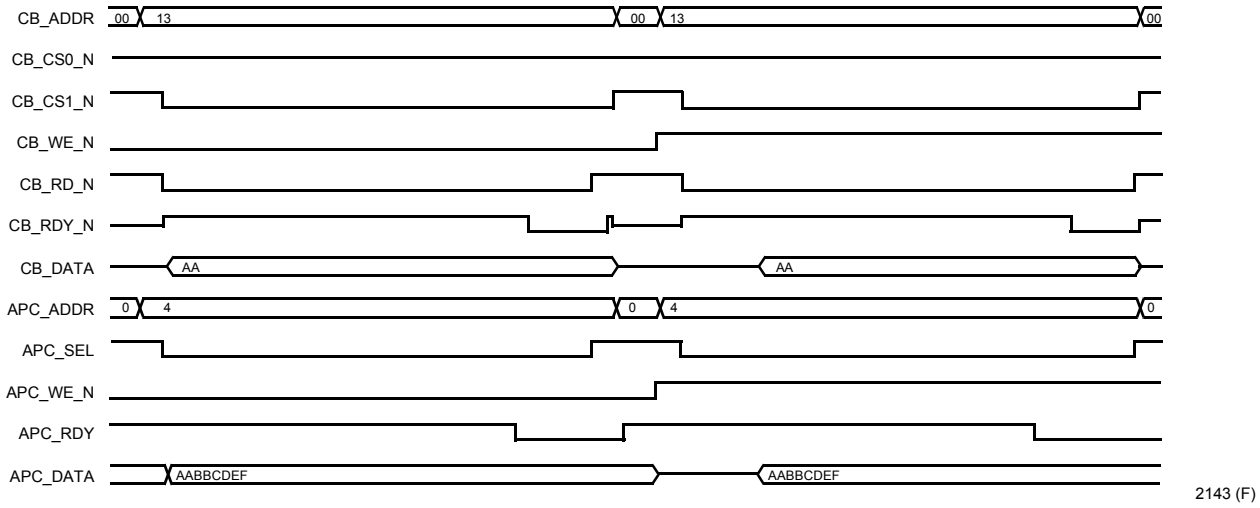

Figure 6. APC Write/Read Cycles.

Register Map

The interface contains two separate register spaces with two separate chip enables. The *PayloadPlus*/APC bridge register space listed in Table 1 is accessed when CS0_N is active (low).

Table 1. *PayloadPlus*/APC Bridge (CS0_N) Register Map

Address	Type	Register	Bits	Default	Name	Description
0x00	R	FPGA ID	7:0	0xC2	ID	*PayloadPlus*/APC bridge design ID.
0x01	R	Version	7:0	0x01	Version	Code revision number.
0x02	W/R	Mask	7:4	—	—	Reserved.
			3	0	mask(3)	0 masks nonzero incomplete cell counter TX.
			2	0	mask(2)	0 masks nonzero overflow error counter TX.
			1	0	mask(1)	0 masks nonzero incomplete cell counter RSP.
			0	0	mask(0)	0 masks nonzero TX overflow error counter RSP.
0x03	W/R	Interrupts	7:4	—	—	Reserved. Write a 1 to clear the associated counter.
			3	0	i_cnt_nz_B	1 indicates nonzero incomplete cell counter TX.
			2	0	e_cnt_nz_B	1 indicates nonzero overflow error counter TX.
			1	0	i_cnt_nz_A	1 indicates nonzero incomplete cell counter RSP.
			0	0	e_cnt_nz_A	1 indicates nonzero TX overflow error counter RSP.
0x04	R	Err_cnt_a	7:0	0x00	—	Overflow error count for RSP.
0x05	R	Inc_cnt_a	7:0	0x00	—	Incomplete cell count for RSP.
0x06	R	Err_cnt_b	7:0	0x00	—	Overflow error count for TX.
0x07	R	Inc_cnt_b	7:0	0x00	—	Incomplete cell count for TX.
0x08	W/R	ADDR_A	7:5	—	—	Reserved.
			4:0	0x00	set_addr_a	Control for PHY address for the RSP port.
0x09	W/R	ADDR_B	7:5	—	—	Reserved.
			4:0	0x00	set_addr_b	Control for PHY address for the FPP port.
0x0A	W/R	ADDR_C	7:5	—	—	Reserved.
			4:0	0x00	set_addr_c	Control for PHY address for the APC port.
0x0B—0x1F	—	—	—	—	—	Reserved.

The APC direct access register set is composed of nine 32-bit registers. These registers are mapped onto the 8-bit configuration bus as 36 addresses at CS1_N as shown in Table 2. Each address in a group of four accesses 8-bits of the complete 32-bit word. For each 32-bit write/read to the APC, the host processor accesses the configuration bus four times. During an access to the most significant byte (MSByte) in any register group, a 32-bit write/read is performed on the APC processor bus. For a write operation, the processor writes data to the three low-order bytes before writing to the MSByte which triggers the actual 32-bit write into the APC register. Conversely, the host processor reads the MSByte first to trigger a 32-bit read from the APC, then accesses each of the low-order bytes to obtain the entire 32-bit word.

Register Map (continued)

Table 2. APC Processor Interface (CS1_N) Register Map:

Binary Address	Hex Address	Type	Register	Bits	Description
xxxx00	—	W/R	—	7:0	Mirror bits 7:0.
xxxx01	—	W/R	—	7:0	Mirror bits 15:8.
xxxx10	—	W/R	—	7:0	Mirror bits 23:16.
000011	0x03	W/R	rMPTR	7:0	MSByte (31:24) APC Register 0x0.
000111	0x07	R	rSTAT1	7:0	MSByte (31:24) APC Register 0x1.
001011	0x0B	R	rSTAT2	7:0	MSByte (31:24) APC Register 0x2.
001111	0x0F	R	rSTAT3	7:0	MSByte (31:24) APC Register 0x3.
010011	0x13	W/R	rDR	7:0	MSByte (31:24) APC Register 0x4.
010111	0x17	W/R	rDRI	7:0	MSByte (31:24) APC Register 0x5.
011011	0x1B	W/R	rXMem	7:0	MSByte (31:24) APC Register 0x6.
011111	0x1F	W	rInsFIFO	7:0	MSByte (31:24) APC Register 0x7.
100011	0x23	R	rCapFIFO	7:0	MSByte (31:24) APC Register 0x8.

Take care when accessing the APC mirror registers. There are actually only three mirror registers in the *PayloadPlus*/APC bridge, so writes/reads to the low-order bytes of any register group will overwrite the contents of the low-order registers. Therefore, the host processor should access the APC mirror registers in a linear fashion and works with only one register group at a time.

For example, when the host processor reads the MSByte of APC register 0, 32 bits are read from the APC and loaded into the APC mirror registers. Subsequent read accesses to the low-order bytes of any of the eight register groups will return the low-order byte's read from APC register 0. A read to the least significant byte (LSByte) of APC register 6 will return the value most recently read from the APC which is actually from register 0.

Similarly, if the host processor writes data into the low-order bytes of the group for APC register 4, writes the low-order bytes for APC register 5, and then writes to the MSByte of the register group for APC register 4, the data written into APC register 4 will be comprised of the MSByte currently being written to APC register 4 and the low-order bytes most recently written (those for APC register 5). The low-order bytes previously written to the register group for APC register 4 are lost.

Port Addresses

The PHY addresses of the FPP, RSP, and APC ports are set via control registers in the *PayloadPlus*/APC bridge register map (see Table 1). Each port responds with CLAV during the next clock cycle whenever its input address matches the contents of its set_addr register. The PHY is selected for data transfer whenever its input address matches its set_addr register during the clock cycle before ENAB goes active (low).

TX Interface

The APC UTOPIA port (slave) includes two separate interfaces. The TX interface accepts data from the APC (master) and transfers cells into a buffer. The TX interface supports MPHY polling and provides cell level handshake as defined in the *ATM Forum Technical Committee Utopia Level 2, Version 1.0* specification. Parity is not used in this release of the *PayloadPlus*/APC bridge. The TX interface includes error checking for incomplete cells and for write attempts while the buffers are full (overflow). Error checking features are accessed via the *PayloadPlus*/APC bridge register map (see Table 1).

The cell buffers are effectively FIFOs that are partitioned into three sections. Each section is large enough to store one complete ATM cell (27 words x 17 bits). As the RSP/TX interfaces complete each cell, a cell available flag is set for the current section signaling the FPP/RX interface that a complete cell is now available in the buffer. The write pointer then advances to the next section of the cell buffer.

Tx Interface (continued)

Figure 7 illustrates a cell transfer on the TX interface. In this example, the PHY port address is 0x18. The APC polls the PHY by placing its address on TX_ADDR. During the next clock cycle the PHY asserts TX_CLAV high indicating that it is ready to receive at least one complete cell from the APC. Then the APC selects the PHY by placing its address on TX_ADDR while TX_ENAB_N is high and taking TX_ENAB_N low during the following clock cycle. The TX interface waits until TX_SOC is asserted before starting to write the 27 word cell into the current section of its cell buffer. The TX_SOC signal may be asserted coincident with TX_ENAB_N going low as shown in Figure 7, or it can occur any number of clock cycles after TX_ENAB_N becomes active.

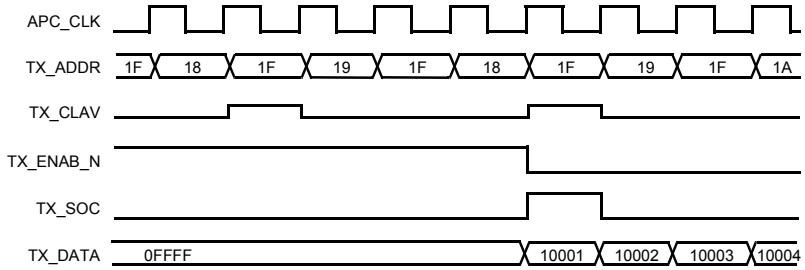

Figure 7. TX Interface Polling and Start of Cell

The ATM layer device can interrupt transmission of a cell on the TX interface for any number of clock cycles by taking TX_ENAB_N high as shown in Figure 8. The APC does not support cell interruption and once a cell is started it will transmit an entire cell; however, this capability is included to provide full UTOPIA Level 2 compliance for the TX interface. The ATM layer device must reselect the PHY by putting its address on TX_ADDR during the cycle before TX_ENAB_N returns low. If the ATM layer device does not reselect the PHY and complete the cell before asserting the next TX_SOC, the PHY flushes data from the current section of the cell buffer and increments the incomplete cell counter. A nonzero count is indicated in the status register, and an interrupt is generated via the configuration bus interface unless masked.

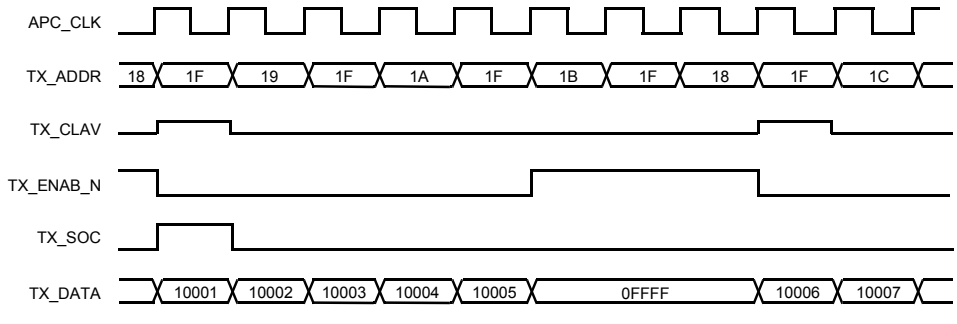

Figure 8. ATM Layer Interrupting Cell Transfer

Tx Interface (continued)

The APC can also transmit cells back-to-back if polling during the current cell indicates that another cell can be accepted. This is shown in Figure 9. Finally, if the APC selects the PHY and asserts TX_SOC while TX_CLAV indicates that the cell buffer is full, the overflow counter is incremented, a nonzero count is indicated in the status register, and an interrupt is generated unless masked.

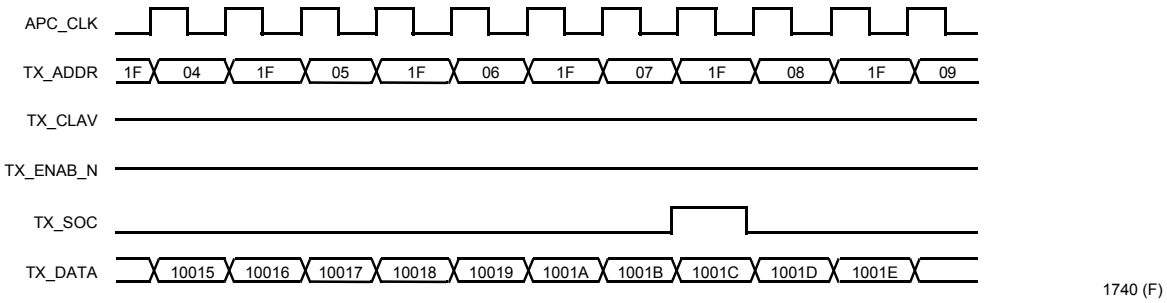

Figure 9. Back-to-Back Cell Transmission

RX Interface

The RX interface supports MPHY polling by the APC and signals that a cell is available when the cell available flag for the current section of the cell buffer is active. When selected, the RX interface transfers data from the cell buffer to the APC as described in the *ATM Forum Technical Committee Utopia Level 2, Version 1.0* specification.

Figure 10 illustrates a cell transfer on the RX interface. In this example, the PHY port address is 0x18. The APC polls the PHY by placing its address on RX_ADDR. During the next clock cycle the PHY asserts RX_CLAV high indicating that it is ready to send at least one complete cell to the APC. The APC then selects the PHY by placing its address on RX_ADDR while RX_ENAB_N is high and taking RX_ENAB_N low during the following clock cycle. The RX interface asserts RX_SOC during the next clock cycle while sending the first word of the 27 word cell.

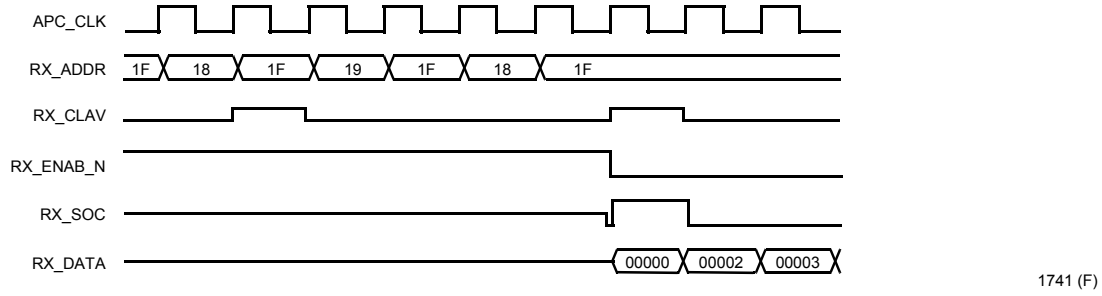

Figure 10. RX Interface Polling and Start of Cell

RX Interface (continued)

The ATM layer device can interrupt cell reception by taking RX_ENAB_N high as shown in Figure 11; however, the APC does not support cell interruption and will transfer a cell as 27 continuous words from the RX interface. If an ATM layer device that does support cell interruption is used, the word that is active when RX_ENAB_N goes low must be captured by the ATM layer device.

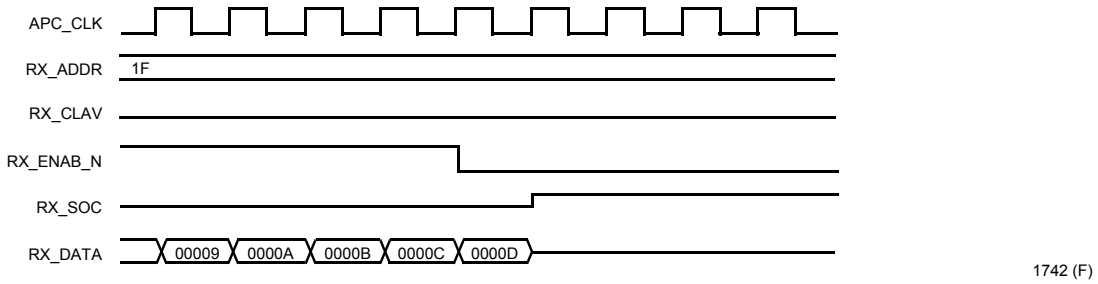

Figure 11. ATM Layer Interruption of Cell Reception

To resume reception, the ATM Layer device must reselect the PHY by placing its address on RX_ADDR during the clock cycle before RX_ENAB_N returns low as shown in Figure 12. Reception is resumed on the next rising-edge of the clock.

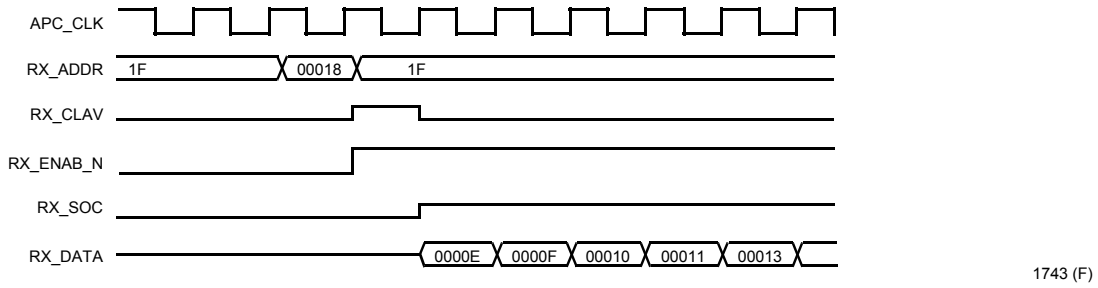

Figure 12. ATM Layer Resumption of Cell Reception

If the APC holds RX_ENAB_N active, and another cell is available in the cell buffer, the RX interface will send cells back-to-back as shown in Figure 13. If another cell is not yet available and the APC continues to assert RX_ENAB_N low, data is ignored until the RX interface asserts the RX_SOC signal along with the first word of the next available cell.

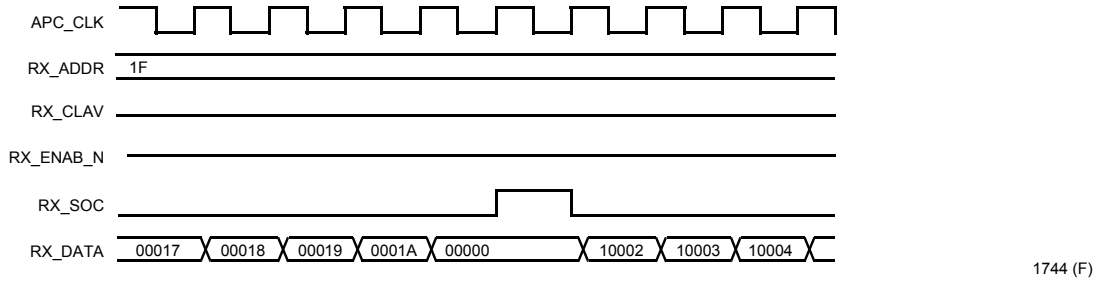

Figure 13. Back-to-Back Cell Reception

RSP Interface

The RSP port (slave) is a UTOPIA Level 3 TX interface. The RSP interface accepts data from the RSP (master) and transfers cells into a buffer. The RSP interface supports MPHY polling and provides cell-level handshaking as defined in the *ATM Forum Technical Committee Utopia 3 Physical Layer Interface* specification. Parity is not used in this release of the *PayloadPlus*/APC bridge. The RSP interface includes error checking for incomplete cells and for write attempts while the buffers are full (overflow). Error checking features are accessed via the *PayloadPlus*/APC bridge register map (see Table 1).

The cell buffers are effectively FIFOs that are partitioned into three sections. Each section is large enough to store one complete ATM cell (27 words x 17 bits). As the RSP/TX interfaces complete each cell, a cell available flag is set for the current section signaling the FPP/RX interface that a complete cell is now available in the buffer. The write pointer then advances to the next section of the cell buffer.

Figure 14 illustrates a cell transfer on the RSP interface. In this example, the PHY port address is 0x04. The RSP polls the PHY by placing its address on RSP_ADDR. During the next clock cycle the PHY asserts RSP_CLAV high indicating that it is ready to receive at least one complete cell from the RSP. Then the RSP selects the PHY by placing its address on RSP_ADDR while RSP_ENAB_N is high and taking RSP_ENAB_N low during the following clock cycle. The RSP interface waits until RSP_SOC is asserted before starting to write the 27 word cell into the current section of its cell buffer. The RSP_SOC signal may be asserted coincident with RSP_ENAB_N going low as shown in Figure 14, or it can occur any number of clock cycles after RSP_ENAB_N goes active.

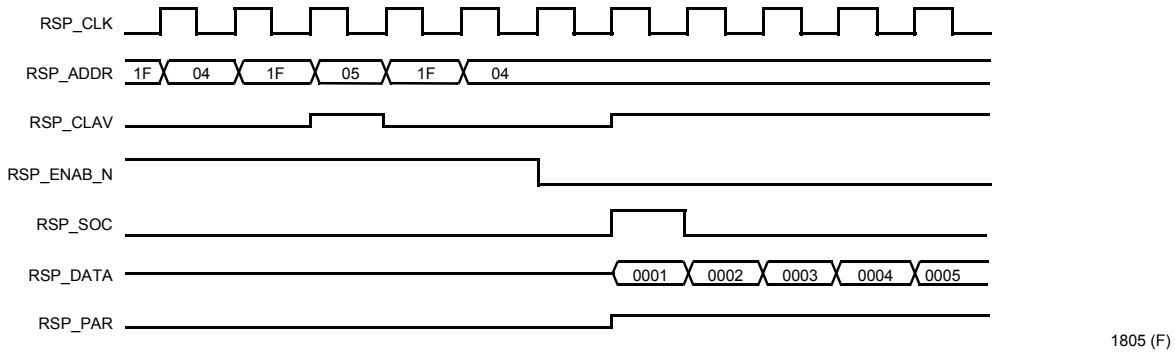

Figure 14. RSP Interface Polling and Start of Cell

Once a cell is started, all 27 words are written into the buffer continuously. If the RSP layer device does not complete the cell before asserting the next RSP_SOC, the PHY flushes data from the current section of the cell buffer and begins writing the new cell into the buffer. The incomplete cell counter is incremented. A nonzero count is indicated in the status register, and an interrupt is generated via the configuration bus interface unless masked. The RSP can transmit cells back to back if polling during the current cell indicates that another cell can be accepted. This is shown in Figure 15. Finally, if the RSP selects the PHY and asserts RSP_SOC while RSP_CLAV indicates that the cell buffer is full, the overflow counter is incremented, a nonzero count is indicated in the status register, and an interrupt is generated unless masked.

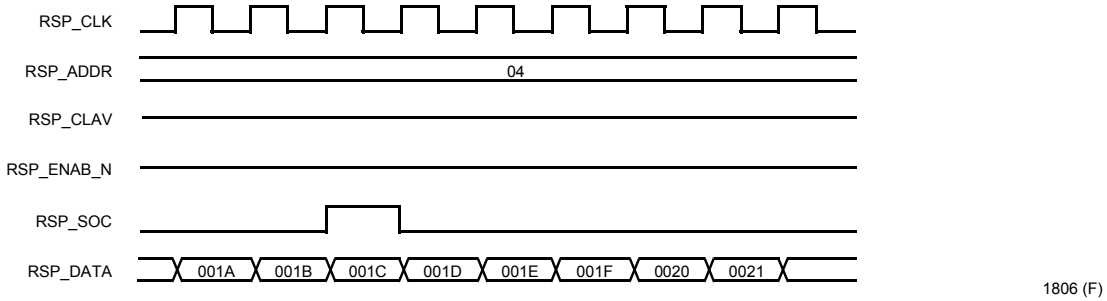

Figure 15. Back-to-Back Cell Transmission

FPP Interface

The FPP port (slave) is a UTOPIA Level 3 RX interface. The FPP interface supports MPHY polling by the FPP and signals that a cell is available when the cell available flag for the current section of the cell buffer is active. When selected, the FPP interface transfers data from the cell buffer to the FPP as described in the *ATM Forum Technical Committee Utopia 3 Physical Layer Interface* specification.

Figure 16 illustrates a cell transfer on the FPP interface. In this example, the PHY port address is 0x04. The FPP polls the PHY by placing its address on FPP_ADDR. During the second clock cycle the PHY asserts FPP_CLAV high indicating that it is ready to send at least one complete cell to the FPP. The FPP then selects the PHY by placing its address on FPP_ADDR while FPP_ENAB_N is high and taking FPP_ENAB_N low during the following clock cycle. The FPP interface asserts FPP_SOC while sending the first word of the 27 word cell.

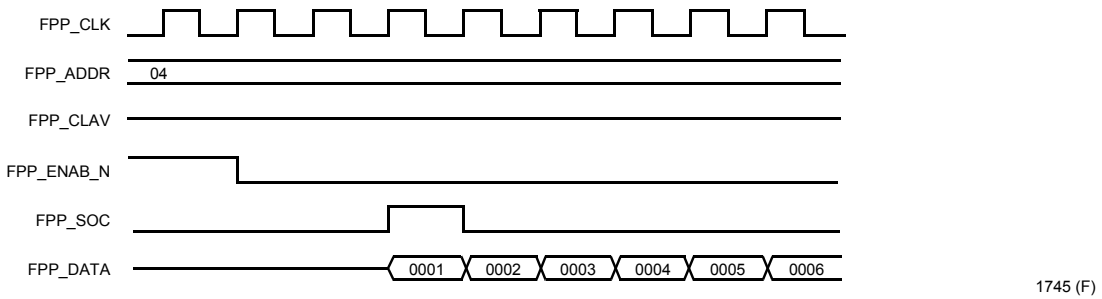

Figure 16. FPP Interface Polling and Start of Cell

If the FPP holds FPP_ENAB_N active beyond the 25th byte of the current cell and another cell is available in the cell buffer, the FPP interface will send cells back to back as shown in Figure 17. If another cell is not yet available and the FPP continues to assert RX_ENAB_N low, data is ignored until the *PayloadPlus*/APC bridge asserts FPP_SOC along with the first word of the next available cell.

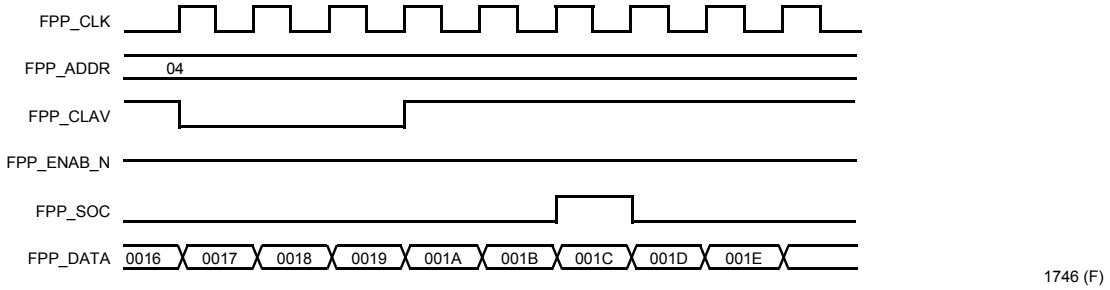

Figure 17. Back-to-Back Cell Reception

To prevent back to back cell reception, the FPP must deassert FPP_ENAB_N before or during the 25th word of the current cell as shown in Figure 18. The interface will complete the cell and then wait until FPP_ENAB_N returns low before starting the next cell.

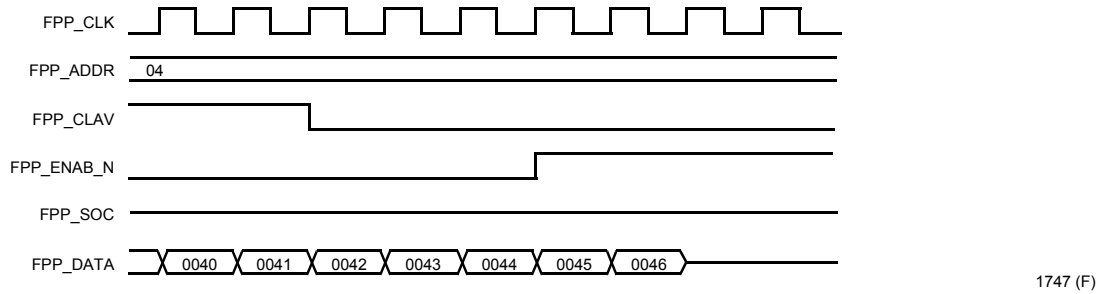

Figure 18. End of Cell Reception

Configuration

The *ORCA* OR3T20 is a reconfigurable field programmable gate array (FPGA) device based on a static random access memory (SRAM). The *PayloadPlus*/APC bridge design must be loaded into the device every time system power is applied. This process is called configuration and it is accomplished via self-configuration from a serial configuration read-only memory.

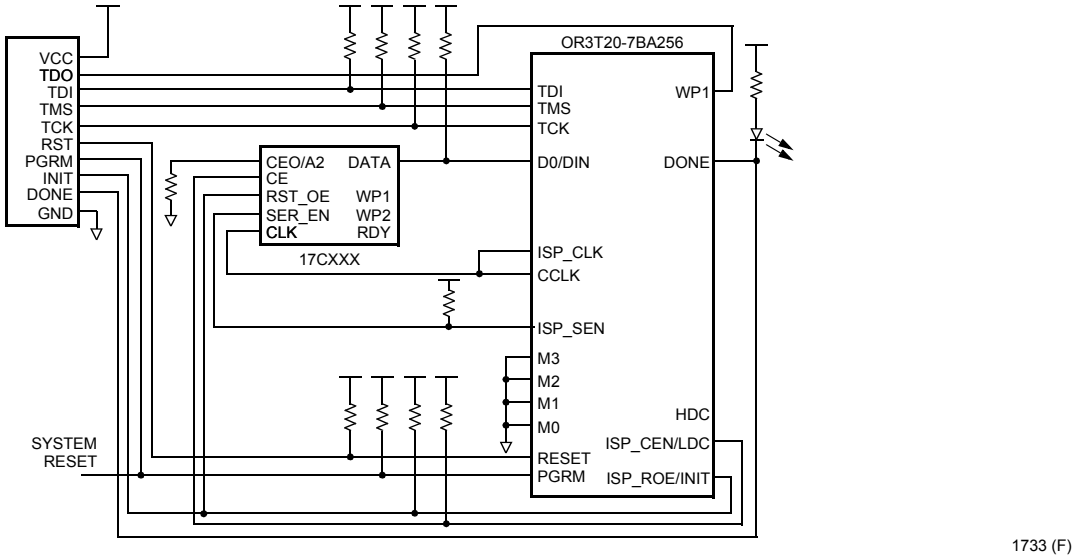

Figure 19. Board Level Connections for Self-Configuration

The serial configuration signals, and optional in-system programmability (ISP) signals and JTAG signals are connected as shown in Figure 19. A JTAG serial download cable and the ORCA Foundry control center can be used to program the electrically eraseable programmable read-only memory (EEPROM) after manufacture and facilitates future firmware upgrades, if necessary. A one-time programmable serial configuration PROM can also be used.

JTAG Interface

The JTAG test access port (TAP) is active both before and after device configuration. If used, it is connected as shown in Figure 19. If the JTAG interface is not used, the TDI, TMS, and TCK inputs must be connected to V_{CC} via 1.5 kΩ pull-up resistors. The JTAG interface supports bypass, boundary-scan, and device configuration operations whenever power is applied. After device configuration, the JTAG interface also includes support for configuration download/read-back (for troubleshooting) and in-system programmability (ISP) for an external serial configuration EEPROM (if present). Details on use of the JTAG interface for boundary scan and in-system programmability are found in the *ORCA OR3C/T Field Programmable Gate Array* Data Sheet (DS99-087FPGA) and associated application notes.

Pin Assignments

Table 3 lists pin assignments, and signal descriptions for an implementation using the OR3T20 FPGA device in a 256 pin ball grid array (BGA) package.

Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256

Pin	Pad	OR3T20	Type	Name	Description	Note*
C2	PL1D	I/O	B	APC_DATA(31)	APC processor interface bus (MSB).	—
D2	PL1C	I/O	B	APC_DATA(30)	APC processor interface bus.	—
D3	PL1B	I/O	B	APC_DATA(29)	APC processor interface bus.	—
E4	PL1A	I/O-A0	B	APC_DATA(28)	APC processor interface bus.	—
C1	—	—	—	—	—	—
D1	—	—	—	—	—	—
E3	—	—	—	—	—	—
E2	PL2D	I/O	I	RX_ADDR(0)	APC port receive address bit (0) (LSB).	—
E1	PL2C	I/O	I	RX_ADDR(1)	APC port receive address bit (1).	—
F3	PL2B	I/O	I	RX_ADDR(2)	APC port receive address bit (2).	—
G4	PL2A	I/O-A1	I	RX_ADDR(3)	APC port receive address bit (3).	—
F2	—	—	—	—	—	—
F1	PL3D	I/O-A2	I	RX_ADDR(4)	APC port receive address bit (4).	—
G3	PL3C	I/O	T	RX_CLAV	APC port receive cell available.	—
G2	PL3B	I/O	T	RX_SOC	APC port receive start of cell.	—
G1	PL3A	I/O-A3	I	RX_ENAB_N	APC port receive enable.	—
H3	PL4D	I/O	B	CB_DATA(7)	Configuration bus data bit.	—
H2	PL4C	I/O	B	CB_DATA(6)	Configuration bus data bit.	—
H1	PL4B	I/O	B	CB_DATA(5)	Configuration bus data bit.	—
J4	PL4A	I/O-A4	B	CB_DATA(4)	Configuration bus data bit.	—
J3	PL5D	I/O-A5	B	CB_DATA(3)	Configuration bus data bit.	—
J2	PL5C	I/O	B	CB_DATA(2)	Configuration bus data bit.	—
J1	PL5B	I/O	B	CB_DATA(1)	Configuration bus data bit.	—
K2	PL5A	I/O-A6	B	CB_DATA(0)	Configuration bus data bit (LSB).	—
K3	PECKL	I-ECKL	I	CB_WE_N	Configuration bus write enable (active-low).	—
K1	PL6C	I/O	I	CB_ADDR(5)	Configuration bus address bit.	—
L1	PL6B	I/O	I	CB_ADDR(4)	Configuration bus address bit.	—
L2	PL6A	I/O-MPI_CLK	I	CB_ADDR(3)	Configuration bus address bit.	—
L3	PL7D	I/O	I	CB_ADDR(2)	Configuration bus address bit.	—
L4	PL7C	I/O	I	CB_ADDR(1)	Configuration bus address bit.	—
M1	PL7B	I/O	I	CB_ADDR(0)	Configuration bus address bit (LSB)	—
M2	PL7A	I/O-MPI_RW	I	CB_RD_N	Configuration bus read enable (active-low).	—
M3	PL8D	I/O-MPI_ACK	T	CB_RDY_N	Configuration bus ready acknowledge (active-low).	—
M4	PL8C	I/O	I	CB_CS1_N	*PayloadPlus*/APC bridge register space select (active-low).	—
N1	PL8B	I/O	O	CB_IRQ_N	*PayloadPlus*/APC bridge interrupt request (active-low).	—
N2	PL8A	I/O-MPI_BI	I	CB_CS1_N	APC register space select (active-low).	—

* The symbols contained in this column describe special connection requirements. The symbol meanings are as follows: PU—requires a pull up resistor, PD—requires a pull down resistor, NC—not connected, 1—must be tied high, LED—connected to a light emmitting diode.

Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
N3	PL9D	I/O	O	APC_SEL	Chip-select to APC (active-low).	—
P1	PL9C	I/O	O	APC_WE_N	Read/Write control to APC (active-low).	—
P2	PL9B	I/O	I	APC_RDY	Ready acknowledge from APC.	—
R1	PL9A	I/O-MPI_IRQ	—	—	—	—
P3	PL10D	I/O-A12	I	RSP_ADDR(0)	RSP port transmit address bit (0).	—
R2	PL10C	I/O	I	RSP_ADDR(1)	RSP port transmit address bit (1).	—
T1	PL10B	I/O	I	RSP_ADDR(2)	RSP port transmit address bit (2).	—
P4	PL10A	I/O-A13	I	RSP_ADDR(3)	RSP port transmit address bit (3).	—
R3	PL11D	I/O	I	RSP_ADDR(4)	RSP port transmit address bit (4).	—
T2	PL11C	I/O	T	RSP_CLAV	RSP port transmit cell buffer available.	PU
U1	PL11B	I/O	I	RSP_ENAB_N	RSP port transmit enable.	—
T3	PL11A	I/O-A14	I	RSP _SOC	RSP port transmit start of cell.	—
U2	—	—	—	—	—	—
V1	PL12D	I/O	—	—	—	—
T4	PL12C	I/O	OD	ISP_SEN	ISP PROM write enable.	PU
U3	—	—	—	—	—	—
V2	—	—	—	—	—	—
W1	PL12B	I/O-SECKLL	—	—	—	—
V3	—	—	—	—	—	—
W2	PL12A	I/O-A15	OD	ISP_CLK	ISP PROM serial clock signal.	1
Y1	PCCLK	CCLK	O	Reserved	Self-configuration clock.	1
W3	—	—	—	—	—	—
Y2	PB1A	I/O-A16	—	—	—	—
W4	—	—	—	—	—	—
V4	PB1B	I/O	—	—	—	—
U5	PB1C	I/O	I	RSP_PAR	RSP port transmit parity.	NC
Y3	PB1D	I/O	I	RSP_DATA(15)	RSP port transmit data bus.	—
Y4	—	—	—	—	—	—
V5	—	—	—	—	—	—
W5	PB2A	I/O-A17	—	—	—	—
Y5	PB2B	I/O	I	RSP_DATA(14)	RSP port transmit data bus.	—
V6	PB2C	I/O	I	RSP_DATA(13)	RSP port transmit data bus.	—
U7	PB2D	I/O	I	RSP_DATA(12)	RSP port transmit data bus.	—
W6	PB3A	I/O	—	—	—	—
Y6	PB3B	I/O	I	RSP_DATA(11)	RSP port transmit data bus.	—
V7	PB3C	I/O	I	RSP_DATA(10)	RSP port transmit data bus.	—
W7	PB3D	I/O	I	RSP_DATA(9)	RSP port transmit data bus.	—
Y7	PB4A	I/O	—	—	—	—

* The symbols contained in this column describe special connection requirements. The symbol meanings are as follows: PU—requires a pull up resistor, PD—requires a pull down resistor, NC—not connected, 1—must be tied high, LED—connected to a light emmitting diode.

Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
V8	PB4B	I/O	I	RSP_DATA(8)	RSP port transmit data bus.	—
W8	PB4C	I/O	I	RSP_DATA(7)	RSP port transmit data bus.	—
Y8	PB4D	I/O	I	RSP_DATA(6)	RSP port transmit data bus.	—
U9	PB5A	I/O	—	—	—	—
V9	PB5B	I/O	I	RSP_DATA(5)	RSP port transmit data bus.	—
W9	PB5C	I/O	I	RSP_DATA(4)	RSP port transmit data bus.	—
Y9	PB5D	I/O	I	RSP_DATA(3)	RSP port transmit data bus.	—
W10	PB6A	I/O	—	—	—	—
V10	PB6B	I/O	I	RSP_DATA(2)	RSP port transmit data bus.	—
Y10	PB6C	I/O	I	RSP_DATA(1)	RSP port transmit data bus.	—
Y11	PB6D	I/O	I	RSP_DATA(0)	RSP port transmit data bus (LSB).	—
W11	PECKB	I-ECKB	I	RSP_CLK	RSP port UTOPIA clock.	—
V11	PB7B	I/O	T	FPP_DATA(0)	FPP port receive data bus (LSB).	—
U11	PB7C	I/O	T	FPP_DATA(1)	FPP port receive data bus.	—
Y12	PB7D	I/O	T	FPP_DATA(2)	FPP port receive data bus.	—
W12	PB8A	I/O	—	—	—	—
V12	PB8B	I/O	T	FPP_DATA(3)	FPP port receive data bus.	—
U12	PB8C	I/O	T	FPP_DATA(4)	FPP port receive data bus.	—
Y13	PB8D	I/O	T	FPP_DATA(5)	FPP port receive data bus.	—
W13	PB9A	I/O-HDC	O	Reserved	High during configuration pin.	NC
V13	PB9B	I/O	T	FPP_DATA(6)	FPP port receive data bus.	—
Y14	PB9C	I/O	T	FPP_DATA(7)	FPP port receive data bus.	—
W14	PB9D	I/O	T	FPP_DATA(8)	FPP port receive data bus.	—
Y15	PB10A	I/O-LDC	T	ISP_CEN	ISP PROM chip enable/low during config.	PU
V14	PB10B	I/O	T	FPP_DATA(9)	FPP port receive data bus.	—
W15	PB10C	I/O	T	FPP_DATA(10)	FPP port receive data bus.	—
Y16	PB10D	I/O	T	FPP_DATA(11)	FPP port receive data bus.	—
U14	—	—	—	—	—	—
V15	—	—	—	—	—	—
W16	PB11A	I/O-INIT	OD	ISP_ROE	ISP PROM reset/oe signal.	PU
Y17	—	—	—	—	—	—
V16	—	—	—	—	—	—
W17	PB11B	I/O	T	FPP_DATA(12)	FPP port receive data bit(12).	—
Y18	PB11C	I/O	T	FPP_DATA(13)	FPP port receive data bit(13).	—
U16	PB11D	I/O	T	FPP_DATA(14)	FPP port receive data bit(14).	—
V17	PB12A	I/O	—	—	—	—
W18	PB12B	I/O	T	FPP_DATA(15)	FPP port receive data bit(15).	—
Y19	PB12C	I/O	T	FPP_PAR	FPP port receive parity.	NC

* The symbols contained in this column describe special connection requirements. The symbol meanings are as follows: PU—requires a pull up resistor, PD—requires a pull down resistor, NC—not connected, 1—must be tied high, LED—connected to a light emmitting diode.

Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
V18	PB12D	I/O	—	—	—	—
W19	—	—	—	—	—	—
Y20	PDONE	DONE	O	DONE	Configuration done indicator.	LED
W20	PRESETN	RESET	I	RESETn	Global reset (active-low).	—
V19	PPRGMN	PRGM	I	PGRM	Self-configuration control (active-low).	PU
U19	PR12A	I/O-M0	I	MODE(0)	Configuration mode bit (0).	PD
U18	—	—	—	—	—	—
T17	—	—	—	—	—	—
V20	—	—	—	—	—	—
U20	PR12B	I/O	B	APC_DATA(23)	APC low order processor interface data bus.	—
T18	PR12C	I/O	B	APC_DATA(22)	APC low order processor interface data bus.	—
T19	PR12D	I/O	I	FPP_ADDR(0)	FPP port receive Address bit (0) (LSB).	—
T20	PR11A	I/O	I	FPP_ADDR(1)	FPP port receive Address bit (1).	—
R18	PR11B	I/O	I	FPP_ADDR(2)	FPP port receive Address bit (2).	—
P17	PR11C	I/O	I	FPP_ADDR(3)	FPP port receive Address bit (3).	—
R19	PR11D	I/O	I	FPP_ADDR(4)	FPP port receive Address bit (4).	—
R20	PR10A	I/O-M1	I	MODE(1)	Configuration mode bit (1).	PU
P18	PR10B	I/O	T	FPP_CLAV	FPP port receive cell available.	—
P19	PR10C	I/O	T	FPP_SOC	FPP port receive start of cell.	—
P20	PR10D	I/O	I	FPP_ENAB_N	FPP port receive enable.	—
N18	PR9A	I/O-M2	I	MODE(2)	Configuration mode bit (2).	PD
N19	PR9B	I/O	B	APC_DATA(21)	APC low order processor interface data bus.	—
N20	PR9C	I/O	B	APC_DATA(20)	APC low order processor interface data bus.	—
M17	PR9D	I/O	B	APC_DATA(19)	APC low order processor interface data bus.	—
M18	PR8A	I/O-M3	I	MODE(3)	Configuration mode bit (3).	PU
M19	PR8B	I/O	B	APC_DATA(18)	APC low order processor interface data bus.	—
M20	PR8C	I/O	B	APC_DATA(17)	APC low order processor interface data bus.	—
L19	PR8D	I/O	B	APC_DATA(16)	APC low order processor interface data bus.	—
L18	PR7A	I/O	—	—	—	—
L20	PR7B	I/O	—	—	—	—
K20	PR7C	I/O	B	APC_DATA(15)	APC low order processor interface data bus.	—
K19	PR7D	I/O	B	APC_DATA(14)	APC low order processor interface data bus.	—
K18	PECKR	I-ECKR	I	FPP_CLK	FPP UTOPIA master clock.	—
K17	PR6B	I/O	B	APC_DATA(13)	APC low order processor interface data bus.	—
J20	PR6C	I/O	B	APC_DATA(12)	APC low order processor interface data bus.	—
J19	PR6D	I/O	B	APC_DATA(11)	APC low order processor interface data bus.	—
J18	PR5A	I/O	B	APC_DATA(10)	APC low order processor interface data bus.	—
J17	PR5B	I/O	B	APC_DATA(9)	APC low order processor interface data bus.	—

* The symbols contained in this column describe special connection requirements. The symbol meanings are as follows: PU—requires a pull up resistor, PD—requires a pull down resistor, NC—not connected, 1—must be tied high, LED—connected to a light emmitting diode.

Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
H20	PR5C	I/O	B	APC_DATA(8)	APC low order processor interface data bus.	—
H19	PR5D	I/O	—	—	—	—
H18	PR4A	I/O-CS1n	B	APC_DATA(7)	APC low order processor interface data bus.	—
G20	PR4B	I/O	B	APC_DATA(6)	APC low order processor interface data bus.	—
G19	PR4C	I/O	B	APC_DATA(5)	APC low order processor interface data bus.	—
F20	PR4D	I/O	B	APC_DATA(4)	APC low order processor interface data bus.	—
G18	PR3A	I/O-CS0n	B	APC_DATA(3)	APC low order processor interface data bus.	—
F19	PR3B	I/O	B	APC_DATA(2)	APC low order processor interface data bus.	—
E20	PR3C	I/O	B	APC_DATA(1)	APC low order processor interface data bus.	—
G17	PR3D	I/O	B	APC_DATA(0)	APC low order processor interface data (LSB).	—
F18	PR2A	I/O-MPI-TS	I	TX_ADDR(0)	APC port transmit address bit (0).	—
E19	PR2B	I/O	I	TX_ADDR(1)	APC port transmit address bit (1).	—
D20	PR2C	I/O	I	TX_ADDR(2)	APC port transmit address bit (2).	—
E18	PR2D	I/O	I	TX_ADDR(3)	APC port transmit address bit (3).	—
D19	PR1A	I/O-WR	I	TX_ADDR(4)	APC port transmit address bit (4).	—
C20	PR1B	I/O	T	TX_CLAV	APC port transmit cell buffer available.	—
E17	PR1C	I/O	I	TX_ENAB_N	APC port transmit enable.	—
D18	PR1D	I/O	I	TX_SOC	APC port transmit start of cell.	—
C19	—	—	—	—	—	—
B20	—	—	—	—	—	—
C18	—	—	—	—	—	—
B19	—	—	—	—	—	—
A20	PRD_CFGN	RD_CFG	I	RD_CFG	External configuration read-back control.	PU
A19	PT12D	I/O-SECKUR	O	APC_ADDR(0)	APC processor interface address (LSB).	—
B18	—	—	—	—	—	—
B17	PT12C	I/O	I	TX_PAR	APC port transmit data parity.	NC
C17	PT12B	I/O	I	TX_DATA(15)	APC port transmit data bus bit 15.	—
D16	PT12A	I/O-RDY	O	APC_ADDR(1)	APC processor interface address.	—
A18	—	—	—	—	—	—
A17	PT11D	I/O	I	TX_DATA(14)	APC port transmit data bus.	—
C16	PT11C	I/O	I	TX_DATA(13)	APC port transmit data bus.	—
B16	PT11B	I/O	I	TX_DATA(12)	APC port transmit data bus.	—
A16	PT11A	I/O-D7	O	APC_ADDR(2)	APC processor interface address.	—
C15	—	—	—	—	—	—
D14	PT10D	I/O	I	TX_DATA(11)	APC port transmit data bus.	—
B15	PT10C	I/O	I	TX_DATA(10)	APC port transmit data bus.	—
A15	PT10B	I/O	I	TX_DATA(9)	APC port transmit data bus.	—

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Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
C14	PT10A	I/O-D6	O	APC_ADDR(3)	APC processor interface address.	—
B14	PT9D	I/O	I	TX_DATA(8)	APC port transmit data bus.	—
A14	PT9C	I/O	I	TX_DATA(7)	APC port transmit data bus.	—
C13	—	—	—	—	—	—
B13	PT9B	I/O	I	TX_DATA(6)	APC port transmit data bus.	—
A13	PT9A	I/O-D5	B	APC_DATA(24)	APC processor interface bus.	—
D12	PT8D	I/O	I	TX_DATA(5)	APC port transmit data bus.	—
C12	PT8C	I/O	I	TX_DATA(4)	APC port transmit data bus.	—
B12	PT8B	I/O	I	TX_DATA(3)	APC port transmit data bus.	—
A12	PT8A	I/O-D4	B	APC_DATA(25)	APC processor interface bus.	—
B11	PECKT	I-ECKT	I	APC_CLK	APC port UTOPIA clock.	—
C11	PT7C	I/O	I	TX_DATA(2)	APC port transmit data bus.	—
A11	PT7B	I/O	I	TX_DATA(1)	APC port transmit data bus.	—
A10	PT7A	I/O-D3	I	TX_DATA(0)	APC port transmit data bus (LSB).	—
B10	PT6D	I/O	T	RX_DATA(0)	APC port receive data bus (LSB).	—
C10	PT6C	I/O	T	RX_DATA(1)	APC port receive data bus.	—
D10	PT6B	I/O	T	RX_DATA(2)	APC port receive data bus.	—
A9	PT6A	I/O-D2	B	APC_DATA(26)	APC processor interface bus.	—
B9	PT5D	I/O-D1	T	RX_DATA(3)	APC port receive data bus.	—
C9	PT5C	I/O	T	RX_DATA(4)	APC port receive data bus.	—
D9	PT5B	I/O	T	RX_DATA(5)	APC port receive data bus.	—
A8	PT5A	I/O-D0/DIN	B	ISP_DATA	Serial configuration data input/output.	—
B8	PT4D	I/O	T	RX_DATA(6)	APC port receive data bus.	—
C8	PT4C	I/O	T	RX_DATA(7)	APC port receive data bus.	—
A7	PT4B	I/O	T	RX_DATA(8)	APC port receive data bus.	—
B7	PT4A	I/O-DOUT		Reserved	Configuration daisy-chain data output.	—
A6	PT3D	I/O	T	RX_DATA(9)	APC port receive data bus.	—
C7	PT3C	I/O	T	RX_DATA(10)	APC port receive data bus.	—
B6	PT3B	I/O	T	RX_DATA(11)	APC port receive data bus.	—
A5	PT3A	I/O-TDI	I	JTAG_TDI	JTAG Interface data input.	PU
D7	PT2D	I/O	T	RX_DATA(12)	APC port receive data bus.	—
C6	PT2C	I/O	T	RX_DATA(13)	APC port receive data bus.	—
B5	PT2B	I/O	T	RX_DATA(14)	APC port receive data bus.	—
A4	PT2A	I/O-TMS	I	JTAG_TMS	JTAG Interface mode input.	PU
C5	—	—	—	—	—	—
B4	PT1D	I/O	T	RX_DATA(15)	APC port receive data bus.	—
A3	PT1C	I/O	T	RX_PAR	APC port receive parity.	NC
D5	PT1B	I/O	B	APC_DATA(27)	APC processor interface bus.	—
C4	—	—	—	—	—	—

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Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge Implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
B3	—	—	—	—	—	—
B2	—	—	—	—	—	—
A2	PT1A	I/O-TCK	I	JTAG_TCK	JTAG interface clock input.	PU
C3	PRD_DATA	RD_DATA/TDO	O	JTAG_TDO	JTAG interface data output.	PU
A1	VSS	VSS	—	—	—	—
D4	VSS	VSS	—	—	—	—
D8	VSS	VSS	—	—	—	—
D13	VSS	VSS	—	—	—	—
D17	VSS	VSS	—	—	—	—
H4	VSS	VSS	—	—	—	—
H17	VSS	VSS	—	—	—	—
N4	VSS	VSS	—	—	—	—
N17	VSS	VSS	—	—	—	—
U4	VSS	VSS	—	—	—	—
U8	VSS	VSS	—	—	—	—
U13	VSS	VSS	—	—	—	—
U17	VSS	VSS	—	—	—	—
J9	VSS	VSS	—	—	—	—
J10	VSS	VSS	—	—	—	—
J11	VSS	VSS	—	—	—	—
J12	VSS	VSS	—	—	—	—
K9	VSS	VSS	—	—	—	—
K10	VSS	VSS	—	—	—	—
K11	VSS	VSS	—	—	—	—
K12	VSS	VSS	—	—	—	—
L9	VSS	VSS	—	—	—	—
L10	VSS	VSS	—	—	—	—
L11	VSS	VSS	—	—	—	—
L12	VSS	VSS	—	—	—	—
M9	VSS	VSS	—	—	—	—
M10	VSS	VSS	—	—	—	—
M11	VSS	VSS	—	—	—	—
M12	VSS	VSS	—	—	—	—
B1	VDD	VDD	—	—	—	—
D6	VDD	VDD	—	—	—	—
D11	VDD	VDD	—	—	—	—
D15	VDD	VDD	—	—	—	—
F4	VDD	VDD	—	—	—	—
F17	VDD	VDD	—	—	—	—

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Pin Assignments (continued)

Table 3. Interfaces for the *PayloadPlus*/APC Bridge implemented in an OR3T20-7BA256 (continued)

Pin	Pad	OR3T20	Type	Name	Description	Note*
K4	VDD	VDD	—	—	—	—
L17	VDD	VDD	—	—	—	—
R4	VDD	VDD	—	—	—	—
R17	VDD	VDD	—	—	—	—
U6	VDD	VDD	—	—	—	—
U10	VDD	VDD	—	—	—	—
U15	VDD	VDD	—	—	—	—

* The symbols contained in this column describe special connection requirements. The symbol meanings are as follows: PU—requires a pull up resistor, PD—requires a pull down resistor, NC—not connected, 1—must be tied high, LED—connected to a light emmitting diode.

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