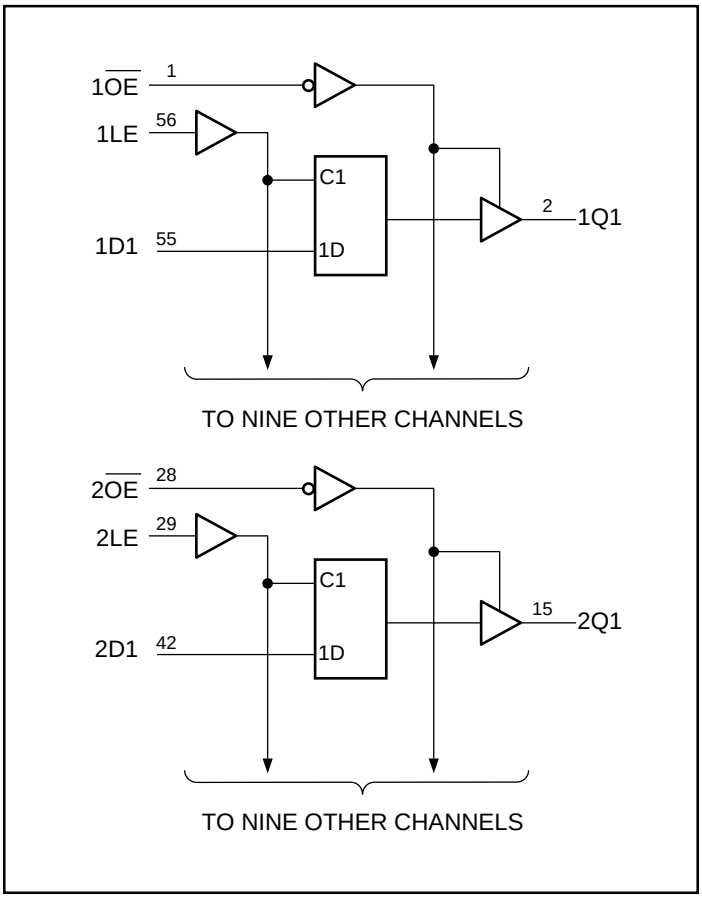
PI74AVC+16841

2.5V 20-Bit Bus Interface D-Type Latch with 3-State Outputs

Product Features

- PI74AVC+16841 is designed for low-voltage operation, V_{CC} = 1.65V to 3.6V
- True ±24mA Balanced Drive @ 3.3V
- I_{OFF} supports partial power-down operation
- 3.6V I/O Tolerant Inputs and Outputs
- All outputs contain a patented DDC (Dynamic DriveControl) circuit that reduces noise without degrading propagation delay.
- Industrial operation: –40°C to +85°C
- Available Packages:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 173 mil wide plastic TVSOP (K)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16841, a 20-bit bus-interface D-type latch, is designed for 1.65V to 3.6V V_{CC} operation.

The device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The device can be used as two 10-bit latches or one 20-bit latch (transparent D-type). The device has noninverting Data (D) inputs and provides true data at its outputs. While the Latch Enable (1LE or 2LE) input is HIGH, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken LOW, the Q outputs are latched at the levels set up at the D inputs.

A buffered Output Enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In that state, outputs neither load nor drive the bus lines significantly.

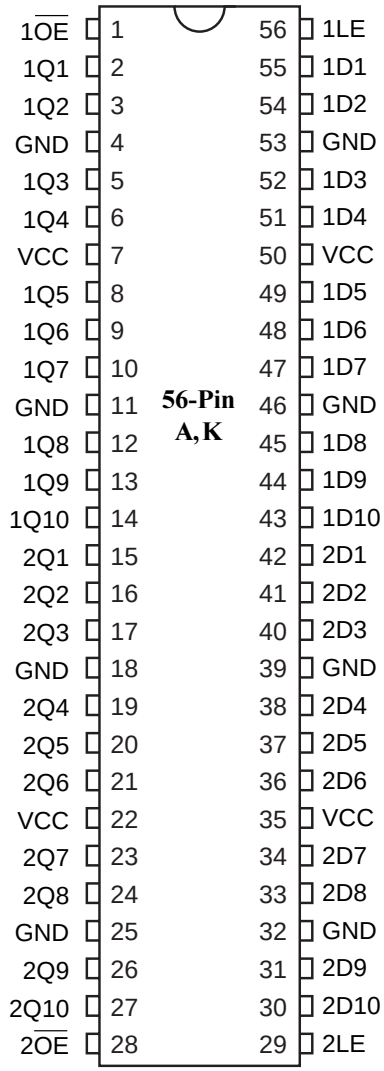
The Output Enable ($\overline{OE}$) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable
D	Data Input
Q	Data Output
GND	Ground
V_{CC}	Power

Product Pin Configuration



Truth Table[1] Each 10-Bit Latch

Inputs			Outputs
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

Note:

1. H= High Signal Level
   L = Low Signal Level
   Z = High Impedance
   X= Irrelevant

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC} ..... –0.5V to +4.6V
Input voltage range, V_I ..... –0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, V_O[1] ..... –0.5V to +4.6V
Voltage range applied to any output in the high or low state, V_O[1,2] ..... –0.5V to V_{CC}+0.5V
Input clamp current, I_{IK} (V_I <0) ..... –50mA
Output clamp current, I_{OK} (V_O <0) ..... –50mA
Continuous output current, I_O ..... ±50mA
Continuous current through each V_{CC} or GND ..... ±100mA
Package thermal impedance, θ_{JA}[3]: package A ..... 64°C/W
package K ..... 48°C/W
Storage Temperature range, T_{stg} ..... –65°C to 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:
1. Input & output negative-voltage ratings may be exceeded if the input and output curent rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if theoutput current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions[1]

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	V_{CC} = 1.2V	V_{CC}		
	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
	V_{CC} = 2.3V to 2.7V	1.7		
	V_{CC} = 3V to 3.6V	2		
V_{IL} Low-level Input Voltage	V_{CC} = 1.2V		GND	
	V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
	V_{CC} = 2.3V to 2.7V		0.7	
	V_{CC} = 3V to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	V_{CC} = 1.65V to 1.95V		– 6	mA
	V_{CC} = 2.3V to 2.7V		– 12	
	V_{CC} = 3V to 3.6V		– 24	
I_{OL} Low-level output current	V_{CC} = 1.65V to 1.95V		6	
	V_{CC} = 2.3V to 2.7V		12	
	V_{CC} = 3V to 3.6V		24	
DtDv Input transition rise or fall rate	V_{CC} = 1.65V to 3.6V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Notes:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C +85°C)

Parameters		Test Conditions[1]	V_{CC}	Min.	Max.	Units
V_{OH}		I_{OH} = –100µA	1.65V to 3.6V	V_{CC} –0.2V		V
		I_{OH} = –6mA V_{IH} = 1.07V	1.65V	1.2		
		I_{OH} = –12mA V_{IH} = 1.7V	2.3V	1.75		
		I_{OH} = –24mA V_{IH} = 2V	3V	2.0		
V_{OL}		I_{OL} = 100µA	1.65V to 3.6V		0.2	
		I_{OL} = 6mA V_{IH} = 0.57V	1.65V		0.45	
		I_{OL} = 12mA V_{IH} = 0.7V	2.3V		0.55	
		I_{OL} = 24mA V_{IH} = 0.8V	3V		0.8	
I_I	Control Inputs	V_I = V_{CC} or GND	3.6V		±2.5	µA
I_{OFF}		V_I or V_O = 3.6V	0		±10	
I_{OZ}		V_I = V_{CC} or GND	3.6V		±10	
I_{CC}		V_O = V_{CC} or GND I_O = 0	3.6V		40	
C_I	Control Inputs	V_I = V_{CC} or GND	2.5V		4	pF
			3.3V		4	
	Data Inputs		2.5V		6	
			3.3V		6	
C_O	Outputs	V_O = V_{CC} or GND	2.5V		8	
			3.3V		8	

Note:
1. Typical values are measured at T_A = 25°C.

Timing requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

	V_{CC} = 1.2V		V_{CC} = 1.5V ± 0.1V		V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_w Pulse duration, LE HIGH					2.2		2.0		1.8		ns
t_{su} Setup time, data before LE↓	1.7		1.2		1.1		0.9		0.8		
t_h Hold time, data after LE↓	2		1.1		1.1		1.1		0.9		

Switching Characteristics

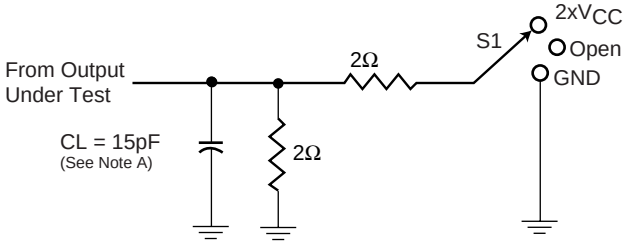
(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

Parameters	From (Input)	To (Output)	V_{CC} = 1.2V	V_{CC} = 1.5V ± 0.1V		V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Units
			Typ.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{pd}	D	Q	6.0	1.2	4.6	1	4.0	0.8	3.1	0.7	2.6	ns
	LE		7.0	1.4	4.8	1.1	4.0	0.8	3.0	0.7	2.8	
t_{en}	$\overline{OE}$	Q	6.0	1.6	4.2	1.6	4.0	1.4	3.5	0.7	3.1	
t_{dis}	$\overline{OE}$	Q	6.0	2.5	5.8	2.3	5.5	1.3	3.4	1.2	3.4	

Operating Characteristics, T_A=25°C

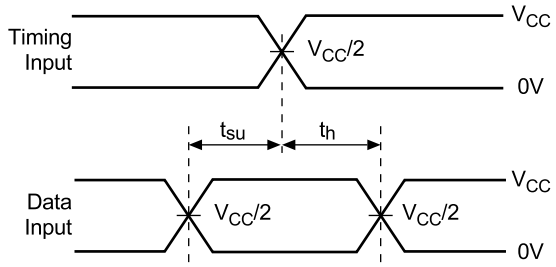
Parameters		Test Conditions	V_{CC} = 1.8V ±0.15V	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz	50	53	59	pF
	Outputs Disabled		25	28	30	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.2V and 1.5V ±0.1V

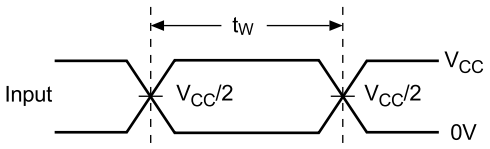


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

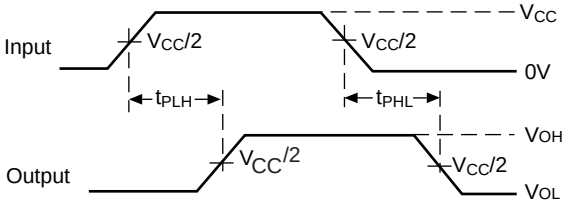
Load Circuit



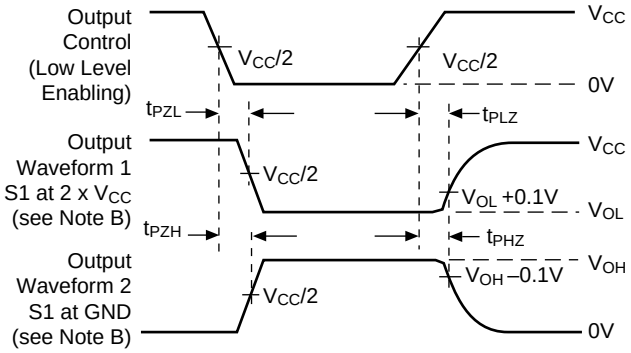
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



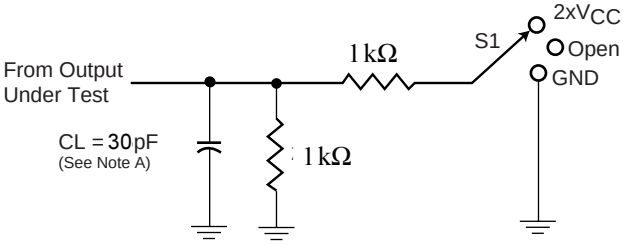
Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

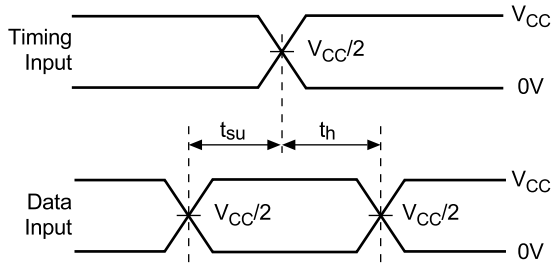
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8V ±0.15V

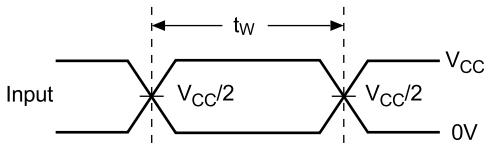


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

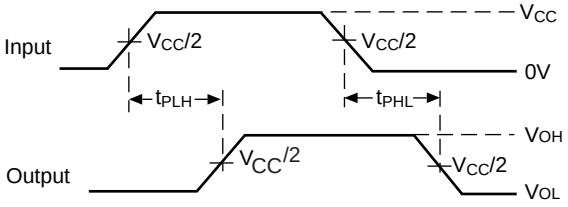
Load Circuit



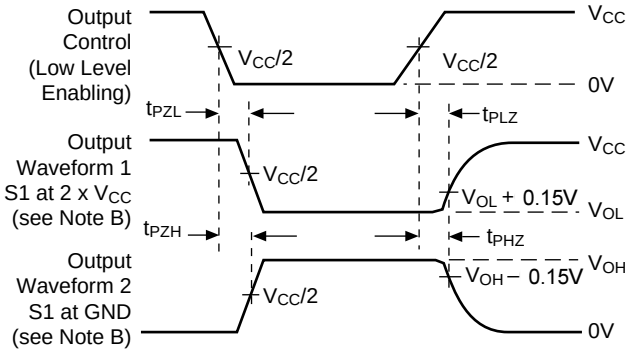
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



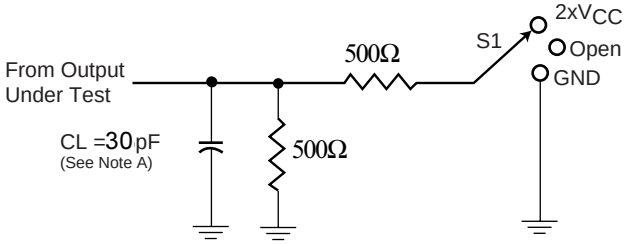
Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

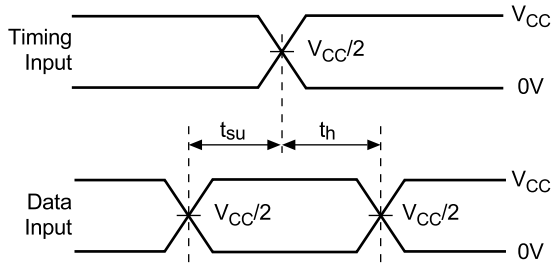
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

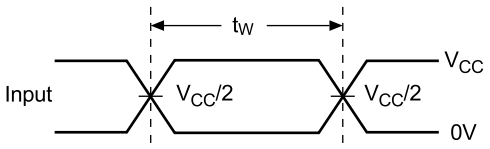


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

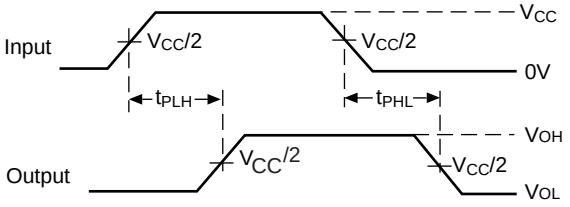
Load Circuit



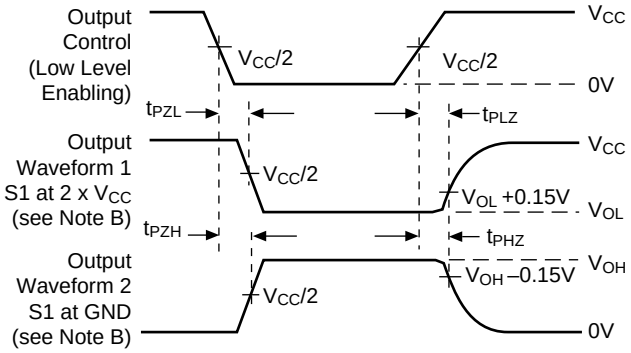
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



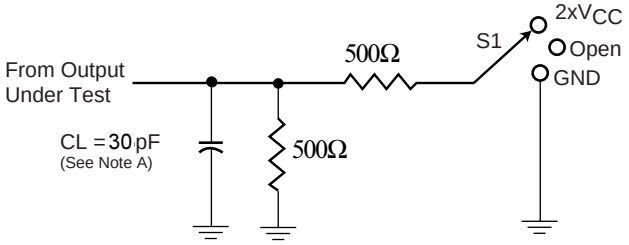
Voltage Waveforms
Enable and Disable Times

Figure 3. Load Circuit and Voltage Waveforms

Notes:

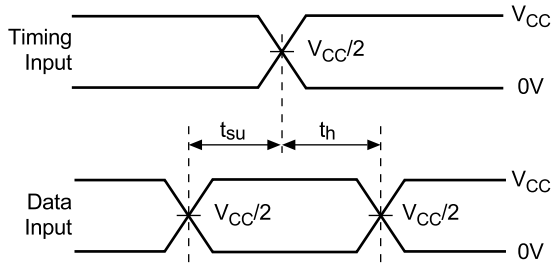
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3V ±0.3V

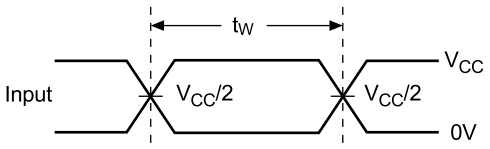


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

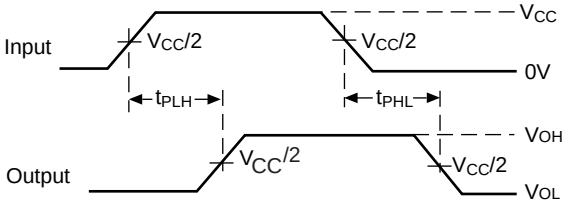
Load Circuit



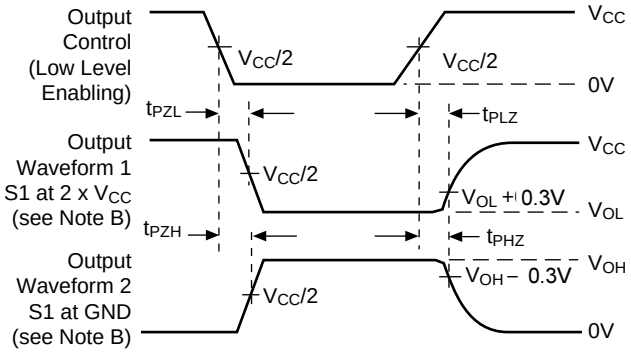
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



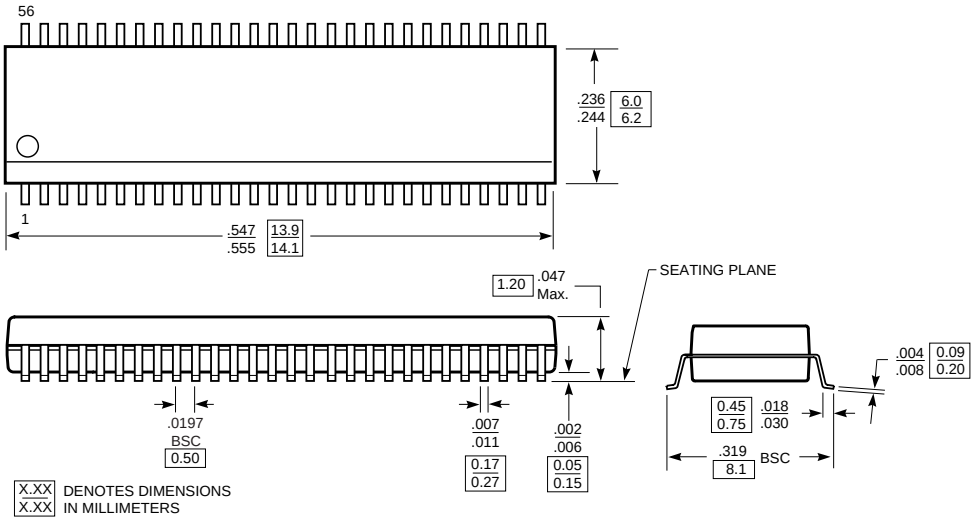
Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

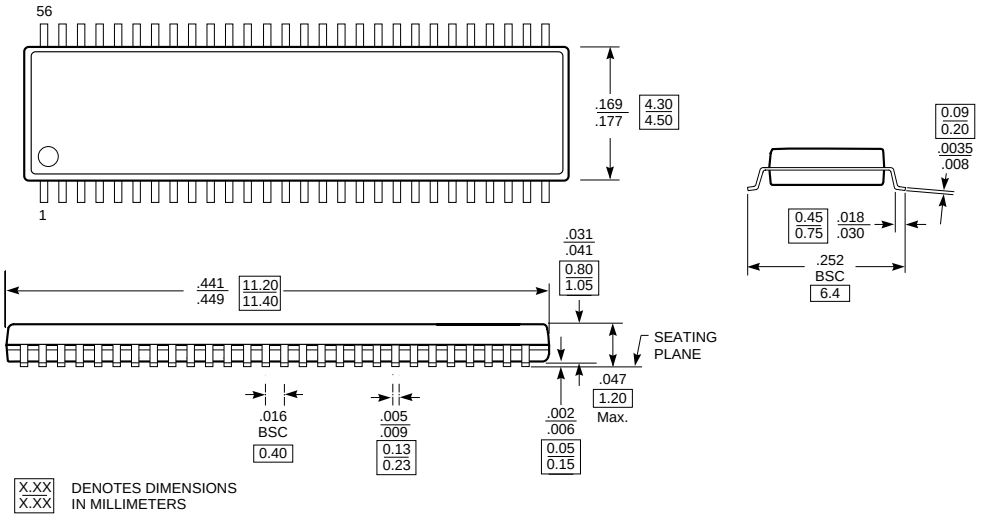
Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

56-pin TSSOP (A) Package



56-pin TVSOP (K) Package



Ordering Information

Ordering Data	Description
PI74AVC+16841A	56-pin, 240-mil wide plastic TSSOP
PI74AVC+16841K	56-pin, 173-mil wide plastic TVSOP