Hardware Reference Manual, DS 1, Feb. 2001

SICOFI®4-TE

Four Channel Codec Filter for Terminal Application

PSB 2134 Version 2.2

Wired Communications

Infineon technologies

Never stop thinking.

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Preface

This document provides detailed technical information about the SICOFI®4-TE. It is intended for anyone considering or using the device for system design or board layout for a broad range of analog telephony applications.

Organization of this Document

This Hardware Reference Manual is organized as follows:

- Chapter 1, Overview
  Includes a general description of the architecture, feature list, and logic symbol.
- Chapter 2, Pin Descriptions
  Illustrates the Pin Configuration and provides detailed functional descriptions.
- Chapter 3, Functional Description
  Provides a block diagram and summarizes the major functional blocks.
- Chapter 4, Operational Description
  Begins with a state diagram and description of the operating states of all four channels and concludes with detailed transmission characteristics.
- Chapter 5, Interface Descriptions
  Describes the Analog, IOM-2 PCM, Signaling, and Serial Microcontroller interfaces.
- Chapter 6, Programming Overview
  Illustrates the register model and coefficient RAM structure, provides a register map and summary, and identifies the programming command sequences.
- Chapter 7, Application Hints
  Describes the development system available for the PSB 2134, and provides guidelines and schematics for board layout.
- Chapter 8, Electrical Characteristics and Timing Diagrams
  Provides detailed tables for the electrical characteristics and includes timing diagrams for the Analog, IOM-2 PCM, Serial Microcontroller, and Signaling interfaces.
- Chapter 9, Test Configuration
  Describes the test loops and cut-offs available for functional tests and diagnostics.
- Chapter 10, Package Outlines
  Illustrates the P-MQFP-64 package in which the PSB 2134 is manufactured.
- The Appendix
  Includes a glossary and an index.

Related Documentation

Other documentation for the PSB 2134 includes a *Product Brief*, a *Product Overview*, a *Programmer's Reference Manual*, and assorted *Application Notes*. Similar documentation is also available for the other members of the SICOFI Codec family including the PSB 2132, PEB 2466, and PEB 2266. Documentation is available by accessing our website: http://www.infineon.com/sicofi

1 Overview

The four-channel codec filter PSB 2134 SICOFI®4-TE is built around a central DSP-core which provides independent filter structures for all channels. Its analog I/O pins are used to connect to external subscriber line interface circuits (SLICs). Their signals are internally routed to the analog-to-digital and digital-to-analog converters (ADC, DAC). The signaling pins carry line status and control information to and from the SLICs. Two programmable clock outputs are available. The SICOFI®4-TE's IOM-2 PCM Interface connects directly to a 768 kbit/s IOM-2 bus, often used in terminal equipment. The digitized voice band signals are available as A-Law or µ-Law codes within selectable 8-bit time slots.

The SICOFI®4-TE modes, features, and filter characteristics are programmed through a serial interface to a microcontroller. The access mechanism is very simple, and can be implemented with as few as three I/O ports.

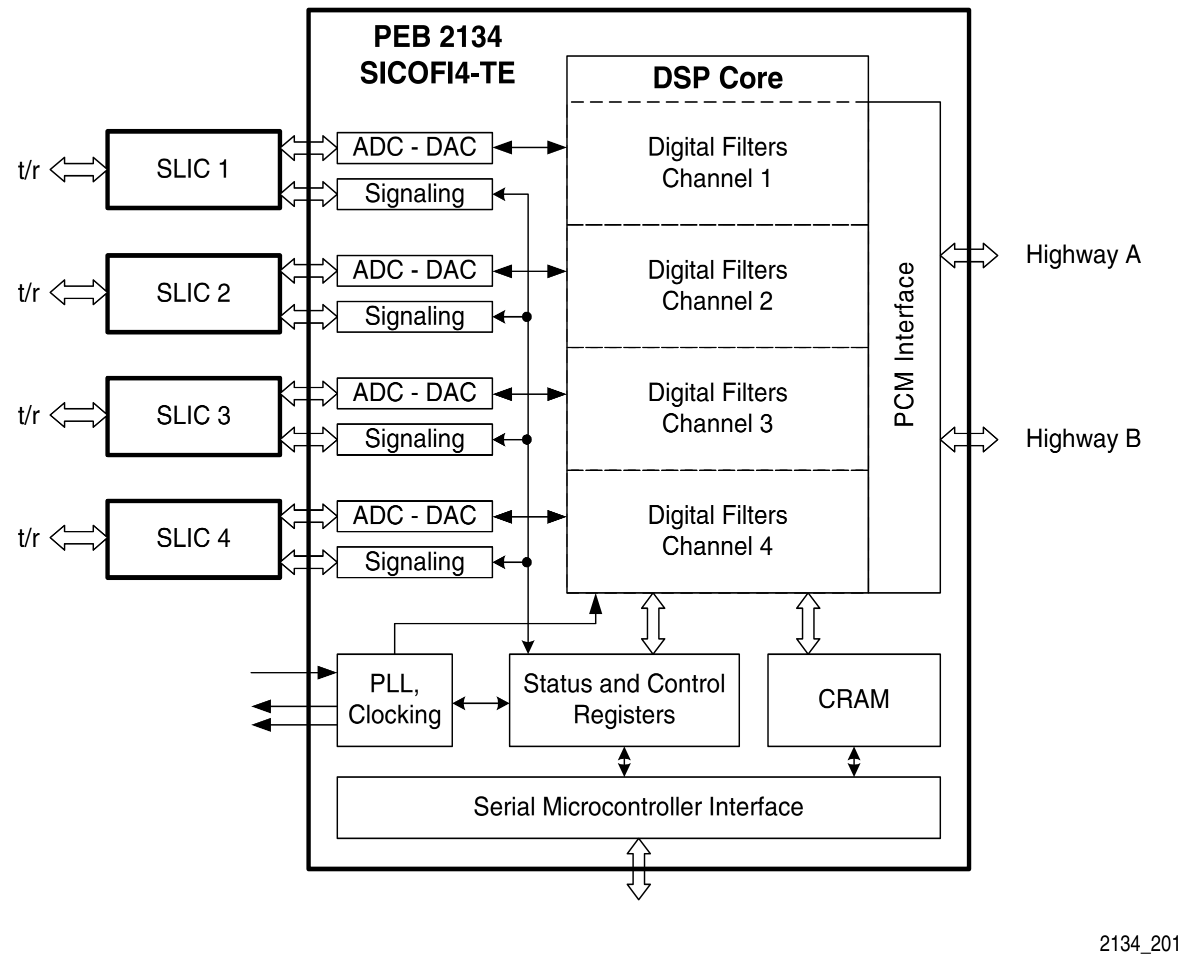


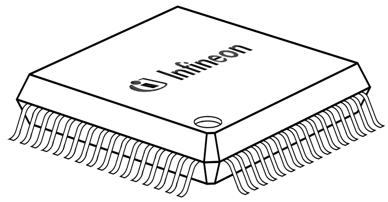
Figure 1 SICOFI®4-TE Architecture

Four Channel Codec Filter with PCM and Microcontroller Interface SICOFI®4-TE

PSB 2134

Version 2.2 **CMOS**

1.1 Features



P-MQFP-64

- Four-channel single chip codec with digital filters
- High analog driving capability (300 Ω, 50 pF) for direct driving of transformers
- Digital Signal Processing (DSP) technique
- Programmable digital filters to adapt transmission behavior, especially for:
  - AC impedance matching
  - Transhybrid balancing
  - Frequency response
  - Signal levels
  - A/µ-Law compression and expansion
- High performance ADC and DAC for excellent linearity and dynamic gain
- Programmable Analog Interface to electronic SLICs or transformer solutions
- Seven SLIC-signaling I/O pins per channel with programmable debouncing
- IOM-2 compatible PCM interface (1.536 MHz DCL, 768 kHz Bit Clock)
- Easy to use 4-pin Serial Microcontroller Interface (SPI compatible) for read/write access
- Single supply voltage (5 V)
- Advanced low-power mixed-signal CMOS technology
- Two programmable tone generators per channel (DTMF possible)
- Level metering function for system tests and for analog input signal testing
- Advanced on-chip functions for device and system diagnostics and manufacturing test
  - Five digital loops
  - Four analog loops
- Support tools include:
  - Hardware development board — STUT 2466
  - QSICOS Coefficient Calculation and Register Configuration Software
- Standard P-MQFP-64 package

Type	Package
PSB 2134 Version 2.2	P-MQFP-64

1.2 Logic Symbol

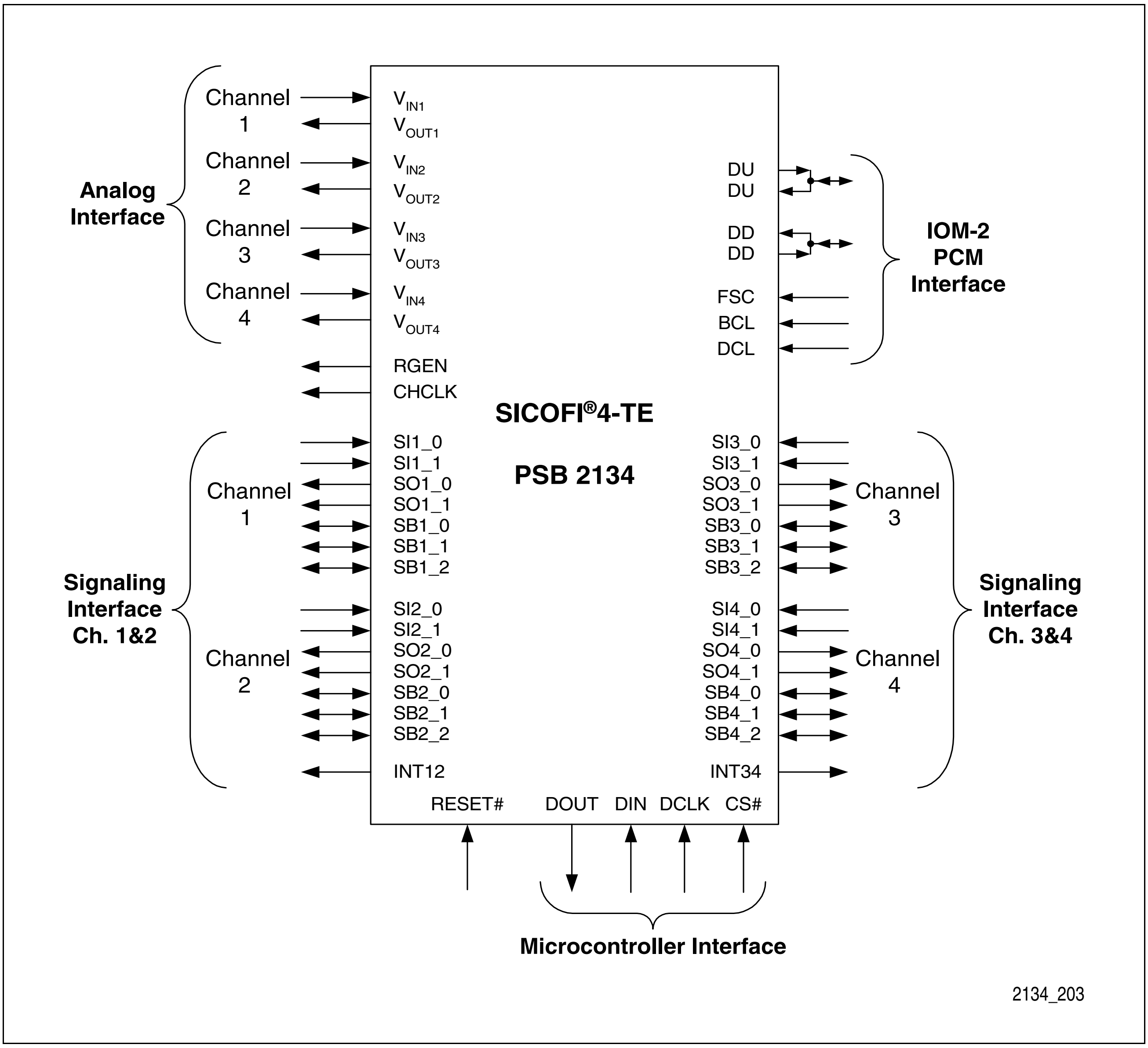


Figure 2 SICOFI®4-TE Logic Symbol

1.3 Typical Applications

Many applications will benefit from the versatility of the SICOFI®4-TE codec and filter. The inherent flexibility enables several products to be developed around one basic architecture, thus affording potentially significant savings in time to market, inventory costs, and support administration.

The following list represents some of the typical applications for which the SICOFI®4-TE codec was designed: Small PBX, Terminal Adapters, and intelligent NTs. Refer to the ***Product Overview***, **Chapter 5 Application Hints** for more information.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

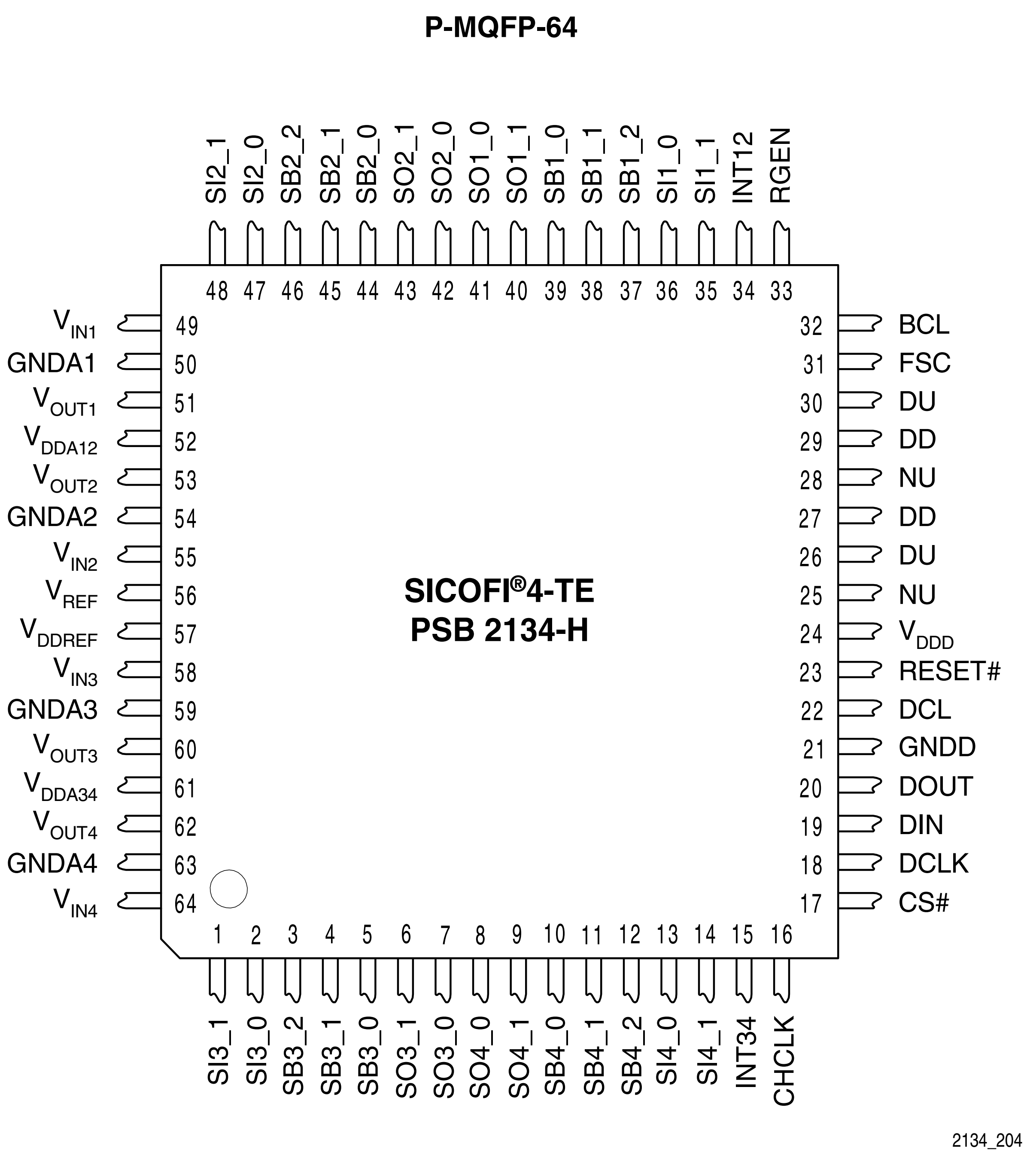


Figure 3 Pin Configuration of SICOFI®4-TE

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin	Symbol	Type	Function	Ch.
1	SI3_1	I	**Signaling Input, Channel 3 Pin 1**	3
2	SI3_0	I	**Signaling Input, Channel 3 Pin 0**	3
3	SB3_2	I/O	**Bi-directional Signaling, Channel 3 Pin 2**	3
4	SB3_1	I/O	**Bi-directional Signaling, Channel 3 Pin 1**	3
5	SB3_0	I/O	**Bi-directional Signaling, Channel 3 Pin 0**	3
6	SO3_1	O	**Signaling Output, Channel 3 Pin 1**	3
7	SO3_0	O	**Signaling Output, Channel 3 Pin 0**	3
8	SO4_0	O	**Signaling Output, Channel 4 Pin 0**	4
9	SO4_1	O	**Signaling Output, Channel 4 Pin 1**	4
10	SB4_0	I/O	**Bi-directional Signaling, Channel 4 Pin 0**	4
11	SB4_1	I/O	**Bi-directional Signaling, Channel 4 Pin 1**	4
12	SB4_2	I/O	**Bi-directional Signaling, Channel 4 Pin 2**	4
13	SI4_0	I	**Signaling Input, Channel 4 Pin 0**	4
14	SI4_1	I	**Signaling Input, Channel 4 Pin 1**	4
15	INT34	O	**Interrupt Output Channels 3 and 4** Active high; only valid if DCL with 1.526 MHz is applied	3, 4
16	CHCLK	O	**Chopper Clock Output** Provides 256, 512, or 16,384 kHz signal; sync. to DCL.	all
17	CS#	I	**Chip Select** Microcontroller Interface chip select, enable to read or write; active low	all
18	DCLK	I	**Data Clock** Microcontroller Interface data clock, shifts data from or to device; maximum clock rate 8192 kHz.	all
19	DIN	I	**Data Input** Microcontroller Interface control data input pin; DCLK determines data rate.	all
20	DOUT	O	**Data Output** Microcontroller Interface control data output pin; DCLK determines data rate: DOUT is high impedance "Z" if no data is transmitted from the SICOFI®4-TE.	all

Pin	Symbol	Type	Function	Ch.
21	GNDD	I	**Digital Ground** Ground reference for all digital signals. Internally isolated from GNDA1(Pin 50), GNDA2 (Pin 54), GNDA3 (Pin 59), and GNDA4 (Pin 63).	all
22	DCL	I	**Master Clock Input** 1536 kHz signal must be applied for any operation. DCL, BCL, and FSC must be synchronous.	all
23	RESET#	I	**Reset Input** Forces the device to default setting mode; active low.	all
24	V_{DDD}	I	**Digital Supply Voltage** +5 V supply for digital circuits (use 100 nF blocking cap.).	all
25	NU		**None Usable** Leave unconnected.	
26	DU	I/O/ tri-state	**IOM-2 Data Upstream** Interface together with Pin 30. Both pins must be connected together. Transmits or receives PCM data in 8-bit bursts every 125 µs. With push-pull resistor.	all
27	DD	I/O/ tri-state	**IOM-2 Data Downstream** Interface together with Pin 29. Both pins must be connected together. Transmits or receives PCM data in 8-bit bursts every 125 µs. With push-pull resistor.	all
28	NU		**None Usable** Leave unconnected.	
29	DD	I/O/ tri-state	**IOM-2 Data Downstream** Interface together with pin 27. Both pins must be connected together. Transmits or receives PCM data in 8 bit bursts every 125 µs. With push-pull resistor.	all
30	DU	I/O/ tri-state	**IOM-2 Data Upstream** Interface together with pin 26. Both pins must be connected together. Transmits or receives PCM data in 8 bit bursts every 125 µs. With push-pull resistor.	all
31	FSC	I	**Frame Synchronization Clock** 8 kHz; reference for individual time slots, indicates start of PCM frame; DCL, BCL, and FSC must be synchronous.	all

Pin	Symbol	Type	Function	Ch.
32	BCL	I	**IOM-2 Bit Clock** Determines rate at which PCM data is shifted into or out of PCM-ports. BCL, DCL, and FSC must be synchronous. If C-MODE = 0 in XR6, single clocking mode is used; 768 kHz must be applied to BCL. If C-MODE = 1 in XR6, double clocking is used; 1536 kHz must be applied to BCL. The data rate at the PCM ports remains 768 kbit/s.	all
33	RGEN	O	**Ring Generator Output** Configurable output clock (T = 2 … 28 ms), synchronous to DCL. Square-wave signal with duty cycle 1:1.	all
34	INT12	O	**Interrupt Output, Channels 1 and 2** Active high; only valid if DCL with 1.526 MHz is applied	1, 2
35	SI1_1	I	**Signaling Input Channel 1, Pin 1**	1
36	SI1_0	I	**Signaling Input Channel 1, Pin 0**	1
37	SB1_2	I/O	**Bi-directional Signaling, Channel 1 Pin 2**	1
38	SB1_1	I/O	**Bi-directional Signaling, Channel 1 Pin 1**	1
39	SB1_0	I/O	**Bi-directional Signaling, Channel 1 Pin 0**	1
40	SO1_1	O	**Signaling Output, Channel 1, Pin 1**	1
41	SO1_0	O	**Signaling Output, Channel 1, Pin 0**	1
42	SO2_0	O	**Signaling Output, Channel 2, Pin 0**	2
43	SO2_1	O	**Signaling Output, Channel 2, Pin 1**	2
44	SB2_0	I/O	**Bi-directional Signaling, Channel 2 Pin 0**	2
45	SB2_1	I/O	**Bi-directional Signaling, Channel 2 Pin 1**	2
46	SB2_2	I/O	**Bi-directional Signaling, Channel 2 Pin 2**	2
47	SI2_0	I	**Signaling Input, Channel 2, Pin 0**	2
48	SI2_1	I	**Signaling Input, Channel 2, Pin 1**	2

Pin	Symbol	Type	Function	Ch.
49	V_{IN1}	I	**Analog Voice (Voltage) Input, Channel 1** Requires a coupling capacitor >39 nF to the SLIC.	1
50	GNDA1	I	**Analog Ground, Channel 1** Internally isolated from GNDD (Pin 21), GNDA2 (Pin 54), GNDA3 (Pin 59), and GNDA4 (Pin 63).	1
51	V_{OUT1}	O	**Analog Voice (Voltage) Output, Channel 1** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance. (See Chapter **5.1 Analog Interface**)	1
52	V_{DDA12}	I	**Analog Supply Voltage**, **Channels 1 and 2** +5 V (100 nF blocking capacitor required).	1, 2
53	V_{OUT2}	O	**Analog Voice (Voltage) Output, Channel 2** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance. (See Chapter **5.1 Analog Interface**)	2
54	GNDA2	I	**Analog Ground, Channel 2** Internally isolated from GNDD (Pin 21), GNDA1 (Pin 50), GNDA3 (Pin 59), and GNDA43 (Pin 63).	2
55	V_{IN2}	I	**Analog Voice (Voltage) Input**, **Channel 2** Requires a coupling capacitor >39 nF to the SLIC.	2
56	V_{REF}	I/O	**Reference Voltage** Must connect to a 220 nF cap. to ground.	all
57	V_{DDREF}	I	**Analog Supply Reference Voltage** +5 V (100 nF blocking capacitor required).	all
58	V_{IN3}	I	**Analog Voice (Voltage) Input, Channel 3** Requires a coupling capacitor >39 nF to the SLIC.	3
59	GNDA3	I	**Analog Ground, Channel 3** Internally isolated from GNDD (Pin 21), GNDA1 (Pin 50), GNDA2 (Pin 54), and GNDA4 (Pin 63).	3
60	V_{OUT3}	O	**Analog Voice (Voltage) Output, Channel 3** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance. (See Chapter **5.1 Analog Interface**)	3
61	V_{DDA34}	I	**Analog Supply Voltage, Channels 3 and 4** +5 V (100 nF blocking capacitor required).	3

Pin	Symbol	Type	Function	Ch.
62	V_{OUT4}	O	**Analog Voice (Voltage) Output, Channel 4** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance. (See Chapter **5.1 Analog Interface**)	4
63	GNDA4	I	**Analog Ground, Channel 4** Internally isolated from GNDD (Pin 21), GNDA1 (Pin 50), GNDA2 (Pin 54), and GNDA3 (Pin 59).	4
64	V_{IN4}	I	**Analog Voice (Voltage) Input**, **Channel 4** Requires a coupling capacitor >39 nF to the SLIC.	4

3 Functional Description

The SICOFI®4-TE in combination with four Subscriber Line Interface Circuits (SLIC) provides four analog telephone lines. The SLIC can be either a transformer or an electronic circuit with operational amplifiers. It must have a defined input impedance towards the analog line for maximum power transfer and return loss. Also, the signal reflections that are generated by the hybrid inside the SLIC must be eliminated. Along with its other features, the SICOFI®4-TE has built-in impedance matching and transhybrid balancing to perform these tasks.

3.1 DSP-based Architecture

The impedance matching and transhybrid balancing functions are performed by loop filters between the transmit path (analog to PCM) and the receive path (PCM to analog). The filter characteristics must be adjusted according to the local requirements of each market. In the analog domain, filters must be optimized in hardware; this is generally both tedious and time-consuming. This is not the case with the DSP-based SICOFI®4-TE four-channel codec. Its integrated signal processor implements the impedance matching and transhybrid balancing functions as digital, programmable filters. It also performs frequency response corrections and level adjustments to enable the design of a truly universal and internationally applicable analog telephone interface. Transmission characteristics and frequency behavior are enhanced by the accuracy of the digital filters, which do not fluctuate over temperature or with age.

As an additional benefit of its DSP-based architecture, the PSB 2134 also provides two tone generators per channel. An on-chip level-metering unit allows line-characterization without extra hardware; it can also be used to detect specific tones, e.g., modem tones.

3.2 Programming and Control

A very simple Microcontroller Interface is used to program the SICOFI®4-TE functions. The same port provides access to 28 general purpose I/O pins of the Signaling Interface. This allows efficient and convenient monitoring and control of other tip/ring functions, such as on-/off-hook detection, ground-key detection, switching of ring signals and test relays. The Serial Microcontroller Interface provides a programming and control interface and is generic and non-proprietary for use with any microcontroller. It can be implemented with as few as three signal lines, since the data receive and data transmit pins may be strapped together.

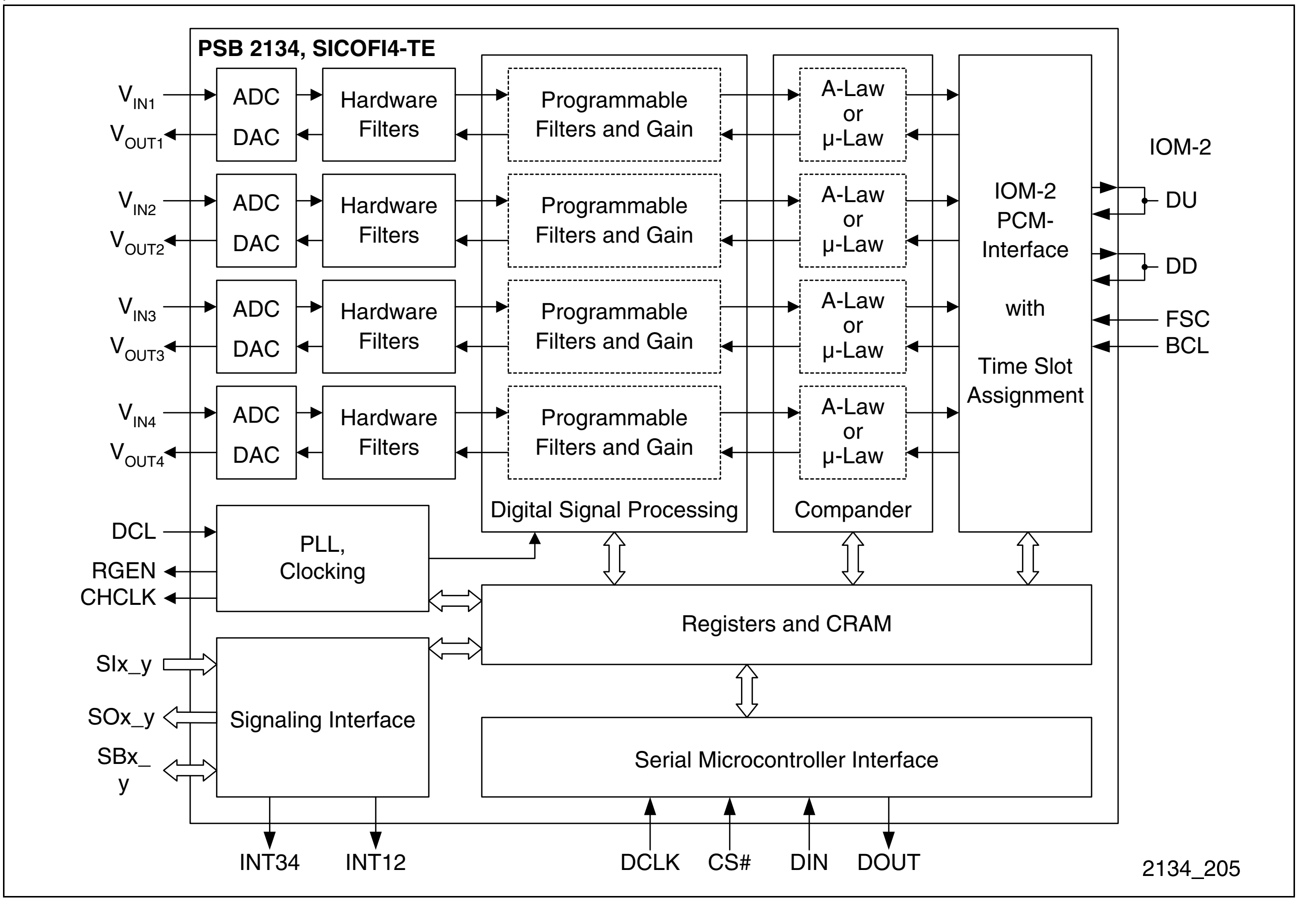


Figure 4 SICOFI®4-TE Block Diagram

Figure 4 shows the functional blocks and the interface pins of the SICOFI®4-TE:

- Four independent bi-directional voice channels;
- Oversampling sigma-delta A/D and D/A converters with excellent resolution, dynamic range, linearity, accuracy and signal-to-noise performance;
- Hardware filters for decimation and interpolation of the ADC and DAC bit stream, and pre-processing of the voice data to reduce the load of the DSP;
- DSP core with programmable, channel-independent filter structures for impedance matching, transhybrid balancing, frequency correction and level adjustments;
- Configurable A-Law or µ-Law compressor and expander units;
- An IOM-2 PCM interface with time slot assignment, one input and one output connected to DU, and one input and one output connected to DD;
- Three clock inputs, DCL, BCL, and FSC also apply to the IOM-2 PCM Interface;
- 28 signaling input and output pins, accessible through registers;
- Two interrupt outputs, one for each channel-pair 1&2, and 3&4;
- On-chip PLL for an internal 16,384 kHz clock;
- Eight common configuration registers (XR-Registers) affecting all four channels;
- Four sets of six channel-specific registers (CR-Registers);
- Coefficient RAM (CRAM) for filter coefficients storage for each channel; and
- The Serial Microcontroller Interface has four signals: DIN, DOUT, DCLK, and CS#.

4 Operational Description

Each channel of the SICOFI®4-TE can be in one of two stable states: “Standby” and “Operating”. These states can be switched by programming Bit 0 (PU) in the channel-specific configuration register CR1. “Standby” is a power-saving state. Keeping all unused channels in this state reduces the overall system power dissipation. The third state, “Reset”, is transient and is reached after applying power to the device (Power On), after asserting a logic low signal to the RESET#-pin (HW-Reset), or after issuing an XOP command with Bit 7 (RST) set to "1" (SW-Reset). All four channels would be affected in any case.

4.1 Operating States

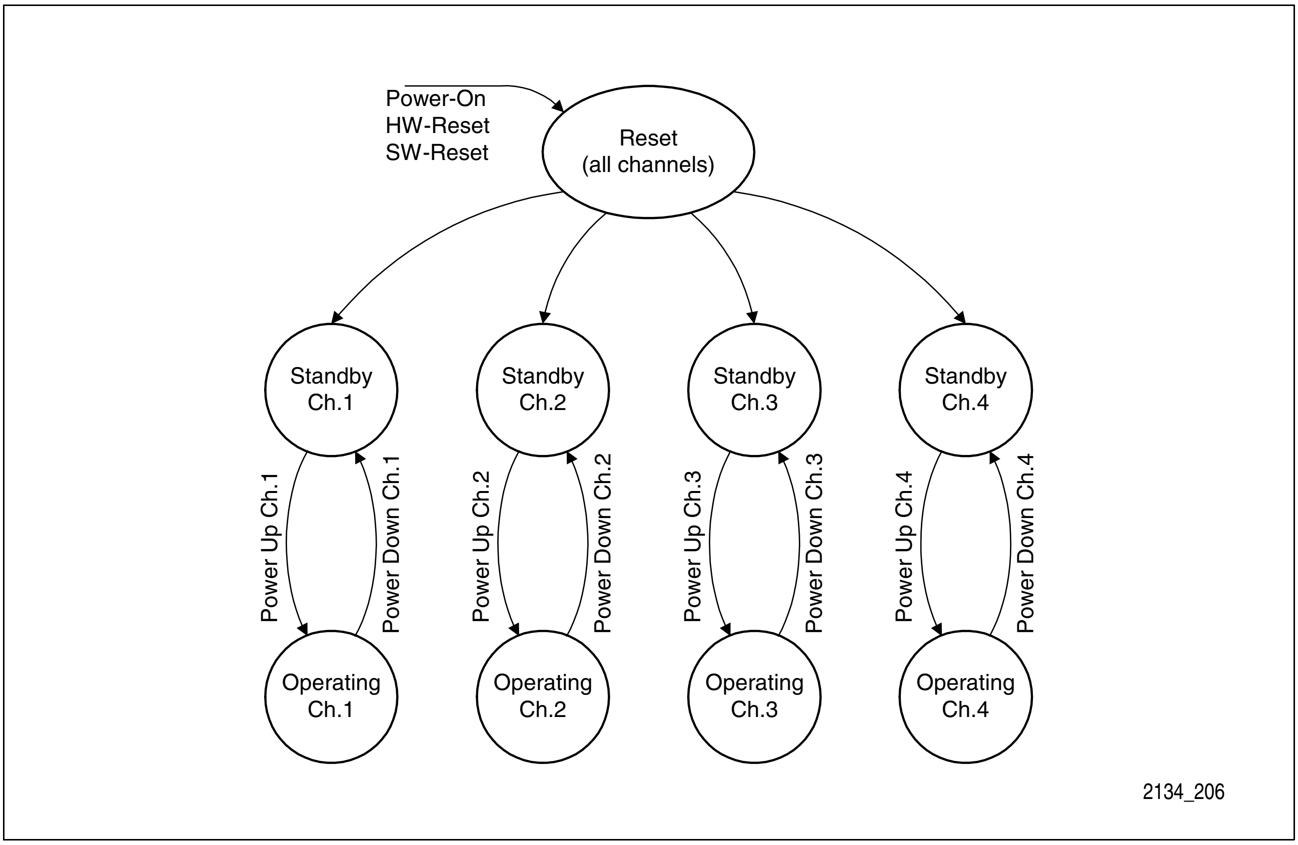


Figure 5 SICOFI®4-TE State Diagram

4.1.1 Power On

All input pins must be at GND level before applying VDD to the SICOFI®4-TE. Otherwise, the device may not enter the Reset State. In this case, the SICOFI®4-TE can be reset by HW- or SW-Reset, or can be initialized by setting all registers to zero.

4.1.2 Hardware Reset

Voltage levels lower than 1.2 V applied to Pin 23 (RESET#) for more than 3 µs will reset the SICOFI®4-TE. Spikes that are shorter than 1 µs will be ignored. When RESET# is released the SICOFI®4-TE will enter Standby State.

Table 2 Register Values and Accessibility

Register	SICOFI®4-TE State		
	Reset	Standby	Operating
CR0... CR4	00_H	user configurable	user configurable
XR0... XR7	00_H	user configurable	user configurable
CRAM	unchanged	user configurable	user configurable

Table 3 Input and Output Pin Behaviorr

Pin	SICOFI®4-TE State		
	Reset	Standby	Operating
DIN	ignored	serial input	serial input
DOUT	high impedance	serial output	serial output
DU, DD	inactive	inactive	receiving/transmitting PCM data during programmed time slot
V_{OUT1} , V_{OUT2} , V_{OUT3} , V_{OUT4}	high impedance	high impedance	analog output
V_{IN1} , V_{IN2} , V_{IN3} , V_{IN4}	ignored	ignored	analog input
SBx_y	configured as input	programmable as input or output	programmable as input or output
SOx_y	GNDD	digital output	digital output
SIx_y	ignored	digital input	digital input
RGEN	high	programmable frequency	programmable frequency
CHCLK	high	programmable freq. (not 16,384 kHz)	programmable frequency

Note: The 1536 kHz DCL clock must be applied for all device functions.

Table 4 Power Dissipation

No. of Channels Operating	Typical Power Dissipation
None	2.5 mW
1	70 mW
2	90 mW
3	110 mW
4	130 mW

4.2 Transmission Characteristics

4.2.1 Overload Point

The overload point of the SICOFI®4-TE A/D converters is at 2.223 V. This is the peak amplitude of a sine wave level of 1.572 Vrms. Higher input signal levels will be distorted. Theoretical load capacities for A-Law and μ-Law encoded signals are defined in ITU-T Recommendation G.711. These values correspond to the SICOFI®4-TE overload point:

Table 5 Maximum Signal Levels

Encoding Law	IOM-2 PCM Interface	Analog Interface
	Theoretical Load Capacity (according to ITU-T G.711)	**Max. Sine Wave Level (SICOFI®4-TE Overload Point)**
A-Law	3.14 dBm0	1.572 Vrms
μ-Law	3.17 dBm0	

4.2.2 0 dBm0-Levels

The analog voltage levels corresponding to a 0 dBm0 sine wave signal can be calculated from the maximum signal levels shown in **Table 5**. The results are shown in **Table 6**.

Table 6 Analog Voltage Levels Corresponding to 0 dBm0-Level

Encoding Law	Analog Sine Wave Level corresponding to 0 dBm0 PCM Level
A-Law	1.572 Vrms*10^(-3.14/20) = 1.095 V rms
μ-Law	1.572 Vrms*10^(-3.17/20) = 1.091 V rms

Note: Periodic PCM codes for a 1 kHz sine wave signal with 0 dBm0 level can be found in ITU-T G.711.

4.2.3 Compressor Gain Relative to Coding Law

The **µ-Law** compressor unit of the SICOFI®4-TE automatically adds 1.94 dBm0 gain, which has to be considered for the total gain calculation. The accumulated gain of all programmable transmit filters (AX1+AX2+FRX) must not exceed 6 dB if the device is set to µ-Law operation. If the device is set to A-Law operation, then the accumulated gain must not exceed 8 dB.

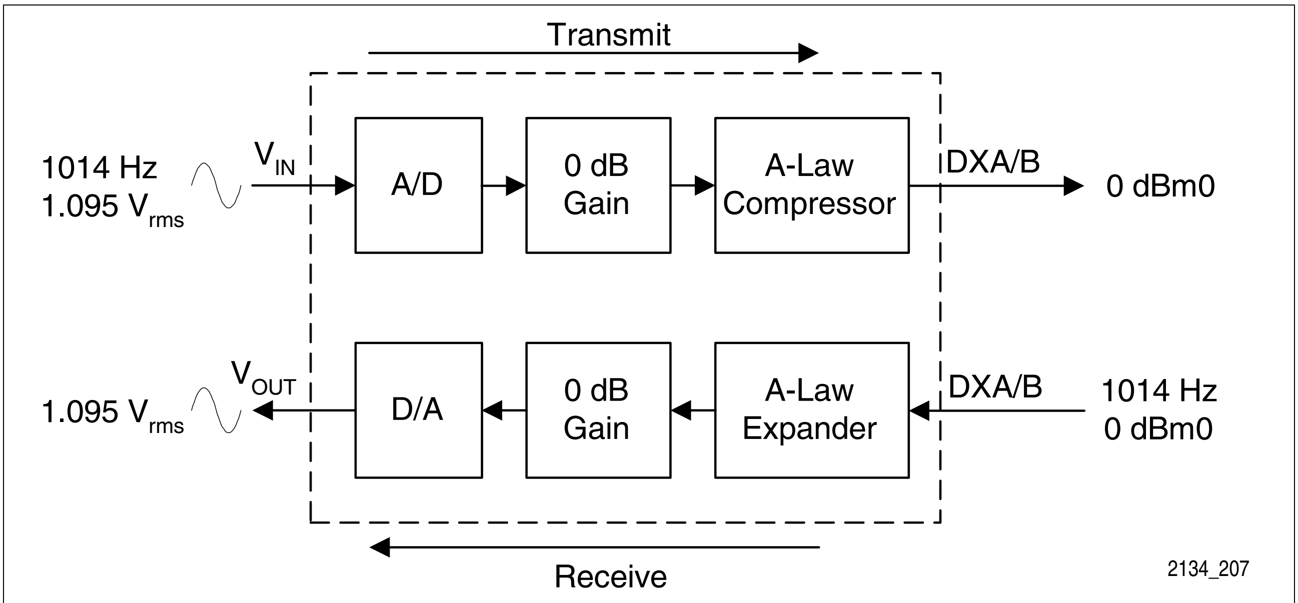


Figure 6 Analog and PCM Signal Levels in A-Law Mode

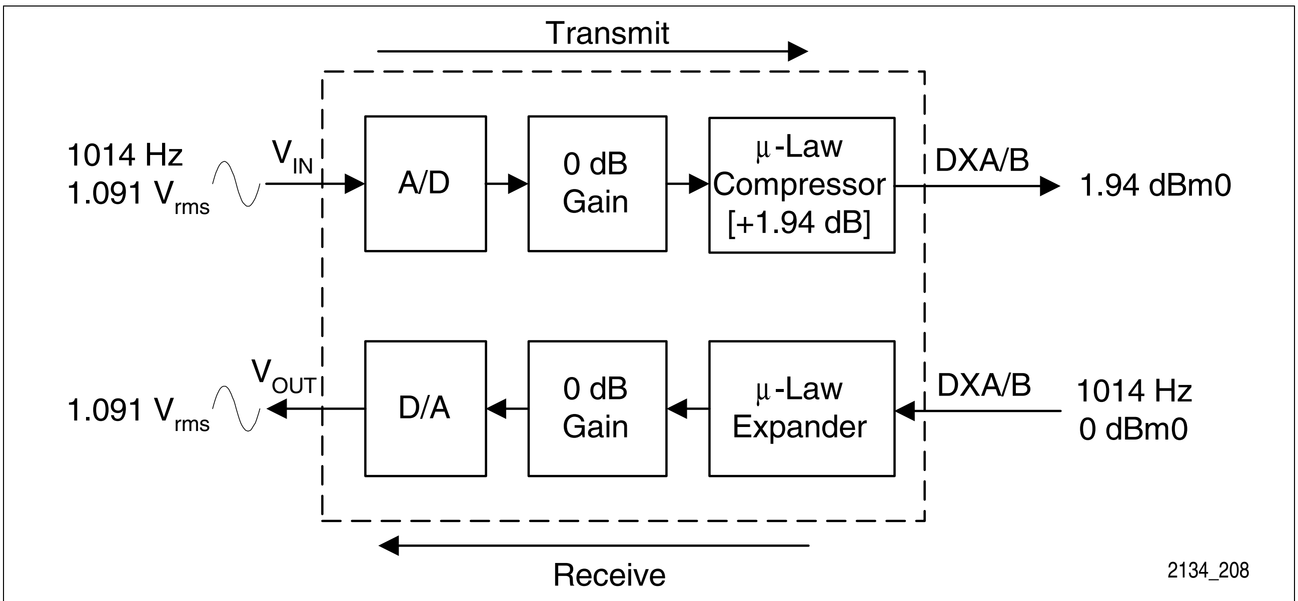


Figure 7 Analog and PCM Signal Levels in µ-Law Mode

4.2.4 Operating Conditions

The figures in this document are based on the subscriber-line board requirements. Proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires a complete knowledge of the analog environment in which the SICOFI®4-TE is to be used. Unless otherwise stated, the transmission characteristics are guaranteed within the following operating conditions:

- T_A = 0 °C to 70 °C;
- V_{DD} = 5 V ± 5%;
- GNDA1,2,3,4 = GNDD = 0 V;
- Load on V_{OUT}: R_L > 300 Ω; C_L < 50 pF;
- H(IM) = H(TH) = 0;
- H(R1) = H(FRX) = H(FRR) = 1;
- HPR and HPX enabled;
- AR = 0 to –8 dB (AR = AR1 + AR2 + FRR + R1);
- AX = 0 to +8 dB for A-Law,
  AX = 0 to +6 dB for µ-Law (AX = AX1 + AX2 + FRX);
- f = 1014 Hz; 0 dBm0; A-Law or µ-Law;
- AGX = 0 dB, +6.02 dB; and
- AGR = 0 dB, –6.02 dB.

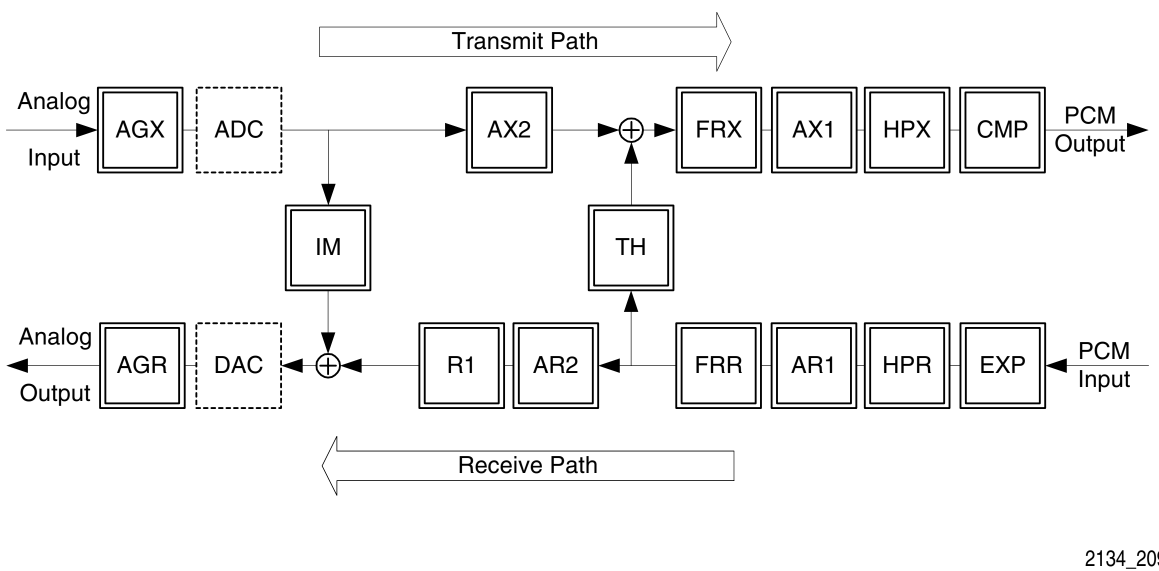


Figure 8 Simplified Signal Flow Diagram

4.2.5 Gain Accuracy

Table 7 Gain Accuracy

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Absolute Gain	G	–0.80	±0.10	+0.80	dB	T_A = 25 °C, V_{DD} = 5 V, AGX = AGR = 0 dB
Variation with Temperature				±0.05	dB	T_A = 0 °C to 70 °C
Variation with Supply Voltage				±0.05	dB	V_{DD} = 5 V ± 5%
Variation with Analog Gain				±0.05	dB	AGX= +6.02 dB, AGR= –6.02 dB

4.2.6 Gain Tracking (Receive and Transmit)

The gain deviation for a 1014 Hz sine-wave input signal will stay within limits shown in **Table 8**. All values are relative to the gain of a 0 dBm0 input signal.

Table 8 Gain Deviations with Input Level

Input Level	Symbol	Gain Deviation			Unit	Test Conditions
		min.	typ.	max.		
-55 to -50 dBm0	ΔG			±1.4	dB	1014 Hz sine-wave test signal. Reference level is at 0 dBm0.
-50 to -37 dBm0	ΔG			±0.5	dB	
-37 to 3 dBm0	ΔG			±0.25	dB	

4.2.7 Frequency Response

Table 9 Attenuation with Frequency in Transmit and Receive Direction

Input Frequency	Receive Loss		Transmit Loss		Unit	Test Conditions
	min.	max.	min.	max.		
0 Hz to 100 Hz	0		> 2		dB	0 dBm0 input signal level. 1014 Hz reference frequency
100 Hz to 200 Hz	0		0		dB	
200 Hz to 300 Hz	-0.125		-0.125	1	dB	
300 Hz to 3.0 kHz	-0.125	0.125	-0.125	0.125	dB	
3.0 kHz to 3.2 kHz	-0.125	0.3	-0.125	0.3	dB	
3.2 kHz to 3.4 kHz	-0.125	0.65	-0.125	0.65	dB	
> 3.4 kHz	0		0		dB	

4.2.8 Group Delay

4.2.8.1 Group Delay, Absolute Values

Table 10 shows the limit values for the Absolute Group Delay. The maximum delays are valid when the SICOFI®4-TE is operating with H(TH) = H(IM) = 0, and H(FRR) = H(FRX) = 1, and include the delay through the A/D and D/A converters. The typical delays are the average of all different time slot delays during one IOM-2 frame.

Table 10 Group Delay, Absolute Values

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Transmit Delay	D_{XA}	300	375	450	µs	0 dBm0 input signal level, f_{Test} at $T_G$min.
Receive Delay	D_{RA}	300	375	450	µs	

4.2.8.2 Group Delay Distortion with Frequency

The Group Delay Distortion in transmit and receive direction will stay within the limits shown in **Table 11**. Group Delay Distortion values are referenced to the minimum value of Group Delay ($T_G$min).

Table 11 Group Delay Distortion with Frequency

Frequency	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
500 Hz to 600 Hz	Δt_G			300	µs	0 dBm0 input signal level, reference point is at $T_G$min.
600 Hz to 1.0 kHz	Δt_G			150	µs	
1.0 kHz to 2.6 kHz	Δt_G			100	µs	
2.6 kHz to 3.0 kHz	Δt_G			300	µs	

4.2.9 Noise

Table 12 Idle Channel Noise in Transmit Direction

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
A-Law, psophometric (V_{IN} = 0 V)	N_{TP}			–66.0	dBm0p
µ-Law, C-message (V_{IN} = 0 V)	N_{TC}			19.0	dBrnc0

Table 13 Idle Channel Noise in Receive Direction

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
A-Law, psophometric (idle code + 0)	N_{RP}		–85	–77.0	dBm0p
µ-Law, C-message (idle code + 0)	N_{RC}		5	13.0	dBrnc0

4.2.10 Harmonic and Intermodulation Distortion

Table 14 Harmonic and Intermodulation Distortion

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Harmonic Distortion 2nd, 3rd order	*HD*		–44		dB	0 dBm0; f = 1014 Hz
Intermodulation R_2	*IMD*		–46		dB	Equal-level, 4-tone method (EIA-464) at composite level of -13 dBm0; f = 300 Hz to 3400 Hz
R_3	*IMD*		–56		dB	

4.2.11 Total Distortion

Table 15 Signal-to-Total Distortion Ratio Measured with Sine Wave

Input Level	Symbol	Min. Values		Unit	Test Conditions
		A-Law	µ-Law		
-45 dB	S/D	23.5	26.0	dB	sine wave f=1014 Hz, receive and transmit, **µ-Law:** C-message weighted, **A-Law:** psophometrically weighted.
-40 dB	S/D	28.5	30.0	dB	
-30 dB	S/D	34.5	34.5	dB	
> -28 dB	S/D	35.4	35.4	dB	

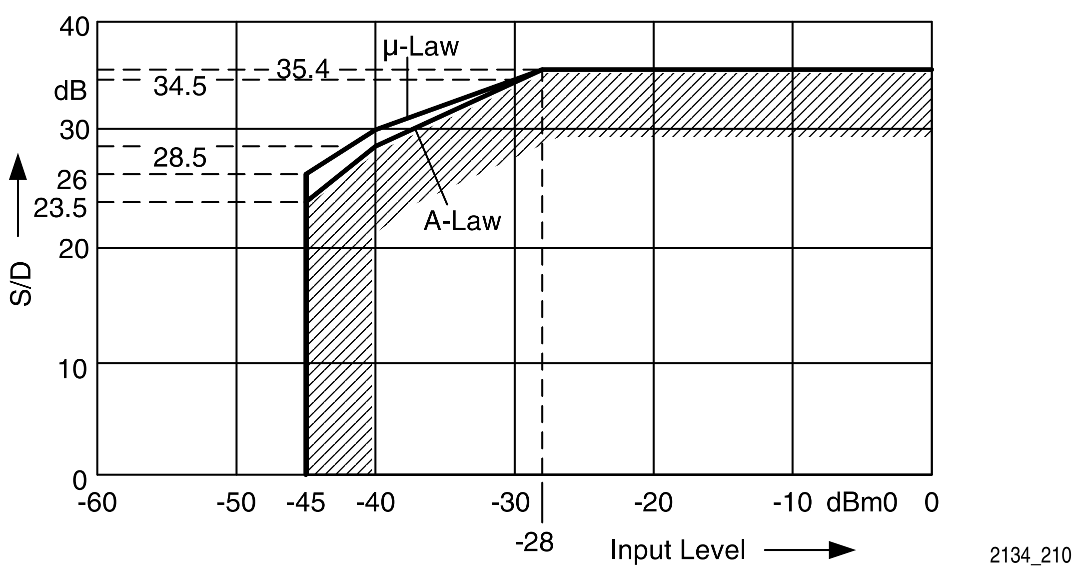


Figure 9 Total Distortion Measured with Sine-Wave, Receive and Transmit

4.2.12 Single Frequency Distortion

Table 16 Single Frequency Distortion

Test Input Signal	Frequency Range	max. Input Level
Receive Direction	300 Hz to 3.4kHz	0 dBm0
Transmit Direction	0 Hz to 12 kHz	0 dBm0

Any resulting signal with a frequency different from the test input signal will stay at least 28 dB below the input signal level.

4.2.13 Overload Compression

This is measured with a 1014 Hz sine-wave signal. The overload point in µ-Law Mode is at 3.17 dBm0.

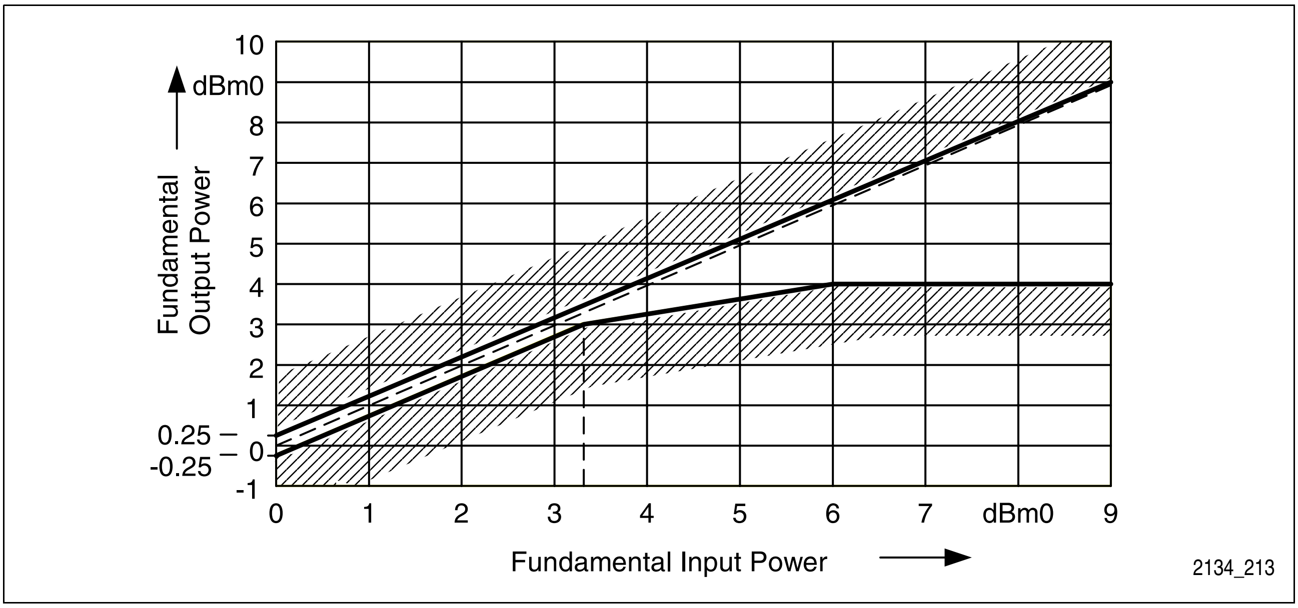


Figure 10 Overload Compression (µ-Law Coding, Transmit Direction)

4.2.14 Crosstalk

Table 17 Crosstalk Between Channels

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Crosstalk, 0dBm0	CT		– 80	– 75	dB	f = 200 Hz to 3400 Hz, any combination of directions and channels

4.2.15 Out-of-Band Discrimination in Transmit Direction

With any 0 dBm0 sine-wave signal below 100 Hz and in the range from 3.4 kHz to 100 kHz (out-of-band signal) applied to an analog input (V_{INx}), the level of any resulting frequency component at the digital output will stay at least X dB (see **Table 18**) below the output level of a 0 dBm0 1kHz sine-wave reference signal at the analog input.

Table 18 Out-of-Band Signals Applied to the Analog Inputs (V_{INx})

Input Frequency	Min. Output Signal Rejection X	Unit	Test Conditions
0 Hz to 60 Hz	25	dB	0 dBm0 sine-wave input signal on V_{IN}
60 Hz to 100 Hz	10	dB	
3.4 kHz to 4 kHz	$-14\left(\sin\left(\pi\frac{4000-f}{1200}\right)-1\right)$	dB	
4 kHz	15	dB	
4 kHz to 4.6 kHz	$-18\left(\sin\left(\pi\frac{4000-f}{1200}\right)-\frac{7}{9}\right)$	dB	
4.6 kHz to 100 kHz	40	dB	

The Hardware Filters behind the A/D Converters reject teletax pulses with their poles at 12 kHz ±150 Hz and 16 kHz ±150 Hz.

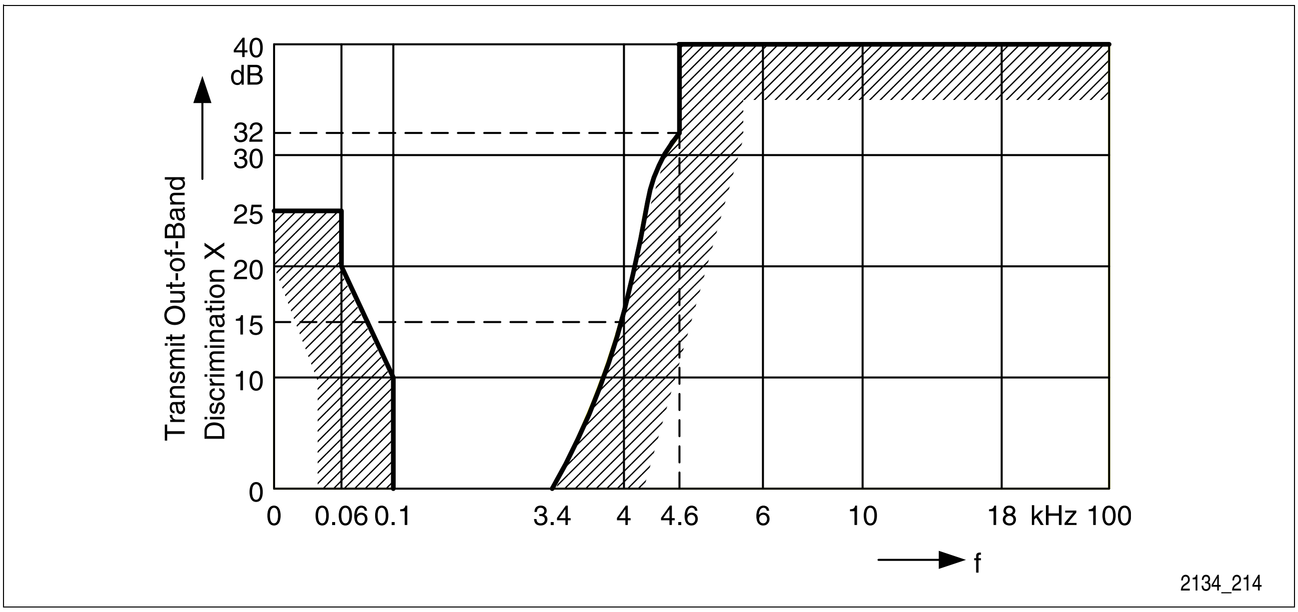


Figure 11 Out-of-Band Discrimination in Transmit Direction

4.2.16 Out-of-Band Discrimination in Receive Direction

With any 0 dBm0 sine-wave frequency in the range from 300 Hz to 3.99 kHz applied to the digital input (DU or DD), the level of any resulting out-of-band signal at the analog output will stay at least X dB (see **Table 19**) below the output level of a 0 dBm0 1kHz sine-wave reference signal at the digital input.

Table 19 Out-of-Band Signals at the Analog Outputs (V_{OUTx})

Output Frequency	Min. Output Signal Rejection X	Unit	Test Conditions
3.4 kHz to 4.6 kHz	$-14\left(\sin\left(\pi\frac{4000-f}{1200}\right)-1\right)$	dB	0 dBm0 sine-wave input signal on digital input (DU or DD)
4.6 kHz to 10.55 kHz	$35+22\frac{f-4600}{5950}$	dB	
4 kHz	15	dB	
4.6 kHz	28	dB	
>10.55 kHz	57	dB	

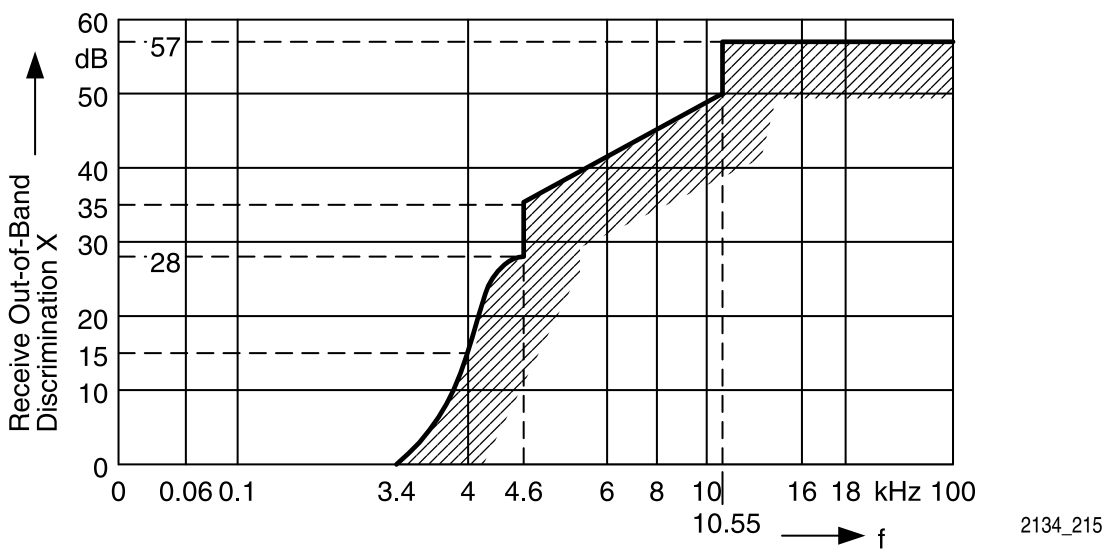


Figure 12 Analog Output: Out-of-Band Signals

4.2.17 Out-of-Band Idle Channel Noise at Analog Output

With an idle code (any sequence of constant PCM octets) applied to the digital input, the level of any resulting out-of-band power spectral density at the analog output, measured with 3 kHz bandwidth, will be not greater than the limit curve shown in **Figure 13**.

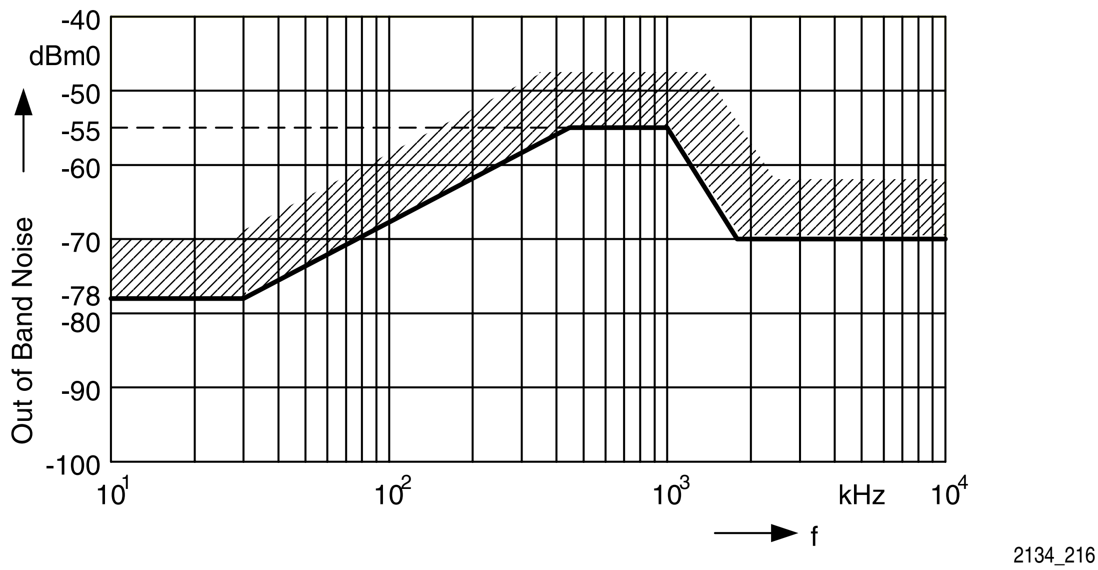


Figure 13 Analog Output: Out-of-Band Idle Channel Noise

4.2.18 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain, group delay, and deviations inherent to the A/D- and D/A-converters, as well as to all external components used with a tip/ring interface (SLIC, OP's etc.).

Transhybrid loss test setup:

The SICOFI®4-TE test loop “DLB-ANA” is selected (see **Figure 31**), which connects the analog output with the analog input. The programmable filters FRR, AR, FRX, AX are by-passed. The IM-filter is disabled, (H(IM)=0). The balancing filter TH is enabled with optimized coefficients for this configuration ($V_{OUT} = V_{IN}$).

A 0 dBm0 sine wave signal with a frequency in the range of 300 Hz to 3400 Hz is applied to the digital input. The signal levels of the resulting echo at the digital output will stay below the values shown in **Table 20**.

Table 20 Transhybrid Loss

Input Frequency	Symbol	Transhybrid Loss		Unit	Test Condition
		min.	typ.		
300 Hz	THL_{300}	19	40	dB	T_A = 25 °C; V_{DD} = 5 V AGX = AGR = 0 dB; typical variation of amplitude: ± 0.15 dB delay: ± 0.5 µs.
500 Hz	THL_{500}	25	45	dB	
2500 Hz	THL_{2500}	21	40	dB	
3000 Hz	THL_{3000}	19	35	dB	
3400 Hz	THL_{3400}	19	35	dB	

5 Interface Description

The SICOFI®4-TE provides four interfaces:

- Analog Interface,
- IOM-2 PCM Interface,
- Signaling Interface, and
- Serial Microcontroller Interface.

A general description of these interface is given in the ***Product Overview*, Chapter 4**. Refer to the ***Programmers Reference Manual*** for information on the configuration and operation of the four interfaces.

The subsequent chapters in this manual explain how to connect the SICOFI®4-TE to subscriber line interface circuits (SLICs), microcontrollers, and IOM-2 PCM highways.

5.1 Analog Interface

The Analog Interface in combination with a Subscriber Line Interface Circuit (SLIC) forms a configurable tip & ring (t/r) telephone line. The AC transmission characteristic of the SICOFI®4-TE—SLIC combination can be controlled by programming the digital filter structures inside the SICOFI®4-TE. The correct filter coefficients are determined by the targeted AC transmission behavior (e.g. Telco specification) and by the transfer functions of the SLIC.

The SICOFI®4-TE can be interfaced directly to electronic SLICs or transformer solutions. The high driving capability of up to 300 Ohms eliminates the need for an external amplifier that is normally used with transformer SLICs.

The peak amplitude of the analog inputs and outputs is at 2.223 V (overload point).

Out-of-band signals applied to the analog inputs are suppressed by the on-chip digital hardware filters. The poles of these filters are fixed at 12 kHz and 16 kHz which suppresses the echo signal from teletax pulses very efficiently: As long as the amplitude of the teletax echo stays below the overload threshold of 2.223 Vp (1.57 Vrms), the voice signal in the transmit path will not be disturbed. Thus, the on-chip hardware filters can eliminate the need for external teletax filters.

5.1.1 Coupling Capacitors at the Analog Interface

A coupling capacitor >39 nF must be used on the V_{IN}-pins in the transmit direction. The required value for the coupling capacitor on the V_{OUT}-pins depends on the input resistance of the SLIC-circuitry (R_{Load}). It has to be chosen to fulfil the frequency response requirement in the receive direction. **Figure 14** can be used to determine an appropriate value for the coupling capacitor (C_{Ext1}).

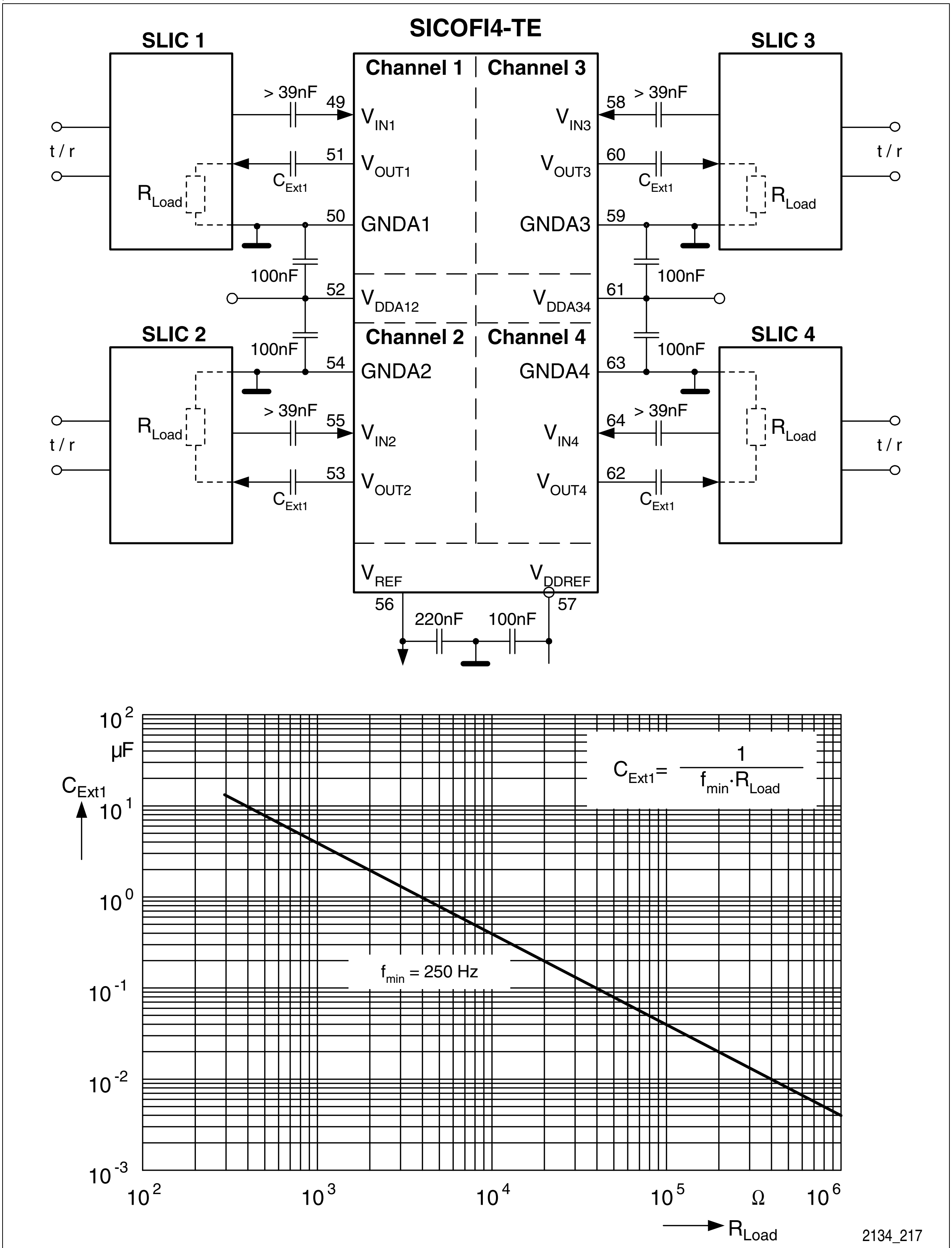


Figure 14 Analog Interface to Four Subscriber Line Interface Circuits (SLICs)

5.1.2 Analog Interface Pins

Table 21 Analog Interface Pins

Symbol	Pin	Function
V_{IN1}	49	Analog Input, Channel 1, 2, 3, 4 Requires a coupling capacitor >39 nF to the SLIC, see **Figure 14**.
V_{IN2}	55	
V_{IN3}	58	
V_{IN4}	64	
V_{OUT1}	51	Analog Output, Channel 1, 2, 3, 4 Requires a coupling capacitor to the SLIC. The capacitor’s value depends on the input impedance of the SLIC, see **Figure 14**.
V_{OUT2}	53	
V_{OUT3}	60	
V_{OUT4}	62	
GNDA1	50	Analog Ground, Channel 1, 2, 3, 4 Not internally connected to GNDD or the other GNDAx.
GNDA2	54	
GNDA3	59	
GNDA4	63	
V_{DDA12}	52	Analog Supply Voltage, Channels 1+2 and 3+4 +5 V (100 nF blocking capacitor required, see **Figure 14**).
V_{DDA34}	61	
V_{DDREF}	57	Analog Supply Reference Voltage, +5 V (100 nF blocking capacitor required, see **Figure 14**).
V_{REF}	56	Reference Voltage Must connect to a 220 nF cap. to ground, see **Figure 14**.

5.2 IOM-2 PCM Interface

The SICOFI®4-TE’s IOM-2 PCM Interface can be connected directly to an IOM-2 interface in terminal mode (3 IOM channels, 768 kbit/s). The device uses the IOM-clock DCL at 1536 kHz as a master clock. The bit clock input BCL can be at either 768 kHz or 1536 kHz. FCS is an 8 kHz input. The SICOFI®4-TE has data input Pin 30 and data output Pin 26 assigned to the IOM Data Upstream signal, DU. Further, input Pin 27 and output Pin 29 are assigned to the IOM Data Downstream signal, DD. This configuration allows transmission and reception of PCM data on either DU or DD. It further enables internal connections of channels, by programming the receive time slot of one channel to the transmit time slot of the other channel, and vice versa.

The IOM-2 PCM Interface has the following characteristics and features:

- Data rate of 768 kbit/s,
- Bit clock input (BCL) configurable for 768 kHz or 1536 kHz,
- IOM-2 DCL signal used as 1536 kHz master clock for the device; must be applied for all device functions,
- 12 time slots per IOM-2 frame,
- PCM data format serialized 8 bits with MSB first,
- Configurable A-Law or µ-Law coding,
- Independent time slot assignment for each channel and direction,
- Internal voice connection between channels possible,
- Programmable sampling slopes, and
- Programmable frame delay.

5.2.1 IOM-2 PCM Interface Pins

Table 22 IOM-2 PCM Interface Pins

Symbol	Pin	Function
DCL	22	Master Clock input, 1536 kHz.
BCL	32	Bit Clock input at 768 kHz or 1536 kHz.
FSC	31	Frame Synchronization Clock, 8 kHz.
DD	27	Data Downstream input, connect to Pin 29.
DU	30	Data Upstream input, connect to Pin 26.
DU	26	Data Upstream output, connect to Pin 30.
DD	29	Data Downstream output, connect to Pin 27.

5.2.2 IOM-2 PCM Receive and Transmit Example

Each SICOFI®4-TE voice channel should be assigned to one of the following time slots: B1, B2, IC1, IC2, IC3, or IC4. **Figure 15** illustrates the positions of these time slots. **Table 23** shows the corresponding register settings.

Table 23 IOM-2 Time Slot Selection

IOM-2 Time Slot	Reception on:		Transmission on:	
	DD	DU	DU	DD
B1	CR4 = 0000 0000	CR4 = 1000 0000	CR5 = 0000 0000	CR5 = 1000 0000
B2	CR4 = 0000 0001	CR4 = 1000 0001	CR5 = 0000 0001	CR5 = 1000 0001
IC1	CR4 = 0000 0100	CR4 = 1000 0100	CR5 = 0000 0100	CR5 = 1000 0100
IC2	CR4 = 0000 0101	CR4 = 1000 0101	CR5 = 0000 0101	CR5 = 1000 0101
IC3	CR4 = 0000 1000	CR4 = 1000 1000	CR5 = 0000 1000	CR5 = 1000 1000
IC4	CR4 = 0000 1001	CR4 = 1000 1001	CR5 = 0000 1001	CR5 = 1000 1001

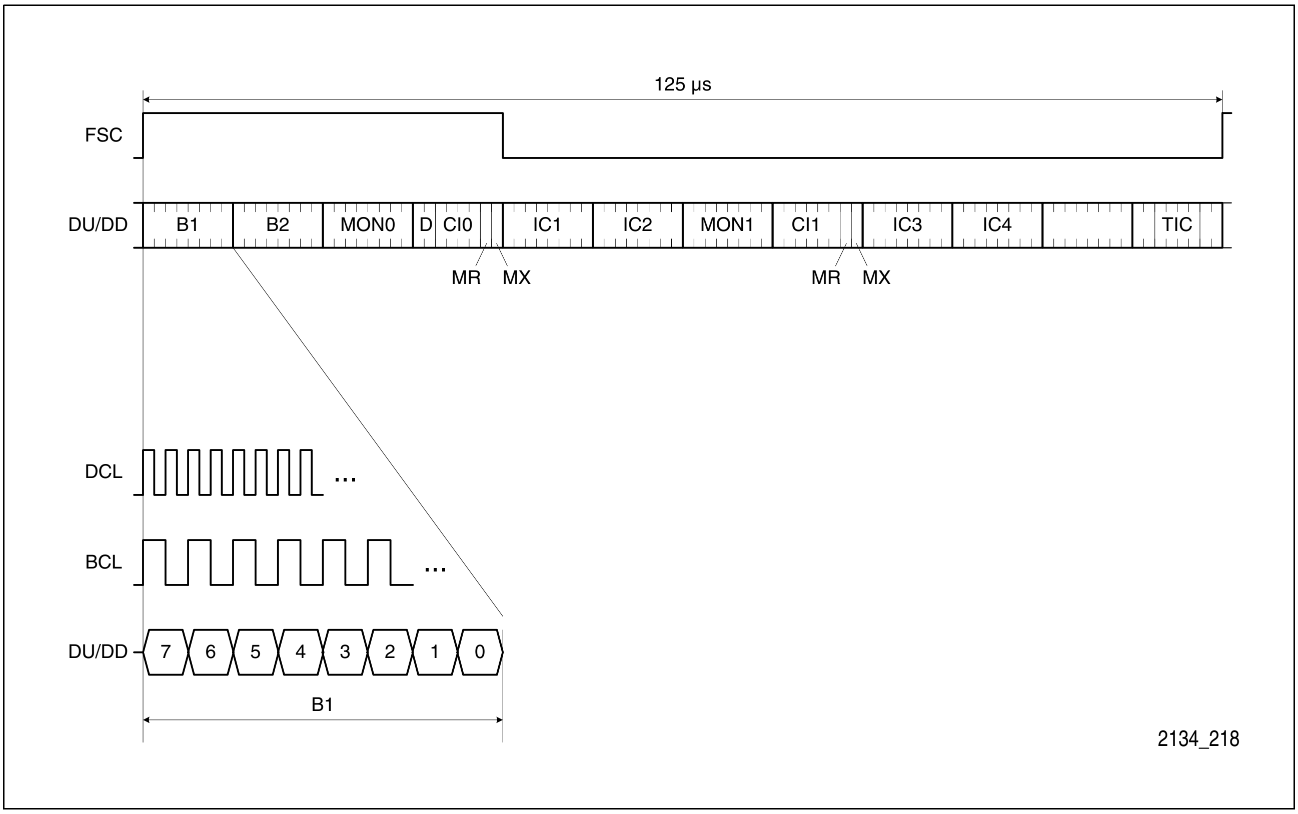


Figure 15 IOM-2 PCM Interface Time Slot Positions

5.3 Signaling Interface

The SICOFI®4-TE Signaling Interface is used to monitor and control supervision and signaling functions on up to four subscriber lines. The device generates interrupt signals to indicate signaling status changes on any of the input pins.

The Signaling Interface consists of the following I/O pins and functions:

- 28 signaling pins (2 input pins, 2 output pins, and 3 user-configurable bi-directional pins per channel),
- Debouncing functions,
- 2 interrupts, indicating changes on any of the signaling inputs, (one for each of the channel-pairs 1&2 and 3&4),
- 1 output signal for ringing,
- 1 chopper clock output.

5.3.1 Signaling Interface Pins

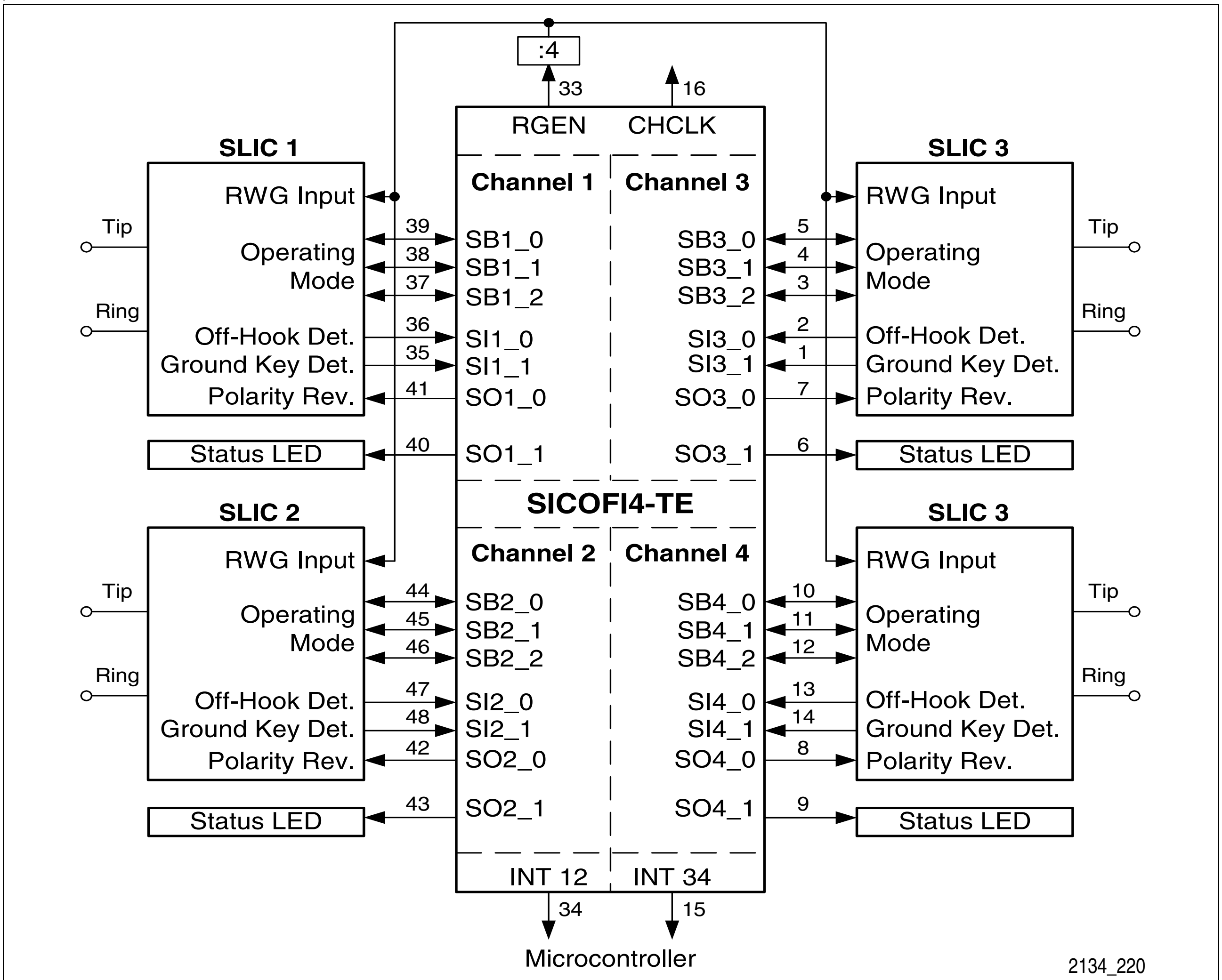


Figure 16 Signaling Example: Four Subscriber Lines

Table 24 Signaling Interface: Pins and Functions for SLIC Interfaces

Symbol	Pin				Function
	Ch1	Ch2	Ch3	Ch4	
SIx_0	36	47	2	13	Signaling Input Channel x, Pin 0.
SIx_1	35	48	1	14	Signaling Input Channel x, Pin 1.
SOx_0	41	42	7	8	Signaling Output, Channel x, Pin 0.
SOx_1	40	43	6	9	Signaling Output, Channel x, Pin 1.
SBx_0	39	44	5	10	Bi-directional Signaling, Channel x, Pin 0.
SBx_1	38	45	4	11	Bi-directional Signaling, Channel x, Pin 1.
SBx_2	37	46	3	12	Bi-directional Signaling, Channel x, Pin 2.
INT12	34		–		Interrupt Output, Channels 1+2, active high.
INT34	–		15		Interrupt Output, Channels 3+4, active high.

5.3.2 Debouncing Functions and Interrupt Generation

All signaling inputs are sampled at programmable intervals (Field N in register XR4). If all the inputs assigned to one channel-pair (1&2 or 3&4) have been stable for two subsequent samples their values are stored in the signaling registers and the associated interrupt output (INT12 or INT34) is set high. The debouncing functions and interrupt generation require a 1536 kHz signal on Pin 22 (DCL). If, for power savings reasons, DCL is temporarily disabled, a signaling change interrupt can be generated by external hardware. Refer to the ***Programmer's Reference Manual*** for further details on this function.

5.3.3 Clock Output Signals

Two programmable Clock Output signals are provided by the PSB 2134:

- RGEN (Pin 33) divided by four can drive the ring input of a ringing SLIC. It is configured in register XR4.Field T.
- CHCLK (Pin 16) is configured in register XR5.CHCLK.
- CHCLK = 16,384 kHz: Requires at least one channel in POWER-UP state.

Table 25 Clock Programming

RGEN		CHCLK	
XR4.Field T	**Output (Pin 33)**	**XR5.CHCLK**	**Output (Pin 16)**
0000	High level (+5V)	00	High level (+5V)
0001 to 1110	Clock period = T *2ms (min. 2 ms, max. 28 ms)	01	512 kHz signal
		10	256 kHz signal
1111	Low level (0V)	11	16,384 kHz signal

5.4 Serial Microcontroller Interface

The Serial Microcontroller Interface is used to access the SICOFI®4-TE's internal registers and the Coefficient RAM (CRAM). The Serial Microcontroller Interface consists of four pins: two data pins (DIN, DOUT), one clock pin (DCLK) and one pin for chip select (CS#). If DIN and DOUT are strapped together, only three microcontroller I/O pins are required to build this interface.

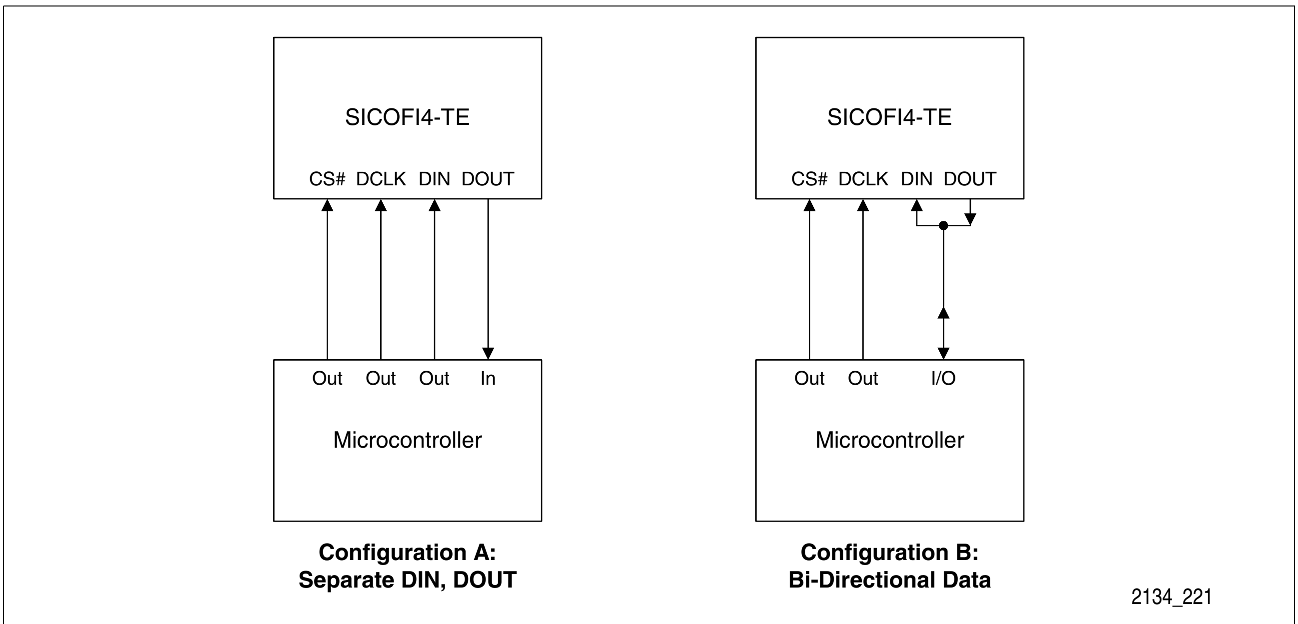


Figure 17 Serial Microcontroller Interface

5.4.1 Serial Microcontroller Interface Pins

Table 26 Serial Microcontroller Interface: Pins and Functions

Symbol	Pin	Function
CS#	17	Chip Select, enable to read or write data, active low.
DCLK	18	Data Clock, shifts data from or to device; max. clock rate is 8192 kHz.
DIN	19	Control Data Input; sampled with rising edge of DCLK.
DOUT	20	Control Data Output; bits are shifted with the falling edge of DCLK; DOUT is in high impedance state when no data is transmitted from the SICOFI®4-TE.

5.4.2 Write Access

Following a falling edge of CS#, the first eight bits received on DIN specify the type of command. The data bytes following a write command are stored in the selected configuration registers or the selected part of the Coefficient RAM. The number of data bytes depends on the type of command. After every command CS# must be set to ’1’.

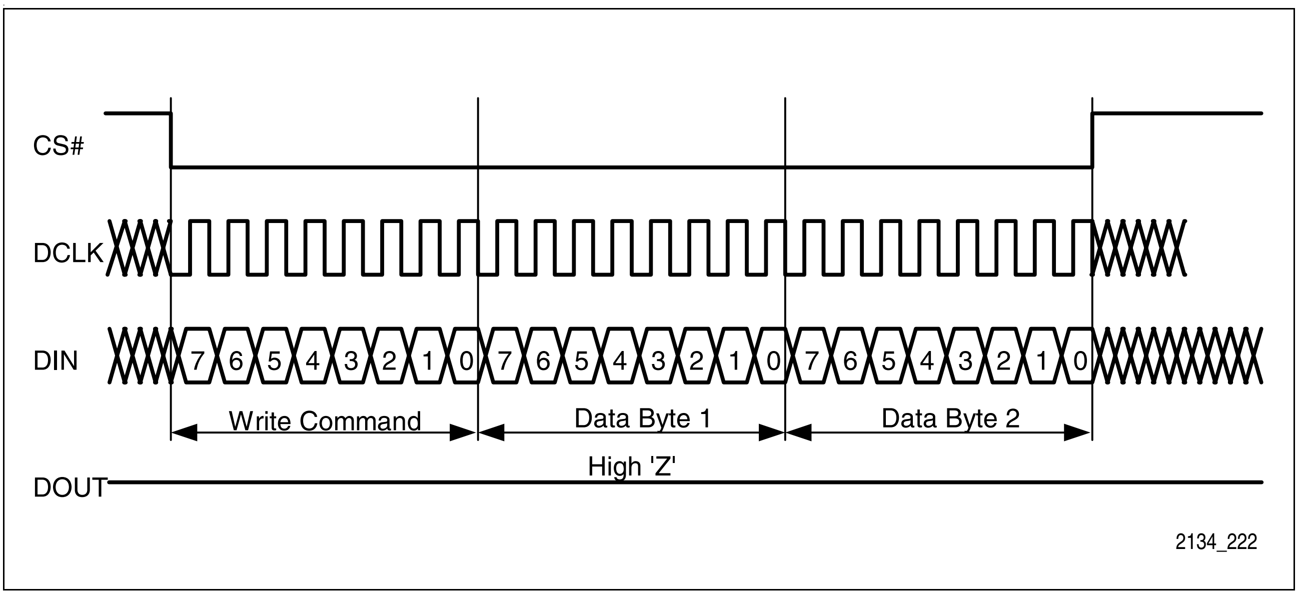


Figure 18 Example for a Two-Byte Write Access

5.4.3 Read Access

If the first eight bits received via DIN represent a read command, the SICOFI®4-TE will initiate its response via DOUT. An identification byte (81_H) is followed by the requested number of data bytes (contents of configuration registers or contents of the CRAM). During execution of a read command, the device will ignore data on DIN. After every command CS# must be set to ’1’.

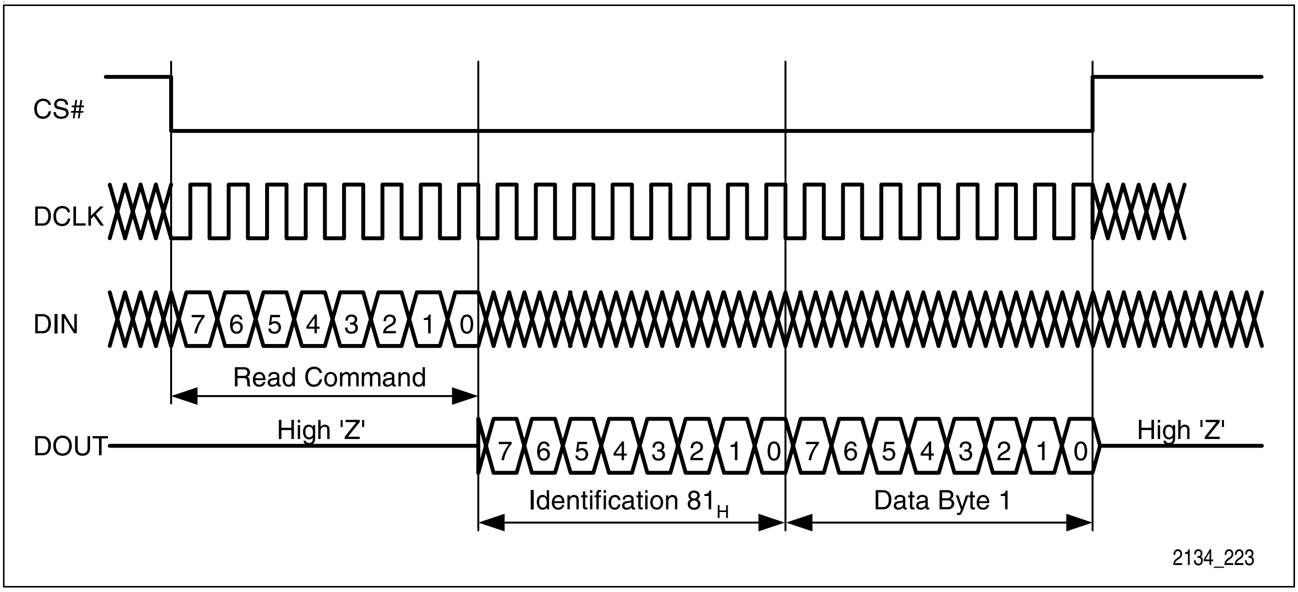


Figure 19 Example for a One-Byte Read Access

For byte-by-byte transfer, the high time of DCLK can be prolonged, resulting in a user-defined ‘waiting time’ between bytes. This mechanism can be used for writing to and reading from the device.

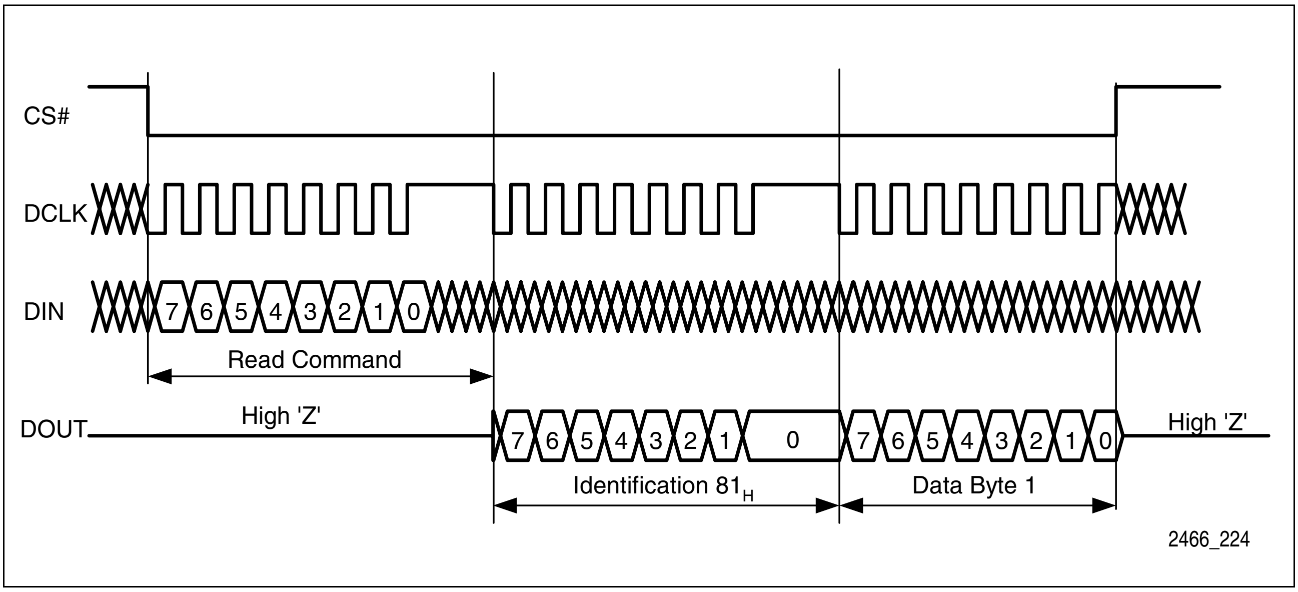


Figure 20 Example for a Read Access with Byte-by-Byte Transfer

Read and write commands can be chained by leaving CS# low after the completion of each command sequence.

For read or write access to individual registers, the command sequence may be terminated by rising CS# after the transmission of any number of bytes.

5.4.4 Three-Wire Access

DIN and DOUT may be strapped together and connected to a single I/O pin of the microcontroller. The interface remains fully functional with only three wire connections. After every command CS# must be set to '1'.

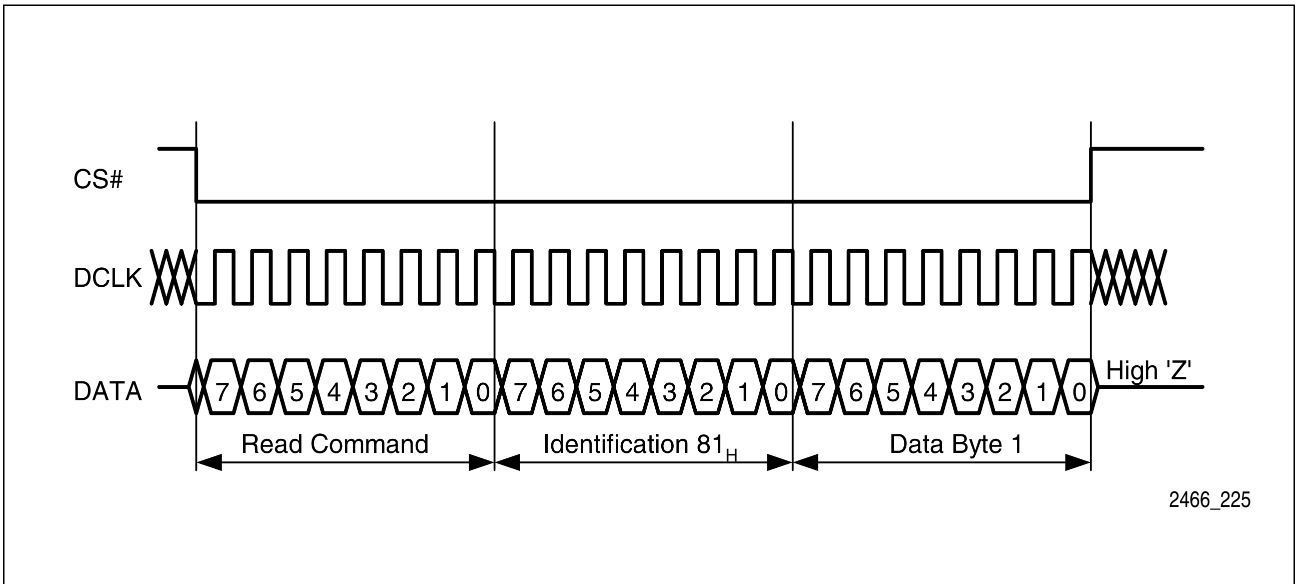


Figure 21 Bi-Directional Data Signal: DIN and DOUT Strapped Together

6 Programming Overview

The transmission characteristics and interfaces of the PSB 2134 can be adapted to various environments. Configuring the functional blocks and programming the digital filter behavior is accomplished by loading values to the Configuration Registers and the Coefficient RAM (CRAM). Software utilities are available to determine the appropriate register and CRAM values (see ***Programmer's Reference Manual***).

6.1 Programming Overview

The SICOFI®4-TE has eight Common Configuration Registers (XR0 to XR7). Settings in these registers affect all four channels.

Each of the four channels has six Channel-Specific Configuration Registers (CR0 to CR5). Settings in these registers affect only the designated channel.

The filters of each channel are individually programmable through channel-specific coefficients in CRAM. There are four global sets of TH Filter coefficients that can be assigned to any channel. All of the filter blocks and their locations are illustrated in **Figure 8**

6.1.1 Register Model

Channel-specific and Common Configuration Registers and coefficients are shown in **Table 27**.

Table 27 Register Model

Configuration Registers and CRAM	Type
XR0 to XR7 (8 bytes)	common
CR0 to CR5 (6 bytes)	channel-specific
IM/R1 Coefficients (16 bytes)	
FRR, FRX Coefficients (16 bytes)	
AR1, AR2, AX1, and AX2 Coefficients (8 bytes)	
IM, FRR, FRX, AR, AX, TG1, TG2Coefficients (8 bytes)	
TG1, TG2 Coefficients (8 bytes)	
TH Coefficient Set 1 (24 bytes)	one coefficient set per channel
TH Coefficient Set 2 (24 bytes)	
TH Coefficient Set 3 (24 bytes)	
TH Coefficient Set 4 (24 bytes)	

6.1.2 Register Maps

Table 28 ***Read* Access to Common Configuration Register (XR) Map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XR0	SI4_1	SI4_0	SI3_1	SI3_0	SI2_1	SI2_0	SI1_1	SI1_0
XR1	SB4_1	SB4_0	SB3_1	SB3_0	SB2_1	SB2_0	SB1_1	SB1_0
XR2	PSB4_1	PSB4_0	PSB3_1	PSB3_0	PSB2_1	PSB2_0	PSB1_1	PSB1_0
XR3	SB4_2	SB3_2	SB2_2	SB1_2	PSB4_2	PSB3_2	PSB2_2	PSB1_2
XR4	Field N (Signal Debounce)				Field T (Configure RGEN)			
XR5	0	0	CR_DU	CR_DD	CHCLK		Version	
XR6	C-Mode	X-S	R-S	DRV_0	Shift	PCM-OFFSET		
XR7	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Table 29 ***Write* Access to Common Configuration Register (XR) Map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XR0	SO4_1	SO4_0	SO3_1	SO3_0	SO2_1	SO2_0	SO1_1	SO1_0
XR1	SB4_1	SB4_0	SB3_1	SB3_0	SB2_1	SB2_0	SB1_1	SB1_0
XR2	PSB4_1	PSB4_0	PSB3_1	PSB3_0	PSB2_1	PSB2_0	PSB1_1	PSB1_0
XR3	SB4_2	SB3_2	SB2_2	SB1_2	PSB4_2	PSB3_2	PSB2_2	PSB1_2
XR4	Field N (Signal Debounce)				Field T (Configure RGEN)			
XR5	0	0	CR_DU	CR_DD	CHCLK		Version	
XR6	C-Mode	X-S	R-S	DRV_0	Shift	PCM-OFFSET		
XR7	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Table 30 **Channel-Specific Configuration Register (CR) Map (Read & Write)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CR0	TH	IM/R1	FRX	FRR	AX	AR	TH-SEL	
CR1	ETG2	ETG1	PTG2	PTG1	LAW	0	0	PU
CR2	COT/R			0	IDR	LM	LMR	V+T
CR3	TEST-Loops				AGX	AGR	D-HPX	D-HPR
CR4	RLINE	0	0	0	RS3	RS2	RS1	RS0
CR5	XLINE	0	0	0	XS3	XS2	XS1	XS0

6.1.3 CRAM Structure

Coefficient RAM (CRAM) is used to store the individual coefficients calculated for each channel. The coefficients can be written and read through the Microcontroller Interface. The IM, FRX, FRR, AX, AR, TG1, TG2, and TH coefficients are accessed through the Coefficient Operation (COP) Command Sequences which include the channel address (see ***Programmer's Reference Manual*** **Chapter 6.5**).

Channel-specific coefficients always belong to their designated channel. Common coefficients (TH) can be assigned to any of the four channels through field TH-SEL in CR0 (see **Figure 22**).

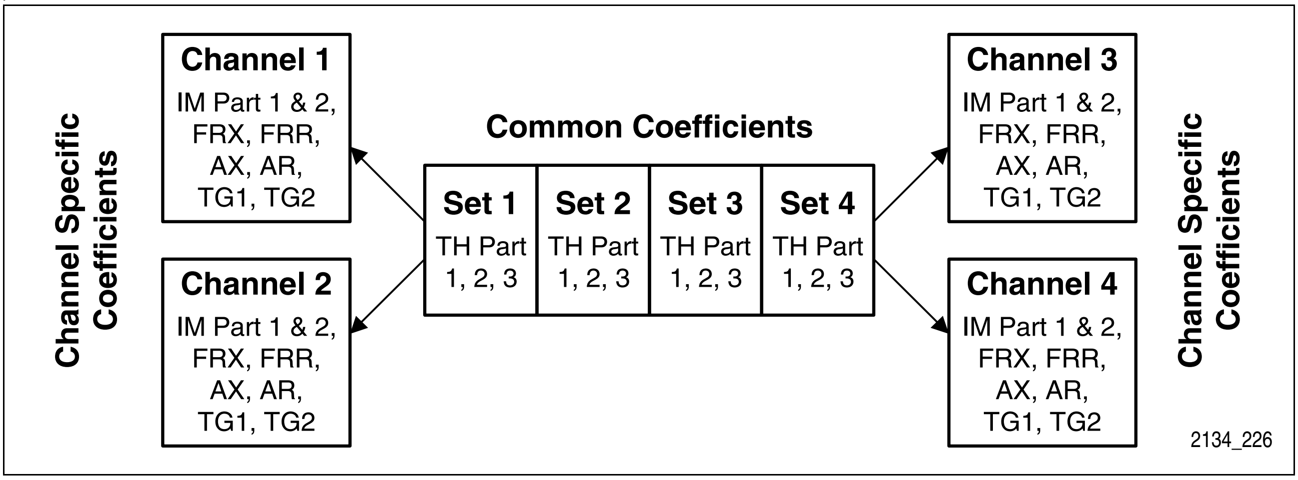


Figure 22 Channel-Specific and Common Coefficients

Table 31 Coefficient RAM (CRAM) Structure per Channel

IM Part 1	8 Coefficient Bytes
IM Part 2	8 Coefficient Bytes
FRX	8 Coefficient Bytes
FRR	8 Coefficient Bytes
AX	4 Coefficient Bytes
AR	4 Coefficient Bytes
TG1	4 Coefficient Bytes
TG2	4 Coefficient Bytes

Table 32 Coefficient RAM (CRAM) Structure per Set

TH Part 1	8 Coefficient Bytes
TH Part 2	8 Coefficient Bytes
TH Part 3	8 Coefficient Bytes

6.2 Types of Commands and Data Bytes

Coefficients and register contents are programmed and accessed through command sequences via the Microcontroller Interface. There are three types of command sequences:

- **Ex**tended **Op**eration (XOP) for access to the Common Configuration Registers (XR0 to XR7) including the Control Registers for the signaling interface.
- **S**tatus **Op**eration (SOP) for access to the Channel-Specific Registers (CR0 to CR5), e.g. enabling and disabling of filters, time slot assignment, and test loops.
- **C**oefficient **Op**eration (COP) for access to the CRAM structures. Coefficients can be written to the SICOFI®4-TE, and also read back.

Table 33 Types of Commands and Data Bytes.

	7	6	5	4	3	2	1	0
XOP	RST	0	RW	**1**	**1**	LSEL		
SOP	AD		RW	**1**	**0**	LSEL		
COP	AD		RW	**0**	CODE			

With the first byte received via DIN, a command type is selected through bits 3 and 4. A two-bit address field (AD) in the COP and SOP commands allows access to the channel-specific structures (CRAM and CR registers). Since the XR Registers are common for all channels, no address field is required within the XOP command byte.

All three commands allow read and write access, as indicated by bit 5 (RW). The bit fields LSEL and CODE specify the type and the length of data that follows the command.

7 Application Hints

7.1 Support Tools

7.1.1 Development Board

The Evaluation Package EASY 2466 includes the following hardware:

- One SICOFI®4-TE Evaluation Board STUT 2466 with connectors for four optional SLIC daughter cards and BNC connectors to a PCM backplane.
- One microcontroller board EVC50x with RS-232 interface that translates data from a PC to SICOFI®4-TE format.
- Two SLIC Babyboards STUT 5502 with HARRIS SLIC HC 5502 mounted.

The QSICOS software enables the calculation of the coefficients and the download of the setup file to the evaluation board.

This setup allows measurements and optimization of the actual behavior of a complete transmission system. The EASY 2466 evaluation system connects directly to industry-standard test equipment.

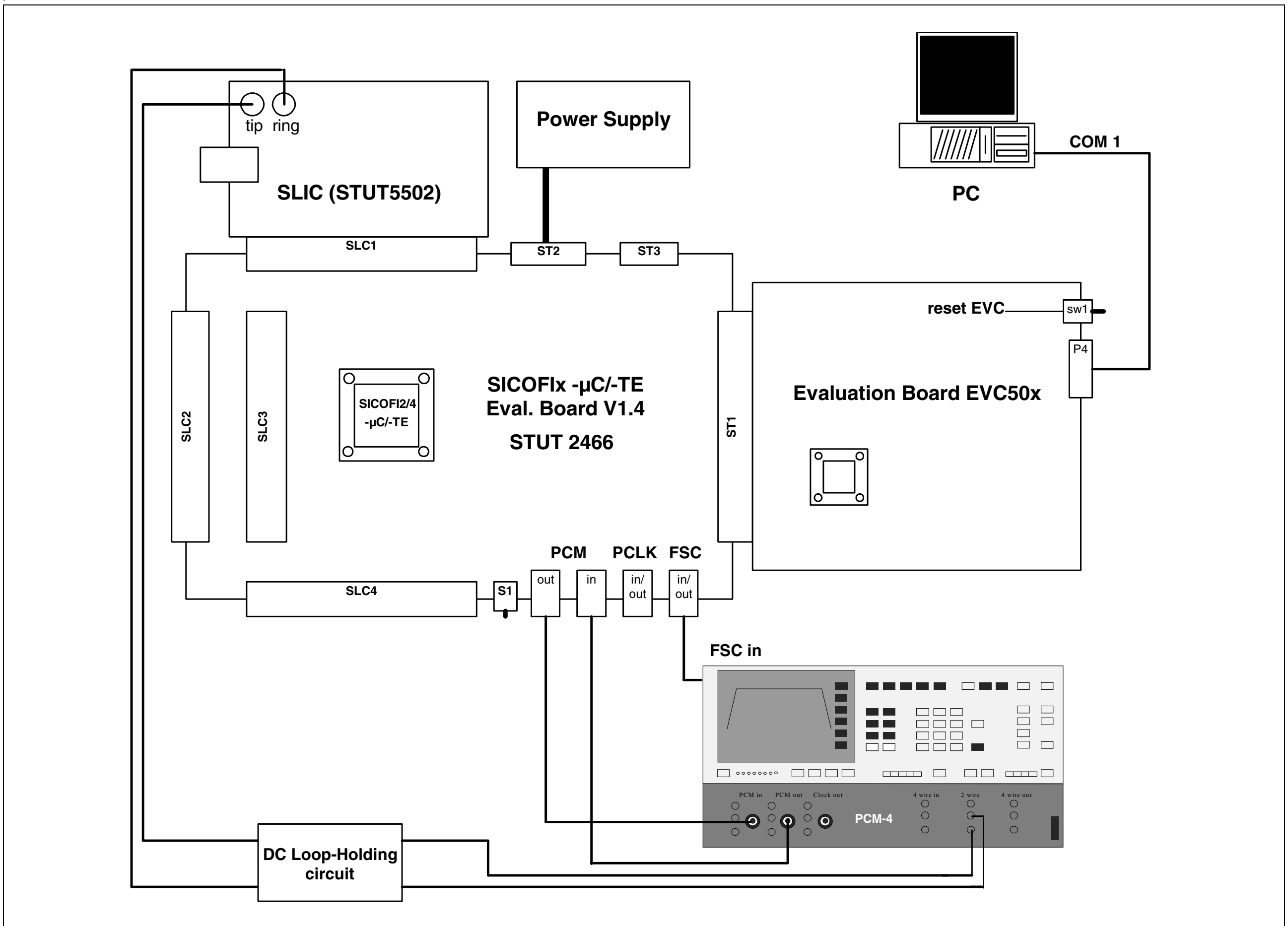


Figure 23 Development System with STUT 2466 Evaluation Board

7.2 Guidelines for Board Design

7.2.1 Filter Capacitors

- For high frequency noise rejection, use 100 nF SMD ceramic capacitors on pins V_{DDA12}, V_{DDA34} and V_{DDREF} and connect to GND. Additional 2.2 µF tantalum capacitors are recommended.
- Use one 100 nF SMD ceramic capacitor on pin V_{DDD} and connect to GNDD.
- Use a 1 µF – 10 µF tantalum capacitor from +5 V supply to GND (central blocking).

***Note:** All blocking capacitors MUST be placed as close as possible to the SICOFI®4-TE pins.*

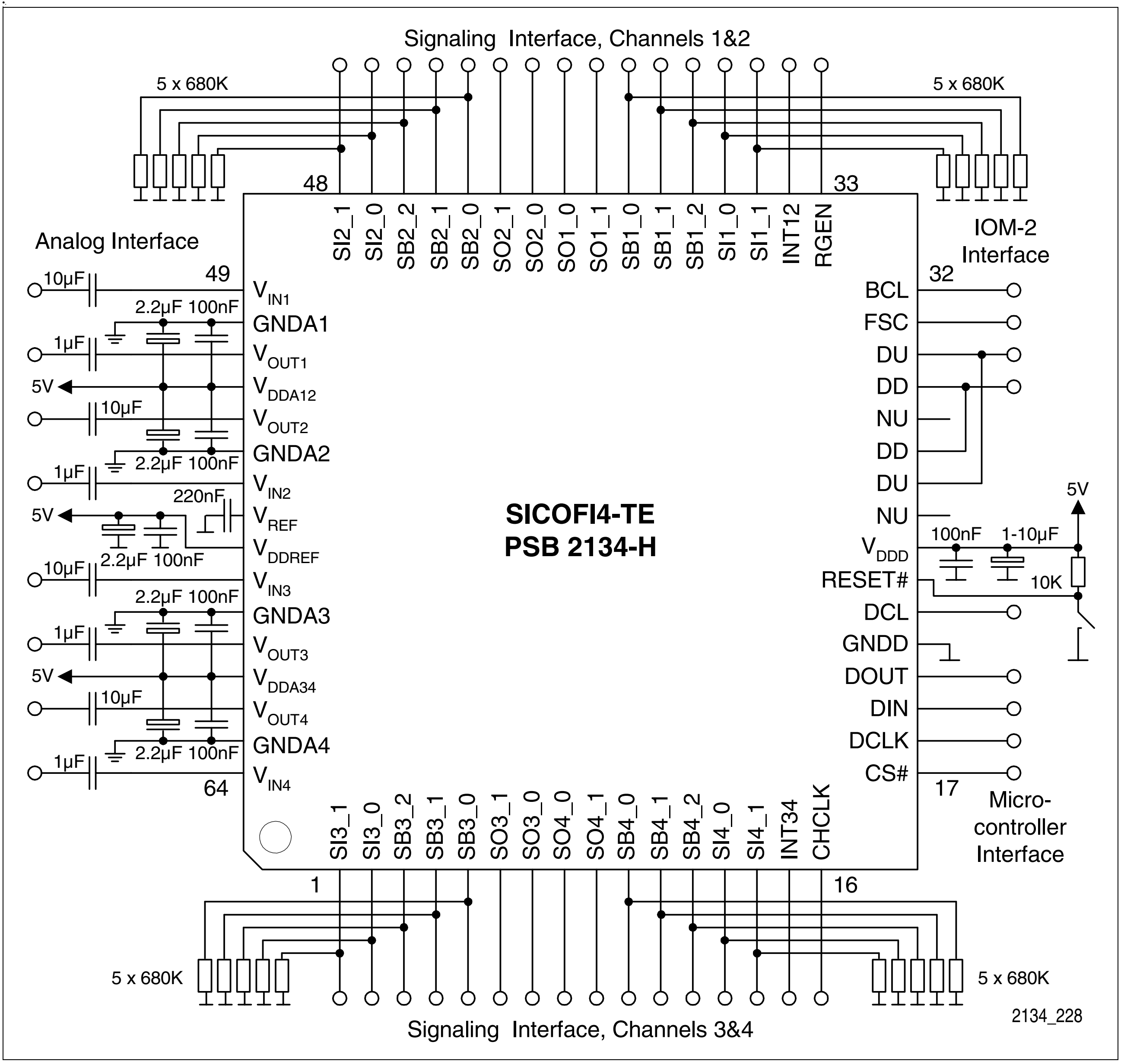


Figure 24 SICOFI®4-TE Test Circuit Configuration

7.3 Proposal for SICOFI®4-TE Board Design

For a new layout design it is recommended to use a separate ground-layer which gives the possibilty to connect all ground-pins of the SICOFI®4-TE (GNDA and GNDD) low-ohmic together.

Furthermore, an optimum board layout should follow these recommendations

- Separate all digital supply lines from analog supply lines as far as possible
- Applying the standard practice regarding blocking capacitors is recommended
- Place all SLIC circuits as close as possible to the Vinx/Voutx pins of the SICOFI
- Separate all analog circuitry (especially SLIC and Vinx/Voutx) as far as possible from any digital signal source (esp. clock signals)

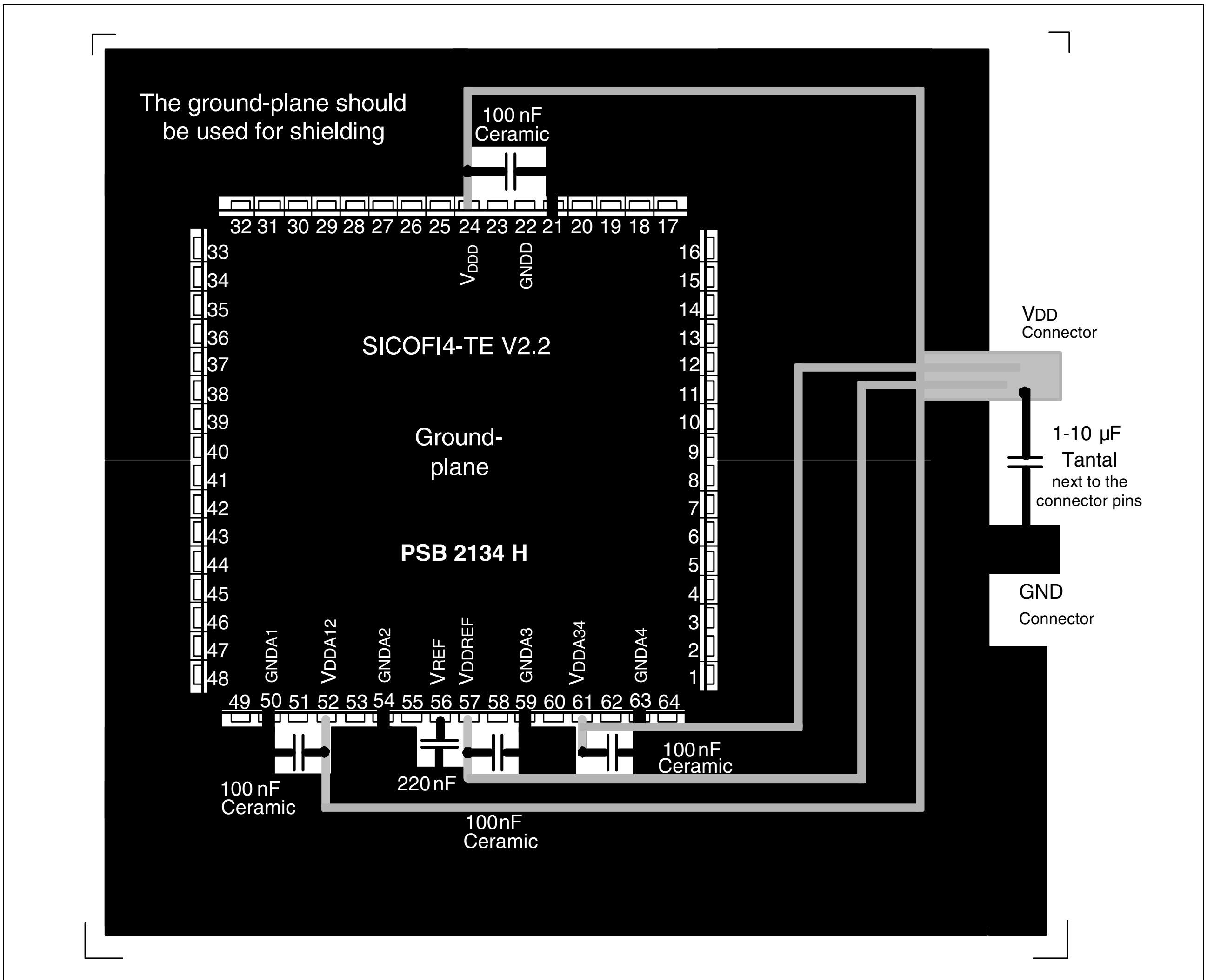


Figure 25 Proposal for a Ground Concept

VDD is the grey colored layer and the Ground-plane is the black colored layer. The Ground-plane should be on both sides of the board on the top and on the ground layer.

8 Electrical Characteristics and Timing Diagrams

8.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
V_{DD} referred to GNDD		–0.3	7.0	V	
GNDA to GNDD		–0.6	0.6	V	
Analog input and output voltage Referred to V_{DD} = 5 V; Referred to GNDA = 0 V		 –5.3 –0.3	 0.3 5.3	 V V	
All digital input voltages Referred to GNDD = 0 V; (V_{DD} = 5 V) Referred to V_{DD} = 5 V; (GNDD = 0 V)		 –0.3 –5.3	 5.3 0.3	 V V	
DC input and output current at any input or output pin (free from latch-up)			10	mA	
Storage temperature	T_{STG}	–60	125	°C	
Ambient temperature under bias	T_A	–10	80	°C	
Power dissipation (package)	P_D		1	W	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 Operating Range

V_{DD} = 5 V ±5%; GNDD = 0 V; GNDA = 0 V; T_A = 0 °C to +70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current:	I_{DD}					FSC = 8 kHz, FSC, DCL, BCL active no loads, PCM idle codes, V_{IN}= 0V.
Standby			0.5	1.0	mA	
1 channel operating			14	25	mA	
2 channels operating			18	30	mA	
3 channels operating			22	35	mA	
4 channels operating			26	40	mA	
Power supply rejection ratio (either direction)	$PSRR$	30			dB	Ripple: sine wave 1014 Hz, 70 mVrms, on every supply pin, AGX=AGR=AX=AR=0dB (see **Chapter 4.2.4**)

8.3 Digital Interface

V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V; T_A = 0 °C to +70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input voltages:					
Low level	V_{IL}	–0.3	0.8	V	
High level	V_{IH}	2.0		V	
Output voltages:					
Low level	V_{OL}		0.45	V	I_{OL} = – 2 mA
Low level	V_{OL}		0.8	V	I_{OL} = – 5 mA
High level	V_{OH}	4.4		V	I_{OH} = 0.4 mA
High level	V_{OH}	4.0		V	I_{OH} = 2 mA
High level	V_{OH}	2.4		V	I_{OH} = 5 mA
Input leakage current	V_{IL}		±1	µA	$-0.3 \leq V_{IN} \leq V_{DD}$

8.4 Analog Interface

V_{DD} = 5 V ±5%; GNDD = 0 V; GNDA = 0 V; T_A = 0 °C to +70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input resistance	R_i	160	270	380	kΩ	$0 \leq V_{IN} \leq V_{DD}$
Output resistance	R_O			0.25	Ω	
Output load	R_L C_L	300		 50	Ω pF	
Input leakage current	I_{IL}		±0.1	±1.0	µA	$0 \leq V_{IN} \leq V_{DD}$
Input offset voltage	V_{IO}			±50	mV	
Output offset voltage	V_{OO}			±50	mV	
Input voltage range (AC)	V_{IN}			±2.223	V	

8.4.1 Coupling Capacitors at the Analog Interface

Coupling capacitors are required on pins V_{IN} and V_{OUT}.

The recommended value for V_{IN} is >39 nF. The required value for the V_{OUT} capacitor depends on the input impedance of the SLIC (see **Figure 14** in **Chapter 5.1**).

8.5 Reset Timing

To reset the SICOFI®4-TE to Reset State, logic low pulses applied to pin RESET# must be below 1.2 V (TTL-Schmitt-Trigger Input) and must persist longer than 3 µs.

Note: Spikes shorter than 1 µs will be ignored.

8.6 IOM-2 PCM Interface Timing

8.6.1 Single Clocking Mode

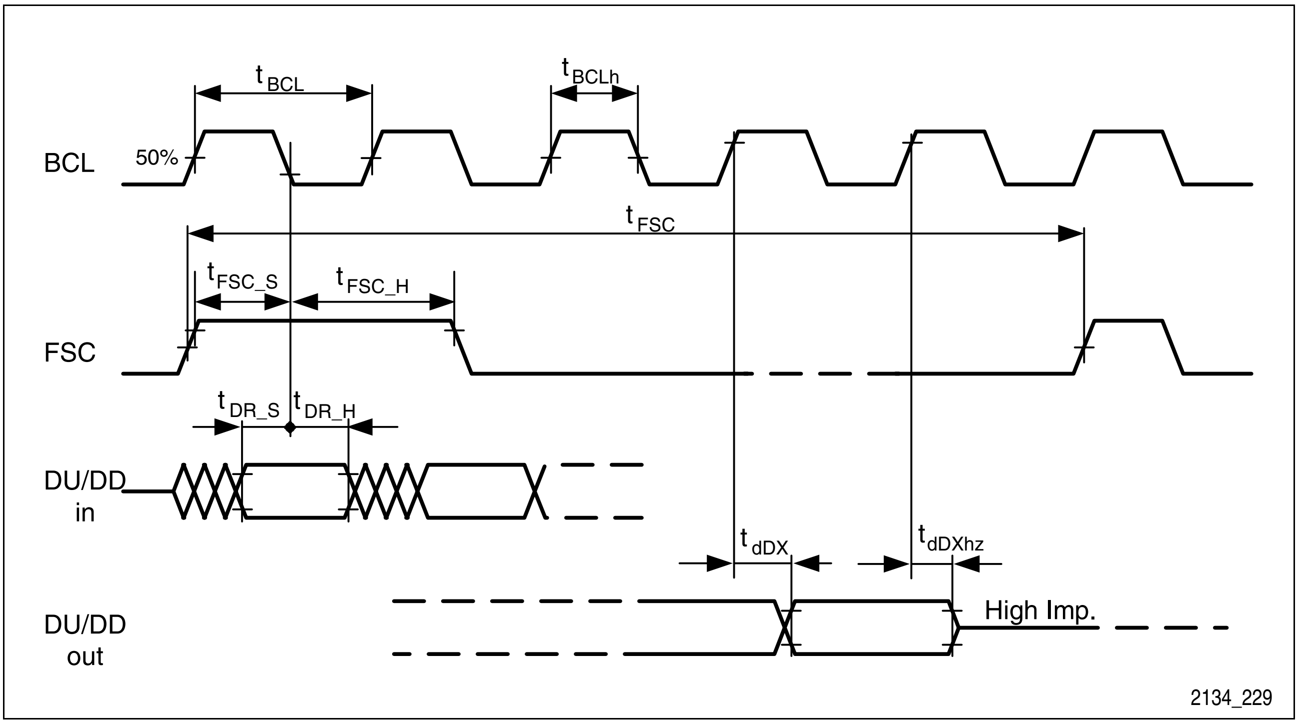


Figure 26 PCM Interface Timing in Single Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of BCL	t_{BCL}		1/768000		µs
BCL high time	t_{BCLh}	0.4^*t_{BCL}	$t_{BCL}/2$	0.6^*t_{BCL}	µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	40	50		ns
DU/DD setup time	t_{DR_s}	10	50		ns
DU/DD hold time	t_{DR_h}	10	50		ns
DU/DD delay time [1)]	t_{dDX}	25		t_{dDX_min} + t_{C_Load}	ns
DU/DD delay time to high Z	t_{dDXhz}	25		50	ns

[1)] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processing, and a second component $t_{C\_Load} = 0.4ns^*C_{Load}/pF$, caused by external circuitry (C-load).

8.6.2 Double Clocking Mode

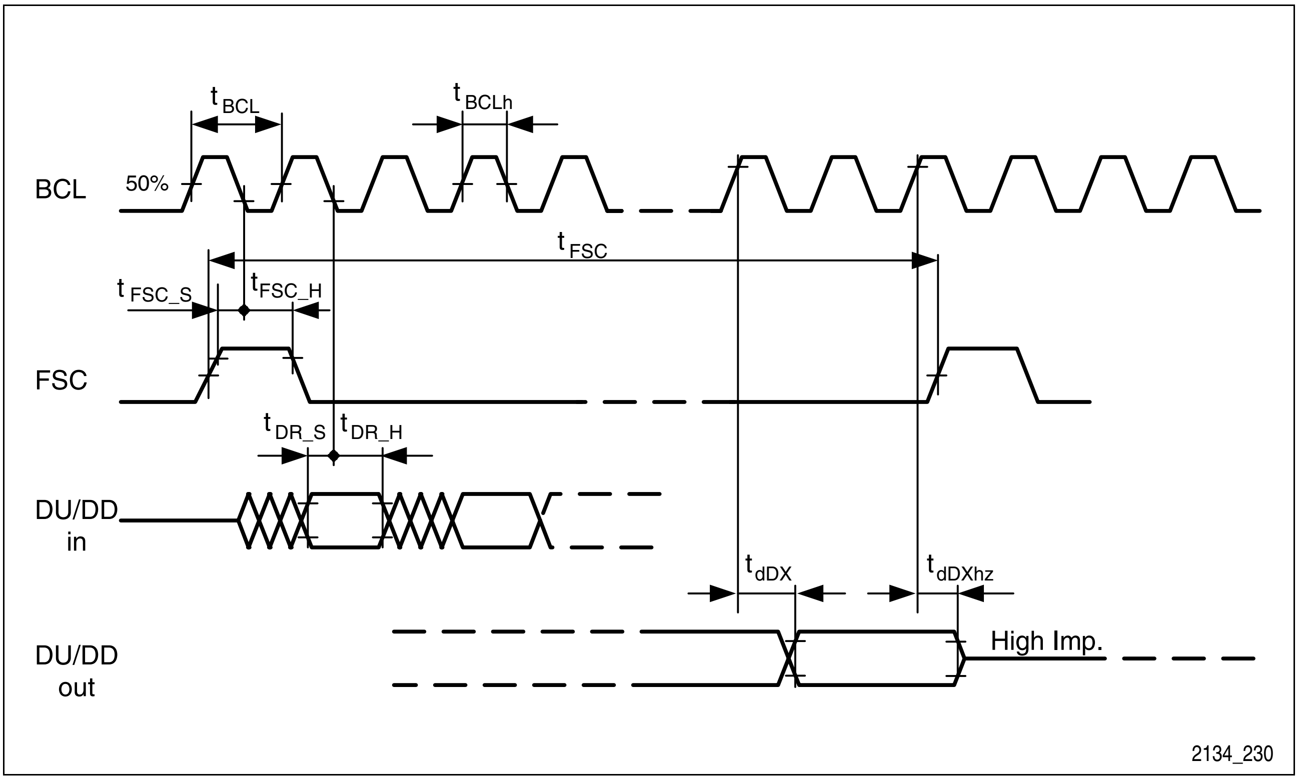


Figure 27 PCM Interface Timing in Double Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of BCL	t_{BCL}		1/1536000		µs
BCL high time	t_{BCLh}	$0.4 * t_{BCL}$	$t_{BCL}/2$	$0.6 * t_{BCL}$	µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	40	50		ns
DU/DD setup time	t_{DR_s}	10	50		ns
DU/DD hold time	t_{DR_h}	10	50		ns
DU/DD delay time [1)]	t_{dDX}	25		$t_{dDX\_min} + t_{C\_Load}$	ns
DU/DD delay time to high Z	t_{dDXhz}	25		50	ns

[1)] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processing, and a second component $t_{C\_Load} = 0.4ns * C_{Load}/pF$, caused by external circuitry (C-load).

8.7 Microcontroller Interface Timing

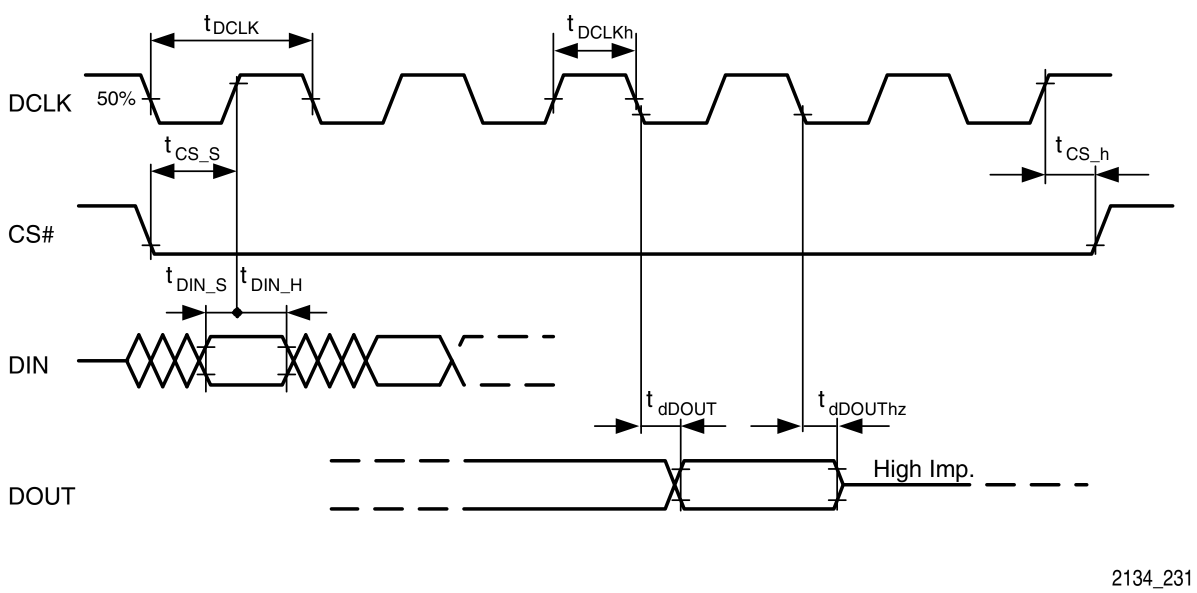


Figure 28 Timing of the Microcontroller Interface

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of DCLK	t_{DCLK}	1/8192			ms
DCLK high time	t_{DCLKh}	$0.4*t_{DCLK}$	$t_{DCLK}/2$	$0.6*t_{DCLK}$	µs
CS# setup time	t_{CS_s}	10	50		ns
CS# hold time	t_{CS_h}	30	50		ns
DIN setup time	t_{DIN_s}	10	50		ns
DIN hold time	t_{DIN_h}	10	50		ns
DOUT delay time [1)]	t_{dDOUT}	30		$t_{dDOUT\_min} + t_{C\_Load}$	ns
DOUT delay time to high Z	$t_{dDOUThz}$	30		50	ns

[1)] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processing, and a second component $t_{C\_Load} = 0.4ns*C_{Load}/pF$, caused by external circuitry (C-load).

8.8 Signaling Interface Timing

8.8.1 Timing from the Microcontroller Interface to the SO/SB-pins

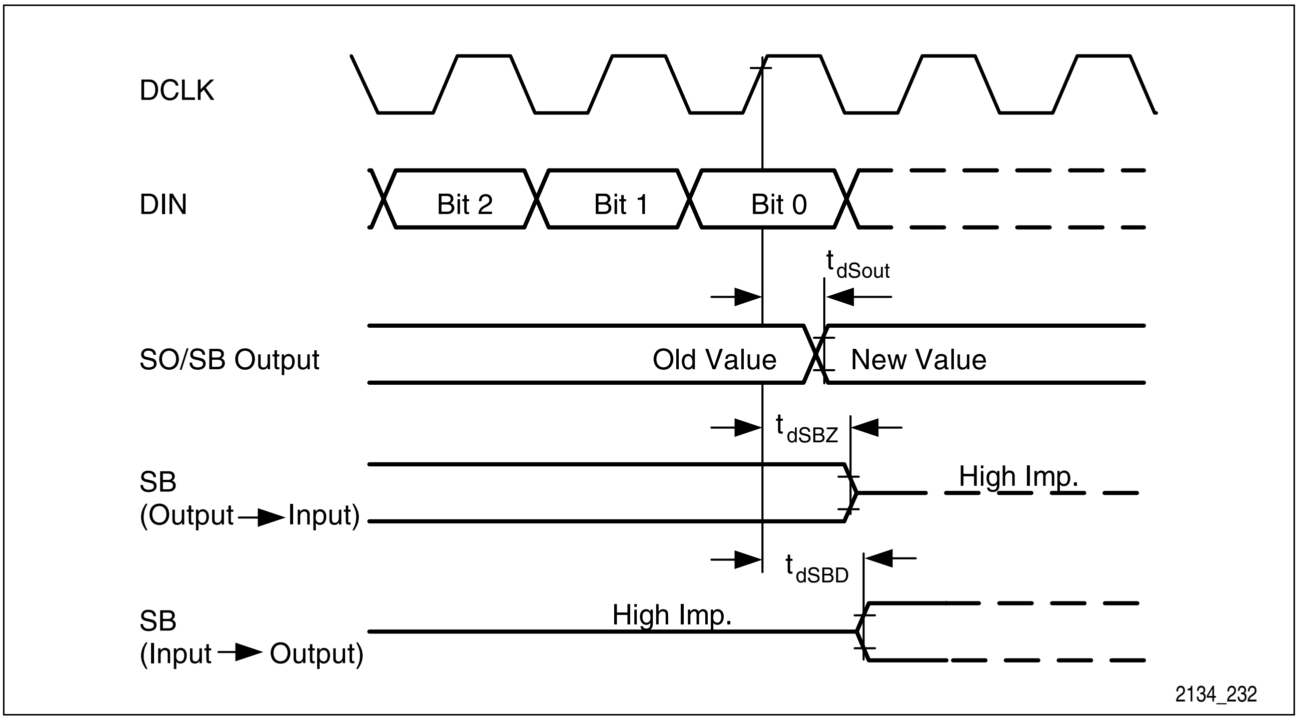


Figure 29 Signaling Output Timing (Data Downstream)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SO/SB delay time [1)]	t_{dSout}	30		t_{dSout_min}+ t_{C_Load}	ns
SB to ‘Z’ - time	t_{dSBZ}	40		100	ns
SB to ‘drive’-time	t_{dSBD}	40		t_{dSBD_min}+ t_{C_Load}	ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processing, and a second component t_{C_Load} = 0.4ns*C_{Load}/pF, caused by external circuitry (C-load).

8.8.2 Timing from the SI/SB-pins to the Microcontroller Interface

The register update and interrupt behavior resulting from signaling input changes (data upstream – pins SI and SB, if programmed as signaling inputs) depend on internal sampling clocks, counters and register settings. See **Chapter 5.3.2** for a functional description.

9 Test Modes

Each SICOFI®4-TE channel has four test loops that feed the analog input signal back to the analog output (analog test loops), and five test loops that feed the PCM input signal back to the PCM output.

Note: The signal path can also be cut off at two different points per receive and transmit direction.

9.1 Analog Loops

The four analog loops feed signals from the transmit path back into the receive path. **Figure 30** shows the locations of the analog loops.

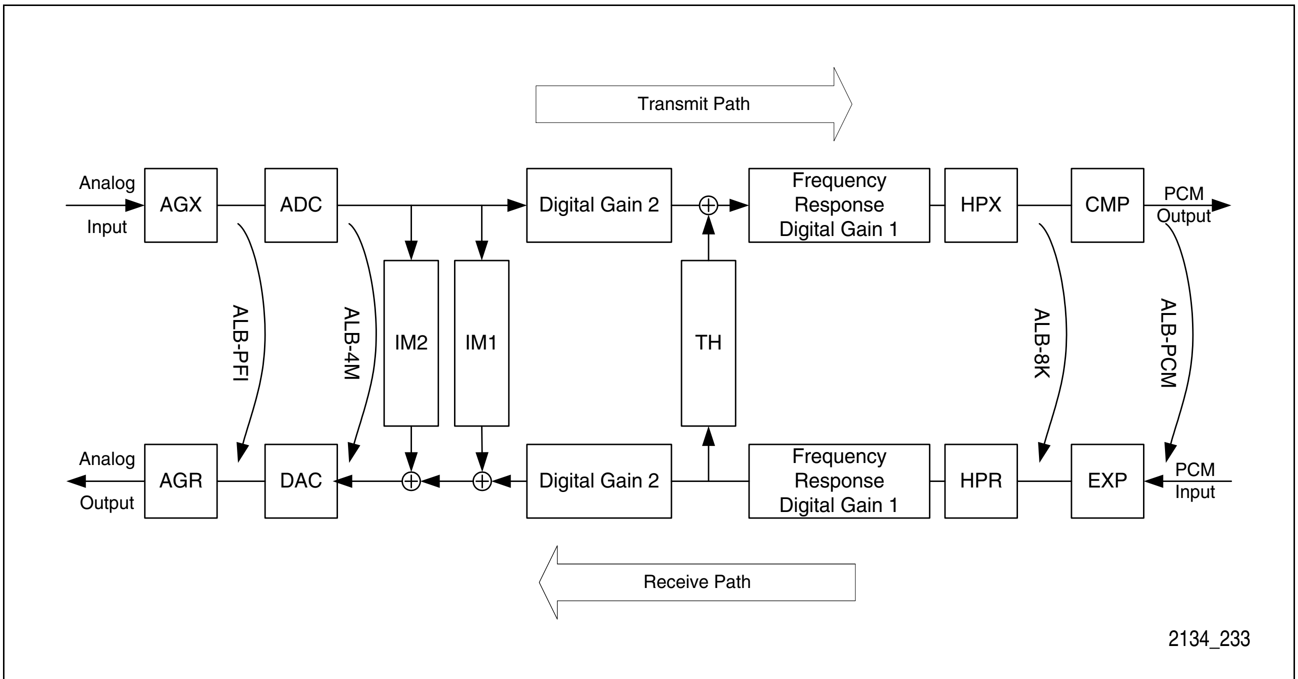


Figure 30 Analog Loops

Table 34 Analog Loop Programming in Register CR3, Bits 7 to 4

Test-Loops	Analog Loops (CR3.7 = 0)	
0000	All loops are disabled (normal operation).	
0001	ALB-PFI	Analog Loop Back via PREFI-POFI is selected.
0011	ALB-4M	Analog Loop Back via 4 MHz is selected.
0100	ALB-PCM	Analog Loop Back via 8 kHz (PCM) is selected and **in all channels active**. *(required slope setting in XR6.6, XR6.5 = 00 or 11).*
0101	ALB-8K	Analog Loop Back via 8 kHz (linear) is selected.

9.2 Digital Loops

The digital loops feed signals from the receive path back to the transmit path. There are five digital loops, which are shown in **Figure 31**.

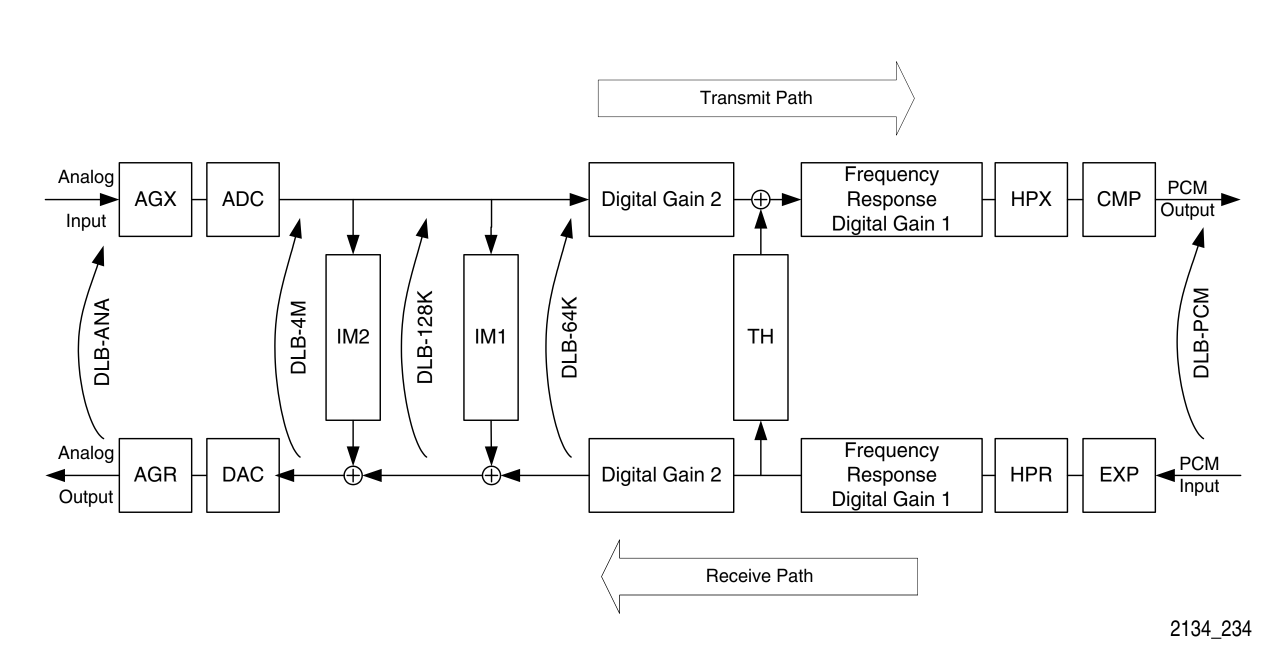


Figure 31 Digital Loops

Table 35 Digital Loop Programming in Register CR3, Bits 7 to 4

Test-Loops	Digital Loops (CR3.7 = 1)	
1000	DLB-ANA	Digital Loop Back via analog port is selected.
1001	DLB-4M	Digital Loop Back via 4 MHz is selected.
1100	DLB-128K	Digital Loop Back via 128 kHz is selected.
1101	DLB-64K	Digital Loop Back via 64 kHz is selected.
1111	DLB-PCM	Digital Loop Back via PCM Registers is selected.

9.3 Cut-Off's

The transmit path and the receive path can be cut off at two locations each. **Figure 32** shows the locations in the signal paths.

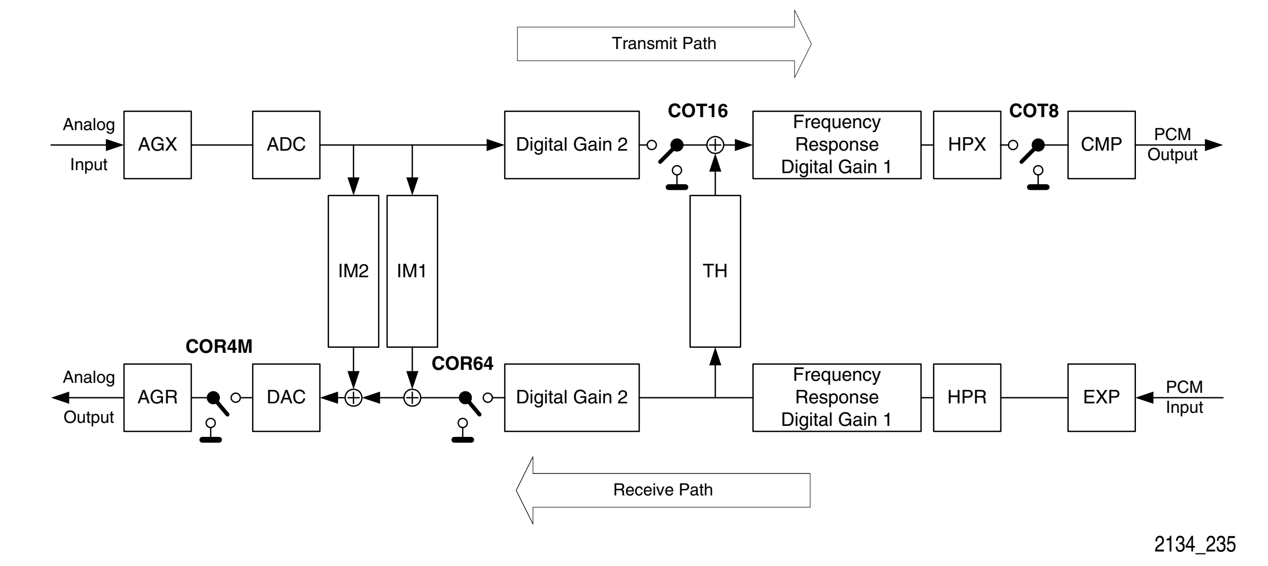


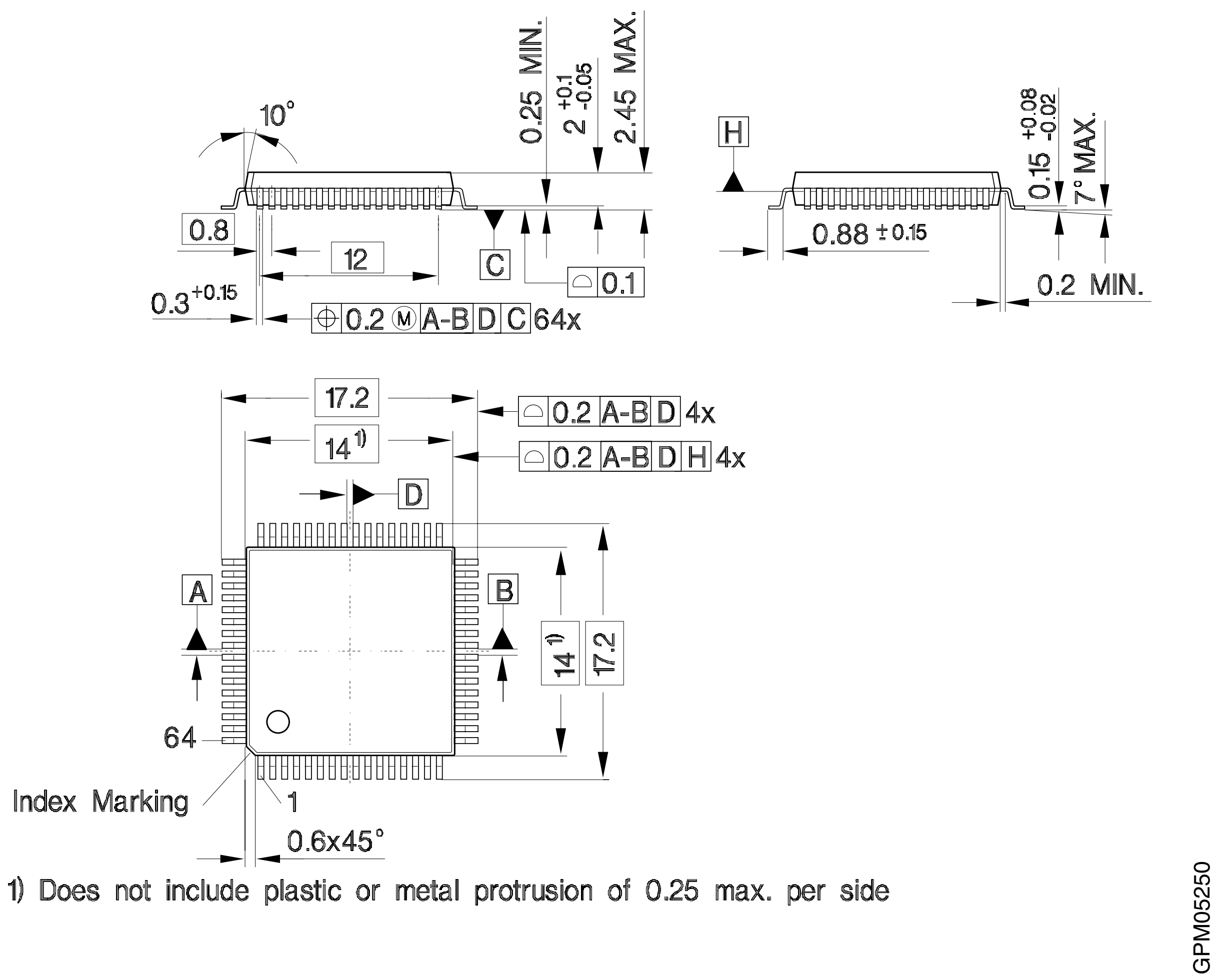
Figure 32 Cut-Off's

Table 36 Cut-Off Programming in Register CR2, Bits 7 to 5.

COT/R	Cut-Off's in the Transmit and the Receive Paths	
000	All Cut-offs disabled (Normal Operation).	
001	COT16	Cut Off Transmit path at 16 kHz (input of TH-Filter).
010	COT8	Cut Off Transmit path at 8 kHz (shortens the input of the compressor unit to ground, resulting in PCM idle codes in the transmit time slot).
101	COR4M	Cut Off Receive path at 4 MHz (POFI-output).
110	COR64	Cut Off Receive path at 64 kHz (IM-filter input).

10 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

11 Glossary

AC	**A**lternating **C**urrent
ADC	**A**nalog-to-**D**igital **C**onverter
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CRAM	**C**oefficient **RAM**
DAC	**D**igital-to-**A**nalog **C**onverter
DC	**D**irect **C**urrent
DLC	**D**igital **L**oop **C**arrier
DSP	**D**igital **S**ignal **P**rocessor
DTMF	**D**ual **T**one **M**ulti **F**requency
FIR	**F**inite **I**mpulse **R**esponse
FTTC	**F**iber-**T**o-**T**he-**C**urb
IIR	**I**nfinite **I**mpulse **R**esponse
IOM-2	**I**SDN-**O**riented **M**odular **2**nd Generation
ISDN	**I**ntegrated **S**ervices **D**igital **N**etwork
ITU	**I**nternational **T**elecommunication **U**nion
ITU-T	**I**nternational **T**elecommunication **U**nion-**T**elecommunication Standardization Sector (formerly CCITT)
NT	**N**etwork **T**ermination
PBX	**P**rivate **B**ranch E**x**change
PCM	**P**ulse **C**ode **M**odulation
POTS	**P**lain **O**ld **T**elephone **S**ystem
PSTN	**P**ublic **S**witched **T**elephone **N**etwork
PTT	**P**ost **T**elephone **T**elegraph
QSICOS	**Q**uad **SI**COFI **Co**efficient **S**oftware
RITL	**R**adio-**I**n-**T**he-**L**oop
RT	**R**emote **T**erminal
SICOFI	**Si**gnal Processor **Co**dec **Fi**lter
SLIC	**S**ubscriber **L**ine **I**nterface **C**ircuit
t/r	**t**ip/**r**ing
TA	**T**erminal **A**dapter

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