General Description

The PMB 2302, PMB 2303 are single chip dual Phase Locked Loop (PLL) synthesizers with programmable frequency dividers for use in mobile communication equipment. It is fabricated using Siemens B6HF silicon bipolar process.

The circuit consists of high speed dual modulus dividers, shift registers, programmable counters (2 A-, 2 N- and 2 R-counters), phase detectors with charge pump and a control logic block.

Since one of the high speed dual modulus dividers is able to handle frequencies of up to 1.25 GHz (2.5 GHz), there is no need to add a dedicated external prescaler. The second dual modulus divider handles frequencies up to 500 MHz. The switching signals for the dividing ratios are generated by the corresponding A-counters.

The A-counter and the N-down-counter are programmable via the 3-wire bus. They are clocked by the dual modulus divider output signals. The carry outputs of the N-counters are connected to the frequency inputs of the corresponding phase detectors and are controlling the loading of the programmed A-/N-counter start values.

The two 11 bit R-counters are also programmable and are serving as reference frequency dividers. Their carry outputs are connected to the corresponding reference frequency inputs of the phase detector and are controlling the loading of the programmed counter start values.

The phase detectors are of PFD-type (phase and frequency sensitive). They have a linear output characteristic in the 0˚ phase error region.

The control logic handles phase detectors output polarity, charge pump output currents and software-generated power-on (all circuit parts except the shift registers and data latches).

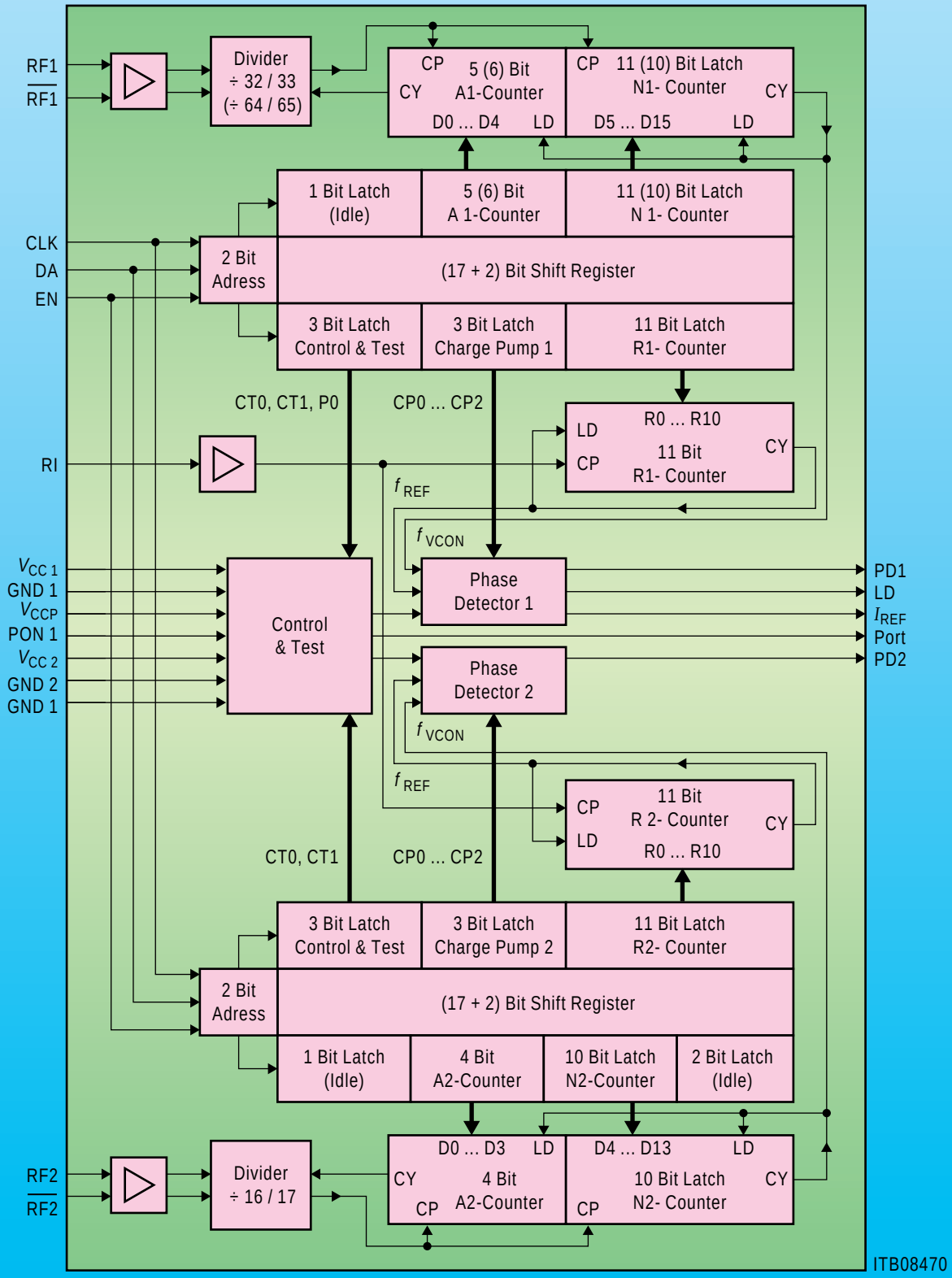
Applications

All mobile communication analog and digital systems as RF- and IF synthesizers

Type	Package
PMB 2302-R	P-TSSOP-20-1 (Shrink, SMD)
PMB 2303-R	P-TSSOP-20-1 (Shrink, SMD)

Features

- Integrated prescaler
- Low operating current
- Different power-down modes
- High input sensitivity, high input frequency
- Two fast phase detectors without dead zone
- Linearization of the phase detector output by current sources
- Large dividing ratios for small channel spacing
- PLL1 PMB 2302 PMB 2303
  max. freq. 1.25 GHz 2.5 GHz
  prescaler: :32/:33 :64/:65
  A1-counter 0 to 31 0 to 63
  N1-counter 32 to 2047 64 to 1023
  R1-counter 3 to 2047 3 to 2047
- PLL2 PMB 2302 PMB 2303
  max. freq. 500 MHz 500 MHz
  prescaler: :16/:17 :16/:17
  A2-counter 0 to 15 0 to 15
  N2-counter 16 to 1023 16 to 1023
  R2-counter 3 to 2047 3 to 2047
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} = 10 MHz)
- Switchable polarity and phase detector current programmable
- 1 port output (TTL push-pull)
- External current setting for phase detector outputs
- Lock detect output with gated pulse (quasi digital lock detect)
- Operating voltage 2.7 V to 5.5 V
- P-TSSOP-20 package
- Temperature range – 30 °C to 85 °C



Block Diagram