PE9602

2.2 GHz Integer-N

Rad-tolerant PLL

for Space Application

DESCRIPTION

Peregrine's PE9602 is a high performance integer-N PLL capable of frequency synthesis up to 2.2 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption., when compared with existing commercial space PLLs.

The PE9602 features a 10/11 dual modulus prescaler, counters and phase noise comparator as shown in Figure 1. Counter values are programmable through either a serial or parallel interfae and also can be directly hard-wired.

The PE9602 is optimized for commercial space applications. Single Event Latch up (SEL) is physically impossible and Single Event Upset (SEU) is better than 10^{-9} errors per bit/day. Fabricated in Peregrine's UTSi® (Ultra Thin Silicon) CMOS techology, the PE9602 offers excellent RF performance and intrinsic radiation tolerane.

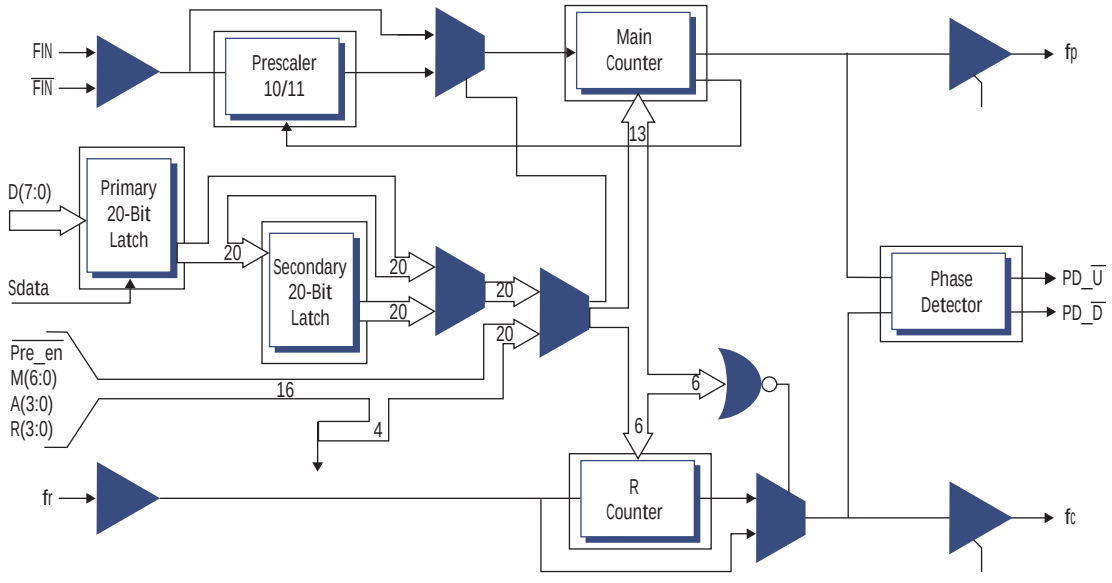
FEATURES

- 2.2 GHz operation
- ÷10/11 prescaler
- Internal phase detector
- Serial, parallel or hard-wire programmable
- Low power—25 mA at 3 V
- Input referred phase noise of -157 dBm @ 1 MHz comparison frequency

BENEFITS

- SEL immune due to UTSi CMOS
- SEU < 10^{-9} error/bit-day
- 100 krad total dose
- Reduced design cycles and enhanced reliability
- 44-pin CQFJ

FIGURE 1. PE9602 BLOCK DIAGRAM



SPECIFICATIONS

TABLE 1. DC CHARACTERISTICS

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Operational supply current; Prescaler disable Prescaler enabled	V_{DD} = 2.85 to 3.15 volt		 10 25		 mA mA
I_{stby}	Total standby current				25	µA

TABLE 2. AC CHARACTERISTICS

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Unit
Main Divider (Including Prescaler)					
f_{in}	Operating frequency		200 (Note 1)	2200	MHz
P_{fin}	Input level range	External AC coupling	–10	5	dBm
Reference Divider					
f_r	Operating frequency			100	MHz
V_{fr}	Input sensitivity	External AC coupling (Note 2)	0.5		V_{p-p}

Note 1: Lower frequency limit is DC for input waveforms with edge rates of at least 80 mV/ns.

Note 2: CMOS logic levels may be used if DC coupled.

Peregrine Semiconductor Corporation
6175 Nancy Ridge Drive
San Diego, California 92121
Tel (619) 455-0660
Fax (619) 455-0770
http://www.peregrine-semi.com

Peregrine Europe
Parc Club du Golf, bat 9
Aix-en-Provence, Cedex 3
13856 France
Tel 33(44239)3360
Fax 33(44239)7227