

## OCTAL T1/E1/J1 Line Interface Device

### FEATURES

- Monolithic device which integrates 8 T1/J1 or E1 shorthaul and longhaul line interface circuits. T1/J1 or E1 operation is selectable on a per-device basis.
- Meets or exceeds T1/J1 and E1 shorthaul and longhaul network access specifications including ANSI T1.102, T1.403, T1.408, AT&T TR 62411, ITU-T G.703, G.704 as well as ETSI 300-011, CTR-4, CTR-12 and CTR-13.
- Provides encoding and decoding of B8ZS, HDB3 and AMI line codes.
- Provides receive equalization, clock recovery, and line performance monitoring.
- Provides transmit and receive jitter attenuation.
- Provides support for redundancy.
- Provides digitally programmable longhaul and shorthaul line build-out.
- Provides a selectable, per channel independent de-jittered T1 or E1 recovered clock for system timing and redundancy.
- Provides PRBS generators and detectors on each tributary for error

testing at DS1 and E1 rates as recommended in ITU-T O.151.

- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a hardware-only mode for operation without a microprocessor.
- Provides line and digital loopback modes.
- Supports programmable inband loopback codes.
- Uses line rate system clock.
- Provides an IEEE 1149.1 (JTAG) compliant test access port (TAP) and controller for boundary scan test.
- Implemented in a low power 3.3 V tolerant 1.8/3.3 V CMOS technology.
- Available in a high density 288-pin Tape-SBGA (23 mm x 23 mm) package.
- Provides a -40 °C to +85 °C industrial temperature operating range.

- High-density SBI bus interface. Supports seamless interconnection of up to 11 OCTLIUs to TE-32, TEMAP-84 and AAL1gator-32 using only 27 wires.

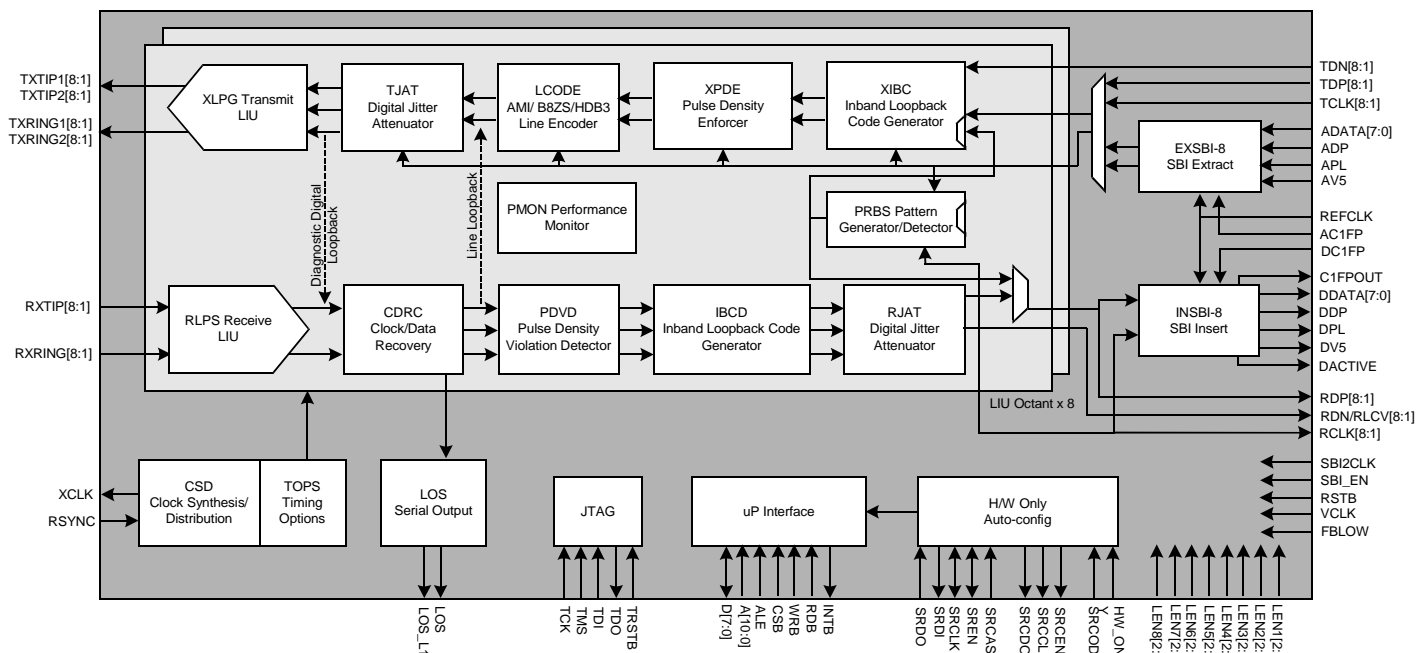
### RECEIVE SECTION

- Supports T1 signal reception for distances with up to 36 dB of cable attenuation (at 772kHz).
- Supports E1 signal reception for distances with up to 36 dB of cable attenuation (at 1.024MHz).
- Performs B8ZS or AMI decoding when processing a bipolar DS-1 signal, and HDB3 or AMI decoding when processing a bipolar E1 signal.
- Tolerates more than 0.3 UI peak-to-peak, high frequency jitter as required by AT&T TR 62411 and Bellcore TR-TSY-000170.
- Detects line code violations, B8ZS/HDB3 line code signatures, loss of signal, and successive zeroes conditions.
- Supports G.772 compliant non-intrusive protected monitoring points.

### SYSTEM INTERFACE

- Supports the following system interfaces:
  - 8 independently configurable serial clock and data lines supporting single-rail or dual-rail data.

### BLOCK DIAGRAM



**OCTAL T1/E1/J1 Line Interface Device****TRANSMIT SECTION**

- Generates DSX-1 shorthaul and DS-1 longhaul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.
- Generates E1 pulses compliant to G.703 recommendations.
- Provides line outputs that are current limited and may be tristated for protection or redundant applications.
- Provides a digital phase locked loop for generation of a low jitter transmit clock complying with all jitter attenuation, jitter transfer, and residual

jitter specifications of AT&T TR 62411 and ETSI TBR 12 and TBR 13.

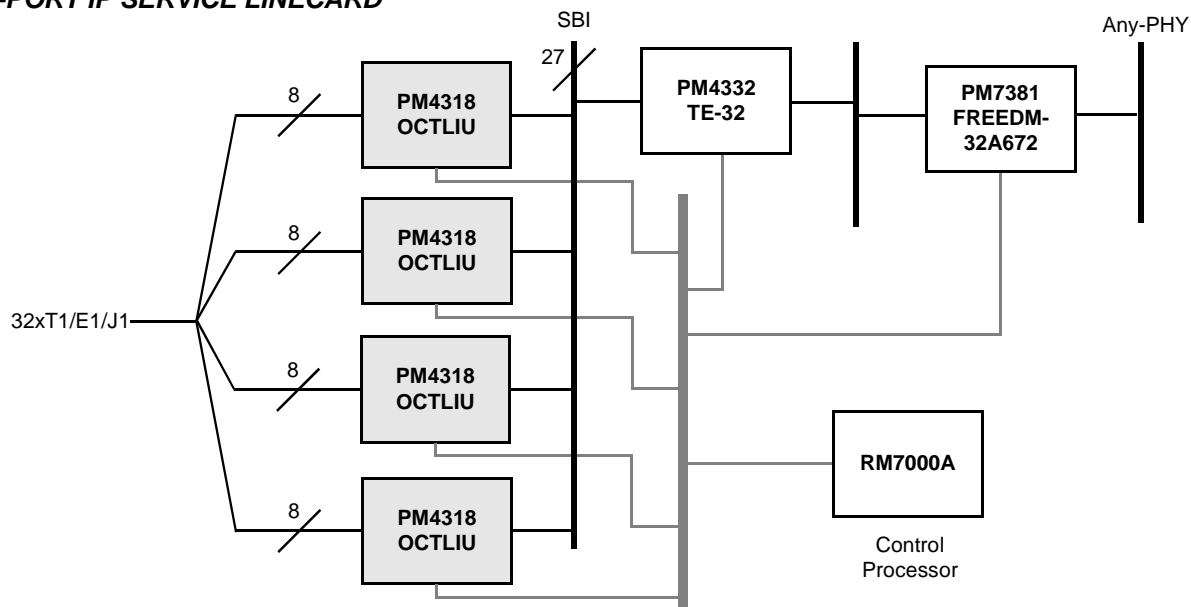
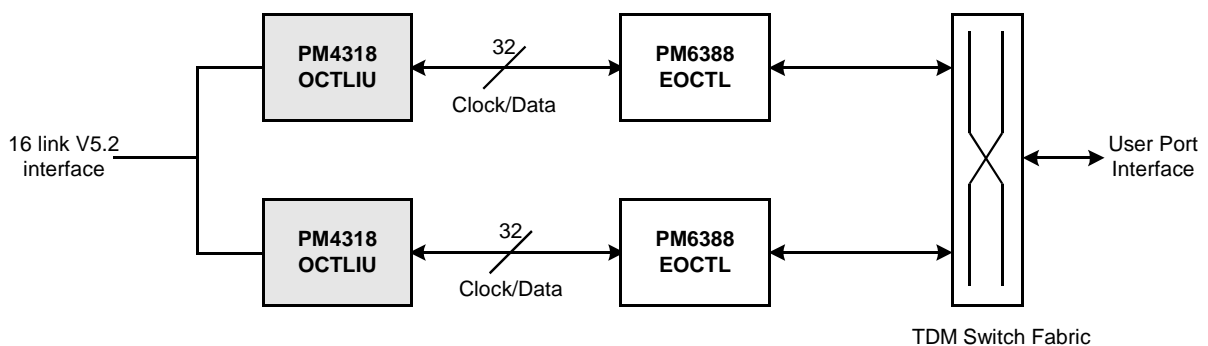
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.
- Supports all ones transmission for alarm indication signal (AIS) generation.

**GENERAL**

- Can be configured to act as a converter between the SBI interface and serial clock/data. In this mode, the LIUs are unused.

**APPLICATIONS**

- Metro Optical Access Equipment.
- Edge Router Linecards.
- Multiservice ATM Switch Linecards.
- DSLAMs.
- 3G Wireless Equipment.
- Voice Gateways.
- Digital Private Branch Exchanges (PBX).
- Digital Access Cross-Connect Systems (DACS).

**TYPICAL APPLICATIONS****32-PORT IP SERVICE LINECARD****16 PORT V5.2 INTERFACE**

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