32 Link CES/DBCES AAL1 SAR

FEATURES

- Supports 32 structured/unstructured T1, E1, or two unstructured DS3, E3 or STS-1/STM-0 links over ATM.
- Compliant with ATM Forum's CES (AF-VTOA-0078), and ITU-T I.363.1.
- Supports up to 1024 VCs.
- Supports n x 64 (consecutive channels) and m x 64 (non-consecutive channels) structured data format with channel associated signaling (CAS) support.
- Internal E1/T1 clock synthesizers provided for each line which can be controlled via internal synchronous residual time stamp (SRTS) or an internal programmable weighted moving average adaptive clocking algorithm in unstructured mode. Clock synthesizers can also be controlled externally to provide customization of SRTS or adaptive clocking methods.
- Provides transparent transmission of CCS and CAS and termination of CAS signaling.
- Compliant with ATM Forum's Dynamic Bandwidth Circuit Emulation Service (DBCES) AF-VTOA-0085. Supports idle channel detection via processor intervention, CAS signaling, or data pattern detection. Provides idle channel indication on a per channel basis.
- Supports AAL0 mode, selectable on a per VC basis.
- Provides transmit and receive buffers which can be used for OAM cells as well as any other user-generated cells such as AAL5 cells for ATM signaling.

LINE INTERFACE

- Supports the following flexible line interfaces:
  - 32 T1, E1 or 2 DS3 links using the 19.44 MHz Scalable Bandwidth Interconnect (SBI™) bus. Can map any SBI tributary to any of the 32 AAL1 links.
  - 16 individual T1 or E1 lines.
  - Eight H-MVIP lines at 8 MHz.
  - Two unstructured DS3, E3 or STS-1/STM-0 lines.
- Provides lineside loopback support on a per channel basis.

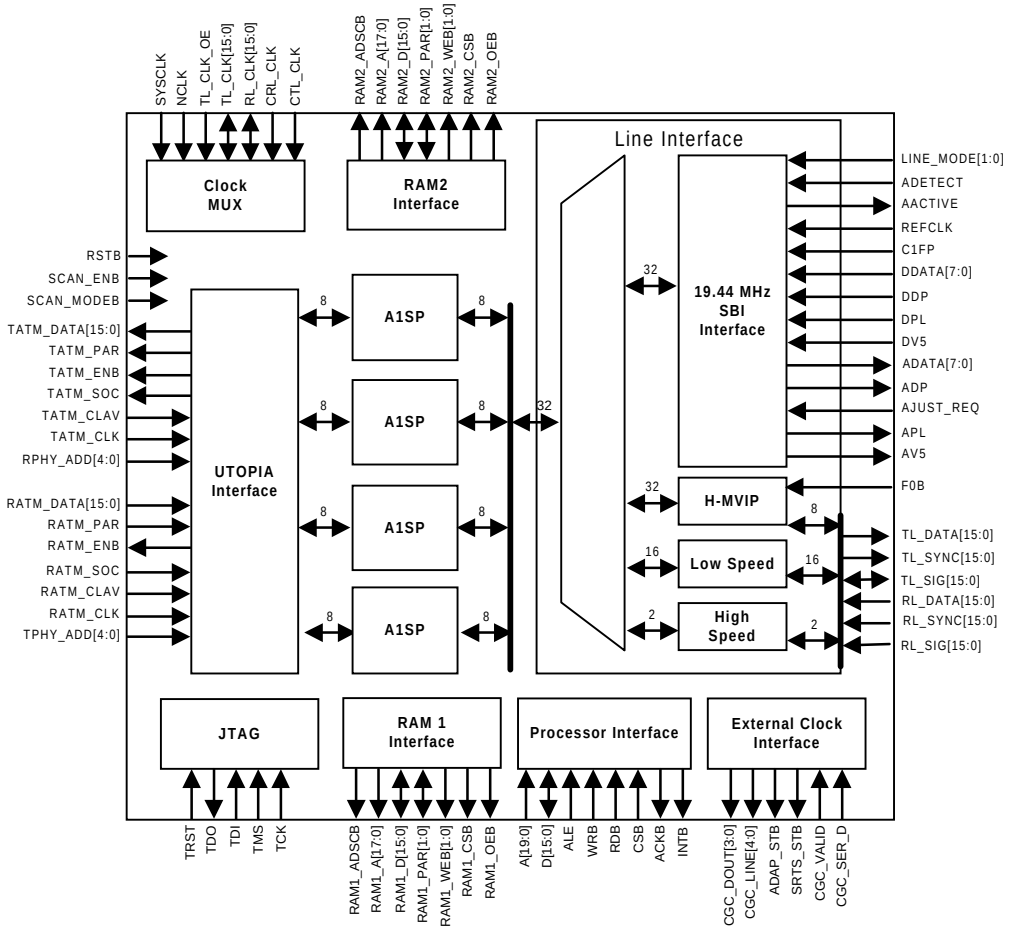
UTOPIA INTERFACE

- Supports 52 MHz, 8/16-bit Level 2, Multi-Phy Mode (MPHY) with parity, 8/16-bit Level 1, SPHY and 8-bit Level 1, ATM Master modes.
- The receive UTOPIA port can be configured as a single PHY or as four separate PHYs.
- Provides an optional 8/16-bit Any-PHY™ slave interface.
- Provides a three cell FIFO for UTOPIA loopback support on a per VC basis or a global basis.

TRANSMIT SECTION

- Provides individually enabled per-VC data and signaling conditioning in the transmit cell direction and per DS0 data and signaling conditioning in the transmit line direction. Includes DS3 AIS conditioning support in both directions.
- Provides per-VC configuration of time slots allocated, CAS support, partial cell size, data and signaling conditioning, ATM Cell header definition.
- Generates AAL1 sequence numbers, pointers and SRTS values in accordance with ITU-T I.363.1. Multicast connections are supported.
- Provides a patented frame based calendar queue service algorithm with anti-clumping add-queue mechanism that produces minimal CDV. In unstructured mode uses non-frame based scheduling to optimize CDV.
- Queues are added by making entries into an add queue FIFO to minimize queue activation overhead.

BLOCK DIAGRAM



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RECEIVE SECTION

- Provides per-VC configuration of time slots allocated, partial cell size, sequence number processing options, cell delay variation tolerance buffer depth, maximum buffer depth.
- Supports Fast Sequence Number processing and Robust Sequence Number processing.

GENERAL

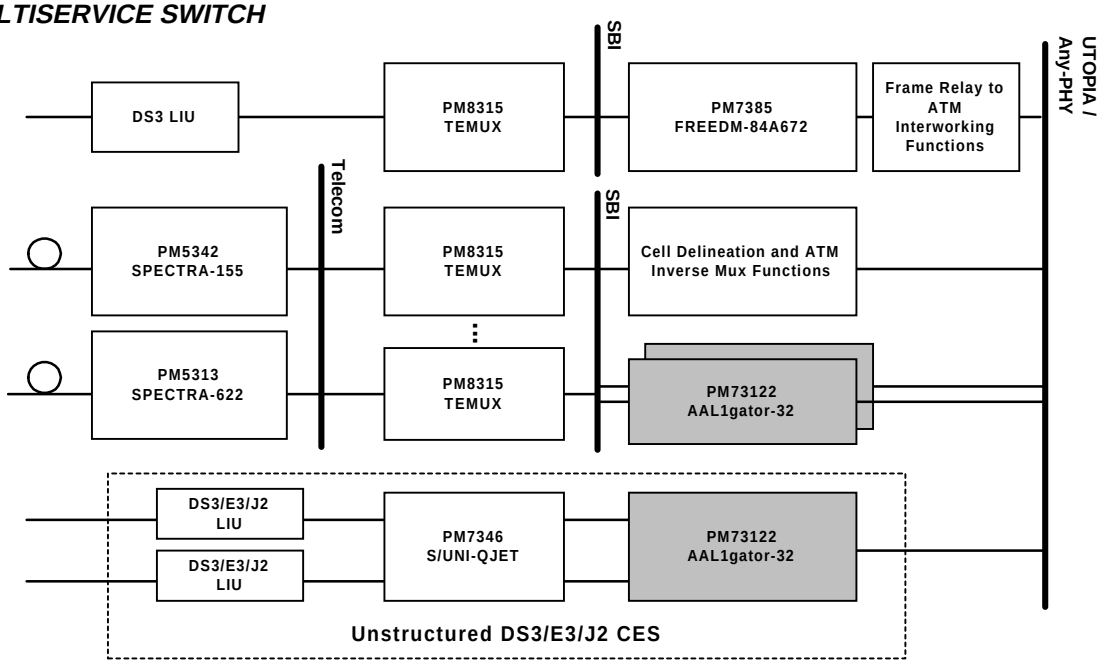
- Provides a microprocessor interface for configuration, management, and statistics gathering.
- Provides single maskable, open-collector interrupt with master interrupt register to facilitate processing for AAL1, RAM, UTOPIA and SBI exceptions.
- Provides multiple counters in the Cell Transmit and Receive directions as required by the ATM Forum's CES-IS 2.0 MIB.
- Provides a seamless interface to two external 256K x 16(18) (10 ns) Synchronous SRAMs or ZBT RAMs.
- Low-power 2.5V CMOS with 3.3V, 5V tolerant I/O.
- 352-pin super ball grid array (SBGA) package.

APPLICATIONS

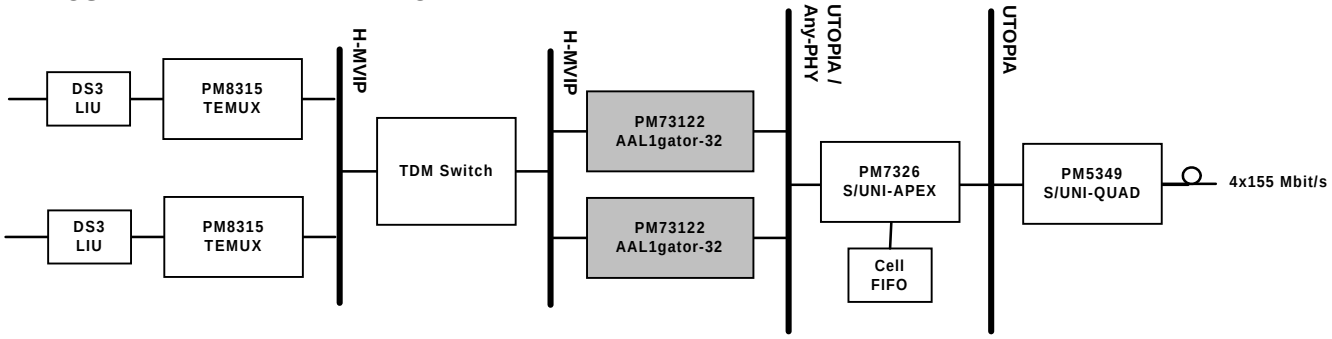
- Multiservice Switch CES Port Cards.
- DACS with an ATM interface.
- Optical Line Termination in an ATM Passive Optical Network (APON)

TYPICAL APPLICATIONS

ATM MULTISERVICE SWITCH



DACS WITH AN ATM INTERFACE



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