# Frame Engine and Data Link Manager

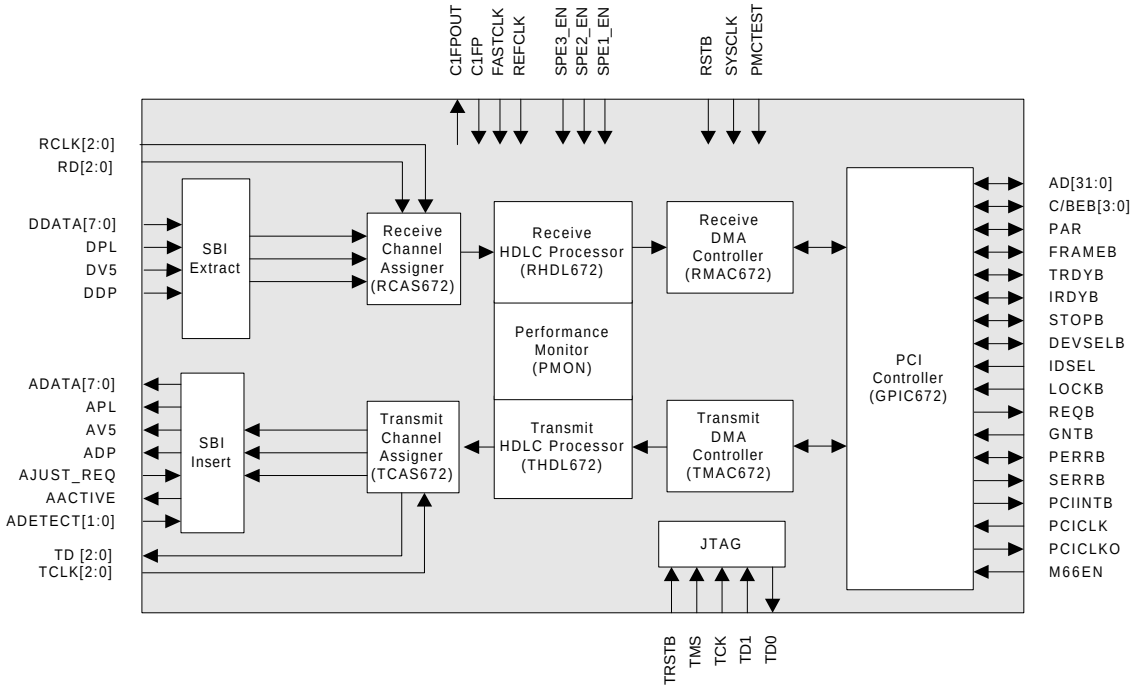
## FEATURES

- Single-chip multi-channel HDLC controller with a 66 MHz, 32 bit PCI 2.1 compliant bus for configuration, monitoring and transfer of packet data.
- On-chip DMA controller with scatter/gather capabilities.
- Supports up to 672 bi-directional HDLC channels assigned to a maximum of 84 channelised or unchannelised links conveyed via a 19.44 MHz Scalable Bandwidth Interconnect (SBI™) interface.
- Data on the SBI interface is divided into three Synchronous Payload Envelopes (SPEs). Each SPE can be configured independently to carry data for either 28 T1/J1 links, 21 E1 links, or one unchannelised DS-3 link.
- Supports three bi-directional HDLC channels each assigned to an unchannelised link with arbitrary rate link of up to 52 MHz when SYSCLK is running at 40 MHz. Each link may be configured individually to replace one of the SPEs conveyed on the SBI interface.
- For each channel, the HDLC receiver supports programmable flag sequence detection, bit de-stuffing and frame check sequence validation. The receiver supports the validation of both CRC-CCITT and CRC-32 frame check sequences.
- For each channel, the HDLC transmitter supports programmable flag sequence generation, bit stuffing and frame check sequence generation. The transmitter supports the generation of both CRC-CCITT and CRC-32 frame check sequences. The transmitter also aborts packets under the direction of the host or automatically when the channel underflows.
- Provides 32 Kbytes of on-chip memory for partial packet buffering in both the transmit and receive directions. This memory may be configured to support a variety of different channel configurations from a single channel with 32 Kbytes of buffering to 672 channels, each with a minimum of 48 bytes of buffering.
- Provides a standard five signal P1149.1 JTAG test port for boundary scan board test purposes.
- Supports 3.3 Volt I/O on non-PCI signals. Supports 3.3 Volt PCI signaling environment.
- 352 pin enhanced ball grid array (SBGA) package.

## APPLICATIONS

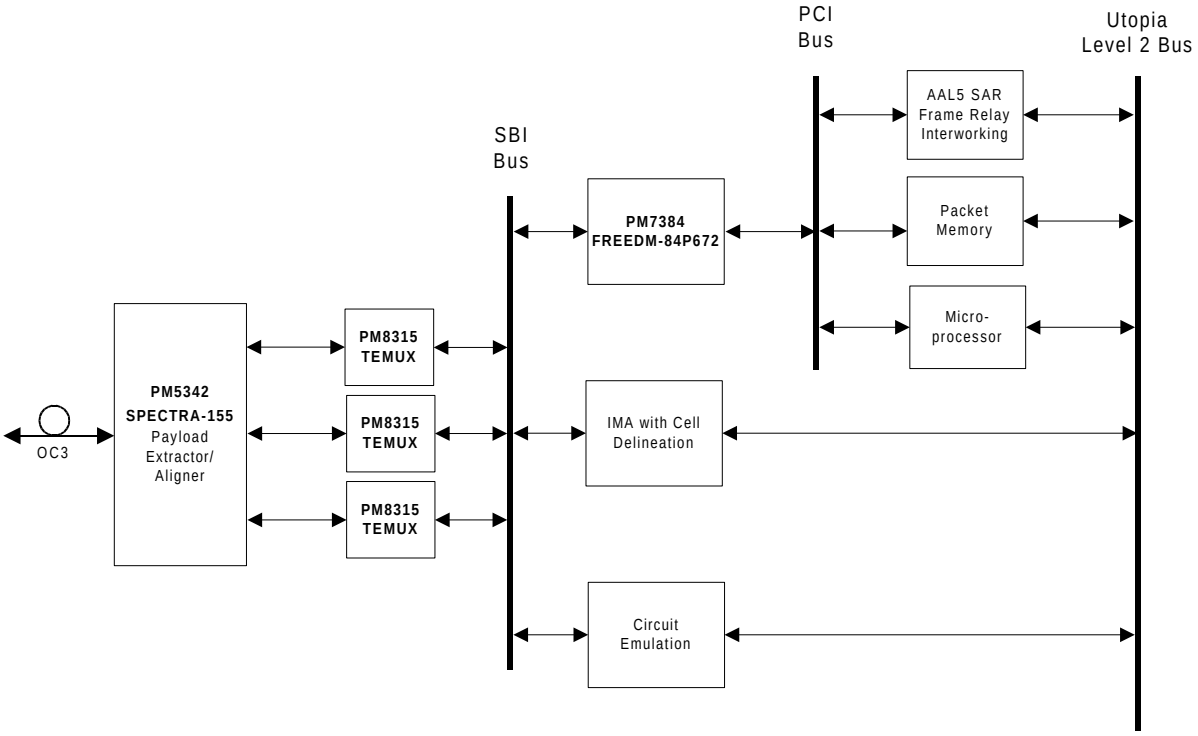
- PPP interfaces for routers.
- Internet/Edge Routers.
- Frame Relay/Multiservice Switches.
- Packet-based DSLAM equipment.
- Remote Access Concentrators.
- Multiservice Access Concentrators.

## BLOCK DIAGRAM

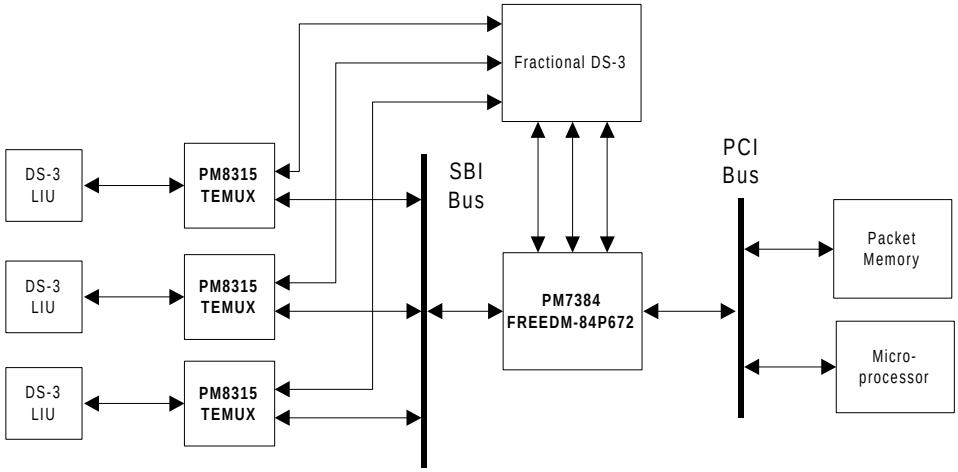


## TYPICAL APPLICATION

### *INTEGRATED SERVICES APPLICATION*




### *N X DS-3 INTERFACE*

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