

Quad 155 Mb/s ATM and Packet Over SONET/SDH Physical Layer Device

FEATURES

- Quad channel ATM and Packet over SONET OC-3c (155 Mb/s) PHY.
- Provides on-chip clock and data recovery and clock synthesis.
- Exceeds Bellcore-GR-253 jitter requirements.
- Inserts and extracts ATM cells or POS packets into/from SONET SPE.
- Filters and captures Automatic Protection Switch bytes (K1 and K2) and detects APS byte failure.
- Detects signal degrade and signal failure thresholds crossing alarms.
- Captures and debounces synchronization status byte (S1).
- Extracts and inserts the 16- or 64-byte section trace (J0) and path trace (J1) messages.
- Extracts and inserts section/line data communication channels (DCC).

- Provides circuitry to meet holdover, wander and long term stability.
- Provides a generic 8-bit microprocessor interface for device control and register access.
- Provides standard IEEE 1149.1 JTAG test port for boundary scan.

ATM

- Implements the ATM Forum User Network Interface Specification.
- Performs cell payload scrambling and descrambling.
- Provides a UTOPIA Level 2-compliant system interface.
- Provides synchronous 4-cell transmit and receive FIFO buffers.

PACKET OVER SONET

- Generic design that supports packet based protocols like PPP, HDLC and Frame Relay.

- Implements the PPP over SONET/SDH specification according to RFC 1619 and 1662 of the IETF.
- Performs flag sequence detection and insertion.
- Performs CRC-CCITT and CRC-32 FCS generation and validation.
- Performs byte stuffing and destuffing.
- Checks for minimum and maximum packet lengths.

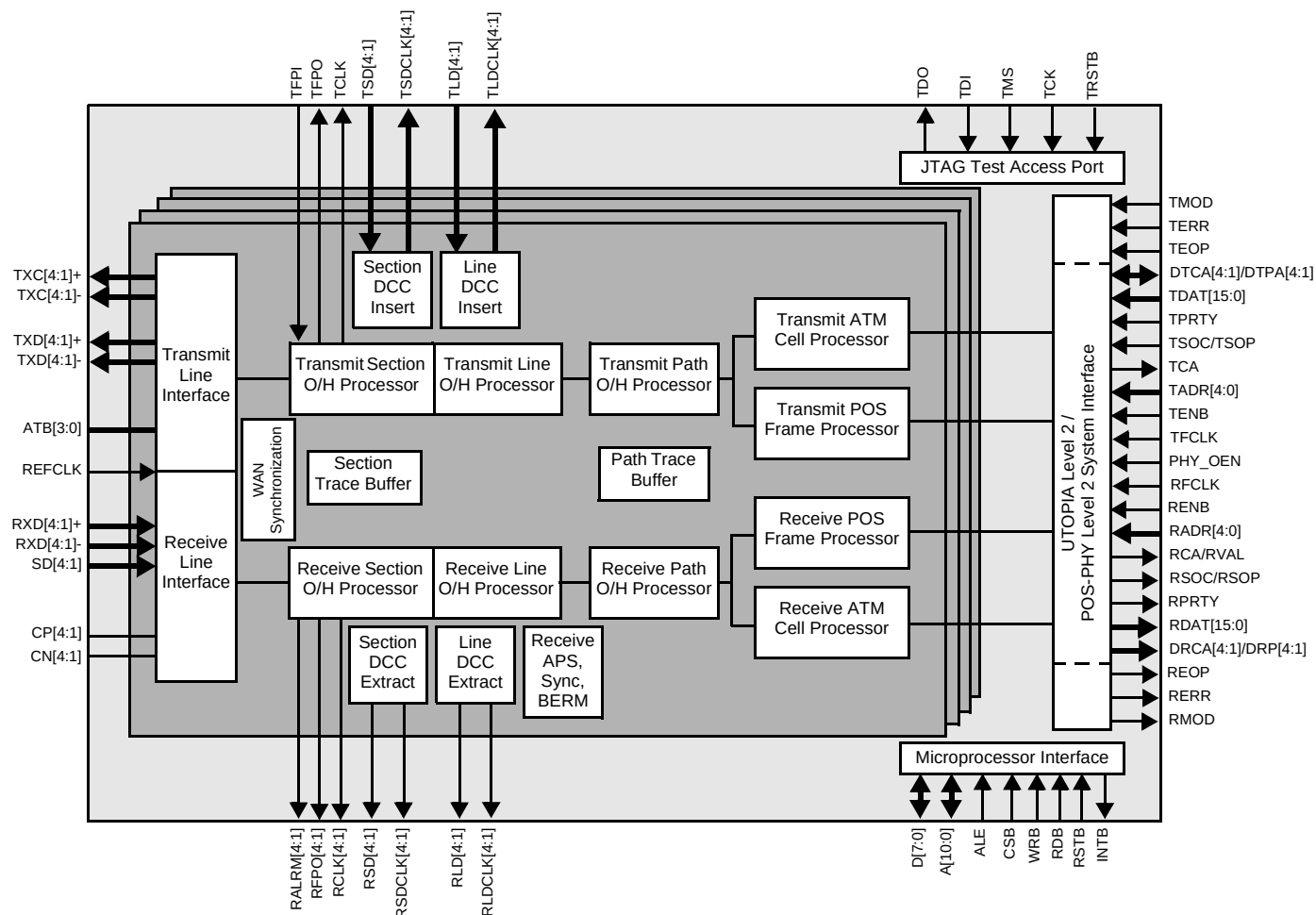
PACKAGING

- Low power, 3.3 V CMOS technology.
- Packaged in a 304-pin Ball Grid Array (BGA) package.
- Industrial temp. range (-40° to +85°C).

APPLICATIONS

- WAN and Edge ATM Switches
- Multiprotocol Switches
- Layer 3 Switches
- Routers, Packet Switches, and Hubs

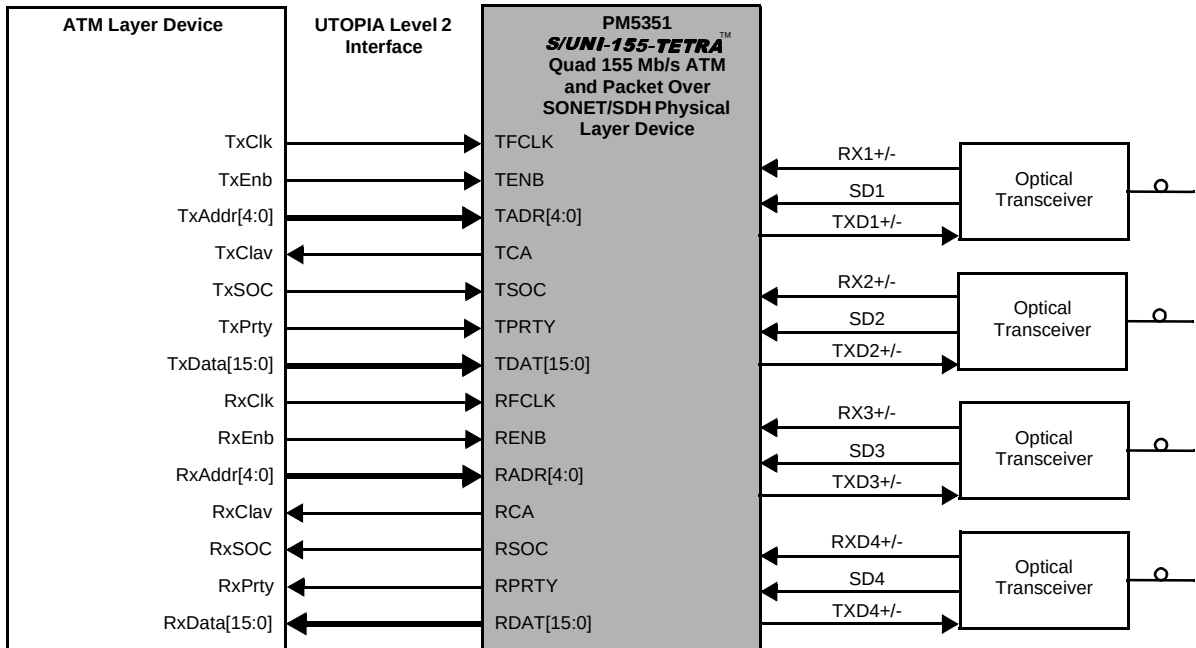
BLOCK DIAGRAM



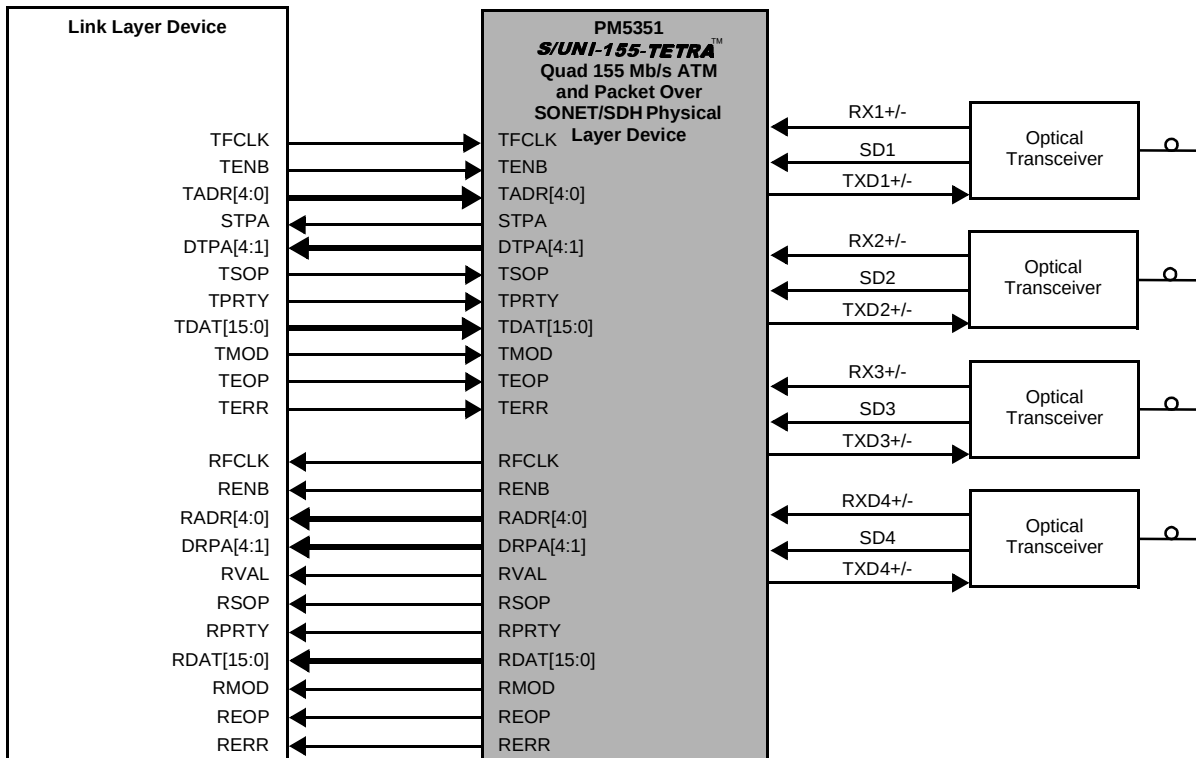
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TYPICAL APPLICATIONS

STS-3c (STM-1) ATM SWITCH PORT APPLICATION



STS-3c (STM-1) PACKET OVER SONET APPLICATION



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