ATM SAR and PHY Processor for PCI Bus

FEATURES

- Combines PHY, ATM, AAL5, and PCI DMA Controller on a single device to simplify the design, programming, and manufacturing of ATM adapters.
- Conforms to ATM Forum User-Network Interface (UNI) Specification Version 3.1, Bellcore Standard TA-NWT-001113, and ITU-T Recommendations I.432 and I.363.

HOST INTERFACE

- Provides a 32-bit, 33 MHz Peripheral Component Interconnect (PCI) Local Bus Specifications Version 2.1 interface and supports both bus-master and bus-slave access modes. Other 32-bit system buses can be accommodated using external glue logic.
- Implements an efficient DMA controller to manage the transfer of packets between the SAR engine and the host memory with minimum PCI Host intervention. There is no need for a local packet memory.
- The transmit and receive DMA channels support scatter/gather capabilities where a packet can be stored in non-contiguous buffers.
- Provides an 8-cell FIFO in the transmit direction and a 96-cell FIFO in the receive direction to allow for up to 270 µs of PCI bus latency in the receive direction.

PHYSICAL LAYER

- Incorporates the industry standard PMC PM5346 S/UNI-LITE™ to provide SONET and SDH interfaces at STS-3c/STM-1 (155.52 Mb/s) and STS-1 (51.84 Mb/s) rates.
- Provides on-chip clock recovery and clock synthesis units that are compliant with Bellcore TR-NWT-000253 Issue 2 and ITU-T Recommendation G.958 jitter requirements.
- Performs SONET/SDH framer, overhead, and cell processing functions at STS-3c/STM-1 and STS-1 rates.

ATM AND ADAPTATION LAYERS

- Supports the simultaneous segmentation and reassembly of 128 open Virtual Circuits (VCs) in both transmit and receive directions.
- Provides leaky bucket Peak Cell Rate (PCR) enforcement using eight programmable peak queues coupled with sub-rate control on a per-VC basis.
- Implements Sustainable Cell Rate (SCR) enforcement using a token generation mechanism on a per-VC basis.
- Provides an internal VC parameter storage for both the 128 transmit and 128 receive VCs to simplify the design of the ATM adapter and to sustain a high data throughput rate.

MULTIPURPOSE PORT

- In bypass mode, provides an 8-bit SCI-PHY™ or UTOPIA-compliant port to connect to an external physical layer processor such as PM7345 S/UNI-PDH™ for DS3/E3 UNI.
- In non-bypass mode, supports the insertion and extraction of Constant Bit Rate (CBR) cells that carry encoded video and audio signals.

MICROPROCESSOR INTERFACE

- In slave mode, provides a generic 8-bit microprocessor port for the configuration, control, and monitoring by an optional microprocessor.
- In master mode, allows for the control of two external devices without glue logic.

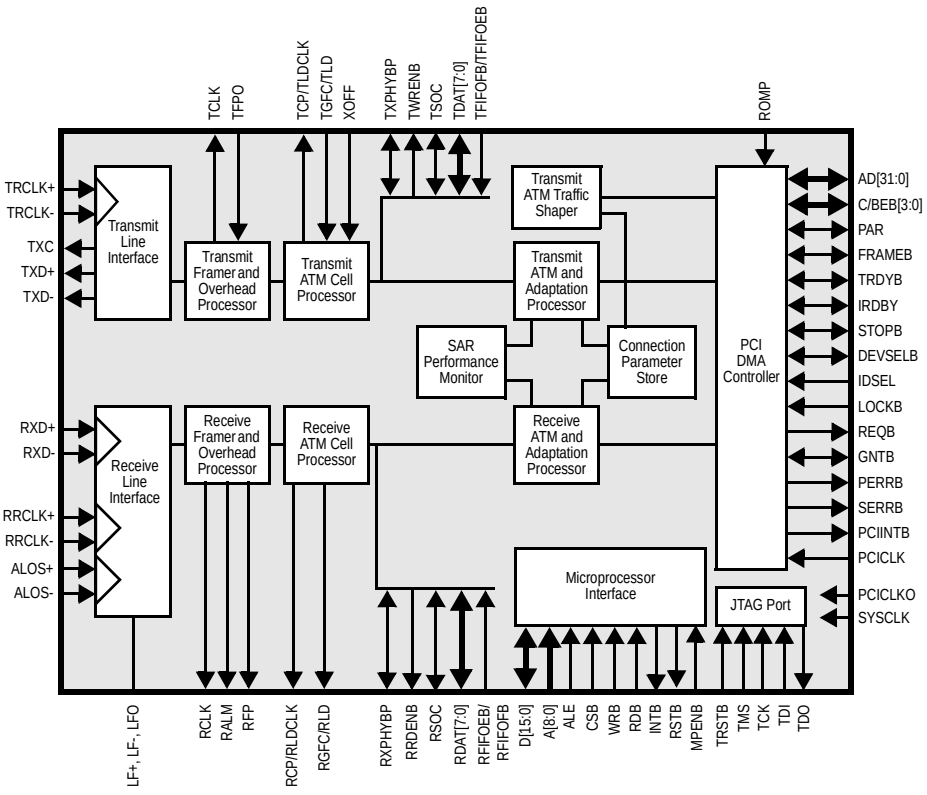
PACKAGING

- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Implemented in low power, 0.6 micron, +5 V CMOS technology with TTL and Pseudo ECL (PECL) compatible inputs and outputs.
- Packaged in 208-pin Plastic Quad Flat Pack (PQFP) package.

APPLICATIONS

- ATM Workstations and Adapters
- ATM Bridges, Switches, and Hubs
- Multimedia Terminals

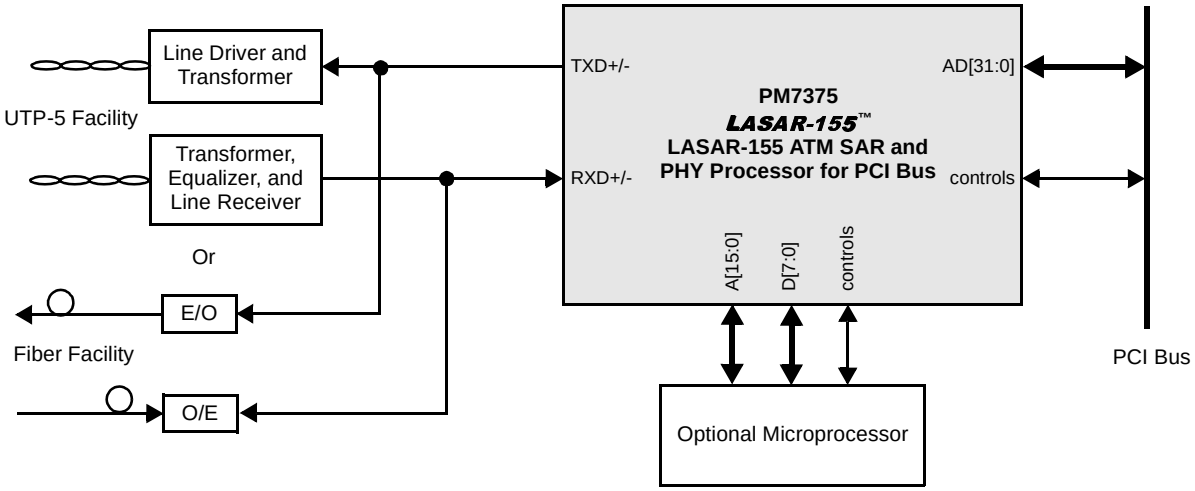
BLOCK DIAGRAM



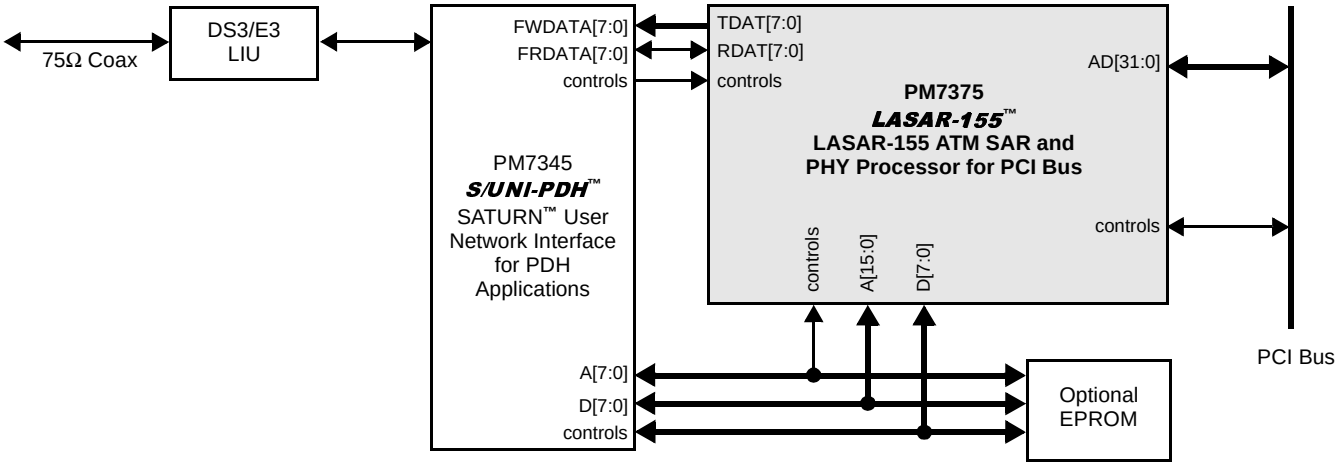
ATM SAR and PHY Processor for PCI Bus

TYPICAL APPLICATIONS

ATM ADAPTER FOR PCI BUS



INTERFACE TO EXTERNAL PHYSICAL LAYER PROCESSOR (S/UNI-PDH)



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to:
document@pmc-sierra.com
or contact the head office,
Attn: Document Coordinator

All product documentation is available on our web site at:
http://www.pmc-sierra.com
For corporate information, send email to:
info@pmc-sierra.com

PMC-931138 (R6)

October, 1998