

622 Mbit/s ATM Physical Layer Device

FEATURES

GENERAL

- ATM OC-12c (622 Mbit/s) PHY
- Provides on-chip clock and data recovery and clock synthesis.
- Exceeds Bellcore-GR-253 jitter tolerance and transmit jitter requirements.
- Provides a generic 8-bit microprocessor interface for device control and register access.
- Provides standard IEEE 1149.1 JTAG test port for boundary scan.

SONET RECEIVER

- Recovers clock and data.
- Frames to and descrambles recovered stream.
- Filters and captures Automatic Protection Switch bytes (K1,K2) and detects APS byte failure.
- Detects signal degrade and signal failure threshold crossing alarms.
- Captures and debounces synchronization status byte (S1).

- Counts received section BIP-8 (B1), line BIP-24 (B2), and path BIP-8 (B3) errors, and line and path FEBEs.
- Detects LOS, OOF, LOF, LAIS, LRDI, LOP, PAIS, PRDI and PERDI.
- Provides divide by 8 recovered clock.
- Provides 8 KHz receive frame pulses.

SONET TRANSMITTER

- Provides a transmit frame pulse input to align the transport frame to a system reference.
- Provides transmit clock as timing reference for transmit outputs.
- Inserts register programmable APS (K1, K2) and synchronization status (S1) bytes.
- Inserts PAIS, PRDI, LAIS and LRDI.
- Scrambles transmit data stream.

ATM PROCESSOR

- Implements the ATM Forum User Network Interface Specification.
- Inserts and extracts ATM cells into and from the SONET SPE.

- Performs cell payload scrambling and descrambling.
- Provides UTOPIA Level 2 and 8-bit 100 MHz UTOPIA Level 3 compliant system interfaces.
- Provides synchronous 4 cell transmit and receive FIFO buffers.

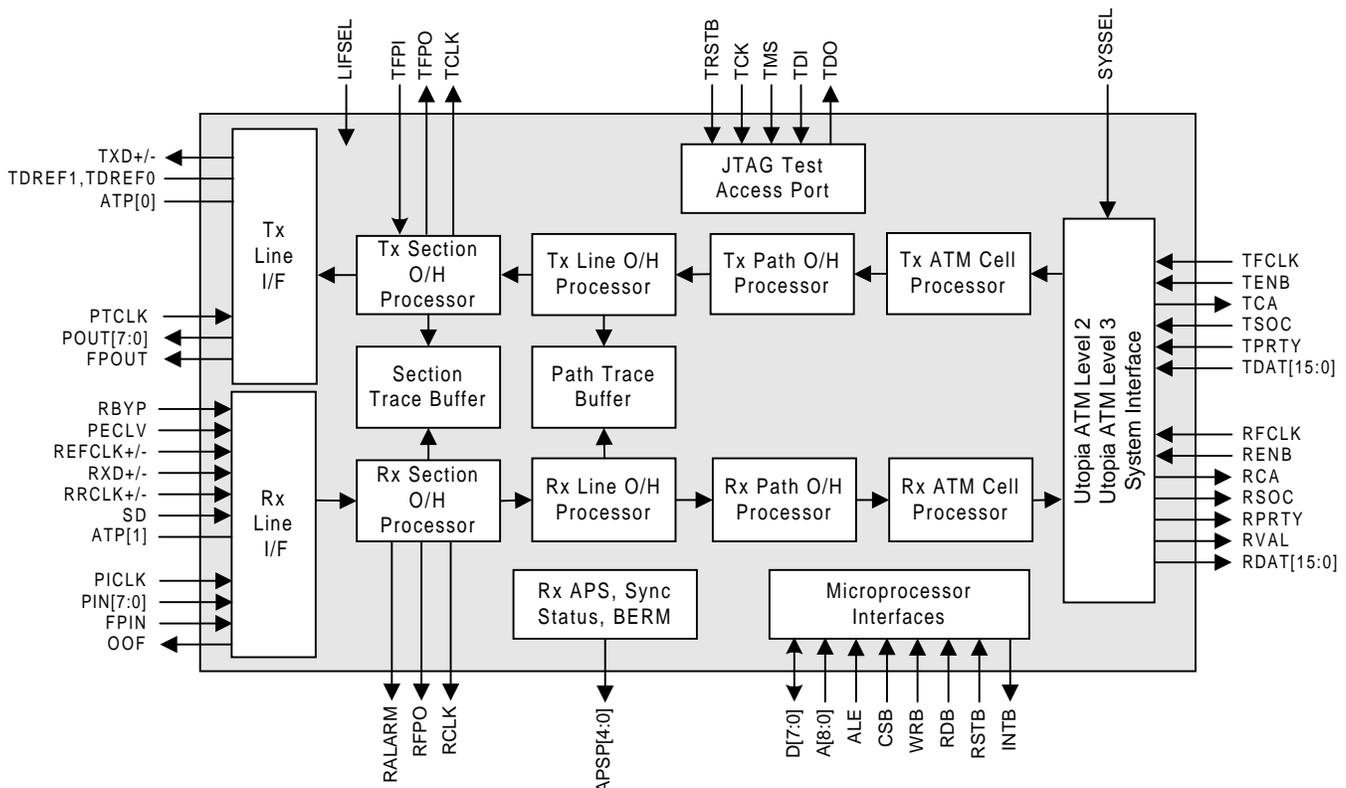
PACKAGING

- Implemented in low power 3.3 Volt CMOS technology.
- Packaged in a 304 pin ball grid array (BGA) package.
- Industrial temperature range (-40°C to +85°C).

APPLICATIONS

- Enterprise and Edge ATM switches.
- ATM switches and hubs.
- Multiprotocol switches.

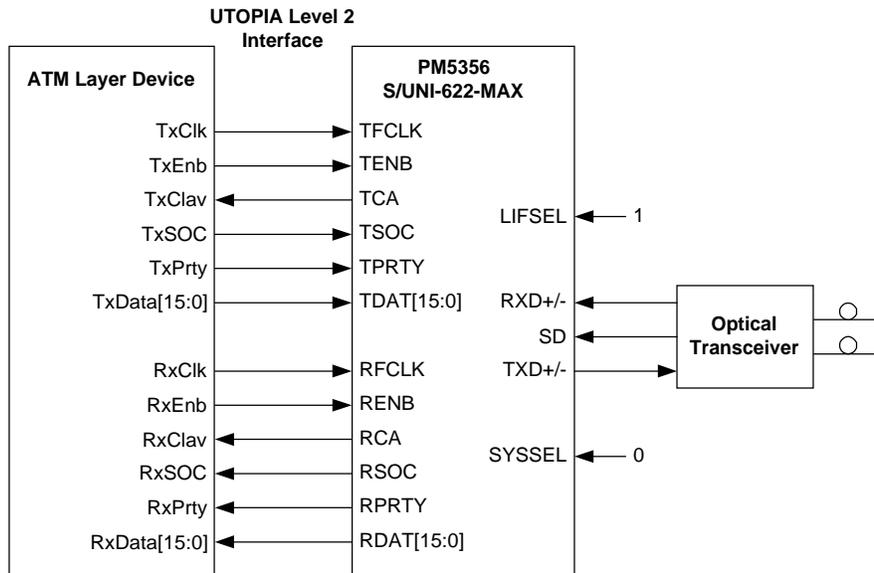
BLOCK DIAGRAM



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TYPICAL APPLICATIONS

UTOPIA LEVEL 2 APPLICATION



UTOPIA LEVEL 3 APPLICATION

