PM5342

SPECTRA-155

SONET/SDH PAYLOAD EXTRACTOR/ALIGNER

DATA SHEET

PROPRIETARY AND CONFIDENTIAL

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1 FEATURES

- Monolithic SONET/SDH PAYLOAD EXTRACTOR/ALIGNER for use in STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) or STS-3c (STM-1/AU4) interface applications, operating at serial interface speeds of up to 155.52 Mbit/s.
- Provides integrated clock recovery and clock synthesis to allow a direct interface to optical modules.
- Provides termination for SONET Section and Line, SDH Regenerator Section and Multiplexer Section transport overhead, and path overhead of one or three STS-1 (STM-0/AU3) paths or a single STS-3c (STM-1/AU4) path.
- Maps one or three STS-1 (STM-0/AU3) payloads or a single STS-3c (STM-1/AU4) payload to system timing reference, accommodating plesiochronous timing offsets between the references through pointer processing.
- Maps a DS3 bit stream into a STS-1 (STM-0/AU3) frame or three DS3 bit streams into a STS-3 (STM-1/AU3) frame.
- Provides clear-channel mapping of three 49.536 Mbit/s or 48.384 Mbit/s arbitrary data streams into an STS-3 (STM-1/AU3) frame or a single arbitrary data stream into an STS-1 (STM-0/AU3) frame. Provides clear-channel mapping of a single 149.76 Mbit/s arbitrary data stream into an STS-3c (STM-1/AU4) frame.
- Provides versatile datamode interface and optional x^43+1 payload scrambling/descrambling to support Packet Over SONET applications.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from a Telecom ADD bus interface to a Telecom DROP bus interface.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power +5 Volt CMOS. Device has PECL and TTL compatible inputs and TTL outputs.

- 256 pin Super BGA package. Supports Industrial Temperature Range (-40°C to 85°C) operation.

1.1 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the STS-1 (STM-0/AU3) or STS-3/3c (STM-1/AU3/AU4) receive stream and inserts the framing bytes (A1, A2) and the STS identification byte (J0) into the transmit stream; descrambles the receive stream and scrambles the transmit stream.

- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream and calculates and inserts B1 and B2 in the transmit stream; accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the Z2 (M1) growth byte based on received B2 errors.

- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.

- Extracts and serializes the order wire channels (E1, E2), the data communication channels (D1-D3, D4-D12) and the section user channel (F1) from the receive stream, and inserts the corresponding signals into the transmit stream.

- Extracts and serializes the automatic protection switch (APS) channel (K1, K2) bytes, filtering and extracting them into internal registers for the receive stream. Inserts the APS channel into the transmit stream.

- Extracts and filters the synchronization status message (Z1/S1) byte into an internal register for the receive stream. Inserts the synchronization status message (Z1/S1) byte into the transmit stream.

- Extracts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the receive stream. Detects an unstable section trace message or mismatch with an expected message, and optionally inserts Line and Path AIS on the system DROP side upon either of these conditions. Inserts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the transmit stream.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI), line alarm indication signal (AIS), and protection switching byte failure alarms on the receive stream. Optionally returns line RDI in the transmit stream.

- Provides a transmit and receive ring control port, allowing alarm and maintenance signal control and status to be passed between mate SPECTRA-155s for ring-based add drop multiplexer and line multiplexer applications.

- Configurable to force Line AIS in the transmit stream.

1.2 SONET Path / SDH High Order Path

- Accepts a multiplex of three STS-1 (STM-0/AU3) streams or a single STS-3c (STM-1/AU4) stream, interprets the STS (AU) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream.

- Constructs a byte serial multiplex of three STS-1 (STM-0/AU3) streams or an STS-3c (STM-1/AU4) stream on the transmit side.

- Detects loss of pointer (LOP), loss of tributary multiframe (LOM), path alarm indication signal (PAIS) and path (auxiliary and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS), path remote defect indication (RDI) and path remote anomaly indication (RAI) in the transmit stream.

- Extracts and serializes the entire path overhead from the three STS-1 (STM-0/AU3) or the single STS-3c (STM-1/AU4) receive streams. Inserts the path overhead bytes in the three STS-1 (STM-0/AU3) or single STS-3c (STM-1/AU4) stream for the transmit stream. The path overhead bytes may be sourced from internal registers or from bit serial path overhead input streams. Path overhead insertion may also be disabled.

- Extracts the received path signal label (C2) byte into an internal register and detects for path signal label unstable and for signal label mismatch with the expected signal label that is downloaded by the microprocessor. Inserts the path signal label (C2) byte from an internal register for the transmit stream.

- Extracts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable path trace message or mismatch with an expected message, and inserts Path RAI upon either of these conditions. Inserts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the transmit stream.

- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.

- Counts received path remote error indications (REIs) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) basis on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block bases independent of the accumulation of BIP-8 errors.

- Supports tandem connection origination applications by sourcing a new tandem path maintenance byte (Z5) reporting the received BIP-8 errors and the data link message and correcting subsequent path BIP-8 bytes (B3) to reflect the change in Z5.

- Supports tandem connection termination applications by accumulating the incoming error count (IEC) and extracting the tandem connection data link carried in the tandem path maintenance byte (Z5).

- Maintains existing pointer value during incoming signal failures in tandem path terminating mode.

- Maintains the existing tributary multiframe sequence on the H4 byte until a new phase alignment has been verified.

- Provides a serial alarm port communication of path REI and path RDI alarms to the transmit stream of a mate SPECTRA-155 in the returning direction.

1.3 System Side Interfaces

- Supports Telecombus interfaces by indicating/accepting the location of the STS identification byte (C1), optionally the path trace byte(s) (J1), optionally the first tributary overhead byte(s) (V1), and all synchronous payload envelope bytes in the byte serial stream.

- Supports serial and nibble "Telecombus" interfaces by indicating/accepting the location of the STS identification byte (C1), the path trace byte(s) (J1), optionally the first tributary overhead byte(s) (V1), and all synchronous payload envelope bytes in the stream.

- For Telecombus interfaces, accommodates phase and frequency differences between the receive/transmit streams and the DROP/ADD busses via pointer adjustments.

- Supports serial, nibble and byte data mode interfaces by sourcing the appropriate clock.

- For data mode interfaces, optionally applies a $X^{43}+1$ scrambler/descrambler to the stream.

- Supports a bit serial DS3 data interface for mapping into and out of STS-1 (STM-0/AU3) or STS-3 (STM-1/AU3) SPEs.

- For the DS3 interface, provides optional insertion of framed DS3 AIS in both the ADD and DROP directions.

2 APPLICATIONS

- SONET/SDH Add Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Line Multiplexers
- SONET/SDH Cross Connects
- SONET/SDH Tandem Path Termination Equipment
- SONET/SDH Test Equipment
- Switches and Hubs
- Routers

3 REFERENCES

- American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1991.
- American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring, T1X1.3/93-005R1, April 1993.
- American National Standard for Telecommunications – Synchronous Optical Network (SONET) – Tandem Connection Maintenance, ANSI T1.105.05-1994.
- Committee T1 Contribution, "Draft of T1.105 - SONET Rates and Formats", T1X1.5/94-033R2-1994.
- Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE Issue 2, December 1995.
- ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January, 1996.
- ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.

- ITU Recommendation G.781, - “Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH)”, January, 1994.

- ITU Recommendation G.783, “Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks”, 28 October, 1996.

- ITU Recommendation O.151, “Error Performance measuring Equipment Operating at the Primary Rate and Above”, October, 1992.

- ITU Study Group XVII - Contribution D2166 - "Tandem Connection / Tandem Connection Bundle Maintenance - Working Solution", June 1992.

4 APPLICATION EXAMPLE

The SPECTRA-155 is used to implement an STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) or STS-3c (STM-1/AU4) line Interface. The SPECTRA-155 may find application in many different types of SONET/SDH network elements including switches, terminal multiplexers, and add-drop multiplexers. In such applications, on the line side the SPECTRA-155 typically interfaces directly to electrical optical modules. On the system side, the SPECTRA-155 can directly interface to an Telecombus, a DS3 signal source or a data source (i.e. HDLC controller).

Figure 1 - STS-3 (STM-1/AU3), STS-3c (STM-1/AU4) Application

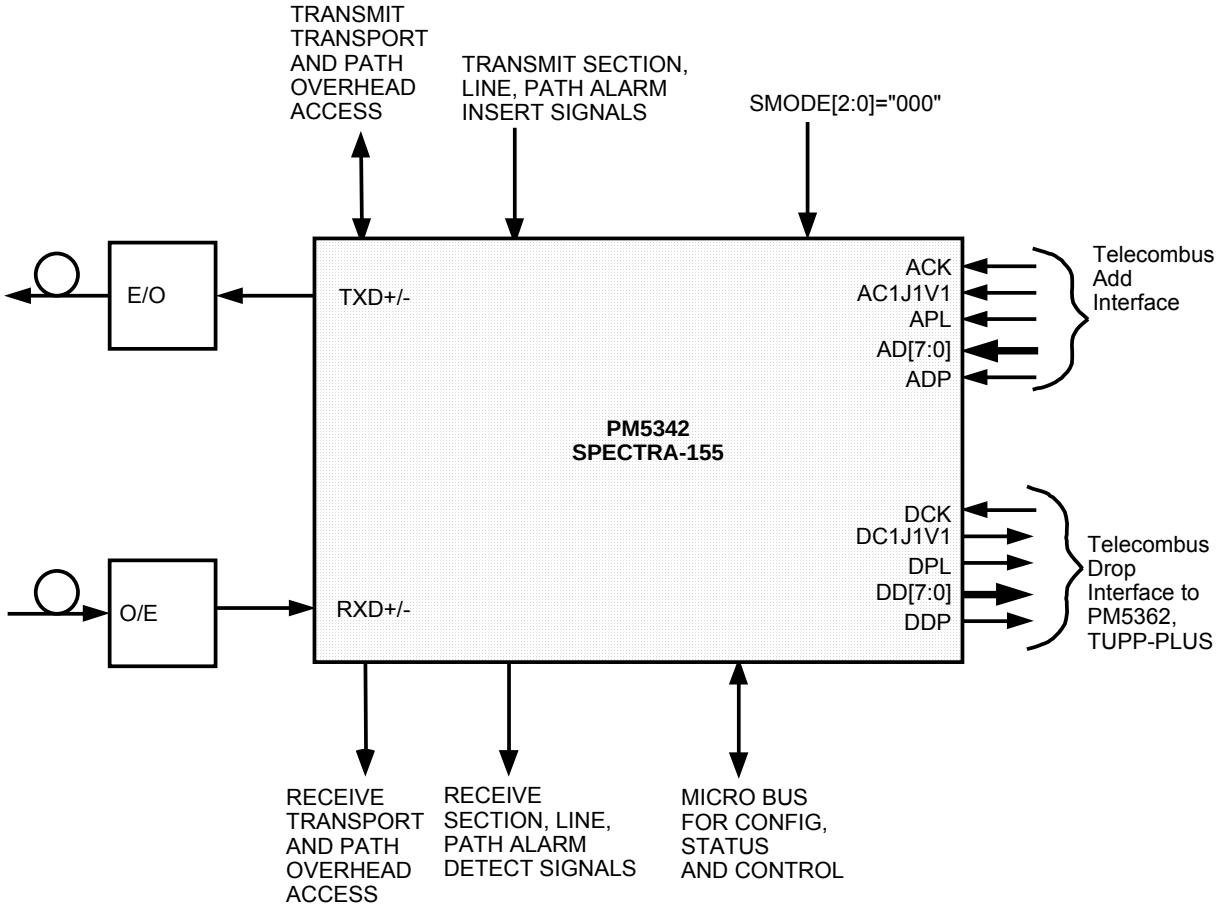


Figure 2 - DS3 Application

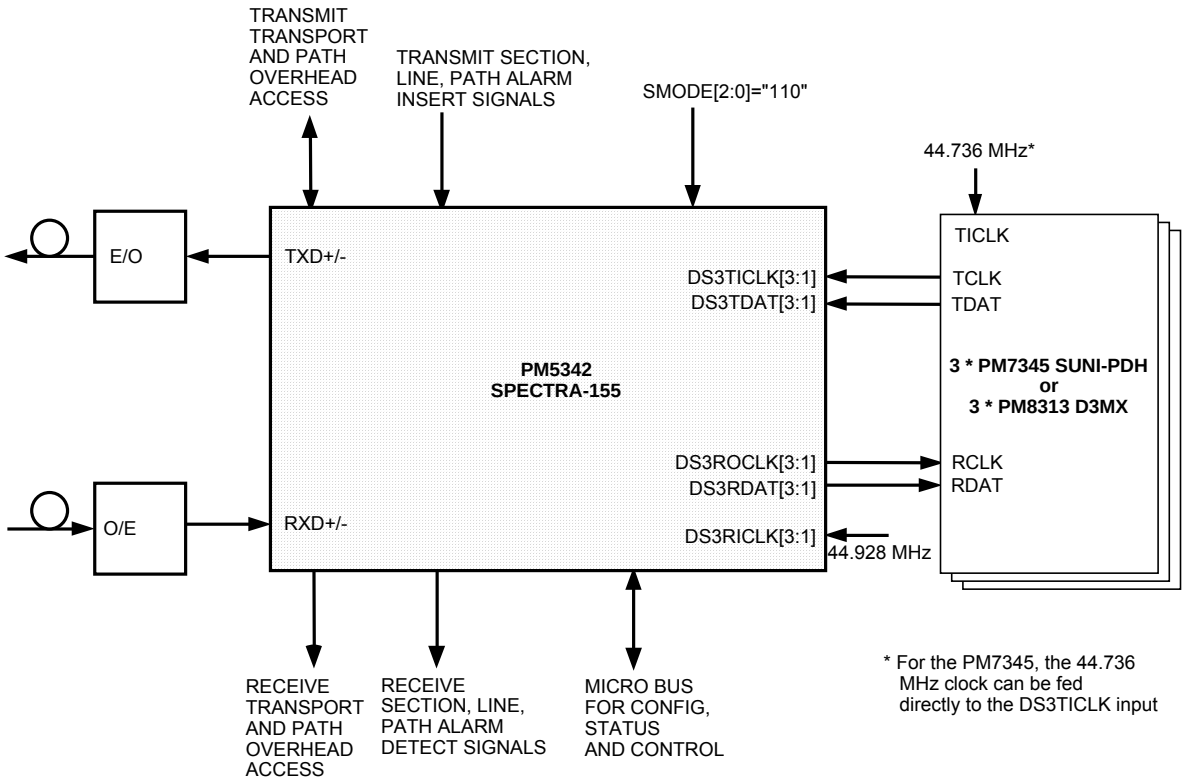


Figure 3 - Serial HDLC Application

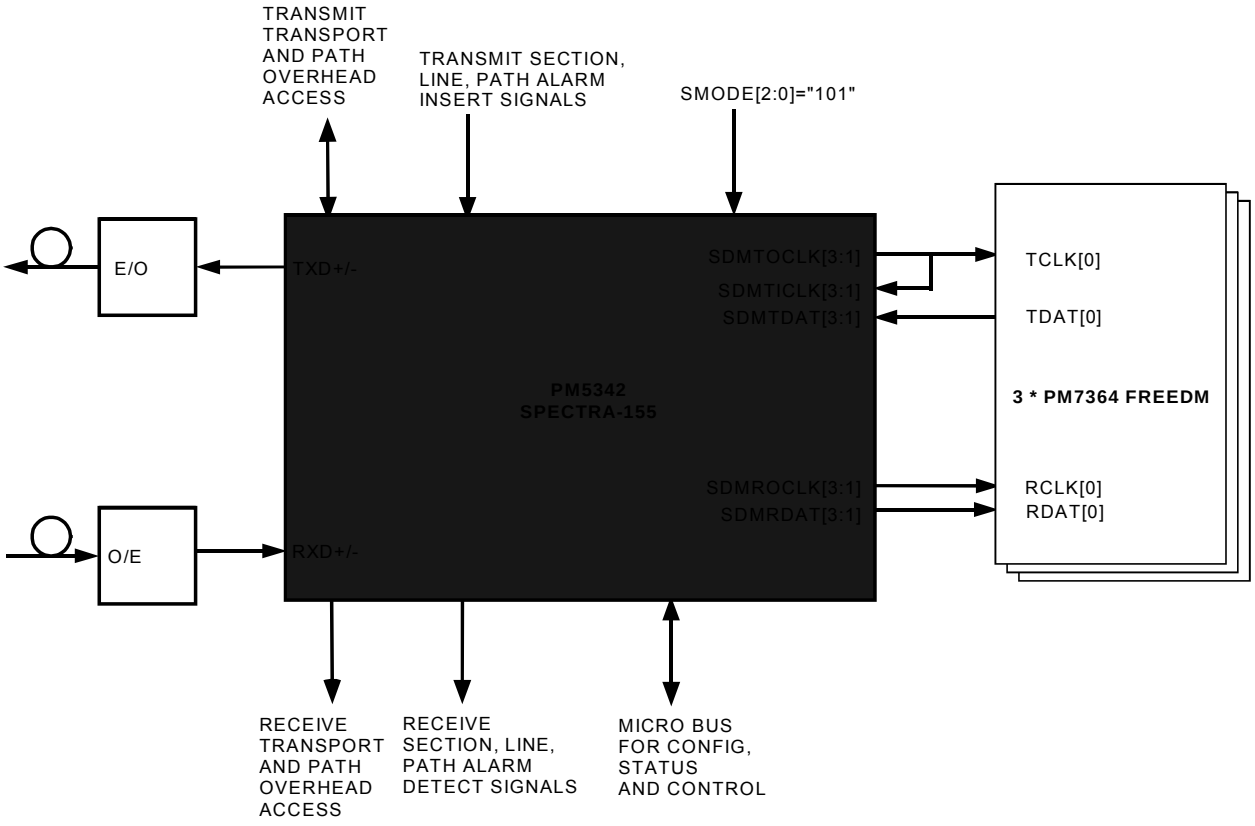


Figure 4 - STS-3/STM-1 Aggregate/Tributary/Cross-Connect Application

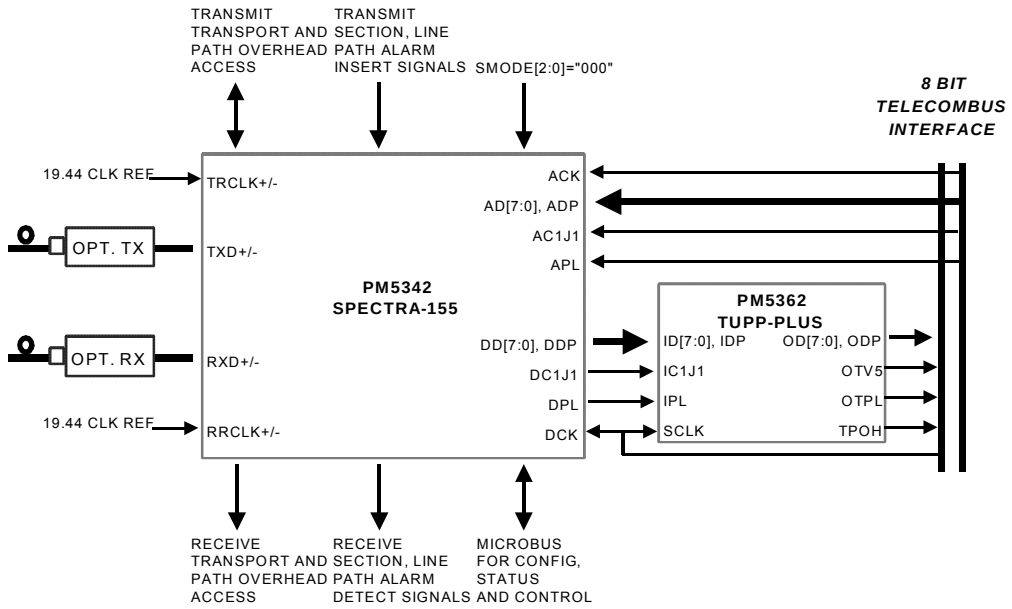


Figure 5 - STS-3/STM-1 Aggregate/Tributary/Cross-Connect Card

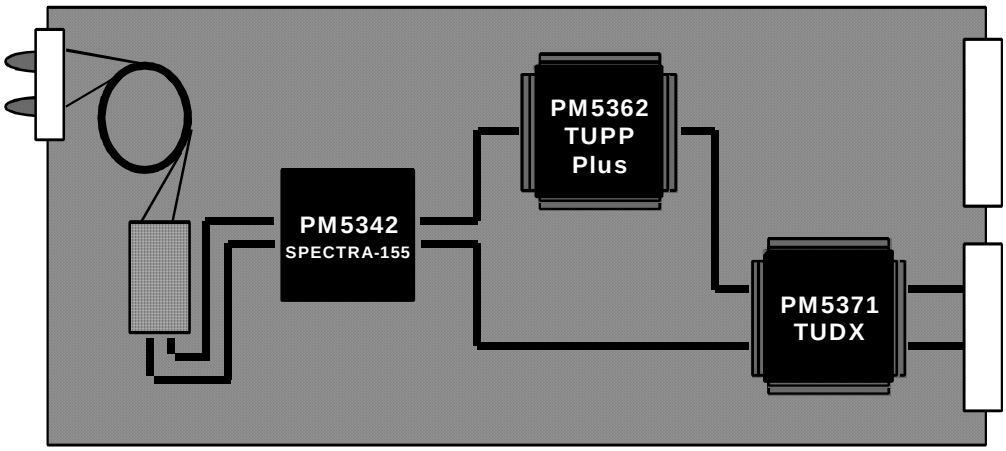


Figure 6 - Packet Over SONET Application

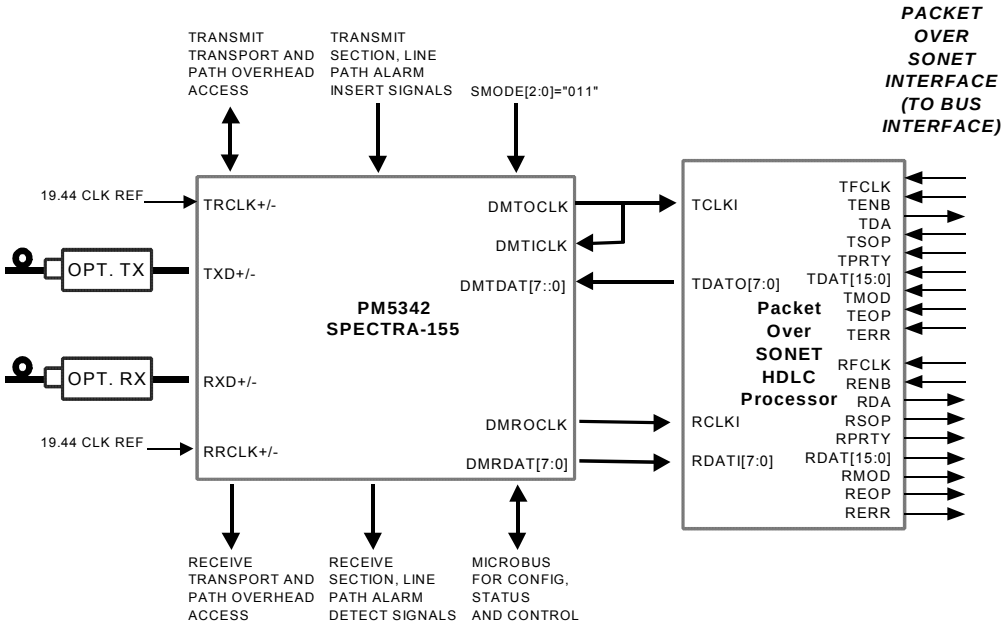
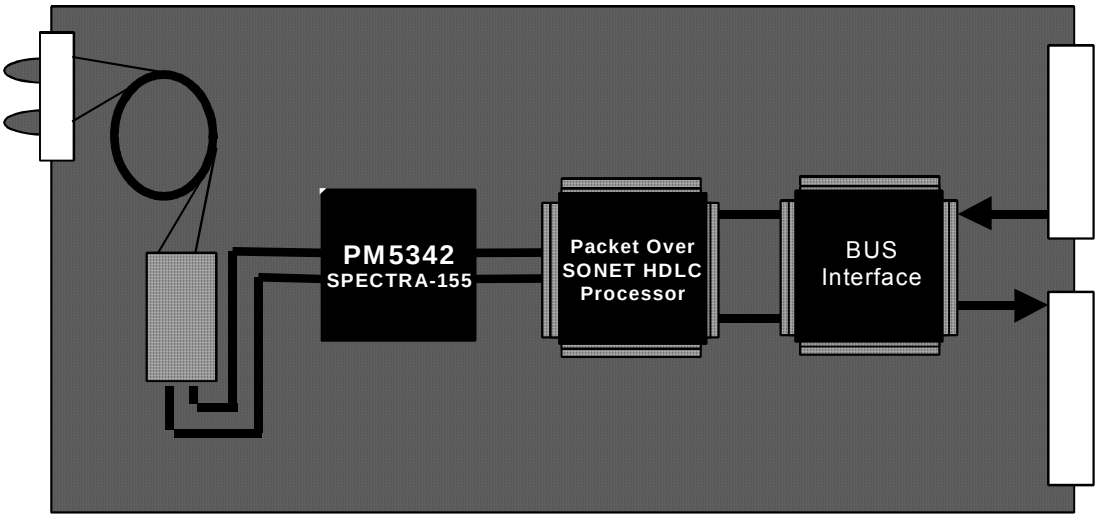


Figure 7 - Packet Over SONET Router WAN Card



5 BLOCK DIAGRAM

Figure 8 - NORMAL MODE

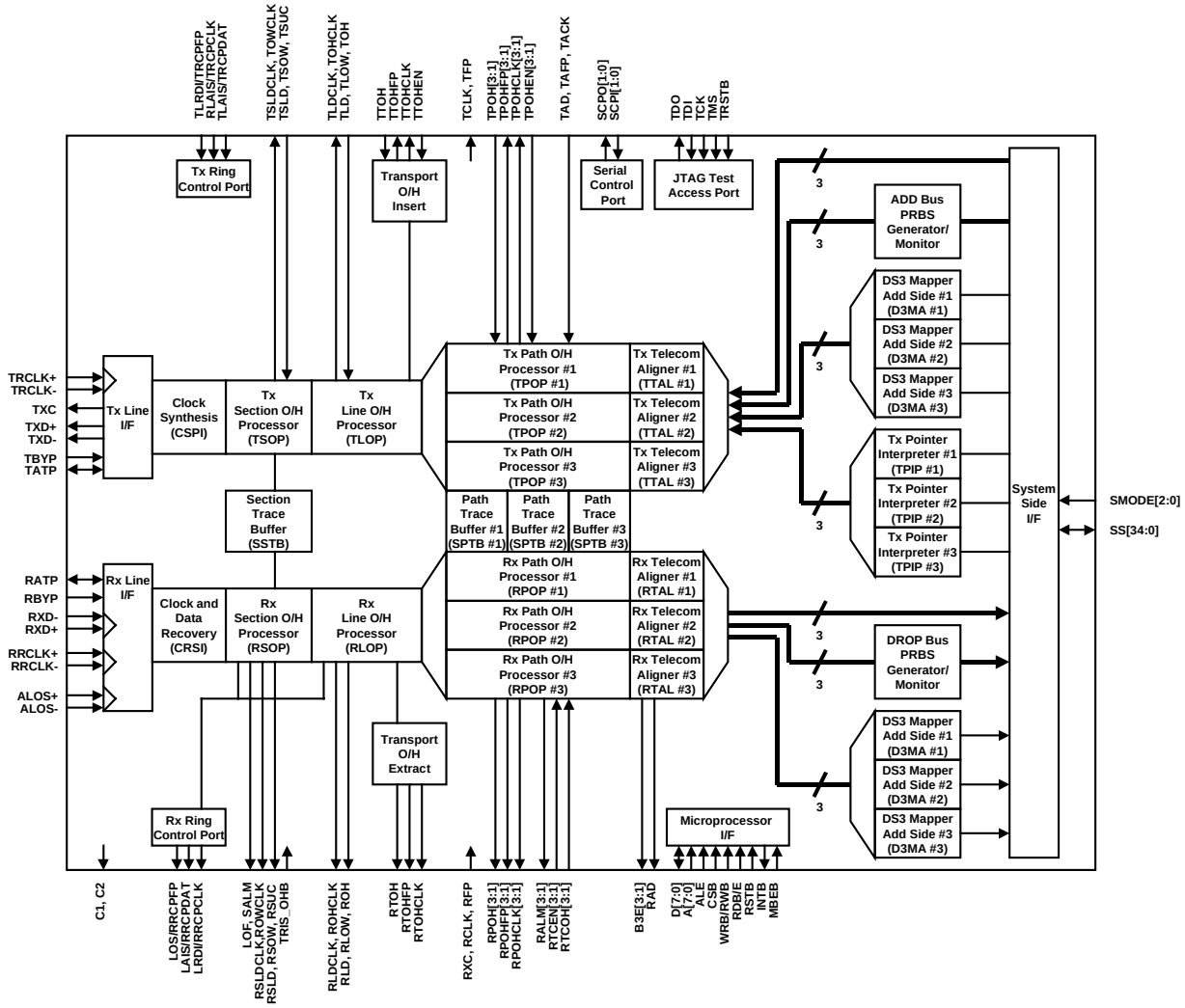


Figure 9 - LOOPBACK MODES

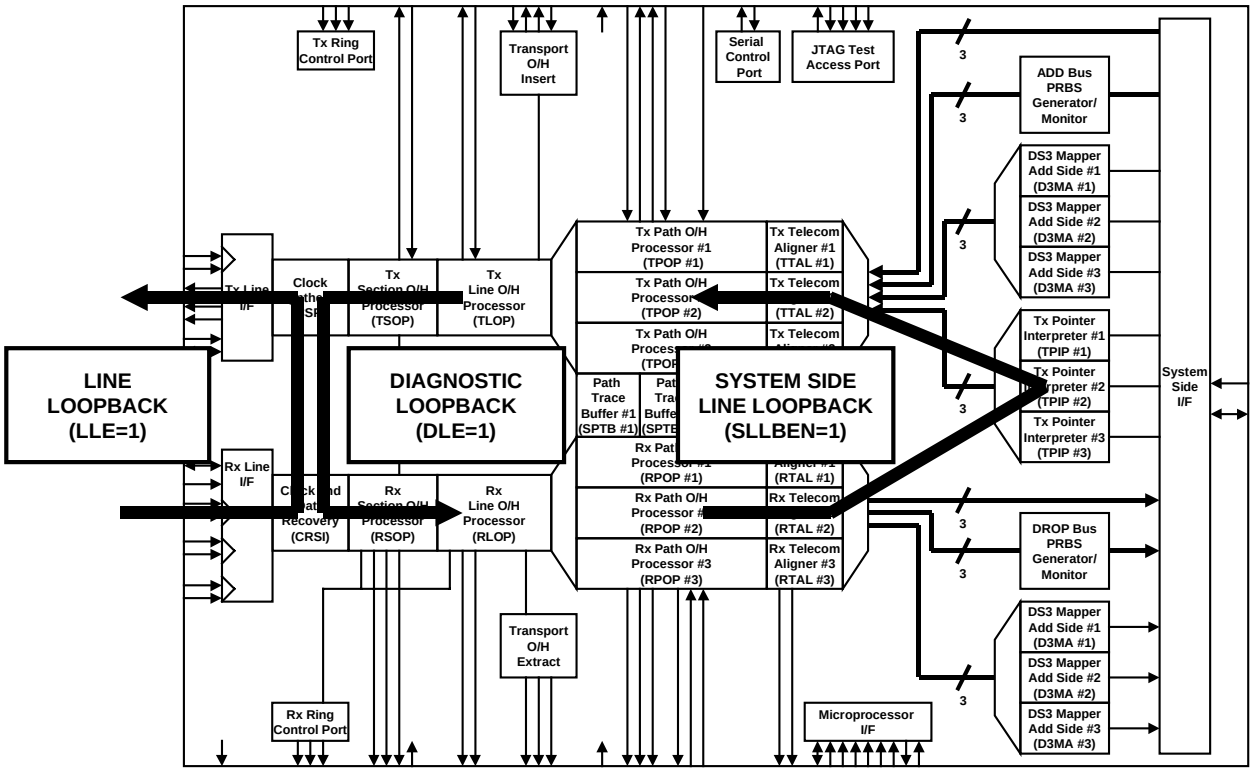


Table 1 - System side modes and SS[34:0] bus mappings.

Signal	Byte Telecombus Mode	Nibble Telecombus Mode	Serial Telecombus Mode	Byte Data Mode	Nibble Data Mode	Serial Data Mode	Serial DS3 Mode
	SMODE=000	SMODE=001	SMODE=010	SMODE=011	SMODE=100	SMODE=101	SMODE=110
SS[0]	DCK	DCK	SDCK[1]	DMROCLK	DMROCLK	Res. Input	DS3RICLK[1]
SS[1]	DFP	DFP	Res. Input	Res. Input	Res. Input	Res. Input	Res. Input
SS[2]	DD[0]	DD[0]	SDCK[2]	DMRDAT[0]	DMRDAT[0]	Res. Input	DS3RICLK[2]
SS[3]	DD[1]	DD[1]	SDCK[3]	DMRDAT[1]	DMRDAT[1]	Res. Input	DS3RICLK[3]
SS[4]	DD[2]	DD[2]	SDC1J1V1[1]	DMRDAT[2]	DMRDAT[2]	SDMROCLK[1]	DS3ROCLK[1]
SS[5]	DD[3]	DD[3]	SDC1J1V1[2]	DMRDAT[3]	DMRDAT[3]	SDMROCLK[2]	DS3ROCLK[2]
SS[6]	DD[4]	Res. Output	SDC1J1V1[3]	DMRDAT[4]	Res. Output	SDMROCLK[3]	DS3ROCLK[3]
SS[7]	DD[5]	Res. Output	SDD[1]	DMRDAT[5]	Res. Output	SDMRDAT[1]	DS3RDAT[1]
SS[8]	DD[6]	Res. Output	SDD[2]	DMRDAT[6]	Res. Output	SDMRDAT[2]	DS3RDAT[2]
SS[9]	DD[7]	Res. Output	SDD[3]	DMRDAT[7]	Res. Output	SDMRDAT[3]	DS3RDAT[3]
SS[10]	DPL	DPL	SDPL[1]	Res. Output	Res. Output	Res. Output	Res. Output
SS[11]	DC1J1V1	DC1J1V1	SDPL[2]	Res. Output	Res. Output	Res. Output	Res. Output
SS[12]	DDP	DDP	SDPL[3]	Res. Output	Res. Output	Res. Output	Res. Output
SS[13]	ACK	ACK	SACK[1]	DMTICLK	DMTICLK	SDMTICLK[1]	DS3TICLK[1]
SS[14]	AD[0]	AD[0]	SACK[2]	DMTDAT[0]	DMTDAT[0]	SDMTICLK[2]	DS3TICLK[2]
SS[15]	AD[1]	AD[1]	SACK[3]	DMTDAT[1]	DMTDAT[1]	SDMTICLK[3]	DS3TICLK[3]
SS[16]	AD[2]	AD[2]	SAC1J1V1[1]	DMTDAT[2]	DMTDAT[2]	Res. Input	DS3RAIS[1]
SS[17]	AD[3]	AD[3]	SAC1J1V1[2]	DMTDAT[3]	DMTDAT[3]	Res. Input	DS3RAIS[2]
SS[18]	AD[4]	Res. Input	SAC1J1V1[3]	DMTDAT[4]	Res. Input	Res. Input	DS3RAIS[3]
SS[19]	AD[5]	Res. Input	SAD[1]	DMTDAT[5]	Res. Input	SDMTDAT[1]	DS3TDAT[1]
SS[20]	AD[6]	Res. Input	SAD[2]	DMTDAT[6]	Res. Input	SDMTDAT[2]	DS3TDAT[2]
SS[21]	AD[7]	Res. Input	SAD[3]	DMTDAT[7]	Res. Input	SDMTDAT[3]	DS3TDAT[3]
SS[22]	APL	APL	SAPL[1]	Res. Input	Res. Input	Res. Input	Res. Input
SS[23]	AC1J1V1	AC1J1V1	SAPL[2]	Res. Input	Res. Input	Res. Input	Res. Input
SS[24]	ADP	ADP	SAPL[3]	Res. Input	Res. Input	Res. Input	Res. Input
SS[25]	GFP	GFP	SDFP[1]	Res. Input	DMTMSN	Res. Input	Res. Input
SS[26]	GMFP	GMFP	SDFP[2]	Res. Input	Res. Input	Res. Input	Res. Input
SS[27]	GD[0]	GD[0]	SDFP[3]	Res. Input	Res. Input	SDMTOCLK[1]	Res. Output
SS[28]	GD[1]	GD[1]	Res. Output	DMTOCLK	DMTOCLK	SDMTOCLK[2]	Res. Output
SS[29]	GPL	GPL	Res. Output	Res. Output	Res. Output	SDMTOCLK[3]	Res. Output
SS[30]	GC1J1V1	GC1J1V1	Res. Output	Res. Output	Res. Output	Res. Output	Res. Output
SS[31]	GDP	GDP	Res. Output	Res. Output	Res. Output	Res. Output	Res. Output
SS[32]	DTPAIS[1]	DTPAIS[1]	SDTPAIS[1]	Res. Input	Res. Input	Res. Input	DS3TAIS[1]
SS[33]	DTPAIS[2]	DTPAIS[2]	SDTPAIS[2]	Res. Input	Res. Input	Res. Input	DS3TAIS[2]
SS[34]	DTPAIS[3]	DTPAIS[3]	SDTPAIS[3]	Res. Input	Res. Input	Res. Input	DS3TAIS[3]

Notes on System Side Modes and SS[34:0] bus mappings:

1. Res. Input pins are Reserved Input pins which must be strapped low. Failure to connect these pins may cause malfunction or damage to the SPECTRA-155.

2. Res. Output pins are Reserved Output pins which must be left unconnected.

6 DESCRIPTION

The PM5342 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER (SPECTRA-155) terminates the transport and path overhead of STS-1 (STM-0/AU3) and STS-3/3c (STM-1/AU3/AU4) streams at 51.84 Mbit/s and 155.52 Mbit/s respectively. The SPECTRA-155 implements significant functions for a SONET/SDH compliant line interface.

The SPECTRA-155 receives SONET/SDH frames via a bit serial interface, recovers clock and data, and terminates the SONET/SDH section (regenerator section), line (multiplexer section), and path. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms. Line remote error indications (M1) are also accumulated. A 16 or 64 byte section trace (J0) message may be buffered and compared against an expected message. In addition, the SPECTRA-155 interprets the received payload pointers (H1, H2), detects path alarm conditions, detects and accumulates path BIPs (B3), monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result and extracts the synchronous payload envelope (virtual container). All transport and path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The extracted SPE (VC) is either placed on a Telecombus DROP bus, serialized into DS3 streams, or serialized into data streams. For Telecombus applications, frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. For the DS3 application, the SPECTRA-155 demaps the three DS3s from the STS-3 (STM-1/AU3) SPE and provides serialized bit streams with derived clocks. For data applications, the SPECTRA-155 either presents the extracted SPE (VC) as a byte/nibble serial stream with an associated clock or presents the STS-3 (STM-1/AU3) SPE into three bit serial streams with associated clocks.

The SPECTRA-155 transmits SONET/SDH frames, via a bit serial interface, and formats section (regenerator section), line (multiplexer section), and path overhead appropriately. The SPECTRA-155 provides transmit path origination for a SONET/SDH STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) or STS-3c (STM-1/AU4) stream. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section and line BIPs (B1, B2) as required to allow performance monitoring at the far end. Line remote error indications (M1)

are optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted. In addition, the SPECTRA-155 generates the transmit payload pointers (H1, H2), creates and inserts the path BIP, optionally inserts a 16 or 64 byte path trace (J1) message, optionally inserts the path status byte (G1). In addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA-155 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPECTRA-155 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors and BIP errors, which are useful for system diagnostics and tester applications.

The inserted SPE (VC) is either sourced from a Telecombus ADD stream, from DS3 serial streams or from data streams. For Telecombus applications, the SPECTRA-155 maps the SPE from a Telecombus ADD bus into the transmit stream. Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the ADD bus are accommodated by pointer adjustments in the transmit stream. For the DS3 application, the SPECTRA-155 maps three DS3s into a STS-3 (STM-1/AU3) SPE. For the data applications, the SPECTRA-155 maps a byte/nibble serial data stream into a STS-1 (STM-0/AU3) SPE or STS-3c (STM-1/AU4) SPE transmit stream or maps three bit serial streams into a STS-3 (STM-1/AU3) SPE transmit stream.

The SPECTRA-155 supports tandem connection termination applications where the tandem connection maintenance byte (Z5) carries the incoming BIP-8 error count (IEC), a tandem data link, and a path AIS code (ISF). The incoming error count is accumulated and the receive data link is serialized for external processing. A new data link can be inserted from a low speed serial input. An incoming signal failure alarm (ISF) is used to convey path AIS in place of all-ones in the pointer (H1, H2).

The transmitter and receiver are independently configurable to allow for asymmetric interfaces. Ring control ports are provide to pass control and status information between mate transceivers. The SPECTRA-155 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

The SPECTRA-155 is implemented in low power, +5 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 256 pin SBGA package.

7 PIN DIAGRAMS

The SPECTRA-155 is available in a 256 pin SBGA package having a body size of 27 mm by 27 mm and a ball pitch of 1.27 mm. There are seven pinout diagrams; each corresponds to a different system side mode (SMODE) configuration.

Figure 10 - Pin diagram: Byte Telecombus Mode (SMODE[2:0]=000)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ DD[0]	SS[5]/ DD[3]	SS[9]/ DD[7]	VSS	SS[15]/ AD[1]	SS[19]/ AD[5]	VSS	VSS	SS[24]/ ADP	SS[28]/ GD[1]	SS[32]/ DTPAIS[1]	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ DFP	SS[4]/ DD[2]	SS[8]/ DD[6]	SS[12]/ DDP	SS[14]/ AD[0]	SS[18]/ AD[4]	SS[21]/ AD[7]	SS[22]/ APL	SS[26]/ GMFP	SS[29]/ GPL	SS[33]/ DTPAIS[2]	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ DD[1]	SS[6]/ DD[4]	SS[10]/ DPL	SS[13]/ ACK	SS[17]/ AD[3]	SS[20]/ AD[6]	SS[23]/ AC1J1V1	SS[27]/ GD[0]	SS[31]/ GDP	SS[34]/ DTPAIS[3]	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ DCK	VDD	SS[7]/ DD[5]	SS[11]/ DC1J1V1	SS[16]/ AD[2]	VDD	SS[25]/ GFP	SS[30]/ GC1J1V1	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD					**BOTTOM VIEW**								A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 11 - Pin diagram: Nibble Telecombus Mode (SMODE[2:0]=001)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ DD[0]	SS[5]/ DD[3]	SS[9]/ Res. Output	VSS	SS[15]/ AD[1]	SS[19]/ Res. Input	VSS	VSS	SS[24]/ ADP	SS[28]/ GD[1]	SS[32]/ DTPAIS[1]	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ DFP	SS[4]/ DD[2]	SS[8]/ Res. Output	SS[12]/ DDP	SS[14]/ AD[0]	SS[18]/ Res. Input	SS[21]/ Res. Input	SS[22]/ APL	SS[26]/ GMFP	SS[29]/ GPL	SS[33]/ DTPAIS[2]	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ DD[1]	SS[6]/ Res. Output	SS[10]/ DPL	SS[13]/ ACK	SS[17]/ AD[3]	SS[20]/ Res. Input	SS[23]/ AC1J1V1	SS[27]/ GD[0]	SS[31]/ GDP	SS[34]/ DTPAIS[3]	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ DCK	VDD	SS[7]/ Res. Output	SS[11]/ DC1J1V1	SS[16]/ AD[2]	VDD	SS[25]/ GFP	SS[30]/ GC1J1V1	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD													A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

BOTTOM VIEW

Figure 12 - Pin diagram: Serial Telecombus Mode (SMODE[2:0]=010)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ SDCK[2]	SS[5]/ SDC1J1V1[2]	SS[9]/ SDD[3]	VSS	SS[15]/ SACK[3]	SS[19]/ SAD[1]	VSS	VSS	SS[24]/ SAPL[3]	SS[28]/ Res. Output	SS[32]/ SDTPAIS[1]	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ Res. Input	SS[4]/ SDC1J1V1[1]	SS[8]/ SDD[2]	SS[12]/ SDPL[3]	SS[14]/ SACK[2]	SS[18]/ SAC1J1V1[3]	SS[21]/ SAD[3]	SS[22]/ SAPL[1]	SS[26]/ SDFP[2]	SS[29]/ Res. Output	SS[33]/ SDTPAIS[2]	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ SDCK[3]	SS[6]/ SDC1J1V1[3]	SS[10]/ SDPL[1]	SS[13]/ SACK[1]	SS[17]/ SAC1J1V1[2]	SS[20]/ SAD[2]	SS[23]/ SAPL[2]	SS[27]/ SDFP[3]	SS[31]/ Res. Output	SS[34]/ SDTPAIS[3]	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ SDCK[1]	VDD	SS[7]/ SDD[1]	SS[11]/ SDPL[2]	SS[16]/ SAC1J1V1[1]	VDD	SS[25]/ SDFP[1]	SS[30]/ Res. Output	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD					BOTTOM VIEW								A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 13 - Pin diagram: Byte Data Mode (SMODE[2:0]=011)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ DMRDAT[0]	SS[5]/ DMRDAT[3]	SS[9]/ DMRDAT[7]	VSS	SS[15]/ DMTDAT[1]	SS[19]/ DMTDAT[5]	VSS	VSS	SS[24]/ Res. Input	SS[28]/ DMTOCLK	SS[32]/ Res. Input	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ Res. Input	SS[4]/ DMRDAT[2]	SS[8]/ DMRDAT[6]	SS[12]/ Res. Output	SS[14]/ DMTDAT[0]	SS[18]/ DMTDAT[4]	SS[21]/ DMTDAT[7]	SS[22]/ Res. Input	SS[26]/ Res. Input	SS[29]/ Res. Output	SS[33]/ Res. Input	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ DMRDAT[1]	SS[6]/ DMRDAT[4]	SS[10]/ Res. Output	SS[13]/ DMTICLK	SS[17]/ DMTDAT[3]	SS[20]/ DMTDAT[6]	SS[23]/ Res. Input	SS[27]/ Res. Input	SS[31]/ Res. Output	SS[34]/ Res. Input	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ DMROCLK	VDD	SS[7]/ DMRDAT[5]	SS[11]/ Res. Output	SS[16]/ DMTDAT[2]	VDD	SS[25]/ Res. Input	SS[30]/ Res. Output	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD					**BOTTOM VIEW**								A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 14 - Pin diagram: Nibble Data Mode (SMODE[2:0]=100)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ DMRDAT[0]	SS[5]/ DMRDAT[3]	SS[9]/ Res. Output	VSS	SS[15]/ DMTDAT[1]	SS[19]/ Res. Input	VSS	VSS	SS[24]/ Res. Input	SS[28]/ DMTOCLK	SS[32]/ Res. Input	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ Res. Input	SS[4]/ DMRDAT[2]	SS[8]/ Res. Output	SS[12]/ Res. Output	SS[14]/ DMTDAT[0]	SS[18]/ Res. Input	SS[21]/ Res. Input	SS[22]/ Res. Input	SS[26]/ Res. Input	SS[29]/ Res. Output	SS[33]/ Res. Input	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ DMRDAT[1]	SS[6]/ Res. Output	SS[10]/ Res. Output	SS[13]/ DMTICLK	SS[17]/ DMTDAT[3]	SS[20]/ Res. Input	SS[23]/ Res. Input	SS[27]/ Res. Input	SS[31]/ Res. Output	SS[34]/ Res. Input	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ DMROCLK	VDD	SS[7]/ Res. Output	SS[11]/ Res. Output	SS[16]/ DMTDAT[2]	VDD	SS[25]/ DMTMSN	SS[30]/ Res. Output	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD					**BOTTOM VIEW**								A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 15 - Pin diagram: Serial Data Mode (SMODE[2:0]=101)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ Res. Input	SS[5]/ SDMROCLK [2]	SS[9]/ SDMRDAT[3]	VSS	SS[15]/ SDMTICLK[3]	SS[19]/ SDMTDAT[1]	VSS	VSS	SS[24]/ Res. Input	SS[28]/ SDMTOCLK [2]	SS[32]/ Res. Input	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ Res. Input	SS[4]/ SDMROCLK [1]	SS[8]/ SDMRDAT[2]	SS[12]/ Res. Output	SS[14]/ SDMTICLK[2]	SS[18]/ Res. Input	SS[21]/ SDMTDAT[3]	SS[22]/ Res. Input	SS[26]/ Res. Input	SS[29]/ SDMTOCLK [3]	SS[33]/ Res. Input	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ Res. Input	SS[6]/ SDMROCLK [3]	SS[10]/ Res. Output	SS[13]/ SDMTICLK[1]	SS[17]/ Res. Input	SS[20]/ SDMTDAT[2]	SS[23]/ Res. Input	SS[27]/ SDMTOCLK [1]	SS[31]/ Res. Output	SS[34]/ Res. Input	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ Res. Input	VDD	SS[7]/ SDMRDAT[1]	SS[11]/ Res. Output	SS[16]/ Res. Input	VDD	SS[25]/ Res. Input	SS[30]/ Res. Output	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD					**BOTTOM VIEW**								A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 16 - Pin diagram: Serial DS3 Mode (SMODE[2:0]=110)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	SMODE[1]	SS[2]/ DS3RICLK[2]	SS[5]/ DS3ROCLK [2]	SS[9]/ DS3RDAT[3]	VSS	SS[15]/ DS3TICLK[3]	SS[19]/ DS3TDAT[1]	VSS	VSS	SS[24]/ Res. Input	SS[28]/ Res. Output	SS[32]/ DS3TAIS[1]	SCPO[0]	TPOH[3]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	SMODE[0]	SS[1]/ Res. Input	SS[4]/ DS3ROCLK [1]	SS[8]/ DS3RDAT[2]	SS[12]/ Res. Output	SS[14]/ DS3TICLK[2]	SS[18]/ DS3RAIS[3]	SS[21]/ DS3TDAT[3]	SS[22]/ Res. Input	SS[26]/ Res. Input	SS[29]/ Res. Output	SS[33]/ DS3TAIS[2]	SCPO[1]	TPOHCLK[3]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	NC3	SMODE[2]	SS[3]/ DS3RICLK[3]	SS[6]/ DS3ROCLK [3]	SS[10]/ Res. Output	SS[13]/ DS3TICLK[1]	SS[17]/ DS3RAIS[2]	SS[20]/ DS3TDAT[2]	SS[23]/ Res. Input	SS[27]/ Res. Output	SS[31]/ Res. Output	SS[34]/ DS3TAIS[3]	TPOHEN[3]	TPOHEN[2]	VDD	VDD	VSS	C
D	TMS	TCK	TDO	VDD	TRIS_OHB	SS[0]/ DS3RICLK[1]	VDD	SS[7]/ DS3RDAT[1]	SS[11]/ Res. Output	SS[16]/ DS3RAIS[1]	VDD	SS[25]/ Res. Input	SS[30]/ Res. Output	VDD	TPOHFP[3]	TPOHFP[2]	VDD	TPOH[2]	TPOHFP[1]	TPOHEN[1]	D
E	B3E[3]	RSTB	TRSTB	TDI													TPOHCLK[2]	TPOH[1]	TPOHCLK[1]	SCPI[1]	E
F	B3E[2]	RALM[2]	RALM[3]	RAD													SCPI[0]	ALE	CSB	WRB/RWB	F
G	RTCOH[3]	RTCEN[3]	RALM[1]	VDD													VDD	RDB/E	MBEB	A[0]	G
H	RTCOH[1]	RTCOH[2]	RTCEN[2]	B3E[1]													INTB	A[1]	A[3]	VSS	H
J	VSS	RPOH[3]	RPOHCLK[3]	RTCEN[1]													A[2]	A[4]	A[5]	A[6]	J
K	VSS	RPOHFP[3]	RPOHCLK[2]	VDD						**BOTTOM VIEW**							A[7]	A[8]	A[9]	D[0]	K
L	RXC	RPOH[2]	RPOHFP[2]	RCLK													VDD	D[1]	D[2]	VSS	L
M	RFP	RPOHCLK[1]	RPOH[1]	LOF													D[6]	D[4]	D[3]	VSS	M
N	VSS	RPOHFP[1]	SALM	RLDCLK													TACK	TFP	D[7]	D[5]	N
P	LOS	ROHCLK	ROH	VDD													VDD	TCLK	TTOHFP	TAFP	P
R	RLD	RLOW	RSUC	RSLD													TLD	TSLDCLK	TSLD	TAD	R
T	RSLDCLK	ROWCLK	RSOW	RTOHFP													TSOW	TTOHCLK	TOH	TOHCLK	T
U	LAIS	LRDI	RTOHCLK	VDD	RBYP	RAVD2	NC_A	RAVS4	ALOS-	NC_B	TAVD3	TAVD1	RLAIS	VDD	TLRDI	TTOHEN	VDD	TLOW	TSUC	TLDCLK	U
V	VSS	VDD	VDD	RTOH	RAVS2	RAVS1	QAVS1	RAVD4	ALOS+	RAVD3	QAVD3	TAVS3	TAVD2	NC5	NC1	NC2	TOWCLK	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TATP	C1	RAVD1	RRCLK-	RAVS3	RXD+	RXD-	QAVS2	TRCLK+	TAVS1	NC4	TBYP	TXD+	TTOH	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	RATP	C2	QAVD1	RRCLK+	NC_F	NC_C	NC_D	QAVD2	TRCLK-	NC_E	TAVS2	TLAIS	TXD-	TXC	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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Table 2 - Line Side Interface Signals (20)

Pin Name	Pin Type	PIN No.	Function
RBYP	Input	U16	The receive bypass (RBYP) input selects whether to bypass the CRU. If RBYP is high, the internal CRU is bypassed and RRCLK+/- should contain the receive line clock used to sample RXD+/-. If RBYP is low, the internal CRU is used and RRCLK+/- should contain the reference clock.
RXD+ RXD-	PECL Input	W12 W11	The receive differential data inputs (RXD+, RXD-) contain the 155.52 Mbit/s receive STS-3/3c (STM-1/AU3/AU4) stream or the 51.84 Mbit/s receive STS-1 (STM-0/AU3) stream. RXD+/- are sampled on the rising edge of RRCLK+/- when clock recovery is disabled (the falling edge may be used by reversing RRCLK+/-). Otherwise the receive clocks are recovered from the RXD+/- bit stream. RXD+/- is expected to be NRZ encoded. Clock recovery bypass is selectable using the RBYP input signal.

Pin Name	Pin Type	PIN No.	Function
RRCLK+ RRCLK-	PECL/ Schmitt TTL Input	Y14 W14	The receive differential reference clock inputs (RRCLK+, RRCLK-) contain a jitter-free 19.44 MHz or 6.48 MHz reference clock when clock recovery is enabled. When clock recovery is bypassed, RRCLK+/- is nominally a 155.52 MHz or 51.84 MHz, 50% duty cycle clock and provide timing for the SPECTRA-155 receive functions. In this case, RXD+/- is sampled on the rising edge of RRCLK+/-. Clock recovery bypass is selectable using the RBYP input signal. In addition, RRCLK+/- can also be used to provide the clock synthesis unit's clock reference using the TREFSRC bit in the SPECTRA-155 Clock Synthesis Control and Status register. The 6.48 MHz reference clock supports only STS-1 (STM-0/AU3) operation when clock recovery is enabled. The 19.44 MHz reference clock supports both STS-1 (STM-0/AU3) and STS-3/3c (STM-1/AU3/AU4) operation when clock recovery is enabled. For TTL operation, please refer to the Operations section.
ALOS+ ALOS-	PECL/ Schmitt TTL Input	V12 U12	The analog loss of signal (ALOS+/-) differential inputs are used to indicate a loss of receive signal power. When ALOS+/- is asserted, the data on the receive data (RXD+/-) pins is forced to all zeros and the phase locked loop switches to the reference clock (RRCLK+/- or TRCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled. Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Pin Type	PIN No.	Function
RCLK	Output	L17	The receive clock (RCLK) output provides a timing reference for the SPECTRA-155 receive line interface outputs. For STS-3/3c (STM-1/AU3/AU4) operation, RCLK is nominally 19.44 MHz. For STS-1 (STM-0/AU3) RCLK is nominally 6.48. RCLK is a divide by eight of the recovered clock or the RRCLK+/- inputs as determined using the RBYP input signal. When not used, RCLK can be held low using the RCLKEN bit in the SPECTRA-155 Clock Control register.
RXC	Output	L20	The receive clock (RXC) output provides a 51.84 MHz timing reference. RXC is a 51.84 MHz, nominally 50% duty cycle clock. For STS-3/3c (STM-1/AU3/AU4) mode, RXC is a divide by three of the recovered clock or the RRCLK+/- inputs as determined using the RBYP input signal. For STS-1 (STM-0/AU3) mode, RXC is the recovered clock or the RRCLK+/- inputs as determined using the RBYP input signal. When not used, RXC can be held low using the RXCEN bit in the SPECTRA-155 Clock Control register.
RFP	Tristate Output	M20	The receive frame pulse (RFP) output is an 8 KHz signal derived from the receive line clock. RFP is pulsed high for one RCLK cycle every 2430 RCLK cycles for STS-3c (STM-1/AU4) or every 810 RCLK cycles for STS-1 (STM-0/AU3). A single discontinuity in RFP position occurs if a change of frame alignment occurs. RFP can be tristated using the TRIS_OHB input and the ROH_TS bit in the SPECTRA-155 Receive Overhead Output Control register. On reset, RFP will be tristate if TRIS_OHB is low.

Pin Name	Pin Type	PIN No.	Function
TBYP	Input	W6	The transmit bypass (TBYP) input selects whether to bypass the CSU. If TBYP is high, the internal CSU is bypassed and TRCLK+/- should contain the transmit line clock used to output data on TXD+/-. If TBYP is low, the internal CSU is used and TRCLK+/- should contain the reference clock.
TRCLK+ TRCLK-	PECL/ Schmitt TTL Input	W9 Y9	The transmit differential reference clock inputs (TRCLK+, TRCLK-) are a jitter-free 19.44 MHz or 6.48 MHz reference clock when clock synthesis is enabled. When clock synthesis is bypassed, TRCLK+/- is nominally a 155.52 MHz or 51.84 MHz, 50% duty cycle clock. This clock provides timing for the SPECTRA-155 transmit functions. TRCLK+/- may be left unconnected when SPECTRA-155 loop timing is enabled using the SPECTRA-155 Configuration Register. Clock synthesis bypass is selectable using the TBYP input signal. In addition, TRCLK+/- can also be used to provide the clock recovery unit's clock reference using the RREFSRC bit in the SPECTRA-155 Clock Recovery Control and Status register. The 6.48 MHz reference clock supports only STS-1 (STM-0/AU3) operation when clock synthesis is enabled. The 19.44 MHz reference clock supports both STS-1 (STM-0/AU3) and STS-3/3c (STM-1/AU3/AU4) operation when clock synthesis is enabled. For TTL operation, please refer to the Operations section.
TXC	Output	Y4	The transmit clock (TXC) output is available when STS-1 (STM-0/AU3) mode of operation is selected using the SPECTRA-155 Configuration register. In STS-1 mode, TXD+/- are updated on the falling edge of TXC. When not used, TXC can be held low using the TXCEN bit in the SPECTRA-155 Clock Control register.

Pin Name	Pin Type	PIN No.	Function
TXD+ TXD-	Output	W5 Y5	The transmit differential data outputs (TXD+, TXD-) contain the 155.52 Mbit/s transmit STS-3/3c (STM-1/AU3/AU4) stream or the 51.84 Mbit/s transmit STS-1 (STM-0/AU3) stream. When the STS-1 (STM-0/AU3) stream is selected, TXD+/- are updated on the falling edge of TXC. TXD+/- is NRZ encoded.
TCLK	Output	P3	The transmit byte clock (TCLK) output provides a timing reference for the SPECTRA-155 transmit line interface outputs. For STS-3/3c (STM-1/AU3/AU4) operation, TCLK is nominally 19.44 MHz. For STS-1 (STM-0/AU3) TCLK is nominally 6.48. TCLK is a divide by eight of the synthesized clock or the TRCLK+/- inputs as determined using the TBYP input signal. When not used, TCLK can be held low using the TCLKEN bit in the SPECTRA-155 Clock Control register.
TFP	Tristate Output	N3	The active high transmit framing position (TFP) signal is an 8 KHz timing marker for the transmitter. TFP goes high for a single TCLK period once every 2430 in STS-3/3c (STM-1/AU3/AU4) mode or 810 in STS-1 (STM-0/AU3) mode TCLK cycles. TFP is updated on the rising edge of TCLK. TFP can be tristate using the TRIS_OHB input and the TOH_TS bit in the SPECTRA-155 Transmit Overhead Input Control register. On reset, TFP will be tristate if TRIS_OHB is low.
C1 C2	Analog	W16 Y16	The analog C1 and C2 pins are provided for connecting an external loop-filter capacitor. A 1 nF ceramic capacitor is required.

Table 3 - Section and Line Status/Overhead Interface Signals (36)

Pin Name	Pin Type	PIN No.	Function
TRIS_OHB	Input	D16	The active low tristate overhead (TRIS_OHB) input enables software registers to control the tristating of the overhead output signals, RSLD, RSLDCLK, TSLDCLK, ROHCLK, ROH, RFP, TOHCLK and TFP. When TRIS_OHB is low, tristating of outputs RSLD, RSLDCLK, ROHCLK, ROH and RFP are controlled using the SPECTRA-155 Receive Overhead Output Control register while outputs TSLDCLK, TOHCLK and TFP are controlled using the SPECTRA-155 Transmit Overhead Input Control register. When TRIS_OHB is high, the above outputs are always driven. TRIS_OHB has an integral pull up resistor.
SALM	Output	N18	The section alarm (SALM) output is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (LAIS) or line remote defect indication (LRDI) alarm is detected. Each alarm indication can be independently enabled using bits in the SPECTRA-155 Section Alarm Output Control register. SALM is set low when none of the enabled alarms are active. The out of frame (OOF) alarm is indicated while the SPECTRA-155 is unable to find a valid framing pattern (A1, A2) in the incoming stream. The SALM is configured to indicate only the OOF condition as a default after a device reset to optionally provide a dedicated output pin for this alarm. Please refer to the (optionally) dedicated output pins for LOS, LOF, LAIS and LRDI for the description of these alarms. SALM is updated on the rising edge of RCLK.

Pin Name	Pin Type	PIN No.	Function
LOS/	Output	P20	Loss of signal (LOS) is active when the ring control port is disabled. Loss of signal (LOS) is set high when a violating period (20 ± 2.5 µs) of consecutive all zeros patterns is detected in the incoming stream. LOS is set low when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all zeros patterns is observed. LOS is updated on the rising edge of RCLK.
RRCPFP			The receive ring control port frame position (RRCPFP) signal identifies bit positions in the receive ring control port data (RRCPDAT) when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the SPECTRA-155 Section/Line Control/Enable Register). RRCPFP is high during the filtered K1, K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, and the send line AIS and send line RDI bit positions in the RRCPDAT stream. RRCPFP is normally connected to the TRCPFP input of a mate SPECTRA-155 in ring-based add-drop multiplexer applications. RRCPFP is updated on the falling edge of RRCPCLK.
LOF	Output	M17	The loss of frame (LOF) signal is set high when an out of frame state persists for 3 ms. LOF is set low when an in frame state persists for 3 ms. LOF is updated on the rising edge of RCLK.

Pin Name	Pin Type	PIN No.	Function
LRDI/	Output	U19	The line remote defect indication (LRDI) signal is active when the ring control port is disabled. LRDI is set high when line RDI is detected in the incoming stream. LRDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LRDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. This alarm indication is also available through register access. LRDI is updated on the rising edge of RCLK.
RRCPCLK			The receive ring control port clock (RRCPCLK) signal provides timing for the receive ring control port when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the SPECTRA-155 Section/Line Control/Enable Register). RRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock and is normally connected to the TRCPCLK input of a mate SPECTRA-155 in ring-based add-drop multiplexer applications. RRCPFP and RRCPDAT are updated on the falling edge of RRCPCLK.

Pin Name	Pin Type	PIN No.	Function
LAIS/	Output	U20	The line alarm indication (LAIS) signal is active when the ring control port is disabled. LAIS is set high when line AIS is detected in the incoming stream. LAIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. This alarm indication is also available through register access. LAIS is updated on the rising edge of RCLK.
RRCPDAT			The receive ring control port data (RRCPDAT) signal contains the receive ring control port data stream when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the SPECTRA-155 Section/Line Control/Enable Register). The receive ring control port data consists of the filtered K1, K2 byte values, the change of APS value bit position, the protection switch byte failure status bit position, the send line AIS and send line RDI bit positions, and the line REI bit positions. RRCPDAT is normally connected to the TRCPDAT input of a mate SPECTRA-155 in ring-based add-drop multiplexer applications. RRCPDAT is updated on the falling edge of RRCPCLK.

Pin Name	Pin Type	PIN No.	Function
RLAIS/	Input	U8	The receive line AIS insertion (RLAIS) signal controls the insertion of line AIS in the receive outgoing stream, when the ring control port is disabled. When RLAIS is high, line AIS is inserted in the outgoing stream. Line AIS is also optionally inserted automatically upon detection of loss of signal, loss of frame, section trace alarms or line AIS in the incoming stream. RLAIS is sampled on the rising edge of RCLK.
TRCPCLK			The transmit ring control port clock (TRCPCLK) signal provides timing for the transmit ring control port when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the SPECTRA-155 Section/Line Control/Enable Register). TRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock and is normally connected to the RRCPCLK output of a mate SPECTRA-155 in ring-based add-drop multiplexer applications. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK.
RSLDCLK	Tristate Output	T20	The receive section/line DCC clock (RSLDCLK) can either be used to clock out the section or line DCC as selected using the RDLSEL bit in the SPECTRA-155 Receive Overhead Output Control register. When section DCC is selected, RSLDCLK is a 192 KHz clock used to update the RSLD output. RSLDCLK is generated by gapping a 216 KHz clock. When line DCC is selected, RSLDCLK is a 576 KHz clock used to update the RSLD output. RSLDCLK is generated by gapping a 2.16 MHz clock. RSLDCLK can be tristate using the TRIS_OHB input and the RSLD_TS bit in the SPECTRA-155 Receive Overhead Output Control register. On reset, RSLDCLK will be tristate if TRIS_OHB is low.

Pin Name	Pin Type	PIN No.	Function
RSLD	Tristate Output	R17	The receive section/line DCC (RSLD) signal contains the section data communications channel (D1-D3) or the line data communications channel (D4-D12) as selected using the RDLSEL bit in the SPECTRA-155 Receive Overhead Output Control register. RSLD can be tristate using the TRIS_OHB input and the RSLD_TS bit in the SPECTRA-155 Receive Overhead Output Control register. On reset, RSLD will be tristate if TRIS_OHB is low. RSLD is updated on the falling edge of RSLDCLK.
ROWCLK	Output	T19	The receive order wire clock (ROWCLK) is a 64 KHz clock used to update the RSOW, RSUC, and RLOW outputs. If selected using the R64SEL bit in the SPECTRA-155 Receive Overhead Output Control register, ROWCLK is generated by gapping a 72 KHz clock; otherwise, ROWCLK is not gapped.
RSOW	Output	T18	The receive section order wire (RSOW) signal contains the section order wire channel (E1) extracted from the incoming stream. RSOW is updated on the falling edge of ROWCLK.
RSUC	Output	R18	The receive section user channel (RSUC) signal contains the section user channel (F1) extracted from the incoming stream. RSUC is updated on the falling edge of ROWCLK.
RLOW	Output	R19	The receive line order wire (RLOW) signal contains the line order wire channel (E2) extracted from the incoming stream. RLOW is updated on the falling edge of ROWCLK.
RLDCLK	Output	N17	The receive line DCC clock (RLDCLK) is a 576 KHz clock used to update the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock.

Pin Name	Pin Type	PIN No.	Function
RLD	Output	R20	The receive line DCC (RLD) signal contains the line data communications channel (D4 - D12) extracted from the incoming stream. RLD is updated on the falling edge of RLDCLK.
ROHCLK	Tristate Output	P19	The receive overhead clock (ROHCLK) can be selected to clock out either the section orderwire (E1), the line orderwire (E2), the line user channel (F1) or the automatic protection switch channel (K1, K2). Selection of the receive overhead clock is made using the ROHSEL bits in the SPECTRA-155 Receive Overhead Output Control register. When either orderwire or user channel clocks are selected, ROHCLK is a 64 KHz clock used to update the ROH output. If selected using the R64SEL bit in the SPECTRA-155 Receive Overhead Output Control register, ROHCLK is generated by gapping a 72 KHz clock; otherwise, ROHCLK is not gapped. When the receive automatic protection switch channel clock is selected, ROHCLK is a 128 KHz clock used to update the ROH output. ROHCLK is generated by gapping a 144 KHz clock. ROHCLK can be tristate using the TRIS_OHB input and the ROH_TS bit in the SPECTRA-155 Receive Overhead Output Control register. On reset, ROHCLK will be tristate if TRIS_OHB is low.

Pin Name	Pin Type	PIN No.	Function
ROH	Tristate Output	P18	The receive overhead (ROH) output can be selected to carry either the section orderwire (E1), the line orderwire (E2), the line user channel (F1) or the automatic protection switch channel (K1, K2). Selection is made using the ROHSEL bits in the SPECTRA-155 Receive Overhead Output Control register. ROH can be tristate using the TRIS_OHB input and the ROH_TS bit in the SPECTRA-155 Receive Overhead Output Control register. On reset, ROH will be tristate if TRIS_OHB is low. ROH is updated on the falling edge of ROHCLK.
RTOHCLK	Output	U18	The receive transport overhead clock (RTOHCLK) is nominally a 5.184 MHz or 1.728 MHz clock that provides timing to process the extracted receive transport overhead, RTOH. RTOHCLK is a gapped 6.48 MHz clock when accessing the transport overhead of an STS-3/3c (STM-1/AU3/AU4) stream. RTOHCLK is a gapped 2.16 MHz clock when accessing the transport overhead of an STS-1 (STM-0/AU3) stream.
RTOH	Output	V17	The receive transport overhead (RTOH) signal contains the receive transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) extracted from the incoming stream. RTOH is updated on the falling edge of RTOHCLK.
RTOHFP	Output	T17	The receive transport overhead frame position (RTOHFP) signal is used to locate the individual receive transport overhead bits in the receive transport overhead, RTOH. RTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH stream. RTOHFP is updated on the falling edge of RTOHCLK.

Pin Name	Pin Type	PIN No.	Function
TLRDI/	Input	U6	The active high transmit line remote defect indication (TLRDI) signal controls the insertion of a remote defect indication in the outgoing stream when the ring control port is disabled. When TLRDI is set high, bits 6, 7, and 8 of the K2 byte are set to the pattern 110. Line RDI may also be inserted using the LRDI bit in the TLOP Control Register, or upon detection of loss of signal, loss of frame, or line AIS in the receive stream, using the bits in the SPECTRA-155 Line RDI Control Register. The TLRDI input takes precedence over the TTOH and TTOHEN inputs. TLRDI is sampled on the rising edge of TCLK.
TRCPFP			The transmit ring control port frame position (TRCPFP) signal identifies bit positions in the transmit ring control port data (TRCPDAT) when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the SPECTRA-155 Section/Line Control/Enable Register). TRCPFP is high during the filtered K1, K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, and the send line AIS and send line RDI bit positions in the TRCPDAT stream. TRCPFP is normally connected to the RRCPFP output of a mate SPECTRA-155 in ring-based add-drop multiplexer applications. TRCPFP is sampled on the rising edge of TRCPCLK.

Pin Name	Pin Type	PIN No.	Function
TLAIS/	Input	Y6	The active high transmit line alarm indication signal (TLAIS) controls the insertion of line AIS in the outgoing stream when the ring control port is disabled. When TLAIS is set high, the complete frame (except the section overhead or regenerator section) is overwritten with the all ones pattern (before scrambling). The TLAIS input takes precedence over the TTOH and TTOHEN inputs. TLAIS is sampled on the rising edge of TCLK.
TRCPDAT			The transmit ring control port data (TRCPDAT) signal contains the transmit ring control port data stream when the ring control port is enabled (the enabling and disabling of the ring control port is controlled by a bit in the SPECTRA-155 Section/Line Control/Enable Register). The transmit ring control port data consists of the filtered K1, K2 byte values, the change of APS value bit position, the protection switch byte failure status bit position, the send line AIS and send line RDI bit positions, and the line REI bit positions. TRCPDAT is normally connected to the RRCPDAT output of a mate SPECTRA-155 in ring-based add-drop multiplexer applications. TRCPDAT is sampled on the rising edge of TRCPCLK.

Pin Name	Pin Type	PIN No.	Function
TSLDCLK	Tristate Output	R3	The transmit section/line DCC clock (TSLDCLK) can either be used to clock in the section or line DCC as selected using the TDLSEL bit in the SPECTRA-155 Transmit Overhead Input Control register. When section DCC is selected, TSLDCLK is a 192 KHz clock used to sample the TSLD input. TSLDCLK is generated by gapping a 216 KHz clock. When line DCC is selected, TSLDCLK is a 576 KHz clock used to sample the TSLD input. TSLDCLK is generated by gapping a 2.16 MHz clock. TSLDCLK can be tristate using the TRIS_OHB input and the TSLDCLK_TS bit in the SPECTRA-155 Transmit Overhead Input Control register. On reset, TSLDCLK will be tristate if TRIS_OHB is low.
TSLD	Input	R2	The transmit section/line DCC (TSLD) signal contains the section data communications channel (D1-D3) or the line data communications channel (D4-D12) as selected using the TDLSEL bit in the SPECTRA-155 Transmit Overhead Input Control register. The TTOHEN input takes precedence over TSLD. TSLD is sampled on the rising edge of TSLDCLK.
TOWCLK	Output	V4	The transmit order wire clock (TOWCLK) is a 64 KHz clock used to sample the TSOW, TSUC, and TLOW inputs. If selected using the T64SEL bit in the SPECTRA-155 Transmit Overhead Input Control register, TOWCLK is generated by gapping a 72 KHz clock; otherwise, TOWCLK is not gapped.

Pin Name	Pin Type	PIN No.	Function
TSOW	Input	T4	The transmit section order wire (TSOW) signal contains the section order wire channel (E1) inserted into the outgoing stream. The TTOHEN input takes precedence over TSOW. TSOW is sampled on the rising edge of TOWCLK.
TSUC	Input	U2	The transmit section user channel (TSUC) signal contains the section user channel (F1) inserted into the outgoing stream. The TTOHEN input takes precedence over TSUC. TSUC is sampled on the rising edge of TOWCLK.
TLOW	Input	U3	The transmit line order wire (TLOW) signal contains the line order wire channel (E2) inserted into the outgoing stream. The TTOHEN input takes precedence over TLOW. TLOW is updated on the rising edge of TOWCLK.
TLDCLK	Output	U1	The transmit line DCC clock (TLDCLK) is a 576 KHz clock used to sample the TLD input. TLDCLK is generated by gapping a 2.16 MHz clock.
TLD	Input	R4	The transmit line DCC (TLD) signal contains the line data communications channel (D4 - D12) inserted into the outgoing stream. The TTOHEN input takes precedence over TLD. TLD is sampled on the rising edge of TLDCLK.

Pin Name	Pin Type	PIN No.	Function
TOHCLK	Tristate Output	T1	The transmit overhead clock (TOHCLK) can be selected to clock in either the section orderwire (E1), the line orderwire (E2), the line user channel (F1) or the automatic protection switch channel (K1, K2). Selection of the transmit overhead clock is made using the TOHSEL bits in the SPECTRA-155 Transmit Overhead Input Control register. When either orderwire or user channel clocks are selected, TOHCLK is a 64 KHz clock used to sample the TOH input. If selected using the T64SEL bit in the SPECTRA-155 Transmit Overhead Input register, TOHCLK is generated by gapping a 72 KHz clock; otherwise, TOHCLK is not gapped. When the transmit automatic protection switch channel clock is selected, TOHCLK is a 128 KHz clock used to sample the TOH input. TOHCLK is generated by gapping a 144 KHz clock. TOHCLK can be tristate using the TRIS_OHB input and the TOHCLK_TS bit in the SPECTRA-155 Transmit Overhead Input Control register. On reset, TOHCLK will be tristate if TRIS_OHB is low.
TOH	Input	T2	The transmit overhead (TOH) input can be selected to carry either the section orderwire (E1), the line orderwire (E2), the line user channel (F1) or the automatic protection switch channel (K1, K2). Selection is made using the TOHSEL bits in the SPECTRA-155 Transmit Overhead Input Control register. The TTOHEN and TPOHEN inputs take precedence over TOH. TOH is sampled on the rising edge of TOHCLK.

Pin Name	Pin Type	PIN No.	Function
TTOH	Input	W4	The transmit transport overhead bus (TTOH) contains the transport overhead bytes (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) and error masks (H1, H2, B1, and B2) which may be inserted, or used to insert bit interleaved parity errors or payload pointer bit errors into the overhead byte positions in the outgoing stream. Insertion is controlled by the TTOHEN input. TTOH is sampled on the rising edge of TTOHCLK.
TTOHFP	Output	P2	The transmit transport overhead frame position (TTOHFP) signal is used to locate the individual transport overhead bits in the transport overhead bus, TTOH. TTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is expected in the incoming stream. TTOHFP is updated on the falling edge of TTOHCLK.
TTOHCLK	Output	T3	The transmit transport overhead clock (TTOHCLK) is nominally a 5.184 MHz (1.728 MHz for STS-1) clock that provides timing for upstream circuitry that sources the transport overhead, TTOH. TTOHCLK is a gapped 6.48 MHz clock when accessing the transport overhead of STS-3/3c (STM-1/AU3/AU4) streams. TTOHCLK is a gapped 2.16 MHz clock when accessing the transport overhead of an STS-1 (STM-0/AU3) stream.

Pin Name	Pin Type	PIN No.	Function
TTOHEN	Input	U5	The transmit transport overhead insert enable (TTOHEN) signal controls the source of the transport overhead data which is inserted in the transmit stream. While TTOHEN is high during the most significant bit of a TTOH byte, values sampled on the TTOH input are inserted into the corresponding transport overhead bit positions (for the A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). While TTOHEN is low during the most significant bit of a TTOH byte, the default values are inserted into these transport overhead byte positions. The TTOHEN input take precedence over TOH. A high level on TTOHEN during most significant bit of TTOH for the H1, H2, B1, or B2 bytes enables an error mask. While the error mask is enabled, a high level on TTOH causes the corresponding H1, H2, B1 or B2 bit positions to be inverted. When the section trace enable (STEN) bit is a logic 1, the J0 byte contents are sourced from the section trace buffer, regardless of the state of TTOHEN. A low level on TTOH allows the corresponding bit positions to pass through the SPECTRA-155 uncorrupted. TTOHEN is sampled on the rising edge of TTOHCLK.

Table 4 - Path Status/Overhead Interface Signals (37)

Pin Name	Pin Type	PIN No.	Function
B3E[3] B3E[2] B3E[1]	Output	E20 F20 H17	The bit interleaved parity error signals (B3E[3:1]) signal is set high for one RPOHCLK period for each path BIP-8 error detected (up to eight per frame) or once if any of the BIP-8 bits are in error depending on whether BIP-8 errors are treated on a bit or block basis. Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed BIP-8 for the previous frame. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only B3E[1] is active. B3E[3:1] is updated on the falling edge of RPOHCLK.

Pin Name	Pin Type	PIN No.	Function
RALM[1]	Output	G18	The Receive Alarm (RALM[1]) signal is the logical OR of the LOP[1], PAIS[1], PRDI[1] , PERDI[1], LOM[1], LOPCON and PAISCON states. Each alarm can be individually enabled using bits in the SPECTRA-155 RALM[1] Output Control register. RALM[1] is updated on the falling edge of RCLK. The loss of pointer signal (LOP[1]) indicates the loss of pointer state in STS-1 (STM-0/AU3) #1 of an STS-3 (STM-1/AU3) SONET/SDH stream. LOP[1] is set high when invalid STS-1 (STM-0/AU3) pointers are received in eight consecutive frames, or if eight consecutive enabled NDFs are detected in the STS-1 (STM-0/AU3) #1 stream. LOP[1] is active in STS-3c (STM-1/AU4) and STS-1 (STM-0/AU3) modes. The path alarm indication signal (PAIS[1]) indicates the path AIS state associated with the STS-1 (STM-0/AU3) #1 of an STS-3 (STM-1/AU3) SONET/SDH stream. PAIS[1] is set high when an all ones pattern is observed in the STS-1 (STM-0/AU3) pointer bytes (H1 and H2) for three consecutive frames in the STS-1 (STM-0/AU3) #1 stream. PAIS[1] is active in STS-3c (STM-1/AU4) and STS-1 (STM-0/AU3) modes. The path remote defect indication signal (PRDI[1]) indicates the path remote state associated with the STS-1 (STM-0/AU3) #1 of an STS-3 (STM-1/AU3) SONET/SDH stream. PRDI[1] is set high when the path RDI alarm bit (bit 5) of the path status (G1) byte is set high for five or ten consecutive frames. PRDI[1] is active in STS-3c (STM-1/AU4) and STS-1 (STM-0/AU3) modes. The path enhanced remote defect indication signal (PERDI[1]) indicates the path enhanced remote state associated with the

Pin Name	Pin Type	PIN No.	Function
			STS-1 (STM-0/AU3) #1 of an STS-3 (STM-1/AU3) SONET/SDH stream. PERDI[1] is set high when the path ERDI alarm code (bits 5,6,7) of the path status (G1) byte is set to the same alarm codepoint for five or ten consecutive frames. EPRDI[1] is active in STS-3c (STM-1/AU4) and STS-1 (STM-0/AU3) modes. The loss of multiframe signal (LOM[1]) indicates the tributary multiframe synchronization status associated with the STS-1 (STM-0/AU3) #1 of an STS-3 (STM-1/AU3) SONET/SDH stream. LOM[1] is set high if a correct four frame sequence is not detected in eight frames. LOM[[1] is active in STS-3c (STM-1/AU4) and STS-1 (STM-0/AU3) modes. The loss of pointer concatenation and path AIS concatenation signals (LOPCON and PAISCON) are the concatenated alarms for STS-3c (STM-1/AU4) SONET/SDH stream.

Pin Name	Pin Type	PIN No.	Function
RALM[2]	Output	F19	The Receive Alarm (RALM[2]) signal is the logical OR of the LOP[2], PAIS[2], PRDI[2], PERDI[2] and LOM[2] states. Each alarm can be individually enabled using bits in the SPECTRA-155 RALM[2] Output Control register. RALM[2] is updated on the falling edge of RCLK. The loss of pointer signal (LOP[2]) indicates the loss of pointer state in STS-1 (STM-0/AU3) #2 of an STS-3 (STM-1/AU3) SONET/SDH stream. LOP[2] is set high when invalid STS-1 (STM-0/AU3) pointers are received in eight consecutive frames, or if eight consecutive enabled NDFs are detected in the STS-1 (STM-0/AU3) #2 stream. The path alarm indication signal (PAIS[2]) indicates the path AIS state associated with the STS-1 (STM-0/AU3) #2 of an STS-3 (STM-1/AU3) SONET/SDH stream. PAIS[2] is set high when an all ones pattern is observed in the STS-1 (STM-0/AU3) pointer bytes (H1 and H2) for three consecutive frames in the STS-1 (STM-0/AU3) #2 stream. The path remote defect indication signal (PRDI[2]) indicates the path remote state associated with the STS-1 (STM-0/AU3) #2 of an STS-3 (STM-1/AU3) SONET/SDH stream. PRDI[2] is set high when the path RDI alarm bit (bit 5) of the path status (G1) byte is set high for five or ten consecutive frames. The path enhanced remote defect indication signal (PERDI[2]) indicates the path enhanced remote state associated with the STS-1 (STM-0/AU3) #2 of an STS-3 (STM-1/AU3) SONET/SDH stream. PERDI[2] is set high when the path ERDI alarm code (bits 5,6,7) of the path status (G1) byte is set to the same alarm codepoint for five or ten consecutive frames.

Pin Name	Pin Type	PIN No.	Function
			The loss of multiframe signal (LOM[2]) indicates the tributary multiframe synchronization status associated with the STS-1 (STM-0/AU3) #2 of an STS-3 (STM-1/AU3) SONET/SDH stream. LOM[2] is set high if a correct four frame sequence is not detected in eight frames.

Pin Name	Pin Type	PIN No.	Function
RALM[3]	Output	F18	The Receive Alarm (RALM[3]) signal is the logical OR of the LOP[3], PAIS[3], PRDI[3], PERDI[3] and LOM[3] states. Each alarm can be individually enabled using bits in the SPECTRA-155 RALM[3] Output Control register. RALM[3] is updated on the falling edge of RCLK. The loss of pointer signal (LOP[3]) indicates the loss of pointer state in STS-1 (STM-0/AU3) #3 of an STS-3 (STM-1/AU3) SONET/SDH stream. LOP[3] is set high when invalid STS-1 (STM-0/AU3) pointers are received in eight consecutive frames, or if eight consecutive enabled NDFs are detected in the STS-1 (STM-0/AU3) #3 stream. The path alarm indication signal (PAIS[3]) indicates the path AIS state associated with the STS-1 (STM-0/AU3) #3 of an STS-3 (STM-1/AU3) SONET/SDH stream. PAIS[3] is set high when an all ones pattern is observed in the STS-1 (STM-0/AU3) pointer bytes (H1 and H2) for three consecutive frames in the STS-1 (STM-0/AU3) #3 stream. The path remote defect indication signal (PRDI[3]) indicates the path remote state associated with the STS-1 (STM-0/AU3) #3 of an STS-3 (STM-1/AU3) SONET/SDH stream. PRDI[3] is set high when the path RDI alarm bit (bit 5) of the path status (G1) byte is set high for five or ten consecutive frames. The path enhanced remote defect indication signal (PERDI[3]) indicates the path enhanced remote state associated with the STS-1 (STM-0/AU3) #3 of an STS-3 (STM-1/AU3) SONET/SDH stream. PERDI[3] is set high when the path ERDI alarm code (bits 5,6,7) of the path status (G1) byte is set to the same alarm codepoint for five or ten consecutive frames.

Pin Name	Pin Type	PIN No.	Function
			The loss of multiframe signal (LOM[3]) indicates the tributary multiframe synchronization status associated with the STS-1 (STM-0/AU3) #3 of an STS-3 (STM-1/AU3) SONET/SDH stream. LOM[3] is set high if a correct four frame sequence is not detected in eight frames.

Pin Name	Pin Type	PIN No.	Function
RPOHCLK[3] RPOHCLK[2] RPOHCLK[1]	Output	J18 K18 M19	The receive path overhead clocks (RPOHCLK[3:1]) provide timing to process the B3E[3:1] signals, to insert tandem path incoming error count and data link, and to sample the extracted path overhead for the corresponding STS-1 (STM-0/AU3) stream. RPOHCLK[3:1] are nominally 576 KHz clocks. RPOHCLK[3:1] is a gapped 648 KHz clock. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only RPOHCLK[1] is active. RTCEN[3:1], and RTCOH[3:1] are sampled on the rising edge of the corresponding RPOHCLK signal. B3E[3:1], RPOH[3:1] and RPOHFP[3:1] are updated on the falling edge of the corresponding RPOHCLK signal. RPOHCLK[1] provides timing for the serial receive alarm indication port (RAD), which is updated on the falling edge of RPOHCLK[1].
RPOH[3] RPOH[2] RPOH[1]	Output	J19 L19 M18	The receive path overhead data signals (RPOH[3:1]) contain the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the path overhead of the corresponding STS-1 (STM-0/AU3) stream. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only RPOH[1] is active. Each RPOH signal is updated on the falling edge of the corresponding RPOHCLK signal.

Pin Name	Pin Type	PIN No.	Function
RPOHFP[3] RPOHFP[2] RPOHFP[1]	Output	K19 L18 N19	The receive path overhead frame position signals (RPOHFP[3:1]) may be used to locate the individual path overhead bits in the path overhead data stream for the corresponding STS-1 (STM-0/AU3) stream. Each RPOHFP[3:1] signal is logic 1 when bit 1 (the most significant bit) of the path trace byte (J1) is present in the corresponding RPOH stream. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only RPOHFP[1] is active. Each RPOHFP signal is updated on the falling edge of the corresponding RPOHCLK signal. RPOHFP[1] may be used to located the BIP error count and path RDI indication bits on the receive alarm port data signal (RAD). RPOHFP[1] is logic 1 when the first of eight BIP error positions from the first STS-1 (STM-0/AU3) or the STS-3c (STM-1/AU4) stream is present on the receive alarm data signal (RAD).
RTCEN[3] RTCEN[2] RTCEN[1]	Input	G19 H18 J17	The receive tandem connection overhead insert enable signals (RTCEN[3:1]) control the insertion of incoming error count and data link in the tandem connection maintenance byte (Z5), on a bit-by-bit basis. When RTCEN is set high, the data on the corresponding RTCOH stream is inserted into the associated bit in the Z5 byte. RTCEN has significance only during the J1 byte positions in the RPOHCLK clock sequence and is ignored at all other times. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only RTCEN[1] is significant. RTCEN is sampled on the rising edge of the corresponding RPOHCLK signal.

Pin Name	Pin Type	PIN No.	Function
RTCOH[3] RTCOH[2] RTCOH[1]	Input	G20 H19 H20	The receive tandem connection overhead data signals (RTCOH[3:1]) contain the incoming error count and data link message to be inserted into the tandem connection maintenance byte (Z5). When RTCEN is set high, the values sampled on RTCOH is inserted into the Z5 byte. When RTCEN is set low, the IEC field of Z5 reports the incoming path BIP error count and the data link field is either set to all ones or passed through unmodified. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only RTCEN[1] is significant. RTCOH is sampled on the rising edge of the corresponding RPOHCLK signal.
RAD	Output	F17	The receive alarm port data signal (RAD) contains the path BIP error count and the path remote alarm indication status of the three receive STS-1 (STM-0/AU3) streams or the single STS-3c (STM-1/AU4) stream. In addition, the RAD contains the transmit K1 and K2 bytes. RAD is updated on the falling edge of RPOHCLK[1].
TPOH[3] TPOH[2] TPOH[1]	Input	A4 D3 E3	The transmit path overhead data signals (TPOH[3:1]) contain the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) and error mask (B3 and H4) which may be inserted, or used to insert BIP and multiframe sequence bit errors into the path overhead byte positions in the transmit stream. Insertion is controlled by the corresponding TPOHEN input, or by bits in internal registers. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only TPOH[1] is significant. Each TPOH input is sampled on the rising edge of the corresponding TPOHCLK output.

Pin Name	Pin Type	PIN No.	Function
TPOHEN[3] TPOHEN[2] TPOHEN[1]	Input	C5 C4 D1	The transmit path overhead insert enable signals (TPOHEN[3:1]), together with internal register bits, control the source of the path overhead data which is inserted in the transmit stream. While TPOHEN is high, values sampled on the TPOH input are inserted into the corresponding path overhead bit position (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). While TPOHEN is low, values obtained from internal registers are inserted into these path overhead bit positions. The TPOHEN input take precedence over TOH. A high level on TPOHEN during the B3 or H4 bit positions enables an error mask. While the error mask is enabled, a high level on input TPOH causes the corresponding B3 or H4 bit position to be inverted. A low level on TPOH allows the corresponding bit position to pass through the SPECTRA-155 uncorrupted. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only TPOHEN[1] is significant. Each TPOHEN input is sampled on the rising edge of the corresponding TPOHCLK output.
TPOHCLK[3] TPOHCLK[2] TPOHCLK[1]	Output	B4 E4 E2	The transmit path overhead clocks (TPOHCLK[3:1]) provide timing to update the corresponding path overhead stream, TPOH. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, TPOHCLK[1] is a 576kHz clock and TPOHCLK[3:2] are inactive. TPOH and TPOHEN are sampled on the rising edge of the corresponding TPOHCLK.

Pin Name	Pin Type	PIN No.	Function
TPOHFP[3] TPOHFP[2] TPOHFP[1]	Output	D6 D5 D2	The path overhead frame position signals (TPOHFP[3:1]) may be used to locate the individual path overhead bits in the overhead data stream, TPOH. TPOHFP is logic 1 when bit 1 (the most significant bit) of the Path Trace byte (J1) is present in the TPOH stream. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only TPOHFP[1] is active. Each TPOHFP output is updated on the falling edge of the corresponding TPOHCLK output.
TAD	Input	R1	The transmit alarm port data signal (TAD) contains the path REI count and the path PRDI status of the three associated receive STS-1 (STM-0/AU3) streams or the single STS-3c (STM-1/AU4) stream. In addition, the TAD input contains the K1 and K2 bytes from a mate SPECTRA-155. TAD is sampled on the rising edge of TACK.
TAFP	Input	P1	The transmit alarm port frame pulse signal (TAFP) marks the first bit of the transmit alarm message in each SONET/SDH frame. TAFP is pulsed high to mark the first path REI bit location of the first STS-1 (STM-0/AU3) stream or the first path REI bit location of the single STS-3c (STM-1/AU4) stream. TAFP is sampled on the rising edge of TACK.
TACK	Input	N4	The transmit alarm port clock (TACK) provides timing for transmit alarm port. TACK is nominally a 576 KHz clock. Inputs TAD and TAFP are sampled on the rising edge of TACK.

Table 5 - System Side Interface Signals (38)

Pin Name	Pin Type	PIN No.	Function
SMODE[2] SMODE[1] SMODE[0]	Input	C16 A17 B17	The system mode select (SMODE[2:0]) signal is used to select the operation of the system side interface. SMODE[2:0] selects the operation of system signals SS[34:0] and in some cases the direction of the signals. SMODE[2:0] should be strapped to one of the codepoints below: 000 -Byte Telecombus Mode 001 -Nibble Telecombus Mode 010 -Serial Telecombus Mode 011 -Byte Data Mode 100 -Nibble Data Mode 101 -Serial Data Mode 110 -Serial DS3 Mode 111 -Reserved

Pin Name	Pin Type	PIN No.	Function
SS[0]	I/O	D15	The system (SS[34:0]) signals are used to interface the SPECTRA-155 to data sinks and sources. The signal descriptions are listed below for the modes selected using the SMODE[2:0] inputs.
SS[1]	Input	B16	
SS[2]	I/O	A16	
SS[3]	I/O	C15	
SS[4]	Output	B15	
SS[5]	Output	A15	
SS[6]	Output	C14	
SS[7]	Output	D13	
SS[8]	Output	B14	
SS[9]	Output	A14	
SS[10]	Output	C13	
SS[11]	Output	D12	
SS[12]	Output	B13	
SS[13]	Input	C12	
SS[14]	Input	B12	
SS[15]	Input	A12	
SS[16]	Input	D11	
SS[17]	Input	C11	
SS[18]	Input	B11	
SS[19]	Input	A11	
SS[20]	Input	C10	
SS[21]	Input	B10	
SS[22]	Input	B9	
SS[23]	Input	C9	
SS[24]	Input	A8	
SS[25]	Input	D9	
SS[26]	Input	B8	

Pin Name	Pin Type	PIN No.	Function
SS[27]	I/O	C8	The system (SS[34:0]) signals are used to interface the SPECTRA-155 to data sinks and sources. The signal descriptions are listed below for the modes selected using the SMODE[2:0] inputs.
SS[28]	Output	A7	
SS[29]	Output	B7	
SS[30]	Output	D8	
SS[31]	Output	C7	
SS[32]	Input	A6	
SS[33]	Input	B6	
SS[34]	Input	C6	

Table 6 - Byte Telecombus Mode (SMODE[2:0]=000)

Pin Name	Pin Type	PIN No.	Function
SS[0]/DCK	Input	D15	The DROP bus clock (DCK) provides timing for the DROP bus interface. DCK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Frequency offsets between RCLK and DCK are accommodated by pointer justification events on the DROP bus. DFP is sampled on the rising edge of DCK. Outputs DPL, DC1J1V1, DDP and DD[7:0] are updated on the rising edge of DCK.
SS[1]/DFP	Input	B16	The active high DROP bus reference frame position signal (DFP) indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the DD[7:0] bus. Note that DFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to DFP. DFP is sampled on the rising edge of DCK.
SS[2]/DD[0] SS[3]/DD[1] SS[4]/DD[2] SS[5]/DD[3] SS[6]/DD[4] SS[7]/DD[5] SS[8]/DD[6] SS[9]/DD[7]	Output	A16 C15 B15 A15 C14 D13 B14 A14	The DROP bus data (DD[7:0]) contains the SONET/SDH receive payload data. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. DD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). DD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). DD[7:0] is updated on the rising edge of DCK.

Pin Name	Pin Type	PIN No.	Function
SS[10]/DPL	Output	C13	The active high DROP bus payload active signal (DPL) indicates when the DD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL is updated on the rising edge of DCK.
SS[11]/ DC1J1V1	Output	D12	The DROP bus composite timing signal (DC1J1V1) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus DD[7:0]. DC1J1V1 pulses high with the DROP bus payload active signal (DPL) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1 pulses high with DPL set high to mark the path trace byte (J1). Optionally, the DC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. DC1J1V1 is updated on the rising edge of DCK.
SS[12]/DDP	Output	B13	The DROP bus data parity signal (DDP) indicates the parity of the DROP bus signals. The DROP data bus (DD[7:0]) is always included in parity calculations. The internal register bits control the inclusion of the DPL and DC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. DDP is updated on the rising edge of DCK.
SS[13]/ACK	Input	C12	The ADD bus clock (ACK) provides timing for the ADD bus and the GENERATED bus interfaces. ACK is nominally a 19.44 MHz or 6.48 MHz, 50% duty cycle clock. Inputs AD[7:0], APL, AC1J1V1, GFP and GMFP are sampled on the rising edge of ACK. Outputs GPL, GC1J1V1, and GD[1:0] are updated on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[14]/ AD[0] SS[15]/ AD[1] SS[16]/ AD[2] SS[17]/ AD[3] SS[18]/ AD[4] SS[19]/ AD[5] SS[20]/ AD[6] SS[21]/ AD[7]	Input	B12 A12 D11 C11 B11 A11 C10 B10	The ADD bus data (AD[7:0]) contains the SONET/SDH transmit payload data. The transport overhead bytes, except the H1 and H2 pointer bytes, are ignored. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1) or optionally by interpreting the H1 and H2 pointer bytes. AD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[7:0] is sampled on the rising edge of ACK.
SS[22]/APL	Input	B9	The ADD bus payload active signal (APL) indicates when AD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. APL is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[23]/ AC1J1V1	Input	C9	The ADD bus composite timing signal (AC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the ADD data bus AD[7:0]. AC1J1V1 pulses high with the ADD bus payload active signal (APL) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). Optionally, the AC1J1V1 pulses high with APL set high to mark the path trace byte (J1). Optionally, the AC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes are controlled using the DISJ1V1 bit in the SPECTRA-155 Path/Mapper Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (AD[7:0]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. AC1J1V1 is sampled on the rising edge of ACK.
SS[24]/ADP	Input	A8	The ADD bus data parity signal (ADP) indicates the parity of the ADD bus signals. The ADD data bus (AD[7:0]) is always included in parity calculations. Internal register bits controls the inclusion of the APL and AC1J1V1 signals in parity calculations and the sense (odd/even) of the parity. ADP is sampled on the rising edge of ACK.
SS[25]/GFP	Input	D9	The active high GENERATED bus reference frame position signal (GFP) indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the GD[1:0] bus. Note that GFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to GFP. GFP is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[26]/ GMFP	Input	B8	The active high GENERATED reference multiframe position signal (GMFP) is used to align the SONET/SDH tributary multiframe boundary on the GENERATED bus . GMFP should be brought high for a single ACK period every 9720 ACK cycles, or multiples thereof. GMFP may be tied low if such synchronization is not required. A pulse on GMFP realigns the GENERATED bus to be the first of four frames in the multiframe. I.e., the frame containing the V1 bytes. In STS-1 (STM-0/AU3) mode, GMFP is sampled one ACK cycle after the J1 indication on GC1J1V1. In STS-3/3c (STM-1/AU3/AU4) modes, GMFP is sampled three ACK cycles after the J1 indication. GMFP is ignored at other byte positions. GMFP is sampled on the rising edge of ACK.
SS[27]/ GD[0] SS[28]/ GD[1]	Output	C8 A7	The GENERATED bus data (GD[1:0]) contains cyclical multiframe count carried in the H4 byte. The sequence is initialized to 'b01 by a high pulse on GMFP, and increments at the byte following J1. GD[1:0] is updated on the rising edge of ACK.
SS[29]/GPL	Output	B7	The GENERATED bus payload active signal (GPL) indicates when GD[1:0] is carrying a payload byte. GPL distinguishes between payload and transport overhead timeslots in the GENERATED bus. Since the GENERATED bus is expected to have fixed timing relationship with the ADD bus, access modules may use GPL to locate payload timeslots in the ADD bus. GPL is updated on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[30]/ GC1J1V1	Output	D8	The GENERATED bus composite timing signal (GC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the GENERATED data bus GD[1:0]. GC1J1V1 pulses high with the GENERATED bus payload active signal (GPL) set low to mark the first STS-1 (STM-0/AU3) Identification byte or equivalently the STM identification byte (C1). GC1J1V1 pulses high with GPL set high to mark the path trace byte (J1). The GC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries. Since the GENERATED bus is expected to have fixed timing relationship with the ADD bus, access modules may use GC1J1V1 to located the frame, payload and tributary multiframe boundaries on the ADD bus. GC1J1V1 is updated on the rising edge of ACK.
SS[31]/GDP	Output	C7	The GENERATED bus data parity signal (GDP) indicates the parity of the GENERATED bus signals. The GENERATED data bus (GD[1:0]) is always included in parity calculations. The internal register bits control the inclusion of the GPL and GC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. GDP is updated on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[32]/ DTPAIS[1] SS[33]/ DTPAIS[2] SS[34]/ DTPAIS[3]	Input	A6 B6 C6	The active high DROP bus or Transmit path alarm indication signals (DTPAIS[3:1]) controls the insertion of path AIS in the DROP bus DD[7:0] or the transmit stream. The function of each DTPAIS[3:1] input pin is independently controlled by the TPAIS_EN bits in the Transmit Path AIS Control #1, Transmit Path AIS Control #2, and Transmit Path AIS Control #3 registers. In STS-3 mode, each DTPAIS[3:1] corresponds to a separate STS-1. DTPAIS[1] corresponds to STS#1, DTPAIS[2] corresponds to STS#2 and DTPAIS[3] corresponds to STS#3. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only DTPAIS[1] is significant. A high level on DTPAIS forces the insertion of the all ones pattern into the complete SPE and the payload pointer bytes (H1, H2, and H3). Path AIS insertion can also be inserted via register access or in response to ISF code in terminating tandem connection termination equipment applications. DTPAIS[3:1] is sampled on the rising edge of DCK for DROP bus or TCLK for transmit stream Path AIS insertion.

Table 7 - Nibble Telecombus Mode (SMODE[2:0]=001)

Pin Name	Pin Type	PIN No.	Function
SS[0]/DCK	Input	D15	The DROP bus clock (DCK) provides timing for the DROP bus interface. For nibble mode, DCK is nominally a 38.88 MHz or 12.96 MHz, 50% duty cycle clock. Frequency offsets between RCLK and DCK/2 are accommodated by pointer justification events on the DROP bus. DFP is sampled on the rising edge of DCK. Outputs DPL, DC1J1V1, DDP and DD[3:0] are updated on the rising edge of DCK.
SS[1]/DFP	Input	B16	The active high DROP bus reference frame position signal (DFP) indicates when the first nibble of the synchronous payload envelope (upper nibble of SPE byte 1 of STS-1 #1) is available on the DD[3:0] bus. Note that DFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to DFP. DFP is sampled on the rising edge of DCK.
SS[2]/DD[0] SS[3]/DD[1] SS[4]/DD[2] SS[5]/DD[3]	Output	A16 C15 B15 A15	The DROP bus data (DD[3:0]) contains the SONET/SDH receive payload data. The transport overhead nibbles, with the exception of the H1, H2 pointer nibbles, are set to zeros. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. DD[3] is the most significant bit (corresponding to bit 1 or 5 of each serial word, the bit received first or fifth, respectively). DD[0] is the least significant bit (corresponding to bit 4 or 8 of each serial word, the fourth or last bit received, respectively). DD[3:0] is updated on the rising edge of DCK.
SS[6] SS[7] SS[8] SS[9]	Output	C14 D13 B14 A14	Reserved.

Pin Name	Pin Type	PIN No.	Function
SS[10]/DPL	Output	C13	The active high DROP bus payload active signal (DPL) indicates when the DD[3:0] is carrying a payload nibble. It is set high during path overhead and payload nibbles and low during transport overhead nibbles. DPL is set high during the H3 nibbles to indicate a negative pointer justification event and set low during the nibbles following H3 to indicate a positive pointer justification event. DPL is updated on the rising edge of DCK.
SS[11]/ DC1J1V1	Output	D12	The DROP bus composite timing signal (DC1J1V1) indicates the frame, payload and tributary multiframe boundaries on the DROP data bus DD[3:0]. DC1J1V1 pulses high with the DROP bus payload active signal (DPL) set low to mark the most significant nibble of the first STS-1 (STM-0/AU3) Identification byte or equivalently the most significant nibble of the STM identification byte (C1). DC1J1V1 pulses high with DPL set high to mark the most significant nibble of the path trace byte (J1). Optionally, the DC1J1V1 signal pulses high on the most significant nibble of the V1 byte to indicate tributary multiframe boundaries. DC1J1V1 is updated on the rising edge of DCK.
SS[12]/DDP	Output	B13	The DROP bus data parity signal (DDP) indicates the parity of the DROP bus signals. The DROP data bus (DD[3:0]) is always included in parity calculations. The internal register bits control the inclusion of the DPL and DC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. DDP is updated on the rising edge of DCK.

Pin Name	Pin Type	PIN No.	Function
SS[13]/ACK	Input	C12	The ADD bus clock (ACK) provides timing for the ADD bus and the GENERATED bus interfaces. ACK is nominally a 38.88 MHz or 12.96 MHz, 50% duty cycle clock for nibble mode operation. Inputs AD[3:0], APL, AC1J1V1, GFP and GMFP are sampled on the rising edge of ACK. Outputs GPL, GC1J1V1, and GD[1:0] are updated on the rising edge of ACK.
SS[14]/ AD[0] SS[15]/ AD[1] SS[16]/ AD[2] SS[17]/ AD[3]	Input	B12 A12 D11 C11	The ADD bus data (AD[3:0]) contains the SONET/SDH transmit payload data. The transport overhead nibbles, except the H1 and H2 pointer nibbles, are ignored. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal (AC1J1V1) or optionally by interpreting the H1 and H2 pointer nibbles. AD[3] is the most significant bit (corresponding to bit 1 or 5 of each serial word, the bit transmitted first or fifth, respectively). AD[0] is the least significant bit (corresponding to bit 4 or 8 of each serial word, the fourth or last bit transmitted, respectively). AD[3:0] is sampled on the rising edge of ACK.
SS[18] SS[19] SS[20] SS[21]	Input	B11 A11 C10 B10	Reserved. Should be tied low when operating in Telecombus nibble mode.

Pin Name	Pin Type	PIN No.	Function
SS[22]/APL	Input	B9	The ADD bus payload active signal (APL) indicates when AD[3:0] is carrying a payload nibble. It is set high during path overhead and payload nibbles and low during transport overhead nibbles. APL is set high during the H3 nibbles to indicate a negative pointer justification event and set low during the nibbles following H3 to indicate a positive pointer justification event. The SPECTRA-155 only samples the most significant nibble of a byte to determine the validity of the byte. The least significant nibble sample is ignored. APL is sampled on the rising edge of ACK.
SS[23]/ AC1J1V1	Input	C9	The ADD bus composite timing signal (AC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the ADD data bus AD[3:0]. AC1J1V1 pulses high with the ADD bus payload active signal (APL) set low to mark the most significant nibble of the first STS-1 (STM-0/AU3) Identification byte or equivalently the most significant nibble of the STM identification byte (C1). Optionally, the AC1J1V1 pulses high with APL set high to mark the most significant nibble of the path trace byte (J1). Optionally, the AC1J1V1 signal pulses high on the most significant nibble of the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes are controlled using the DISJ1V1 bit in the SPECTRA-155 Path/Mapper Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (AD[3:0]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. AC1J1V1 is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[24]/ADP	Input	A8	The ADD bus data parity signal (ADP) indicates the parity of the ADD bus signals. The ADD data bus (AD[3:0]) is always included in parity calculations. Internal register bits controls the inclusion of the APL and AC1J1V1 signals in parity calculations and the sense (odd/even) of the parity. ADP is sampled on the rising edge of ACK.
SS[25]/GFP	Input	D9	The active high GENERATED bus reference frame position signal (GFP) indicates when the most significant nibble of the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) is available on the GD[1:0] bus. Note that GFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to GFP. GFP is sampled on the rising edge of ACK.
SS[26]/ GMFP	Input	B8	The active high GENERATED reference multiframe position signal (GMFP) is used to align the SONET/SDH tributary multiframe boundary on the GENERATED bus . GMFP should be brought high for a single ACK period every 2*9720 ACK cycles, or multiples thereof to identify the most significant nibble of the V1 byte. GMFP may be tied low if such synchronization is not required. A pulse on GMFP realigns the GENERATED bus to be the first of four frames in the multiframe. I.e., the frame containing the V1 bytes. In STS-1 (STM-0/AU3) mode, GMFP is sampled two ACK cycle after the J1 indication on GC1J1V1. In STS-3/3c (STM-1/AU3/AU4) modes, GMFP is sampled six ACK cycles after the J1 indication. GMFP is ignored at other nibble positions. GMFP is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[27]/ GD[0] SS[28]/ GD[1]	Output	C8 A7	The GENERATED bus data (GD[1:0]) contains cyclical multiframe count carried in the H4 byte. The sequence is initialized to 'b01 by a high pulse on GMFP, and increments at the nibble following J1 nibbles. GD[1:0] is updated on the rising edge of ACK.
SS[29]/GPL	Output	B7	The GENERATED bus payload active signal (GPL) indicates when GD[1:0] is carrying a payload byte. GPL distinguishes between payload and transport overhead timeslots in the GENERATED bus. Since the GENERATED bus is expected to have fixed timing relationship with the ADD bus, access modules may use GPL to locate payload timeslots in the ADD bus. GPL is updated on the rising edge of ACK.
SS[30]/ GC1J1V1	Output	D8	The GENERATED bus composite timing signal (GC1J1V1) identifies the frame, payload and tributary multiframe boundaries on the GENERATED data bus GD[1:0]. GC1J1V1 pulses high with the GENERATED bus payload active signal (GPL) set low to mark the most significant nibble of the first STS-1 (STM-0/AU3) Identification byte or equivalently the most significant nibble of the STM identification byte (C1). GC1J1V1 pulses high with GPL set high to mark the most significant nibble of the path trace byte (J1). The GC1J1V1 signal pulses high on the most significant nibble of the V1 byte to indicate tributary multiframe boundaries. Since the GENERATED bus is expected to have fixed timing relationship with the ADD bus, access modules may use GC1J1V1 to locate the frame, payload and tributary multiframe boundaries on the ADD bus. GC1J1V1 is updated on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
SS[31]/GDP	Output	C7	The GENERATED bus data parity signal (GDP) indicates the parity of the GENERATED bus signals. The GENERATED data bus (GD[1:0]) is always included in parity calculations. The internal register bits control the inclusion of the GPL and GC1J1V1 signals in parity calculation and the sense (odd/even) of the parity. GDP is updated on the rising edge of ACK.
SS[32]/ DTPAIS[1] SS[33]/ DTPAIS[2] SS[34]/ DTPAIS[3]	Input	A6 B6 C6	The active high DROP bus or Transmit path alarm indication signals (DTPAIS[3:1]) controls the insertion of path AIS in the DROP bus DD[3:0] or the transmit stream. The function of each DTPAIS[3:1] input pin is independently controlled by the TPAIS_EN bits in the Transmit Path AIS Control #1, Transmit Path AIS Control #2, and Transmit Path AIS Control #3 registers. In STS-3 mode, each DTPAIS[3:1] corresponds to a separate STS-1. DTPAIS[1] corresponds to STS#1, DTPAIS[2] corresponds to STS#2 and DTPAIS[3] corresponds to STS#3. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only DTPAIS[1] is significant. A high level on DTPAIS forces the insertion of the all ones pattern into the complete SPE and the payload pointer bytes (H1, H2, and H3). Path AIS insertion can also be inserted via register access or in response to ISF code in terminating tandem connection termination equipment applications. DTPAIS[3:1] is sampled on the rising edge of DCK for DROP bus or TCLK for transmit stream Path AIS insertion.

Table 8 - Serial Telecombus Mode (SMODE[2:0]=010)

Pin Name	Pin Type	PIN No.	Function
SS[0]/SDCK[1] SS[2]/SDCK[2] SS[3]/SDCK[3]	Input	D15 A16 C15	The Serial DROP bus clocks (SDCK[3:1]) provide timing for the three STS-1 (STM-0/AU3) DROP bus interfaces. SDCK[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SDCK[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. SDCK is nominally a 51.84 MHz, 50% duty cycle clock. Frequency offsets between RCLK and SDCK/8 are accommodated by pointer justification events on the DROP bus. SDFP[3:1] are sampled on the rising edge of the corresponding SDCK. Outputs SDPL, SDC1J1V1 and SDD are updated on the rising edge of the corresponding SDCK.
SS[1]	Input	B16	Reserved. Should be strapped low in this mode of operation.

Pin Name	Pin Type	PIN No.	Function
SS[4]/ SDC1J1V1[1] SS[5]/ SDC1J1V1[2] SS[6]/ SDC1J1V1[3]	Output	B15 A15 C14	The serial DROP bus composite timing signals (SDC1J1V1[3:1]) indicates the frame, payload and tributary multiframe boundaries on the serial DROP data signals SDD[3:1]. SDC1J1V1[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SDC1J1V1[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. SDC1J1V1 pulses high with the DROP bus payload active signal (SDPL) set low to mark the most significant bit of the STS-1 (STM-0/AU3) Identification byte or equivalently the most significant bit of the STM identification byte (C1). SDC1J1V1 pulses high with SDPL set high to mark the most significant bit of the path trace byte (J1). Optionally, the SDC1J1V1 signal pulses high on the most significant bit of the V1 byte to indicate tributary multiframe boundaries. SDC1J1V1 is updated on the rising edge of SDCK.
SS[7]/SDD[1] SS[8]/SDD[2] SS[9]/SDD[3]	Output	D13 B14 A14	The Serial DROP bus data (SDD[3:1]) contains the SONET/SDH receive payload data. SDD[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SDD[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. The transport overhead bits, with the exception of the H1, H2 pointer bits, are set to zeros. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. Bits are output on SDD in the order they were received from the line. SDD is updated on the rising edge of SDCK.

Pin Name	Pin Type	PIN No.	Function
SS[10] /SDPL[1] SS[11] /SDPL[2] SS[12] /SDPL[3]	Output	C13 D12 B13	The active high serial DROP bus payload active signals (SDPL[3:1]) indicates when the associated SDD[3:1] is carrying a payload bit. SDPL[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SDPL[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. SDPL is set high during path overhead and payload bits and low during transport overhead bits. SDPL is set high during the H3 bits to indicate a negative pointer justification event and set low during the eight bits following the H3 bits to indicate a positive pointer justification event. SDPL is updated on the rising edge of SDCK.
SS[13]/ SACK[1] SS[14]/ SACK[2] SS[15]/ SACK[3]	Input	C12 B12 A12	The serial ADD bus clock (SACK[3:1]) signals provides timing for the serial ADD bus interface. SACK[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SACK[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. SACK is nominally a 51.84 MHz, 50% duty cycle clock for serial mode operation. Inputs SAD[3:1], SAPL[3:1], and SAC1J1V1[3:1] are sampled on the rising edge of the corresponding SACK[3:1] clock.

Pin Name	Pin Type	PIN No.	Function
SS[16]/ SAC1J1V1[1] SS[17]/ SAC1J1V1[2] SS[18]/ SAC1J1V1[3]	Input	D11 C11 B11	The serial ADD bus composite timing signals (SAC1J1V1[3:1]) identify the frame, payload and tributary multiframe boundaries on the ADD data buss SAD[3:1]. SAC1J1V1[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SAC1J1V1[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. SAC1J1V1 pulses high with the serial ADD bus payload active signal (SAPL) set low to mark the most significant bit of the STS-1 (STM-0/AU3) Identification byte or equivalently the most significant bit of the STM identification byte (C1). Optionally, the SAC1J1V1 signal pulses high with SAPL set high to mark the most significant bit of the path trace byte (J1). Optionally, the SAC1J1V1 signal pulses high on the most significant bit of the V1 byte to indicate tributary multiframe boundaries. Optional marking of the J1 and V1 bytes are controlled using the DISJ1V1 bit in the SPECTRA-155 Path/Mapper Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD data bus (SAD) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the ADD data bus to allow the V1 position to be identified. SAC1J1V1 is sampled on the rising edge of the associated SACK[3:1].

Pin Name	Pin Type	PIN No.	Function
SS[19]/SAD[1] SS[20]/SAD[2] SS[21]/SAD[3]	Input	A11 C10 B10	The serial ADD bus data (SAD[3:1]) contains the SONET/SDH transmit payload data. SAD[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SAD[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. The transport overhead bits, except the H1 and H2 pointer bits, are ignored. The phase relation of the SPE (VC) to the transport frame is determined by the serial ADD bus composite timing signal (SAC1J1V1) or optionally by interpreting the H1 and H2 pointer bits. Bits are transmitted in the order they are sampled on the SAD inputs. SAD[3:1] are sampled on the rising edge of the associated SACK[3:1].
SS[22]/ SAPL[1] SS[23]/ SAPL[2] SS[24]/ SAPL[3]	Input	B9 C9 A8	The serial ADD bus payload active signals (SAPL[3:1]) indicate when the associate SAD[3:1] is carrying payload bits. SAPL[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SAPL[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. SAPL is set high during path overhead and payload bits and low during transport overhead bits. SAPL is set high during the H3 bits to indicate a negative pointer justification event and set low during the 8 bits following H3 bits to indicate a positive pointer justification event. The SPECTRA-155 only samples SAPL at the most significant bit of a byte to determine the validity of the byte. The other samples are ignored. SAPL is sampled on the rising edge of the associated SACK.

Pin Name	Pin Type	PIN No.	Function
SS[25]/ SDFP[1] SS[26]/ SDFP[2] SS[27]/ SDFP[3]	Input	D9 B8 C8	The active high serial DROP bus reference frame position signals (SDFP[3:1) indicate when the first bit of the synchronous payload envelope (most significant bit of SPE byte 1) is on the associated SDD[3:1] stream. SDFP[1] corresponds to the STS-1 (STM-0/AU3) #1 of a STS-3 (STM-1/AU3) stream while SDFP[3] corresponds to the STS-1 (STM-0/AU3) #3 of a STS-3 (STM-1/AU3) stream. Note that SDFP has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to SDFP. SDFP[3:1] are sampled on the rising edge of the associated SDCK[3:1] signals.
SS[28] SS[29] SS[30] SS[31]	Output	A7 B7 D8 C7	Reserved.

Pin Name	Pin Type	PIN No.	Function
SS[32] SDTPAIS[1] SS[33] SDTPAIS[2] SS[34] SDTPAIS[3]	Input	A6 B6 C6	The active high serial DROP bus or Transmit path alarm indication signals (DTPAIS[3:1]) controls the insertion of path AIS in the serial DROP bus SDD[3:1] or the transmit stream. The function of each DTPAIS[3:1] input pin is independently controlled by the TPAIS_EN bits in the Transmit Path AIS Control #1, Transmit Path AIS Control #2, and Transmit Path AIS Control #3 registers. In STS-3 mode, each DTPAIS[3:1] corresponds to a separate STS-1. DTPAIS[1] corresponds to STS#1, DTPAIS[2] corresponds to STS#2 and DTPAIS[3] corresponds to STS#3. In STS-3c (STM-1/AU4) mode or STS-1 (STM-0/AU3) mode, only DTPAIS[1] is significant. A high level on DTPAIS forces the insertion of the all ones pattern into the complete SPE and the payload pointer bytes (H1, H2, and H3). Path AIS insertion can also be inserted via register access or in response to ISF code in terminating tandem connection termination equipment applications. DTPAIS[3:1] is sampled on the rising edge of DCK for DROP bus or TCLK for transmit stream Path AIS insertion.

Table 9 - Byte Data Mode (SMODE[2:0]=011)

Pin Name	Pin Type	PIN No.	Function
SS[0]/ DMROCLK	Output	D15	The data mode receive output clock (DMROCLK) signal provides timing for external data processing devices (i.e. HDLC controllers). In the absence of pointer movements, DMROCLK is nominally an 18.72 MHz clock in STS-3c (STM-1/AU4) generated by gapping a 19.44 MHz clock. In STS-1 (STM-0/AU3) mode, DMROCLK is nominally a 6.192 MHz clock generated by gapping a 6.48 MHz clock when the RDM_FSEN bit in SPECTRA-155 Data Mode Configuration register is set low. DMROCLK is nominally a 6.048 MHz clock when the RDM_FSEN bit is set high. DMRDAT[7:0] is updated on the falling edge of DMROCLK.
SS[1]	Input	B16	Reserved. Must be strapped low when not used.

Pin Name	Pin Type	PIN No.	Function
SS[2]/ DMRDAT[0] SS[3]/ DMRDAT[1] SS[4]/ DMRDAT[2] SS[5]/ DMRDAT[3] SS[6]/ DMRDAT[4] SS[7]/ DMRDAT[5] SS[8]/ DMRDAT[6] SS[9]/ DMRDAT[7]	Output	A16 C15 B15 A15 C14 D13 B14 A14	The data mode receive data (DMRDAT[7:0]) bus contains the SONET/SDH receive payload data for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) modes. Transport overhead and path overhead bytes are not included. In addition, for STS-1 (STM-0/AU3) operation, the fix stuff columns are optionally included using the RDM_FSEN bit in the SPECTRA-155 Data Mode Configuration register. DMRDAT[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DMRDAT[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DMRDAT[7:0] is updated on the falling edge of DMROCLK.
SS[10] SS[11] SS[12]	Output	C13 D12 B13	Reserved.
SS[13]/ DMTICLK	Input	C12	The data mode transmit input (DMTICLK) clock provides timing to clock data into the SPECTRA-155 from a up stream data source. DMTICLK must be tied to DMTOCLK directly. Inputs DMTDAT[7:0] are sampled using the rising edge of DMTICLK.

Pin Name	Pin Type	PIN No.	Function
SS[14]/ DMTDAT[0] SS[15]/ DMTDAT[1] SS[16]/ DMTDAT[2] SS[17]/ DMTDAT[3] SS[18]/ DMTDAT[4] SS[19]/ DMTDAT[5] SS[20]/ DMTDAT[6] SS[21]/ DMTDAT[7]	Input	B12 A12 D11 C11 B11 A11 C10 B10	The data mode transmit data (DMTDAT[7:0]) bus contains the data to be mapped into the SONET/SDH SPE for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) modes. For STS-1 (STM-0/AU3) operation, the fix stuff columns are optionally included using the TDM_FSEN bit in the SPECTRA-155 Data Mode Configuration register. DMTDAT[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). DMTDAT[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). DMTDAT[7:0] are sampled using the rising edge of DMTICLK.
SS[22] SS[23] SS[24] SS[25] SS[26] SS[27]	Input	B9 C9 A8 D9 B8 C8	Reserved. Must be strapped low when not used.

Pin Name	Pin Type	PIN No.	Function
SS[28]/ DMTOCLK	Output	A7	The data mode transmit output clock (DMTOCLK) signal provides timing for upstream external data sources (i.e. HDLC controllers). DMTOCLK is nominally an 18.72 MHz clock in STS-3c (STM-1/AU4) generated by gapping a 19.44 MHz clock. In STS-1 (STM-0/AU3) mode, DMTOCLK is nominally a 6.192 MHz clock generated by gapping a 6.48 MHz clock when the TDM_FSEN bit in SPECTRA-155 Data Mode Configuration register is set low. DMTOCLK is nominally a 6.048 MHz clock when the TDM_FSEN bit is set high. For correct operation, DMTOCLK must be tied to DMTICLK.
SS[29] SS[30] SS[31]	Output	B7 D8 C7	Reserved.
SS[32] SS[33] SS[34]	Input	A6 B6 C6	Reserved. Must be strapped low when not used.

Table 10 - Nibble Data Mode (SMODE[2:0]=100)

Pin Name	Pin Type	PIN No.	Function
SS[0]/ DMROCLK	Output	D15	The data mode receive output clock (DMROCLK) signal provides timing for external data processing devices (i.e. HDLC controllers). In the absence of pointer movements, DMROCLK is nominally an 37.44 MHz clock in STS-3c (STM-1/AU4) generated by gapping a 38.88 MHz clock. In STS-1 (STM-0/AU3) mode, DMROCLK is nominally a 12.384 MHz clock generated by gapping a 12.96 MHz clock when the RDM_FSEN bit in SPECTRA-155 Data Mode Configuration register is set low. DMROCLK is nominally a 12.096 MHz clock when the RDM_FSEN bit is set high. DMRDAT[3:0] is updated on the falling edge of DMROCLK.
SS[1]	Input	B16	Reserved. Must be strapped low when not used.
SS[2]/ DMRDAT[0] SS[3]/ DMRDAT[1] SS[4]/ DMRDAT[2] SS[5]/ DMRDAT[3]	Output	A16 C15 B15 A15	The data mode receive data (DMRDAT[3:0]) bus contains the SONET/SDH receive payload data for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) modes. Transport overhead and path overhead bytes are not included. In addition, for STS-1 (STM-0/AU3) operation, the fix stuff columns are optionally included using the RDM_FSEN bit in the SPECTRA-155 Data Mode Configuration register. DMRDAT[3] is the most significant bit (corresponding to bit 1 or 5 of each serial word, the bit received first or fifth, respectively). DMRDAT[0] is the least significant bit (corresponding to bit 4 or 8 of each serial word, the fourth or last bit received, respectively). DMRDAT[3:0] is updated on the falling edge of DMROCLK.

Pin Name	Pin Type	PIN No.	Function
SS[6] SS[7] SS[8] SS[9] SS[10] SS[11] SS[12]	Output	C14 D13 B14 A14 C13 D12 B13	Reserved.
SS[13]/ DMTICLK	Input	C12	The data mode transmit input (DMTICLK) clock provides timing to clock data into the SPECTRA-155 from a up stream data source. DMTICLK must be tied to DMTOCLK directly. Inputs DMTDAT[3:0] are sampled using the rising edge of DMTICLK.
SS[14]/ DMTDAT[0] SS[15]/ DMTDAT[1] SS[16]/ DMTDAT[2] SS[17]/ DMTDAT[3]	Input	B12 A12 D11 C11	The data mode transmit data (DMTDAT[3:0]) bus contains the data to be mapped into the SONET/SDH SPE for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) modes. For STS-1 (STM-0/AU3) operation, the fix stuff columns are optionally included using the TDM_FSEN bit in the SPECTRA-155 Data Mode Configuration register. DMTDAT[3] is the most significant bit (corresponding to bit 1 or 5 of each serial word, the bit transmitted first or fifth, respectively). DMTDAT[0] is the least significant bit (corresponding to bit 4 or 8 of each serial word, the fourth or last bit transmitted, respectively). DMTDAT[3:0] are sampled using the rising edge of DMTICLK.

Pin Name	Pin Type	PIN No.	Function
SS[18] SS[19] SS[20] SS[21] SS[22] SS[23] SS[24] SS[26] SS[27]	Input	B11 A11 C10 B10 B9 C9 A8 B8 C8	Reserved. Must be strapped low when not used.
SS[25]/ DMTMSN	Input	D9	The data mode transmit most significant nibble (DMTMSN) signal identifies the nibble mapping between DMTDAT and the SONET/SDH SPE byte. When DMTMSN is high, the corresponding nibble on DMTDAT is mapped to the most significant nibble (bits 1 through 4, the first nibble transmitted) of the SONET/SDH SPE byte. When DMTMSN is low, the corresponding nibble on DMTDAT is mapped to the least significant nibble (bits 5 through 8, the last nibble transmitted) of the SONET/SDH SPE byte. DMTMSN must be present for every clock cycle for correct operation. The TCLK output of SPECTRA-155 must be tied to the DMTMSN directly. DMTMSN is sampled using the rising edge of DMTICLK.

Pin Name	Pin Type	PIN No.	Function
SS[28]/ DMTOCLK	Output	A7	The data mode transmit output clock (DMTOCLK) signal provides timing for upstream external data sources (i.e. HDLC controllers). DMTOCLK is nominally an 37.44 MHz clock in STS-3c (STM-1/AU4) generated by gapping a 38.88 MHz clock. In STS-1 (STM-0/AU3) mode, DMTOCLK is nominally a 12.384 MHz clock generated by gapping a 12.96 MHz clock when the TDM_FSEN bit in SPECTRA-155 Data Mode Configuration register is set low. DMTOCLK is nominally a 12.096 MHz clock when the TDM_FSEN bit is set high. For correct operation, DMTOCLK must be tied to DMTICLK.
SS[29] SS[30] SS[31]	Output	B7 D8 C7	Reserved.
SS[32] SS[33] SS[34]	Input	A6 B6 C6	Reserved. Must be strapped low when not used.

Table 11 - Serial Data Mode (SMODE[2:0]=101)

Pin Name	Pin Type	PIN No.	Function
SS[0] SS[1] SS[2] SS[3]	Input	D15 B16 A16 C15	Reserved. Should be strapped low in this mode of operation.
SS[4]/ SDMROCLK[1] SS[5]/ SDMROCLK[2] SS[6]/ SDMROCLK[3]	Output	B15 A15 C14	The serial data mode receive output (SDMROCLK[3:1]) clocks provide timing for up to three external data processing devices (i.e. HDLC controllers). SDMROCLK[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while SDMROCLK[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). When GAPFS bit in the corresponding D3MD Control register is set low, SDMROCLK is nominally a 49.536 MHz clock generated by gapping a 51.84 MHz clock. When GAPFS bit is set high, SDMROCLK is nominally a 48.384 MHz clock. SDMRDAT[3:1] are updated on the falling edge of their associated SDMROCLK[3:1] clocks.

Pin Name	Pin Type	PIN No.	Function
SS[7]/ SDMRDAT[1] SS[8]/ SDMRDAT[2] SS[9]/ SDMRDAT[3]	Output	D13 B14 A14	The serial data mode receive data (SDMRDAT[3:1]) signals contain the SONET/SDH receive payload data. SDMRDAT[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while SDMRDAT[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). Payload bits are presented in the order in which they are received from the line. SONET/SDH serial word alignment is not maintained. Transport overhead and path overhead bytes are not included. In addition, the SPE fixed stuff columns are optionally included using the GAPFS bit in the D3MD Control register. SDMRDAT[3:1] are updated on the falling edge of their associated SDMROCLK[3:1] clocks.
SS[10] SS[11] SS[12]	Output	C13 D12 B13	Reserved.
SS[13]/ SDMTICLK[1] SS[14]/ SDMTICLK[2] SS[15]/ SDMTICLK[3]	Input	C12 B12 A12	The serial data mode input clocks (SDMTICLK[3:1]) provide timing to clock data into the SPECTRA-155 from up to three up stream data sources. SDMTICLK[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while SDMTICLK[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). SDMTICLK[3:1] must be tied to the associated SDMTOCLK[3:1]. Inputs SDMTDAT[3:1] are sampled using the rising edge of the corresponding SDMTICLK[3:1] clock.
SS[16] SS[17] SS[18]	Input	D11 C11 B11	Reserved. Should be strapped low in this mode of operation.

Pin Name	Pin Type	PIN No.	Function
SS[19]/ SDMTDAT[1] SS[20]/ SDMTDAT[2] SS[21]/ SDMTDAT[3]	Input	A11 C10 B10	The serial data mode transmit data (SDMTDAT[3:1]) signals contain the data to be mapped into the SONET/SDH SPE. SDMTDAT[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while SDMTDAT[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3).). Payload bits are transmitted in the order in which they are provided by SDMTDAT. SONET/SDH serial word alignment is not maintained. Transport overhead and path overhead bytes are not included. In addition, the SPE fixed stuff columns are optionally included using the GAPFS bit in the D3MA Control register. SDMTDAT[3:1] are sampled using the rising edge of the associated SDMTICLK[3:1] clock.
SS[22] SS[23] SS[24] SS[25] SS[26]	Input	B9 C9 A8 D9 B8	Reserved. Should be strapped low in this mode of operation.
SS[27]/ SDMTOCLK[1] SS[28]/ SDMTOCLK[2] SS[29]/ SDMTOCLK[3]	Output	C8 A7 B7	The serial data mode transmit output clock (SDMTOCLK[3:1]) signals provide timing for up to three upstream external data sources (eg. HDLC controllers). SDMTOCLK[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while SDMTOCLK[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). When GAPFS bit in the corresponding D3MA Control register is set low, SDMTOCLK is nominally a 49.536 MHz clock generated by gapping a 51.84 MHz clock. When GAPFS bit is set high, SDMTOCLK is nominally a 48.384 MHz clock. For proper operation, SDMTOCLK[3:1] signals must be tied to the associated SDMTICLK[3:1].

Pin Name	Pin Type	PIN No.	Function
SS[30] SS[31]	Output	D8 C7	Reserved.
SS[32] SS[33] SS[34]	Input	A6 B6 C6	Reserved. Should be strapped low in this mode of operation.

Table 12 - Serial DS3 Mode (SMODE[2:0]=110)

Pin Name	Pin Type	PIN No.	Function
SS[0]/ DS3RICLK[1] SS[2]/ DS3RICLK[2] SS[3]/ DS3RICLK[3]	Input	D15 A16 C15	The DS3 receive input clocks (DS3RICLK[3:1]) are provided to the internal SPECTRA-155 DS3 desynchronizers. DS3RICLK[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3RICLK[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3RICLK expected to be nominally 44.928 MHz. DS3RICLK is gapped to generate the nominal 44.736 MHz DS3 clock provided on (DS3ROCLK).
SS[1]	Input	B16	Reserved. Should be strapped low in this mode of operation.
SS[4]/ DS3ROCLK[1] SS[5]/ DS3ROCLK[2] SS[6]/ DS3ROCLK[3]	Output	B15 A15 C14	The DS3 receive output clocks (DS3ROCLK[3:1] are used to update the DS3 received serial data streams at 44.736 MHz. DS3ROCLK[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3ROCLK[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3ROCLK is nominally 44.736 MHz and is generated by gapping DS3RICLK when the DS3_SEL52 bit in the SPECTRA-155 Data Mode Configuration register is set low. DS3ROCLK is generated by gapping an internal 51.84 MHz recovered line clock when the DS3_SEL52 bit is set high. DS3RDAT is updated on the falling edge of DS3ROCLK.

Pin Name	Pin Type	PIN No.	Function
SS[7]/ DS3RDAT[1] SS[8]/ DS3RDAT[2] SS[9]/ DS3RDAT[3]	Output	D13 B14 A14	The DS3 receive data (DS3RDAT[3:1]) output signals contain NRZ encoded DS3 bit streams. DS3RDAT[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3RDAT[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3RDAT is updated on the falling edge of DS3ROCLK.
SS[10] SS[11] SS[12]	Output	C13 D12 B13	Reserved.
SS[13]/ DS3TICLK[1] SS[14]/ DS3TICLK[2] SS[15]/ DS3TICLK[3]	Input	C12 B12 A12	The DS3 transmit input clocks (DS3TICLK[3:1]) are used to sample transmit DS3 data streams. DS3TICLK[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3TICLK[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3TICLK expected to be nominally 44.736 MHz. DS3TDAT is sampled using the rising or falling edge of DS3TICLK as selected using the DS3TICLKB bit in the SPECTRA-155 Clock control register.
SS[16]/ DS3RAIS[1] SS[17]/ DS3RAIS[2] SS[18]/ DS3RAIS[3]	Input	D11 C11 B11	The DS3 receive AIS (DS3RAIS[3:1]) signals force the assertion of DS3 AIS. When DS3RAIS is high, DS3 AIS is inserted on the corresponding DS3RDAT output. DS3RAIS[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3RAIS[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3RAIS is sampled using the rising edge of DS3ROCLK.

Pin Name	Pin Type	PIN No.	Function
SS[19]/ DS3TDAT[1] SS[20]/ DS3TDAT[2] SS[21]/ DS3TDAT[3]	Input	A11 C10 B10	The DS3 transmit data (DS3TDAT[3:1]) signals contain the DS3 streams to be mapped into the SONET/SDH SPE. DS3TDAT[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3TDAT[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3TDAT is sampled using the rising or falling edge of DS3TICLK as selected using the DS3TICLKB bit in the SPECTRA-155 Clock control register.
SS[22] SS[23] SS[24] SS[25] SS[26]	Input	B9 C9 A8 D9 B8	Reserved. Should be strapped low in this mode of operation.
SS[27]	Output	C8	Reserved.
SS[28] SS[29] SS[30] SS[31]	Output	A7 B7 D8 C7	Reserved.
SS[32]/ DS3TAIS[1] SS[33]/ DS3TAIS[2] SS[34]/ DS3TAIS[3]	Input	A6 B6 C6	The DS3 transmit AIS (DS3TAIS[3:1]) signals force the assertion of DS3 AIS. When DS3TAIS is high, DS3 AIS is inserted on the corresponding DS3TDAT input. DS3TAIS[1] corresponds to the STS-1 (STM-0/AU3) #1 stream of an STS-3 (STM-1/AU3) while DS3TAIS[3] corresponds to the STS-1 (STM-0/AU3) #3 stream of an STS-3 (STM-1/AU3). DS3TAIS is sampled using the rising edge of DS3TICLK.

Table 13 - Microprocessor Interface Signals (25)

Pin Name	Pin Type	PIN No.	Function
INTB	OD Output	H4	The active low, open drain interrupt (INTB) signal is asserted when an event is detected on any of the SPECTRA-155 maskable interrupt sources.
A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	K2 K3 K4 J1 J2 J3 H2 J4 H3 G1	The address bus (A[9:0]) selects specific registers during accesses.
ALE	Input	F3	The address latch enable (ALE) signal latches the address bus (A[9:0]) when low. This allows the SPECTRA-155 to be interfaced to a multiplexed address/data bus. The address latches are transparent when ALE is high. The ALE input has an integral pull up resistor.
MBEB	Input	G2	The active low Motorola bus enable (MBEB) signal configures the SPECTRA-155 for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the SPECTRA-155 is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.
CSB	Input	F2	The active low chip select (CSB) signal is asserted during all register accesses.

Pin Name	Pin Type	PIN No.	Function
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	N2 M4 N1 M3 M2 L2 L3 K1	The bidirectional data bus, D[7:0], is used during SPECTRA-155 read and write accesses.
RDB/ E	Input	G3	The active low read enable (RDB) signal is low during a SPECTRA-155 read access. The SPECTRA-155 drives the D[7:0] bus with the addressed register's contents while RDB and CSB are low. The active high external access signal (E) is set high during SPECTRA-155 register access while in Motorola bus mode.
WRB/ RWB	Input	F1	The active low write strobe (WRB) signal is low during a SPECTRA-155 write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. The read/write select signal (RWB) selects between SPECTRA-155 register read and write accesses while in Motorola bus mode. The SPECTRA-155 drives the data bus D[7:0] with the contents of the addressed register while CSB is low and RWB and E are high. The contents of D[7:0] are clocked into the addressed register on the falling E edge while CSB and RWB are low.
RSTB	Schmitt TTL Input	E19	The active low reset (RSTB) signal is low to provide an asynchronous reset to the SPECTRA-155. RSTB is a Schmitt triggered input with an integral pull-up resistor. The minimum reset assertion time is typically less than 100 nS.

Table 14 - Miscellaneous Interface Signals (11)

Pin Name	Pin Type	PIN No.	Function
TATP RATP	Analog	W17 Y17	Two analog test points (TATP, RATP) are provided for production test purposes. These pins must be connected to ground during normal operation.
SCPO[1] SCPO[0]	Tristate Output	B5 A5	The control port (SCPO[1:0]) provides two drive points for controlling auxiliary devices. The signal levels on this output port correspond to the bit values contained in the SPECTRA-155 Output Port register. SCPO[1:0] can be tristate using the TRIS_OHB input and the SCPO_TS bit in the SPECTRA-155 Output Control Port register. On reset, these outputs will be tristate if TRIS_OHB is low.
SCPI[1] SCPI[0]	Input Input	E1 F4	The status port (SCPI[1:0]) is used to monitor the operation of auxiliary devices. An interrupt may be generated when state changes are detected in the monitored signals. State changes and the real-time signal levels on this port are available in the Input SPECTRA-155 Input Port Status/Value register. Each of the inputs contains an internal pull up resistor.
TCK	Input	D19	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	D20	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	E17	When the SPECTRA-155 is configured for JTAG operation, the test data input (TDI) signal carries test data into the SPECTRA-155 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.

Pin Name	Pin Type	PIN No.	Function
TDO	Tristate Output	D18	The test data output (TDO) signal carries test data out of the SPECTRA-155 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	E18	The active low test reset (TRSTB) signal provides an asynchronous SPECTRA-155 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

Table 15 - Power Signals (89)

Pin Name	Pin Type	PIN No.	Function
VDD[29:0]	Power	B2, B3, B18, B19, C2, C3, C18, C19, D4, D7, D10, D14, D17, G4, G17, K17, L4, P4, P17, U4, U7, U17, V2, V3, V18, V19, W2, W3, W18, W19	The power pins should be connected to a well decoupled +5 V in common with the analog power pins.

Pin Name	Pin Type	PIN No.	Function
VSS[28:0]	Ground	A1, A2, A3, A9, A10, A13, A18, A19, A20, B1, B20, C1, C20, H1, J20, K20, L1, M1, N20, V1, V20, W1, W20, Y1, Y2, Y3, Y18, Y19, Y20	The ground pins should be connected to GND in common with the analog ground pins.
TAVD1	Power	U9	Transmit analog +5V power. This pin powers the CSU and the PECL bandgap.
TAVS1	Ground	W8	Transmit analog ground.
TAVD2	Power	V8	Transmit analog +5V power. This pin powers the CSU.
TAVS2	Ground	Y7	Transmit analog ground.
TAVD3	Power	U10	Transmit analog +5V power. This pin powers the TRCLK+/- PECL cell.
TAVS3	Ground	V9	Transmit analog ground.

Pin Name	Pin Type	PIN No.	Function
RAVD1	Power	W15	Receive analog +5V power. This pin powers the CRU bandgap.
RAVS1	Ground	V15	Receive analog ground.
RAVD2	Power	U15	Receive analog +5V power. This pin powers the CRU.
RAVS2	Ground	V16	Receive analog ground.
RAVD3	Power	V11	Receive analog +5V power. This pin powers the ALOS+/- and RXD+/- PECL cells.
RAVS3	Ground	W13	Receive analog ground.
RAVD4	Power	V13	Receive analog +5V power. This pin powers the RRCLK+/- PECL cell.
RAVS4	Ground	U13	Receive analog ground.
QAVD1	Analog Power	Y15	The power pins for the analog core. QAVD1 should be connected to analog +5V.
QAVS1	Analog Ground	V14	The ground pins for the analog core. QAVS1 should be connected to analog GND.
QAVD2	Analog Power	Y10	The power pins for the analog core. QAVD2 should be connected to analog +5V.
QAVS2	Analog Ground	W10	The ground pins for the analog core. QAVS2 should be connected to analog GND.
QAVD3	Analog Power	V10	The power pins for the analog core. QAVD2 should be connected to analog +5V.

Pin Name	Pin Type	PIN No.	Function
NC1		V6,	Reserved. Must not be connected.
NC2		V5,	
NC3		C17,	
NC4		W7,	
NC5		V7,	
NC_A		U14,	
NC_B		U11,	
NC_C		Y12,	
NC_D		Y11,	
NC_E		Y8,	
NC_F		Y13	

Notes on Pin Description:

1. All SPECTRA-155 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except: the ALOS+/-, TRCLK+/-, RXD+/-, and RRCLK+/- inputs which operate at pseudo-ECL (PECL) logic levels.

2. The SPECTRA-155 digital outputs and bidirectionals which have 2 mA drive capability are: RAD, B3E[3:1], RALM[3:1], RPOH[3:1], RPOHFP[3:1], RFP, LOF, SALM, LOS_RRCPFP, ROHCLK, RLDCLK, ROH, RLD, RLOW, RSUC, RSLDCLK, ROWCLK, RSLD, RSOW, LAIS_RRCPDAT, LRDI_RRCPCLK, RTOHFP, RTOHCLK, RTOH, TOWCLK, TLDCLK, TTOHCLK, TOHCLK, TSLDCLK, TTOHFP, TFP, TPOHFP[3:1], and SCPO[1:0].

   The SPECTRA-155 digital outputs and bidirectionals which have 4 mA drive capability are: TDO, RPOHCLK[3:1], RXC, RCLK, TCLK, D[7:0], INTB, TPOHCLK[3:1], SS[31:27], SS[12:2] and SS[0].

   The SPECTRA-155 digital outputs and bidirectionals which have 8 mA drive capability are: TXDN, TXDP and TXC.

3. Inputs TRIS_OHB, SCPI[1:0], ALE, MBEB, RSTB, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VSS, TAVS, RAVS and QAVS ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage to the SPECTRA-155.

5. The VDD, TAVD, RAVD and QAVD power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage to the SPECTRA-155.

6. The TAVD[3:1] and RAVD[4:1] pins provide power to sensitive analog circuitry in the SPECTRA-155. These signals should be connected to the PCB VDD power plane at a point where the supply is clean and as free as possible of digitally induced switching noise. In a typical system, TAVD and RAVD should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system VDD enters the PCB. In some systems a clean VDD supply cannot be readily obtained, and RAVD and TAVD may require separate regulation or filtering as described in the Operations section.

7. Each TAVD and RAVD pin should be separately decoupled using ceramic decoupling capacitors located as close as possible to the SPECTRA-155.

8. The TAVS[3:1] and RAVS[4:1] pins provide the ground return path for sensitive analog circuitry in the SPECTRA-155. These signals should be connected to the PCB ground plane at a point where the ground is clean and as free as possible of digital return currents. In a typical system, TAVS and RAVS should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system ground reference enters the PCB.

9. Do not exceed 20 mA of current on any I/O pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.

10. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

11. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

12. Ensure that all digital power is applied simultaneously, and applied before or simultaneously with the analog power. Refer to the Power Sequencing description in the Operations section.

13. Reserved Input pins must be strapped low. Failure to connect these pins may cause malfunction or damage to the SPECTRA-155.

14. Reserved Output pins must be left unconnected. Connecting these pins may cause malfunction or damage to the SPECTRA-155.

15. In byte and nibble datacom modes, DMTICLK must be shorted to DMTOCLK. The external capacitance must not exceed 30pF.

16. In serial datacom mode, SDMTICLK must be shorted to SDMTOCLK. The external capacitance must not exceed 30pF.

17. In nibble datacom mode, TCLK must be shorted to DMTMSN. The external capacitance must not exceed 30pF.

9 FUNCTIONAL DESCRIPTION

9.1 Receive Line Interface

The Receive Line Interface block performs clock and data recovery and performs serial to parallel conversion. The clock and data recovery unit can be bypassed using primary inputs to allow interworking the SPECTRA-155 with an external CRU.

9.1.1 Clock Recovery Unit (CRU)

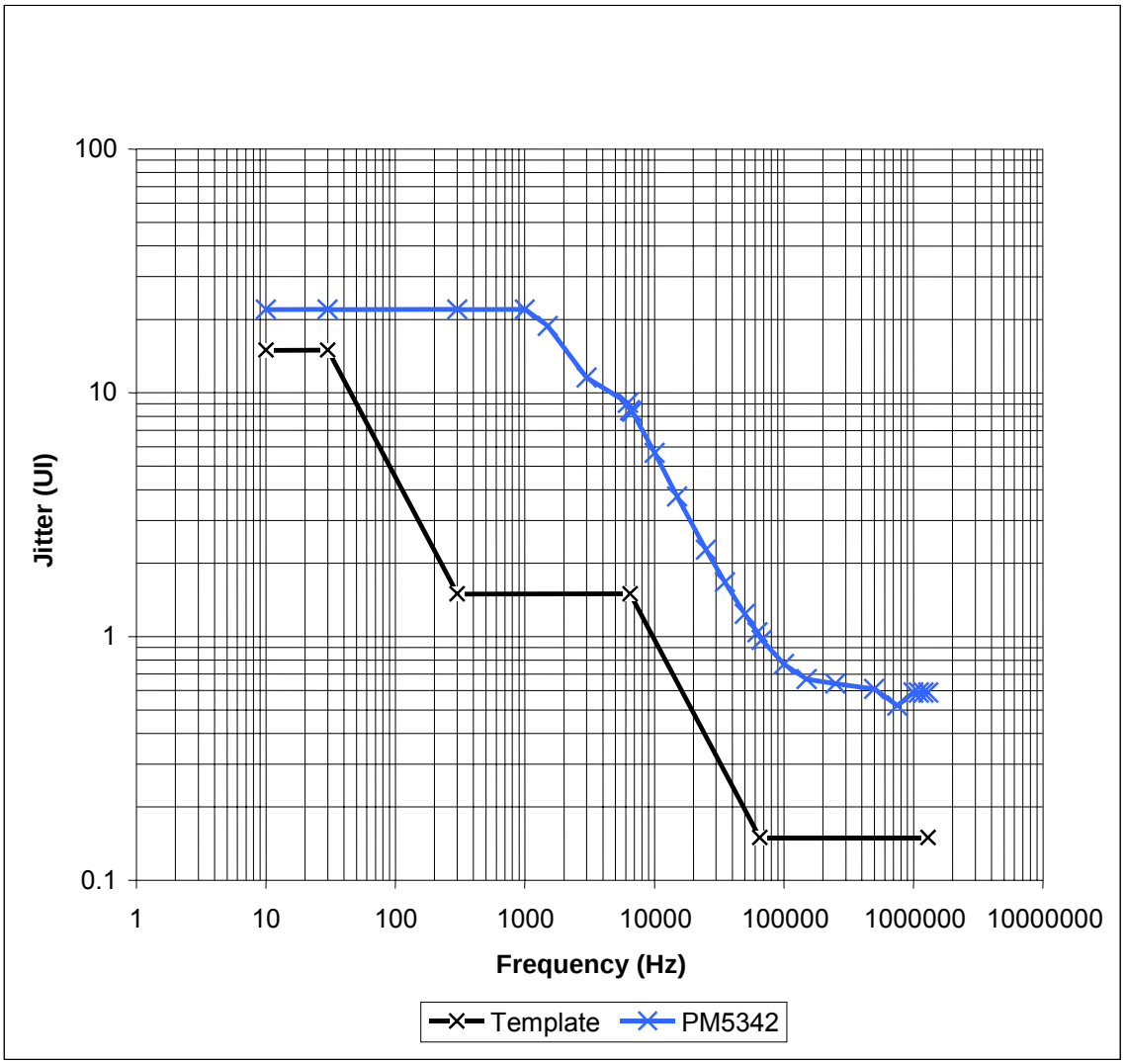
The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET/SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit will continue to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit can be configured to utilize reference clocks at 6.48 or 19.44 MHz. The clock recovery unit also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, RRCLK+/- (TRCLK+/-). When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the RRCLK+/- (TRCLK+/-) reference accuracy in the case of a loss of signal condition. In applications that are required to meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20 ppm. When not loop timed, the RRCLK+/- (TRCLK+/-) accuracy may be relaxed to +/-50 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET/SDH data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by GR-253-CORE as shown below.

Figure 17 - SPECTRA-155 Typical Jitter Tolerance at 155 Mbit/s



Note that for frequencies below 300 Hz the jitter tolerance is greater than 15 UIpp; 15 UIpp is the maximum jitter tolerance of the test equipment. The HP SDX1155B optical module was used in jitter tolerance testing.

9.1.2 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial SONET/SDH stream to a byte serial stream. The SIPO searches for the

SONET/SDH framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

9.2 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) block processes the section overhead (regenerator section) of the receive incoming stream. It can be configured to process an STS-1 (STM-0/AU3), or STS-3/3c (STM-1/AU3/AU4) data stream.

The RSOP block optionally descrambles the received data and extracts the data communication channel, order wire channel and user channel from the section overhead, and provides them as lower rate bit serial outputs (RSLD, RSOW, RSUC) together with associated clock signals (RSLDCLK, and ROWCLK). The complete descrambled SONET/SDH data stream is output by the RSOP in byte serial format. Line AIS is inserted in the receive data stream using input RLAIS or, optionally, automatically when loss-of-signal, loss-of-frame, section trace or loss-of-signal events occur. The automatic insertion of receive line AIS is controlled by the SPECTRA-155 Receive Line AIS Control Register.

Out-of-frame (OOF), loss-of-frame (LOF), and loss-of-signal (LOS) state outputs are provided and section level bit-interleaved parity errors are accumulated. A maskable interrupt is activated by state transitions on the SALM, LOF, or LOS outputs, or by a single B1 error event. Microprocessor readable registers are provided that allow accumulated B1 errors to be read out at intervals of up to one second duration.

The RSOP block frames to the data stream by operating with an upstream pattern detector (the Serial to Parallel Converter block) that searches for occurrences of the framing pattern (A1, A2) in the bit serial data stream. Once the serial to parallel converter has found byte alignment, the RSOP block monitors for the next occurrence of the framing pattern 125µs later. The block declares frame alignment when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the last A2 byte are seen error-free. Depending upon the operating mode, the first algorithm examines 2 bytes (A1,A2) in STS-1 (STM-0/AU3) mode, or 6 bytes (A1A1A1,A2A2A2) in STS-3/3c (STM-1/AU3/AU4) mode. The second algorithm examines only the first occurrence of A1 and the first four bits of the last occurrence of A2 in the sequence, regardless of the operating mode. Once in frame, the RSOP block monitors the framing pattern sequence and declares OOF when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the operating mode selected the first algorithm examines all 2, or 6 framing bytes for bit errors each frame, while the second algorithm examines only the A1 byte and the first four bits of the last A2 byte (i.e. 12 bits total) during each frame.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the serial to parallel converter which always examines all framing bits. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the SPECTRA-155 continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a mean time between OOF occurrences of 33 minutes in STS-1 (STM-0/AU3) mode and 26 seconds in STS-3/3c (STM-1/AU3/AU4) mode. The second algorithm provides a mean time between OOF occurrences of 103 minutes, regardless of operating mode.

The RSOP block provides descrambled data and frame alignment indication signals for use by the Receive Line Overhead Processor.

9.3 Receive Section Trace Buffer

The receive portion of the SONET/SDH Section Trace Buffer captures the received section trace identifier message (J0 byte) into microprocessor readable registers. It contains two pages of trace message memory. One is designated the capture page and the other the expected page. Section trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message. If enabled, an interrupt is generated when the accepted message changes from matching to mismatching the expected message and vice versa. If the current message differs from the previous message for eight consecutive messages, the received message is declared unstable. The received message is declared stable when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, line AIS may be inserted in the received stream when the receive message is in the mismatched or unstable state.

The length of the section trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the section trace buffer synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the section trace buffer synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the section trace message to be

appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

In addition, mode 2 section trace identifier operation is supported. For mode 2 support, a stable message is declared when forty eight of the same section trace identifier message (J0) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

9.4 Receive Line Overhead Processor

The Receive Line Overhead Processor block (RLOP) processes the line overhead (multiplexer section) of a received SONET/SDH data stream. It can be configured to process an STS-1 (STM-0/AU3), or an STS-3/3c (STM-1/AU3/AU4) stream.

The SONET/SDH frame alignment is indicated by the Receive Section Overhead Processor. The RLOP extracts the line data communication channel, line order wire channel and automatic protection switch channel from the line overhead, and provides them as lower rate bit serial outputs (RLD, RLOW, ROH) together with associated clock signals (RLDCLK, ROWCLK, ROHCLK). Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The automatic protection switch bytes (K1, K2) are also extracted into the RASE Receive K1 Register and the RASE Receive K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE Receive K1/K2 Registers

The line level bit-interleaved parity (B2) is computed, and compared to the received B2 bytes. Line BIP-8 errors are accumulated in an internal counter. Registers are provided that allow accumulated line BIP-8 errors to be read out at intervals of up to one second duration.

Signal fail (SF) and signal degrade (SD) threshold crossing alarms are detected and indicated using internal register bits. The bit error rates associated with the SF and SD alarms are programmable over a range of 10^{-3} to 10^{-9}. The

Receive APS, Synchronization Extractor and Bit Error (RASE) block extracts the Automatic Protection Switch (APS) bytes (K1 and K2), extracts the Synchronization Status byte (Z1/S1), and processes the Line BIP-8 (B2) events.

The received line BIP-8/24 error detection code (B2) byte is based on the line overhead and SPE of the receive stream. The line BIP code is a bit interleaved parity calculation using even parity, and the calculated BIP code is compared with the BIP code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 BIP/frame x 8000 frames/second) bit errors can be detected per second for STS-3/3c (STM-1/AU3/AU4) rate and 64000 (8 BIP/frame x 8000 frames/second) for STS-1 (STM-0/AU3) rate.

The line remote error indication (REI) byte (M1) is extracted and accumulated in an internal counter. Registers are provided that allow accumulated line REI events to be read out at intervals of up to one second duration. Bits 2 through 8 of the Z2/M1 byte are used for the line REI function. For STS-1 (STM-0/AU3) streams, the line REI byte has 9 legal values (namely 00H - 08H) representing 0 to 8 line REI events. For STS-3/3c (STM-1/AU3/AU4) streams, the line REI byte has 25 legal values (namely 00H - 18H) representing 0 to 24 line REI events. Illegal Z2/M1 values are interpreted as zero errors.

An interrupt output is provided that may be activated by declaration or removal of line AIS, line RDI, protection switching byte failure alarm, a change of APS code value, a single B2 error event, or a single line REI event. Each interrupt source is individually maskable.

9.5 Receive Transport Overhead Extract

The Receive Transport Overhead Access block (RTOH) extracts the entire receive transport overhead on the RTOH, along with the 5.184 MHz or 1.728 MHz transport overhead clock, RTOHCLK, and the transport overhead frame position signal, RTOHFP, allowing identification of the bit positions in the transport overhead stream.

9.6 Ring Control Port

The Transmit and Receive Ring Control Ports provide bit serial access to section and line layer alarm and maintenance signal status and control. These ports are useful in ring-based add drop multiplexer applications where alarm status and maintenance signal insertion control must be passed between separate SPECTRA-155s (possibly residing on separate cards). Each ring control port consists of three signals: clock, data and frame position. It is intended that the clock, data and frame position outputs of the receive ring control port are connected directly to the clock, data and frame position inputs of the transmit

ring control port on the mate SPECTRA-155. The alarm status and maintenance signal control information that is passed on the ring control ports consists of

- Filtered APS (K1 and K2) byte values
- Change of filtered APS byte value status
- Protection switch byte failure alarm status
- Change of protection switch byte failure alarm status
- Insert the line RDI maintenance signal in the mate SPECTRA-155
- Insert the line AIS maintenance signal in the mate SPECTRA-155
- Insert line REI information in the mate SPECTRA-155.

The same APS byte values must be seen for three consecutive frames before being shifted out on the receive ring control port. The change of filtered APS byte value status is high for one frame when a new, filtered APS value is shifted out.

The protection switch byte failure alarm bit position is high when after twelve consecutive frames, no three consecutive frames contain identical K1 bytes have been received. The bit position is set low when three consecutive frames containing identical K1 bytes have been received. The change of protection switch byte failure alarm status bit position is set high for one frame when the alarm state changes.

The insert line RDI bit position is set high under register control, or when loss of signal, loss of frame, or line AIS alarms are declared. The insert line AIS bit position is set high under register control only.

The insert line REI bit positions are high for one bit position for each detected B2 bit error. Up to 24 line REIs may be indicated per frame for an STS-3/3c (STM-1/AU3/AU4) signal.

9.7 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring. In tandem path origination mode, RPOP generates an IEC based on its received path BIP-8 errors and inserts the tandem path data link. In tandem path termination mode, RPOP accumulates incoming error counts (IEC) and extracts the tandem

connection data link. Optionally, the RPOP will overwrite the fixed stuff columns in a tributary mapped SPE (VC) with zeros or null pointer indications in the NPI bytes.

9.7.1 Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-3c (STM-1/AU4) or STS-1 (STM-0/AU3) stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown below:

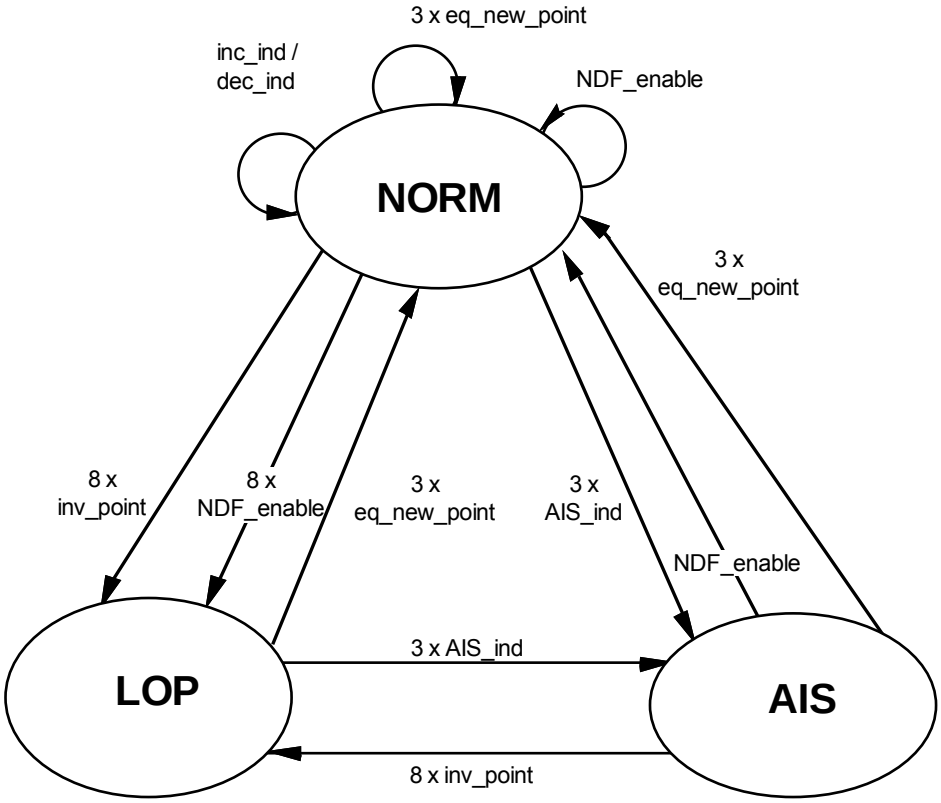
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 18 - Pointer Interpretation State Diagram



The following events (indications) are defined

norm_point : disabled NDF + ss + offset value equal to active offset

NDF_enable: enabled NDF + ss + offset value in range of 0 to 782

AIS_ind: H1 = 'hFF, H2 = 'hFF

inc_ind: disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago

dec_ind: disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago

inv_point: not any of above (i.e., not norm_point, and not NDF_enable, not AIS_ind, and not inc_ind and not dec_ind)

new_point:	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted
dec_req:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted
Note 1	active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
Note 2	enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
Note 3	disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
Note 4	the remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.
Note 5	ss bits are unspecified in SONET and has bit pattern 10 in SDH
Note 6	the use of ss bits in definition of indications may be optionally disabled.
Note 7	the requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
Note 8	new_point is also an inv_point.
Note 9	LOP is not declared if all the following conditions exist: the received pointer is out of range (>782), the received pointer is static, the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.

When the received pointer returns to an in-range value, the SPECTRA-155 will interpret it correctly.

Note 10 LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

Note 11 For the purposes of 8xNDF_enable only, the requirement of the pointer to be within the range of 0 to 782 may be optionally disabled.

The transitions indicated in the state diagram are defined as follows:

inc_ind/dec_ind: offset adjustment (increment or decrement indication)

3 x eq_new_point: three consecutive equal new_point indications

NDF_enable: single NDF_enable indication

3 x AIS_ind: three consecutive AIS indications

8 x inv_point: eight consecutive inv_point indications

8 x NDF_enable eight consecutive NDF_enable indications

Note 1 the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

Note 2 3 x new_point takes precedence over 8 x inv_point and resets the inv_point counter.

Note 3 all three offset values received in 3 x eq_new_point must be identical.

Note 4 "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter detects loss of pointer (LOP) in the incoming STS-1 (STM-0/AU3) or STS3c stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the DROP bus when LOP is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in

DROP bus G1 byte is set to indicate the LOP alarm to the TPOP in a remote SPECTRA-155.

The Pointer Interpreter detects path AIS in the incoming STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the DROP bus when AIS is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the PAIS alarm to the TPOP in a remote SPECTRA-155.

The Pointer Interpreter detects loss of pointer – concatenated (LOPC) in the STS3c stream. LOPC is declared on entry to the LOPC_state as a result of eight consecutive pointers with values other than concatenation indications (‘b1001 xx 1111111111). Path AIS is optionally inserted in the DROP bus when LOPC is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the LOP alarm to the TPOP in a remote SPECTRA-155.

The Pointer Interpreter detects path AIS – concatentated in the incoming STS-3c stream. PAISC is declared on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the DROP bus when AISC is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA-155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the PAIS alarm to the TPOP in a remote SPECTRA-155.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

9.7.2 Multiframe Framer

The multiframe alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, 11 in the two least significant bits. If an unexpected value is detected, the primary multiframe will be kept, and a second multiframe process will, in parallel, check for a phase shift. The primary process will enter out of multiframe state (OOM). A new multiframe alignment is chosen, and OOM state is exited when four consecutive correct multiframe patterns are detected. Loss of multiframe (LOM) is declared after residing in the OOM state for eight frames without re-alignment. A new multiframe alignment is chosen, and LOM state is exited when four consecutive correct multiframe patterns are detected.

9.7.3 Error Monitoring

Three 16-bit counters are provided to accumulate path BIP-8 errors (B3), path remote error indications (REI), and tandem path incoming error counts (IEC). The contents of the counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame. BIP-8 errors are selectable to be counted as bit errors or as block errors via register bits. When in-band error reporting is enabled, the error count is inserted into the path status byte (G1) of the DROP bus. Path REIs are detected by extracting the 4-bit path REI field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors. IECs are detected by extracting the 4-bit IEC field from the tandem path maintenance byte (Z5). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five/ten consecutive frames. PRDI is set low when bit 5 is low for five/ten consecutive frames. Auxiliary RDI alarm is detected by extracting bit 6 of the path status byte. The Auxiliary RDI alarm is indicated when bit 6 is set high for five/ten consecutive frames. The Auxiliary RDI alarm is removed when bit 6 is low for five/ten consecutive frames. The Enhanced RDI alarm is detected when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in

bits 5,6,7 of the path status byte indicates the same non error codepoint for five/ten consecutive frames.

9.7.4 Path Overhead Extract

Path Overhead bytes are extracted, serialized and output the Path Overhead bytes on output RPOH. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) on RPOH. The path overhead clock, RPOHCLK is nominally a 576 KHz clock. RPOH and RPOHFP are updated with timing aligned to RPOHCLK.

9.7.5 Tandem Connection Originate

The RPOP updates the path BIP byte (B3) and the tandem connection maintenance byte (Z5) on the DROP bus when RPOP originates a tandem connection. Incoming BIP-8 errors are counted and encoded in the incoming error count field of the Z5 byte. The tandem connection data link is placed into the data link field of the Z5 byte. The B3 byte is updated to reflect the changes made to the Z5 byte. When LOP or path AIS alarms are declared, the incoming error count field of the Z5 byte is set to indicate incoming signal failure (ISF = 'b1111). The H1, H2 pointer bytes are frozen to the previous active offset. Path overhead and payload bytes are set to all ones. The tandem connection data link remains active and the path BIP-8 byte remains valid.

9.7.6 Receive Alarm Port

Received path BIP errors and path remote defect indications (RDI) are communicated to the transmit path overhead processor (TPOP) in a mate SPECTRA-155 via the receive alarm port. The port carries the count of received path BIP errors. Insertion of path AIS in the DROP bus is reported in the alarm port and will trigger the remote TPOP to signal path RDI in the transmit stream.

The Receive alarm port also reports the APS bytes (K1, K2) that are placed on the transmit stream of the SPECTRA-155. In conjunction with the transmit alarm port of a mate SPECTRA-155, the working SPECTRA-155 can control the APS bytes of the protection SPECTRA-155.

9.8 Receive Path Trace Buffer

The receive portion of the SONET/SDH Path Trace Buffer (SPTB) captures the received path trace identifier message (J1 bytes) into microprocessor readable registers. It contains two pages of trace message memory. One is designated the capture page and the other the expected page. Path trace identifier data bytes from the receive stream are written into the capture page. The expected

identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message. If enabled, an interrupt is generated when the accepted message changes from matching to mismatching the expected message and vice versa. If the current message differs from the previous message the unstable counter is incremented by one. When the unstable count reaches eight, the received message is declared unstable. The received message is declared stable and the unstable counter reset, when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, path AIS may be inserted in the DROP bus when the receive message is in the mismatched or unstable state.

The length of the path trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the SPTB synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the SPTB synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the path trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

In addition, mode 2 path trace identifier operation is supported. For mode 2 support, a stable message is declared when forty eight of the same section trace identifier message (J1) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

The path signal label (PSL) found in the path overhead byte (C2) is processed. An incoming PSL is accepted when it is received unchanged for five consecutive frames. The accepted PSL is compared with the provisioned value. The PSL match/mismatch state is determined as follows:

Table 16 - Path Signal Label match/mismatch state table.

Expected PSL	Accepted PSL	PSLM State
00	00	Match
00	01	Mismatch
00	X ≠ 00	Mismatch

Expected PSL	Accepted PSL	PSLM State
01	00	Mismatch
01	01	Match
01	X ≠ 01	Match
X ≠ 00, 01	00	Mismatch
X ≠ 00, 01	01	Match
X ≠ 00, 01	X	Match
X ≠ 00, 01	Y	Mismatch

Each time an incoming PSL differs from the one in the previous frame, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once on the errored PSL and again on the first error-free PSL. The incoming PSL is considered unstable, when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive frames.

9.9 Receive Telecombus Aligner

The Receive Telecombus Aligner (RTAL) block takes the payload data from an STS-1 (STM-0/AU3) stream from the Receive Path Overhead Processor and inserts it in a Telecombus DROP bus. It aligns the frame of the received STS-1 (STM-0/AU3) stream to the frame of the DROP bus. In an STS-3c (STM-1/AU4) system, the first STS-1 (STM-0/AU3) in a STS-3c (STM-1/AU4) stream is processed by an RTAL in master mode controlling two RTALs in slave mode. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the receive stream and that of the DROP bus.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the receive data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus. DROP bus pointer justification events are indicated and are accumulated in the Performance Monitor (PMON) block. Large differences between the number and type of received pointer justification events as indicated by the RPOP block, and pointer justification events generated by the RTAL block may indicate network synchronization failure.

When the RPOP block detect a loss of multiframe, the RTAL may optionally insert all ones in the tributary portion of the SPE. The path overhead column and the fixed stuff columns are unaffected.

The RTAL may optionally insert the tributary multiframe sequence and clear the fixed stuff columns. The tributary multiframe sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a synchronous payload envelope (virtual container) may optionally be over-written all-zeros in the fixed stuff bytes.

9.9.1 Elastic Store

The Elastic Store perform rate adaptation between the receive data stream and the DROP bus. The entire received payload, including path overhead bytes, is written into in a first-in-first-out (FIFO) buffer at the receive byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Receive pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the DROP bus rate by the Pointer Generator. Analogously, pointer justifications on the DROP bus are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the DROP bus for three frames to alert downstream elements of data corruption.

9.9.2 Pointer Generator

The Pointer Generator generates the DROP bus pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the DROP bus STS-3 (STM-1/AU3) or STS-1 (STM-0/AU3) stream. The algorithm can be modeled by a finite state machine. Within the pointer generator algorithm, five states are defined as shown below:

NORM_state (NORM)

AIS_state (AIS)

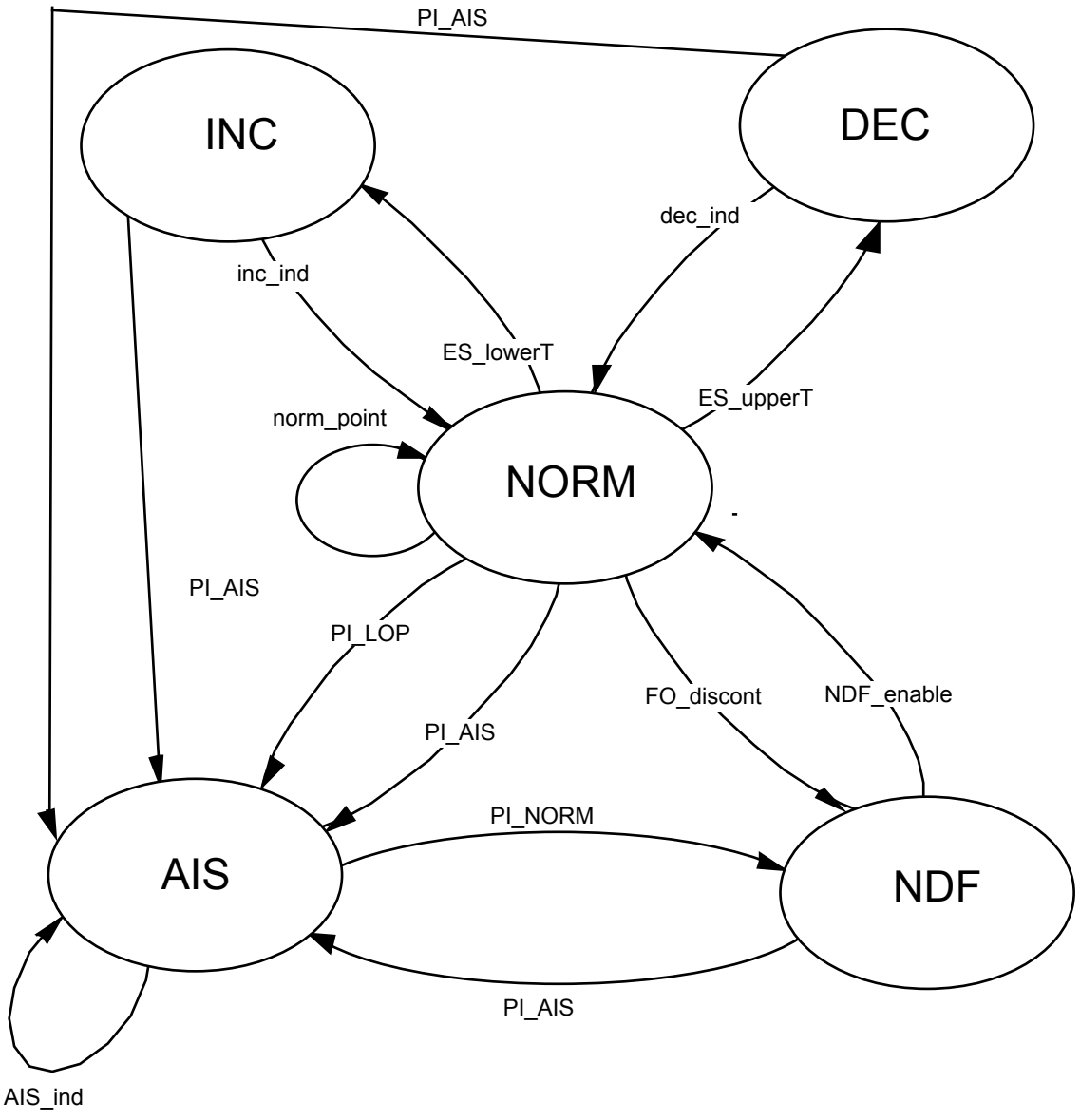
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive Path Overhead Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 19 - Pointer Generation State Diagram



The following events, indicated in the state diagram (Figure 18), are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note 1 A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Note 1 active offset is defined as the phase of the SPE (VC).

Note 2 the ss bits are undefined in SONET, and has bit pattern 10 in SDH

Note 3 enabled NDF is defined as the bit pattern 1001.

Note 4 disabled NDF is defined as the bit pattern 0110.

9.9.3 Tandem Connection Alarm

When terminating a tandem connection, the Tandem Connection Alarm block converts Incoming Signal Failure code (ISF) in the tandem connection maintenance byte (Z5) to path AIS in the DROP bus. The ISF code can be optionally filtered so that path AIS is only inserted after detecting ISF in three consecutive frames. Similarly, path AIS is removed after three consecutive frames where ISF is not present. When filtering is disabled, path AIS is immediately inserted on detection on ISF and removed on detection of inactive ISF code.

A piece of tandem connection originating equipment should signal incoming signal failure by setting the IEC field and the payload bytes to all ones. A piece of tandem connection terminating equipment should detect ISF by only examining the IEC field for all ones. If the upstream tandem connection originating equipment inserts a malformed, non-compliant ISF condition where the payload bytes are not all ones, the SPECTRA-155 toggles in and out of the ISF state. However, in real systems, this behaviour should not be observed because the upstream tandem connection originating equipment inserts a standards compliant ISF condition.

9.10 DS3 Mapper DROP Side

The DS3 Mapper DROP Side (D3MD) block demaps a DS3 signal from an STS-1 (STM-0/AU3) payload. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. The asynchronous DS3 mapping is shown below:

Table 17 - Asynchronous DS3 mapping to STS-1 (STM-0/AU3).

J1	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
STS	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
POH	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I
	2 x 8R	RRCIIIII	25 x 8I	2 x 8R	CCRRRRRR	26 x 8I	2 x 8R	CCRROORS	26 x 8I

R: Fixed Stuff bit - set to logic ‘0’ or ‘1’

C: Stuff Control bit - set to logic ‘1’ for stuff indication

S: Stuff Opportunity bit - when stuff control bit is ‘0’, stuff opportunity is I bit

O: Overhead communication channel

I: DS3 payload information

9.10.1 DS3 Demapper

The D3MD performs majority vote on the received C-bits. If 3 out of 5 C-bits are ‘1’s, the associated S bit is interpreted as a stuff bit. If 3 out of 5 C-bits are ‘0’s, the associated S bit is interpreted as an Information bit. The information bits are written to an elastic store and the Fixed Stuff bits (R) are ignored.

Given a LOS, LOF, LAIS, LOP, PAIS, path signal label mismatch (PSLM) or path signal label unstable (PSLU), path trace message mismatch (TIM) or path trace message unstable (TIU) condition, the D3MD ignores the STS-1 (STM-0/AU3) SPE and writes a DS3 AIS pattern to the elastic store. In addition, the desynchronization algorithm assumes a nominal ratio of data to stuff bits carried in the S bits (1 out of 3 S bits is assumed to be an information (data) bit). DS3 AIS is defined below:

Table 18 - DS3 AIS format.

X (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
X (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
P (p)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
P (p)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (0)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (1)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**
M (0)	**D**	F (1)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (0)	**D**	C (0)	**D**	F (1)	**D**

- valid M-frame alignment bits (M-bits), M-subframe alignment bits (F-bits), and parity bit of the preceding M-frame (P-bits). The two P-bits are identical, either both are zeros or ones.

- all the C-bits in the M-frame are set to zeros

- the X-bits are set to ones
- the information bit (84 Data bits with repeating sequence of 1010..)

9.10.2 Elastic Store

The elastic store block is provided to compensate for frequency differences between the DS-3 stream extracted from the STS-1 (STM-0/AU3) SPE and the incoming DS3RICLK. The DS3 Demapper extracts I bits from the STS-1 (STM-0/AU3) SPE and writes the bits into a 128 bit (16 byte) elastic store. Eight bytes are provided for SONET/SDH overhead (3 bytes for TOH, 1 byte for a positive stuff, 1 byte for POH) and DS3 reserve stuffing bits (2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte). The remaining 8 bytes are provided for path pointer adjustments.

Data is read out of the Elastic Store using a divide by 8 version of the input DS3RICLK clock. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

9.10.3 DS3 Desynchronizer

The Desynchronizer monitors the Elastic Store level to control the de-stuffing algorithm to avoid overflow and underflow conditions. The Desynchronizer assumes either a 51.84 MHz clock (provided internally) or a 44.928 MHz clock (provided via input DS3RICLK).

When using a 44.928 MHz DS3RICLK clock, the DS3 clock is generated using a fixed 8 KHz interval. The 8KHz interval is subdivided into 9 rows. Each row contains either 621 or 622 clock periods. The DS3RICLK contains 624 pulses at 72KHz (9*8KHZ). To generate 621 pulses, a gap pattern of 207 clocks + 1 clock gap + 207 clocks + 1 clock gap + 207 clocks + 1 clock gap is used. To generate 622 pulses, a gap pattern of 207 clocks + 1 clock gap + 207 clocks + 1 clock gap + 208 clocks is used.

When using a 51.84 MHz DS3RICLK clock, the DS3 clock, DS3ROCLK is generated using similar gapping patterns. To generate 621 pulses per row, a gapping pattern of 63 * (7 clocks + 1 clock gap) + 36 * (5 clocks + 1 clock gap) is used. To generate 622 pulses per row, a gapping pattern of 63 * (7 clocks + 1 clock gap) + 35 * (5 clocks + 1 clock gap) + 6 clocks) is used.

The following table illustrates the gap patterns used to generate the desynchronized clock, DS3ROCLK under the normal, DS3 AIS, faster and slower status. The faster pattern is used to drain the elastic store to avoid overflows. The slower pattern is used to allow the elastic store to fill to avoid underflows.

Table 19 - DS3 desynchronizer clock gapping algorithm.

Row Number	Normal or DS3 AIS	Run Faster	Run Slower
1	621	621	621
2	621	621	621
3	622	622	622
4	621	621	621
5	621	622	621
6	622	622	621
7	621	621	621
8	621	622	621
9	622	622	621

9.11 DS3 Mapper ADD Side

The DS3 Mapper ADD Side (D3MA) block maps a DS3 signal into an STS-1 (STM-0/AU3) payload and compensate for any frequency differences between the incoming DS3 serial bit rate (DS3TICLK) and the available STS-1 (STM-0/AU3) SPE mapped payload capacity. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. Please refer to the D3MD block for a description of the DS3 mapping.

9.11.1 DS3 Serializer

Incoming high speed serial data is sampled on the DS3TDAT input, deserialized and written into the Elastic Store.

9.11.2 Elastic Store

The elastic store block is provided to compensate for frequency differences between the DS-3 stream (DS3TDAT) and the STS-1 (STM-0/AU3) SPE capacity. The DS3 Serializer writes data into the elastic store at the DS3TICLK/8 rate while data is read out at the stuffed STS-1 (STM-0/AU3) byte rate. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

The Elastic store is 128 bits (16 bytes) to allow for a fixed read/write pointer lag of 7 bytes (3 bytes for TOH, 1 byte for POH, 2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte). Four bytes are also added on either side for positive and negative threshold detection.

9.11.3 DS3 Synchronizer

The DS3 Synchronizer performs the mapping of the DS3 into the STS-1 (STM-0/AU3) SPE. The DS3 Synchronizer monitors the Elastic Store level to control the stuffing algorithm to avoid overflow (i.e. run faster) and underflow (i.e. run slower) conditions. The fill level of the elastic store is monitored and stuff opportunities in the DS3 mapping are used to center the Elastic Store. To consume a stuff opportunity, the five C-bits on a row are set to ones and the S bit is used to carry an DS3 information bit. When the S bit is not used to carry information, the C-bits on the row are set to zeros.

The DS3 synchronizer uses a fixed bit leaking algorithm which leaks 8 bits of phase buildup in 500 µs. The 8kHz STS-1 (STM-0/AU3) frame interval is subdivided into 9 rows. Each row contains one stuff opportunity. The following table illustrates the stuffing implementation where S means stuff bit and I means an information bit (DS3 data).

Table 20 - DS3 synchronizer bit stuffing algorithm.

Row Number	Normal or DS3 AIS	Run Faster	Run Slower
1	S	S	S
2	S	S	S
3	I	I	I
4	S	S	S
5	S	I	S
6	I	I	S
7	S	S	S
8	S	I	S
9	I	I	S

Under microprocessor control, the incoming DS3 stream can be overwritten with the framed DS3 AIS. When asserting DS3 AIS, a nominal stuff pattern is used as illustrated above. Please refer to the D3MD functional description section for a description of the DS3 AIS frame.

The D3MA outputs the STS-1 (STM-0/AU3) with the mapped DS3 onto an internal ADD bus for further processing by the Transmit Telecombus Aligner block.

9.12 Transmit Pointer Interpreter Processor

The Transmit Pointer Interpreter Processor (TPIP) block takes STS-1 (STM-0/AU3) SPE (VC3) data or STS-3c (STM-1/AU4) SPE (VC4) data from the ADD bus, interprets the pointer (H1, H2), indicates the J1 byte location and detects alarm conditions (PAIS).

The TPIP block allows the SPECTRA-155 to operate with Telecombus like back plane systems which do not indicate the J1 byte position. The TPIP block can be enabled using the DISJ1V1 bit in the SPECTRA-155 Path/Mapper Configuration register. When enabled, the TPIP takes a SONET/SDH stream from the System Side Interface block, processes the stream, identifies the J1 byte location and provides the stream to the corresponding Transmit Telecombus Aligner block.

9.13 Transmit Telecombus Aligner

The Transmit Telecombus Aligner (TTAL) block takes the STS-1 (STM-0/AU3) SPE (VC3) data from the ADD bus and aligns it to the frame of the transmit stream. In an STS-3c (STM-1/AU4) system, the first STS-1 (STM-0/AU3) (first third of VC4) in the stream is processed by an TTAL in master mode controlling two TTALs in slave mode. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the ADD bus and the transmit stream.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the ADD and the transmit stream are accommodated by pointer adjustments in the transmit stream.

The TTAL may optionally insert the tributary multiframe sequence and clear the fixed stuff columns. The tributary multiframe sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a synchronous payload envelope (virtual container) may optionally be over-written with all-zeros in the fixed stuff bytes.

9.13.1 Elastic Store

The Elastic Store block performs rate adaptation between the ADD bus and the transmit stream. The entire ADD bus payload, including path overhead bytes, is

written into in a first-in-first-out (FIFO) buffer at the ADD bus byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. ADD bus pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the transmit stream rate by the Pointer Generator block. Analogously, pointer justifications on the transmit stream are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests are made to the Pointer Generator block based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator block schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is inserted in the transmit stream for three frames to alert downstream elements of data corruption.

9.13.2 Pointer Generator

The Pointer Generator Block generates the transmit stream pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the transmit STS-3 (STM-1/AU3) or STS-1 (STM-0/AU3) stream. The algorithm is identical to that described in the Receive Telecombus Aligner block.

9.13.3 Tandem Connection Alarm

In terminating tandem connection termination equipment applications, the Tandem Connection Alarm block converts Incoming Signal Failure code (ISF) in the tandem connection maintenance byte (Z5) to path AIS in the transmit stream. The ISF code can be optionally filtered so that path AIS is only inserted after detecting ISF in three consecutive frames. Similarly, path AIS is removed after three consecutive frames where ISF is not present. When filtering is disabled, path AIS is immediately inserted on detection of ISF and removed on detection of inactive ISF code.

A piece of tandem connection originating equipment should signal incoming signal failure by setting the IEC field and the payload bytes to all ones. A piece of tandem connection terminating equipment should detect ISF by only examining the IEC field for all ones. If the upstream tandem connection originating equipment inserts a malformed, non-compliant ISF condition where the payload bytes are not all ones, the SPECTRA-155 toggles in and out of the ISF state. However, in real systems, this behaviour should not be observed

because the upstream tandem connection originating equipment inserts a standards compliant ISF condition.

9.14 Transmit Path Trace Buffer

The transmit portion of the SONET/SDH Path Trace Buffer (SPTB) sources the path trace identifier message (J1) for the Transmit Path Overhead Processor block. The length of the trace message is selectable between 16 bytes and 64 bytes. The SPTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transmit Path Overhead Processor block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, SPTB may be programmed to transmit null characters to prevent transmission of partial messages.

9.15 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, path overhead insertion, insertion of the synchronous payload envelope, insertion of path level alarm signals and path BIP-8 (B3) insertion. Path overhead insertion is disabled at intermediate tandem connection nodes.

9.15.1 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE (VC) of the outgoing STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) stream. The fixed stuff columns in the VC3 format may be optionally excluded from BIP calculations. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

9.15.2 Path REI Calculate

The Path REI Calculate Block accumulates path remote error indications on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the path REI bit positions of the path status (G1) byte. The path REI information is derived from path BIP-8 errors detected by the Receive Path Overhead Processor, RPOP. The asynchronous nature of these signals implies that more than eight path REI events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining path REIs are transmitted at the next opportunity. Alternatively, path REI can be accumulated from path REI counts reported on the transmit alarm

port when the local SPECTRA-155 is paired with a receive section of a remote SPECTRA-155. Far end block errors may be inserted under register control for diagnostic purposes. Optionally, path REI insertion may be disabled and the incoming G1 byte passes through unchanged to support applications where the received path processing does not reside in the local SPECTRA-155.

9.15.3 Transmit Alarm Port

Received path BIP errors and remote defect indications (RDI) from Receive Path Overhead Processors (RPOP) in a remote SPECTRA-155 is communicated to the local SPECTRA-155 via the transmit alarm port. When the port is enabled, BIP error counts and defect indications are inserted in the path REI and path RDI positions of the path status byte in the transmit stream.

The transmit alarm port also contains the APS bytes (K1, K2) of the mate working SPECTRA-155. In the protection SPECTRA-155, the APS bytes in the transmit stream may be sourced optionally, from the transmit alarm port.

9.15.4 Path Overhead Insert

The Path Overhead Insert Block provides a bit serial path overhead interface to the TPOP. Any, or all of the path overhead bytes may be sourced from, or modified by the bit serial path overhead stream, TPOH. The individual bits of each path overhead byte are shifted in using the TPOHCLK output. The TPOHFP output is provided to identify when the most significant bit of the Path Trace byte is expected on TPOH. The state of the TPOHEN input, together with an internal register, determines whether the data sampled on TPOH, or the default path overhead byte values are inserted in each STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) stream. For example, a high level on TPOHEN during the path label (C2) bit positions causes the eight values shifted in on TPOH to be inserted in the C2 byte position in the transmit stream. A low level on TPOHEN during the path signal label bit positions causes the default value ('h01) to be inserted. The path trace byte is optionally sourced from the Transmit Path Trace Buffer block.

During the B3 and H4 byte positions in the TPOH stream, a high level on TPOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TPOH causes the corresponding bit in the B3 or H4 byte to be inverted. A low level on TPOH causes the corresponding bit in the B3 or H4 byte to be processed normally without corruption.

9.15.5 SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the transmit stream. When in-band error reporting is enabled, the path REI and path RDI bits of the path status (G1) byte has already been formed by the corresponding Receive Path Overhead Processor and is transmitted unchanged.

9.15.6 GENERATED Bus Controller

The GENERATED bus provides a template for Telecombus interface signals. It is not connected internally to either the DROP nor the ADD buses. The GENERATED Bus Controller block provides timing on the GENERATED bus of the SPECTRA-155. It controls the GC1J1V1 and GPL signals to indicate the position of the STS (STM) frame and the SPE (VC) within the frame. Downstream access modules may then generate AC1J1V1 and APL based upon this alignment. The phase of the synchronous payload envelope (virtual container) in the GENERATED bus transport frame is indicated by separation of the GC1J1V1 pulse marking the J1 byte from the pulse marking the C1 byte. The relative position of the pulses may be changed by:

1. Discontinuous STS (AU) pointer offsets may be generated by accessing internal SPECTRA-155 registers. If a valid value (i.e., $0 \leq$ pointer value $\leq$ 782) is written to the appropriated SPECTRA-155 register, the GC1J1V1 pulse indicating J1 will immediately jump to the corresponding byte position. If a value greater than 782 is transferred, the J1 indication pulse remains in its present byte position.

2. Positive pointer movements may be generated by accessing internal SPECTRA-155 registers. The GPL signal is set low during the positive stuff opportunity byte position, and the GC1J1V1 pulse indicating J1 will be delayed one byte position. Positive pointer movements may be inserted once per frame.

3. Negative pointer movements may be generated by accessing internal SPECTRA-155 registers. The GPL signal is set high during the negative stuff opportunity byte position (H3), and the GC1J1V1 pulse indicating J1 will be advanced one byte position. Negative pointer movements may be inserted once per frame.

The GENERATED Bus Controller block can be configured to ensure that no positive or negative stuffs occur within three frames of the last pointer event . Discontinuous pointer offset events can still occur in any frame. Positive and negative pointer justifications are provided primarily for diagnostic purposes.

9.16 Transmit Transport Overhead Access

The Transmit Transport Overhead Access block (TTOH) allows the complete transport overhead to be inserted using the TTOH, along with the 5.184 MHz or 1.728 MHz transport overhead clock, TTOHCLK, and the transport overhead frame position, TTOHFP. The transport overhead enable signal, TTOHEN, controls the insertion of transport overhead from TTOH. In addition, individual channels can be sourced from inputs TSLD, TOH, TSUC, TLD and TLOW.

9.17 Transmit Line Overhead Processor

The Transmit Line Overhead Processor block (TLOP) processes the line overhead of the transmit stream. It can be configured to process an STS-1 (STM-0/AU3), or STS-3/3c (STM-1/AU3/AU4) stream.

The TLOP optionally inserts the line data communication channel, the line order wire channel, and the automatic protection switch channel into the line overhead of the transmit stream. These line overhead channels are separately fed to the TLOP as bit serial inputs (TLD, TLOW, and TOH). The TLOP provides the bit serial clock for each line overhead channel (TLDCLK, TOWCLK, TOHCLK).

Line RDI may be inserted in the transmit stream under the control of an external input (TLRDI), or a writeable register. The bits in the SPECTRA-155 Line RDI Control Register controls the immediate insertion of Line RDI upon detection of various errors in the received SONET/SDH stream.

Line REI may be inserted automatically in the SONET/SDH stream under the control of the AUTOLREI bit in the SPECTRA-155 Ring Control Register. Receive B2 errors are accumulated and optionally inserted automatically in bits 2 to 8 of the third Z2/M1 byte of the transmit stream for STS-3/3c (STM-1/AU3/AU4) modes, or in bits 2 to 8 of the Z2/M1 byte of the transmit stream for STS-1 (STM-0/AU3) mode. Up to 8 or 24 errors may be inserted per frame for STS-1 (STM-0/AU3) or STS-3/3c (STM-1/AU3/AU4) modes, respectively.

The line BIP (B2) error detection code for the transmit stream is calculated by the TLOP and is inserted into the line overhead. Errors may be inserted in the B2 code for diagnostic purposes. A byte serial stream, along with a frame position indicator is passed to the Transmit Section Overhead Processor.

9.18 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) block processes the section overhead of the transmit stream. It can be configured to process an STS-1 (STM-0/AU3), or an STS-3/3c (STM-1/AU3/AU4) stream.

The TSOP accepts an unscrambled stream in byte serial format from the Transmit Line Overhead Processor. It optionally inserts the section data communication channel, the order wire channel, and the user channel into the section overhead (regenerator section) of the stream. These section overhead channels are input to the SPECTRA-155 as bit serial signals (TOH, TSLD, TSOW, and TSUC). The TSOP provides the bit serial clock for each section overhead channel (TOHCLK, TSLDCLK, and TOWCLK). The line alarm indication signal may optionally be inserted into the data stream under the control of an external input (TLAIS), or a microprocessor writeable register.

The section BIP-8 error detection code (B1) is calculated by the TSOP block and is inserted into the section overhead of the transmit stream. Errors may be inserted in the B1 code for diagnostic purposes. Framing (A1, A2) and identity bytes (J0) are also inserted. Finally, the complete transmit stream is scrambled and output by the TSOP in byte serial format to the Transmit Line Interface.

The TSOP block is intended to operate with a downstream serializer (the Parallel to Serial Converter block) that accepts the transmit stream in byte serial format and serializes it at the appropriate line rate.

9.19 Transmit Section Trace Buffer

The transmit portion of the SONET/SDH Section Trace Buffer sources the section trace identifier message (J0) for the Transmit Transport Overhead Access block. The length of the trace message is selectable between 16 bytes and 64 bytes. The section trace buffer contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transport Overhead Access block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, the buffer may be programmed to transmit null characters to prevent transmission of partial messages.

9.20 Transmit Line Interface

The Transmit Line Interface block performs clock synthesis and performs parallel to serial conversion. The clock synthesis unit can be bypassed using primary inputs to allow operation with an external line rate clock source.

9.20.1 Clock Synthesis

The transmit clock may be synthesized from a 19.44 MHz or 6.48 MHz reference. The phase lock loop filter transfer function is optimized to enable the PLL to track the reference, yet attenuate high frequency jitter on the reference signal. This transfer function yields a typical low pass corner of 1 MHz, above which reference jitter is attenuated at 3 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference, the intrinsic jitter is less than 0.01 UI RMS when measured using a band pass filter with a low cutoff frequency of 12 KHz and a high cutoff frequency of 1.3 MHz.

9.20.2 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the internal byte serial stream to a bit serial stream.

9.21 System Side Interface

9.21.1 Telecombus Interface

The Telecombus Interface supports Byte, Nibble and Serial Telecombus Modes. It performs multiplexing and demultiplexing to support STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) and STS-3c (STM-1/AU4) operation. In addition, it converts serial or nibble ADD and DROP signals to byte signals usable by the TTAL and RTAL blocks.

For a STS-3c (STM-1/AU4) receive stream, it multiplexes the received data from the three Receive Telecombus Aligners (RTAL) at the STS-1 (STM-0/AU3) rate and provides the combined data stream to the DROP bus configured for byte Telecombus or nibble Telecombus mode.

For a STS-3c (STM-1/AU4) transmit stream, the Telecombus interface accepts a byte or a nibble stream and de-multiplex the stream into three STS-1 (STM-0/AU3) streams or equivalence to be processed by the three Transmit Telecombus Aligners (TTAL).

For a STS-3 (STM-1/AU3) receive stream, all three STS-1 (STM-0/AU3) receive streams are independently processed by corresponding RTALs and presented on the DROP bus. The three receive streams can be multiplexed and provided to the DROP bus configured for byte Telecombus or nibble Telecombus operation. In addition the three streams can be independently provided to the DROP bus configured for serial Telecombus operation.

For a STS-3 (STM-1/AU3) transmit stream, the Telecombus interface accepts a byte stream, a nibble stream or three serial streams. For a byte or nibble stream, it de-multiplex the stream into three STS-1 (STM-0/AU3) streams or equivalence to be processed by the three TTALs. For three serial streams, it deserializes the streams into three STS-1 (STM-0/AU3) streams or equivalence to be processed by the three TTALs.

For a STS-1 (STM-0/AU3) receive stream, the STS-1 (STM-0/AU3) receive stream is processed by the corresponding RTAL and presented on the DROP bus. The receive stream can be provided to the DROP bus configured for byte Telecombus, nibble Telecombus or serial Telecombus operation.

For a STS-1 (STM-0/AU3) transmit stream, the Telecombus interface accepts a byte stream, a nibble stream or a serial stream. A byte or a nibble stream is provided directly to the corresponding TTAL. A serial stream is deserialize and provided to the corresponding TTAL.

The Telecombus is very flexible and can support a wide range of system backplane architectures. Table 21shows the system side ADD bus options:

Table 21 - System Side ADD Bus Configuration Options

DISJ1V1 (reg 100H, bit 5)	APL (SAPL[3:1]) Input Pin	AC1J1V1 Input Pin	Comments
0	APL marks payload bytes	AC1J1V1 marks C1, J1 and V1 positions	TPIP block is bypassed.
1	Tied to ground	AC1J1V1 marks C1 position only	TPIP block interprets pointers for J1/V1
1	APL marks payload bytes	AC1J1V1 marks C1 position only	TPIP block interprets pointers for J1/V1
1	APL marks payload bytes	AC1J1V1 marks C1, J1 and V1 positions	TPIP block interprets pointers for J1/V1. Ignores J1/V1 indications on AC1J1V1

Table 22 shows the system side DROP bus options:

Table 22 - System Side DROP Bus Configuration Options

DISV1 (reg 100H, bit 2)	DPL	DC1J1V1
0	DPL marks payload bytes	DC1J1V1 marks C1, J1 and V1 positions
1	DPL marks payload bytes	DC1J1V1 marks C1 and J1 positions only

9.21.2 Data Mode Interface

The Data Mode Interface block provides the necessary interface and mapping function for raw data (without any SONET/SDH overhead) to be transported via STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) and STS-3c (STM-1/AU4) frames. The supported transfer modes on the system Receive/Transmit buses are byte, nibble and serial. Gapped clocks are used to retrieve data for transmission and to provide data extracted from received frames.

In byte data mode, received data (payload bytes) are extracted from STS-1 (STM-0/AU3), or STS-3c (STM-1/AU4) frames and provided with a gapped 6.48 MHz or 19.44 MHz clock respectively. In nibble mode, received data (payload bytes) are extracted from STS-1 (STM-0/AU3), or STS-3c (STM-1/AU4) frames and provided with a gapped 12.96 MHz or 38.88 MHz clock respectively. STS-3 (STM-1/AU3) operation is not supported in byte and nibble modes.

In serial data mode, only STS-1 (STM-0/AU3) and STS-3 (STM-1/AU3) operation are supported. For STS-3 (STM-1/AU3) operation, all three STS-1 (STM-0/AU3) receive streams are independently processed and frame aligned to the corresponding serial Receive buses. Extracted receive streams are provided with gapped 51.84 MHz clocks. For STS-1 (STM-0/AU3) operation, a single receive stream is similarly processed and provided.

For receive byte, nibble and serial data operation, data can optionally be descrambled using a self synchronous $X^{43}+1$ descrambler.

Transmit byte, nibble and serial data operation is the same as receive operation except that the provided gapped clock is used to sample data provided by an external data source.

For transmit byte, nibble and serial data operation, data can optionally be scrambled using an $X^{43}+1$ scrambler.

9.21.3 Serial DS3 Mode Interface

The Serial DS3 Mode Interface block conditions the input and output signals for the D3MA and D3MD blocks. Note, STS-3c (STM-1/AU4) operation is not supported for this interface.

For STS-3 (STM-1/AU3) receive operation, three independent DS3 interfaces are provided to three D3MD blocks for demapping/extraction of three DS3 signals from a SONET/SDH stream. For STS-1 (STM-0/AU3) operation, only one DS3 stream is supported.

For STS-3 (STM-1/AU3) transmit operation, three independent DS3 interfaces are provided to three D3MA blocks for mapping/insertion of DS3 signals into a SONET/SDH stream. For STS-1 (STM-0/AU3) operation, only one DS3 stream is supported.

For applications which drive a T3 line interface, the desynchronised DS-3 streams must be de-jittered externally before it can be connected to the line interface.

9.21.4 Pseudo-Random Bit Sequence Generator (PRSG)

The Pseudo-Random Bit Sequence Generator (PRSG) generates an unframed 2^{23}-1 test sequence as recommended in the ITU O.151 for OC-3 line rate. The PRSG can be enabled to overwrite the ADD bus or DROP bus. Note, only STS-1 (STM-0/AU3), or STS-3c (STM-1/AU4) byte/nibble Telecombus modes are supported.

9.21.5 Pseudo-Random Bit Sequence Monitor (PRSM)

The Pseudo-Random Sequence Monitor (PRSM) block monitors the recovered data for the presence of an unframed 2^{23}-1 test sequence (ITU O.151 recommended sequence) and accumulates pattern errors detected using this pseudo-random pattern. The PRSM declares synchronization when a sequence of 32 correct pseudo-random patterns are detected consecutively. Pattern errors are only counted when PRSM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the PRSM will fall out of synchronization and it will continuously attempt to re-synchronize to the input sequence until it is successful.

An indication of whether or not the pseudo random sequence monitor is synchronized is provided via the SPECTRA-155 PRS Monitor Drop/Add Control registers and, if enabled, an interrupt is generated whenever a loss of synchronization or re synchronization occurs. The PRSM can detect pseudo random sequences in the ADD stream, or in the DROP stream. Note, only STS-1 (STM-0/AU3), or STS-3c (STM-1/AU4) byte/nibble Telecombus modes are supported.

9.22 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The SPECTRA-155 identification code is 253420CD hexadecimal.

9.23 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the SPECTRA-155 to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the SPECTRA-155 while the test mode registers are used to enhance the testability of the SPECTRA-155.

10 REGISTER DESCRIPTION

Table 23 - Normal Mode Register Memory Map

Address A[9:0]	Register
00H	SPECTRA-155 Configuration
01H	SPECTRA-155 Section/Line Control/Enable
02H	SPECTRA-155 Section/Line Interrupt Status
03H	SPECTRA-155 Reset and Identity
04H	TLOP Control
05H	TLOP Diagnostic
06H	TLOP Transmit K1
07H	TLOP Transmit K2
08H	RLOP Control/Status
09H	RLOP Interrupt Enable and Status
0AH	RLOP B2 Error Count #1
0BH	RLOP B2 Error Count #2
0CH	RLOP B2 Error Count #3
0DH	RLOP Line REI Error Count #1
0EH	RLOP Line REI Error Count #2
0FH	RLOP Line REI Error Count #3
10H	RSOP Control
11H	RSOP Interrupt Status
12H	RSOP B1 Error Count #1
13H	RSOP B1 Error Count #2
14H	SPECTRA-155 Output Port
15H	SPECTRA-155 Input Port Interrupt Enable
16H	SPECTRA-155 Reserved
17H	SPECTRA-155 Ring Control
18H	TSOP Control
19H	TSOP Diagnostic

Address A[9:0]	Register
1AH	SPECTRA-155 Transmit Z1/S1
1BH	TSOP Transmit Z0
1CH	SPECTRA-155 Overhead Unused Bytes Control
1DH	SPECTRA-155 Receive Line AIS Control
1EH	SPECTRA-155 Line RDI Control
1FH	SPECTRA-155 Input Port Status/Value
20H	RASE Interrupt Enable
21H	RASE Interrupt Status
22H	RASE Configuration/Control
23H	RASE SF Accumulation Period
24H	RASE SF Accumulation Period
25H	RASE SF Accumulation Period
26H	RASE SF Saturation Threshold
27H	RASE SF Saturation Threshold
28H	RASE SF Declaring Threshold
29H	RASE SF Declaring Threshold
2AH	RASE SF Clearing Threshold
2BH	RASE SF Clearing Threshold
2CH	RASE SD Accumulation Period
2DH	RASE SD Accumulation Period
2EH	RASE SD Accumulation Period
2FH	RASE SD Saturation Threshold
30H	RASE SD Saturation Threshold
31H	RASE SD Declaring Threshold
32H	RASE SD Declaring Threshold
33H	RASE SD Clearing Threshold
34H	RASE SD Clearing Threshold
35H	RASE Receive K1
36H	RASE Receive K2

Address A[9:0]	Register
37H	RASE Receive Z1/S1
38H	SSTB Section Trace Control
39H	SSTB Section Trace Status
3AH	SSTB Section Trace Indirect Address
3BH	SSTB Section Trace Indirect Data
3C-3FH	SSTB Reserved
40H	CRSI Clock Recovery Control/Status/Interrupt
41H	CRSI Phase Lock Loop Mode Select
42H	CSPI Clock Synthesis Control, Status and Interrupt
43H	CSPI Reserved
40H- 77H	Reserved
78H	SPECTRA-155 PRS Generator Control
79H	SPECTRA-155 PRS Monitor DROP Control
7AH	SPECTRA-155 PRS Monitor ADD Control
7BH	SPECTRA-155 PRS Monitor Interrupt Status
7CH	SPECTRA-155 PRS Monitor DROP Count
7DH	SPECTRA-155 PRS Monitor DROP Count
7EH	SPECTRA-155 PRS Monitor ADD Count
7FH	SPECTRA-155 PRS Monitor ADD Count
80H	SPECTRA-155 Clock Control
81H	SPECTRA-155 Receive Overhead Output Control
82H	SPECTRA-155 Transmit Overhead Input Control
83H	SPECTRA-155 Section Alarm Output Control
84H	SPECTRA-155 Path RALM[1] Output Control
85H	SPECTRA-155 Path RALM[2] Output Control
86H	SPECTRA-155 Path RALM[3] Output Control
87H	SPECTRA-155 Data Mode Configuration
88H	SPECTRA-155 Path and DS3 Receive AIS Control #1
89H	SPECTRA-155 Path and DS3 Receive AIS Control #2

Address A[9:0]	Register
8AH	SPECTRA-155 Path and DS3 Receive AIS Control #3
8BH-8FH	SPECTRA-155 Reserved
90H	D3MD #1 Control
91H	D3MD #1 Interrupt Status
92H	D3MD #1 Interrupt Enable
93H	D3MD #1 Reserved
94H	D3MA #1 Control
95H	D3MA #1 Interrupt Status
96H	D3MA #1 Interrupt Enable
97H	D3MA #1 Reserved
98H-9BH	D3MD #2 registers
9CH-9FH	D3MA #2 registers
A0H-A3H	D3MD #3 registers
A4H-A7H	D3MA #3 registers
A8H-AFH	Reserved
B0H	TPIP #1 Status and Control
B1H	TPIP #1 Alarm Interrupt Status
B2H	TPIP #1 Pointer Interrupt Status
B3H	TPIP #1 Alarm Interrupt Enable
B4H	TPIP #1 Pointer Interrupt Enable
B5H	TPIP #1 Pointer LSB
B6H	TPIP #1 Pointer MSB
B7H	TPIP #1 Reserved
B8H	TPIP #1 Path BIP-8 Count LSB
B9H	TPIP #1 Path BIP-8 Count MSB
BAH	TPIP #1 Reserved
BBH	TPIP #1 Reserved
BCH	TPIP #1 Tributary Multiframe Status and Control
BDH	TPIP #1 BIP Control

Address A[9:0]	Register
BEH	TPIP #1 Reserved
BFH	TPIP #1 Reserved
C0H-CFH	TPIP #2 Registers
D0H-DFH	TPIP #3 Registers
E0H	SPECTRA-155 Clock Synthesis Source Select
E1H	SPECTRA-155 Clock Recovery Source Select
E2H	Reserved
E3H	SPECTRA-155 Transmit Path AIS Control #1
E4H	SPECTRA-155 Transmit Path AIS Control #2
E5H	SPECTRA-155 Transmit Path AIS Control #3 / Auxiliary Signal Interrupt Status
E6H	SPECTRA-155 Auxiliary Section/Line Interrupt Status
E7H	SPECTRA-155 Auxiliary Path Interrupt Status #1
E8H	SPECTRA-155 Auxiliary Path Interrupt Status #2
E9H	SPECTRA-155 Auxiliary Path Interrupt Status #3
EAH	SPECTRA-155 Auxiliary Path Enhanced Interrupt Status
EBH	SPECTRA-155 Trace Message Mode 2 Interrupt Status
ECH	SPECTRA-155 Trace Message Mode 2 Status
EDH	SPECTRA-155 Auto Trace Message Mode 1/2 Control
EEH	Reserved
EFH	SPECTRA-155 Receive Concat Path AIS, RDI and Enhanced RDI Control #1
F0H	SPECTRA-155 Receive Path AIS Control #2
F1H	SPECTRA-155 Receive Path AIS Control #3
F2H	SPECTRA-155 Path REI/RDI Control #2
F3H	SPECTRA-155 Path REI/RDI Control #3
F4H	SPECTRA-155 Enhanced Path RDI Control #1
F5H	SPECTRA-155 Enhanced Path RDI Control #2
F6H	SPECTRA-155 Enhanced Path RDI Control #3
F7H	SPECTRA-155 Auxiliary Section/Line Interrupt Enable

Address A[9:0]	Register
F8H	SPECTRA-155 Auxiliary Path Interrupt Enable #1
F9H	SPECTRA-155 Auxiliary Path Interrupt Enable #2
FAH	SPECTRA-155 Auxiliary Path Interrupt Enable #3
FBH	SPECTRA-155 Auxiliary Path Enhanced Interrupt Enable
FCH	SPECTRA-155 Auxiliary Path Status #1
FDH	SPECTRA-155 Auxiliary Path Status #2
FEH	SPECTRA-155 Auxiliary Path Status #3
FFH	SPECTRA-155 Reserved
100H	SPECTRA-155 Path/Mapper Configuration
101H	SPECTRA-155 Receive Path AIS Control #1
102H	SPECTRA-155 Path REI/RDI Control #1
103H	SPECTRA-155 Path/Mapper Interrupt Status
104H	SPECTRA-155 Path Interrupt Status #1
105H	SPECTRA-155 Path Interrupt Status #2
106H	SPECTRA-155 Path Transmit Control
107H	SPECTRA-155 Path Loopback, ADD Bus Control
108H	SPECTRA-155 Input Signal Activity Monitor
109H	SPECTRA-155 Parity Configuration
10AH-10FH	SPECTRA-155 Reserved
110H	RPOP #1, Status and Control
111H	RPOP #1, Alarm Interrupt Status
112H	RPOP #1, Pointer Interrupt Status
113H	RPOP #1, Alarm Interrupt Enable
114H	RPOP #1, Pointer Interrupt Enable
115H	RPOP #1, Pointer LSB
116H	RPOP #1, Pointer MSB
117H	RPOP #1, Path Signal Label
118H	RPOP #1, Path BIP-8 Count LSB
119H	RPOP #1, Path BIP-8 Count MSB

Address A[9:0]	Register
11AH	RPOP #1, Path REI Count LSB
11BH	RPOP #1, Path REI Count MSB
11CH	RPOP #1, Tributary Multiframe Status and Control
11DH	RPOP #1, Tandem Connection and Ring Control
11EH	RPOP #1, Tandem Connection IEC Count LSB
11FH	RPOP #1, Tandem Connection IEC Count MSB
120H-123H	PMON #1 Reserved
124H	PMON #1, Receive Positive Pointer Justification Count
125H	PMON #1, Receive Negative Pointer Justification Count
126H	PMON #1, Transmit Positive Pointer Justification Count
127H	PMON #1, Transmit Negative Pointer Justification Count
128H	RTAL #1, Control
129H	RTAL #1, Interrupt Status and Control
12AH	RTAL #1, Alarm and Diagnostic Control
12BH	Reserved
12CH-12FH	Reserved
130H	TPOP #1, Control
131H	TPOP #1, GENERATED Bus Control
132H	TPOP #1, Reserved
133H	TPOP #1, Current Pointer LSB
134H	TPOP #1, Current Pointer MSB
135H	TPOP #1, Payload Pointer LSB
136H	TPOP #1, Payload Pointer MSB
137H	TPOP #1, Path Trace
138H	TPOP #1, Path Signal Label
139H	TPOP #1, Path Status
13AH	TPOP #1, Path User Channel
13BH	TPOP #1, Path Growth #1
13CH	TPOP #1, Path Growth #2

Address A[9:0]	Register
13DH	TPOP #1, Tandem Connection Maintenance
13EH	TPOP #1, Concatenation LSB
13FH	TPOP #1, Concatenation MSB
140H	TTAL #1, Control
141H	TTAL #1, Interrupt Status and Control
142H	TTAL #1, Alarm and Diagnostic Control
143H	Reserved
144H-147H	Reserved
148H	SPTB #1, Control
149H	SPTB #1, Path Trace Identifier Status
14AH	SPTB #1, Indirect Address
14BH	SPTB #1, Indirect Data
14CH	SPTB #1, Expected Path Signal Label
14DH	SPTB #1, Path Signal Label Status
14EH-14FH	Reserved
150H-15FH	RPOP #2 Registers
160H-167H	PMON #2 Registers
168H-16BH	RTAL #2 Registers
16CH-16FH	Reserved
170H-17FH	TPOP #2 Registers
180H-183H	TTAL #2 Registers
184H-187H	Reserved
188H-18FH	SPTB #2 Registers
190H-19FH	RPOP #3 Registers
1A0H-1A7H	PMON #3 Registers
1A8H-1ABH	RTAL #3 Registers
1ACH-1AFH	Reserved
1B0H-1BFH	TPOP #3 Registers
1C0H-1C3H	TTAL #3 Registers

Address A[9:0]	Register
1C4H-1C7H	Reserved
1C8H-1CFH	SPTB #3 Registers
1D0H-1FFH	Reserved
200H	Master Test
201H-3FFH	Reserved for Test

Notes on Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the SPECTRA-155 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect SPECTRA-155 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the SPECTRA-155 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register Address 00H: SPECTRA-155 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TMODE[1]	1
Bit 6	R/W	TMODE[0]	0
Bit 5	R/W	STEN	0
Bit 4	R/W	LLE	0
Bit 3	R/W	DLE	0
Bit 2	R/W	LTE	0
Bit 1	R/W	RMODE[1]	1
Bit 0	R/W	RMODE[0]	0

RMODE[1:0]:

The RMODE[1:0] bus selects the receive line side operating mode of the SPECTRA-155.

Table 24 - Receive SONET/SDH mode setting.

RMODE[1:0]	MODE
00	STS-1 (STM-0/AU3)
01	Reserved
10	STS-3 (STM-1/AU3)
11	STS-3c (STM-1/AU4)

LTE:

The LTE bit selects the source of timing for the transmit section of the SPECTRA-155. When LTE is a logic zero, the transmitter timing is derived from inputs TRCLK+ and TRCLK-.

When LTE is a logic one, the transmitter timing is derived from the receiver inputs RXD+ and RXD- when the CRU is enabled (RBYP=0) and from RRCLK+ and RRCLK- when the CRU is disabled (RBYP=1).

DLE:

The DLE bit enables the SPECTRA-155 diagnostic loopback. When DLE is a logic one, the transmit stream is connected to the receive stream. Note,

whether loopback is through the CRU or not depends on the RBYP input. Simultaneous diagnostic loopback and line loopback is not supported.

LLE:

The LLE bit enables the SPECTRA-155 line loopback. When LLE is a logic one, RXD+ and RXD-, are connected internally to TXD+ and TXD-, respectively. Simultaneous diagnostic loopback and line loopback is not supported.

STEN:

The STEN bit controls whether the section trace message stored in the section trace buffer is inserted in the transmit stream. When STEN is a logic one, the message in the section trace buffer is inserted in the transmit stream. When STEN is a logic zero, the J0 byte contents are supplied by the TSOP block or via the TTOH input.

TMODE:

The TMODE[1:0] bus selects the transmit line side operating mode of the SPECTRA-155.

Table 25 - Transmit SONET/SDH mode setting.

TMODE[1:0]	MODE
00	STS-1 (STM-0/AU3)
01	Reserved
10	STS-3 (STM-1/AU3)
11	STS-3c (STM-1/AU4)

Register Address 01H: SPECTRA-155 Section/Line Control/Enable

Bit	Type	Function	Default
Bit 7	R/W	RCP	0
Bit 6	R/W	Z0INS	0
Bit 5	R/W	CSPIE	0
Bit 4	R/W	RASEE	0
Bit 3	R/W	CRSIE	0
Bit 2	R/W	RSOPE	0
Bit 1	R/W	SSTBE	0
Bit 0	R/W	RLOPE	0

RLOPE:

The RLOP interrupt enable is an interrupt mask for events detected by the receive line overhead processor. When RLOPE is a logic one, an interrupt is generated when line layer events are detected, provided the associated enable in the RLOP Interrupt Enable and Status register is set.

SSTBE:

The SSTB interrupt enable is an interrupt mask for events detected by the receive section trace buffer. When SSTBE is a logic one, an interrupt is generated when section trace events are detected by the section trace buffer.

RSOPE:

The RSOP interrupt enable is an interrupt mask for events detected by the receive section overhead processor. When RSOPE is a logic one, an interrupt is generated when section layer events are detected, provided the associated enable in the RSOP Control register is set.

CRSIE:

The CRSI interrupt enable is an interrupt mask for events detected by the Clock Recovery Unit or the Serial to Parallel Converter block. When CRSI is a logic one, an interrupt is generated when events are detected, provided the associated enable in the CRSI Clock Recovery Control/Status/Interrupt register is set.

RASEE:

The RASE interrupt enable (RASEE) is an interrupt mask for events detected by the Receive APS and Synchronization Extractor (RASE). RASEE set to a logic one enables an interrupt to be generated when the APS status changes, APS alarm or a threshold crossing, provided the associated enable in the RASE Interrupt Enable register is set.

CSPIE:

The CSPI interrupt enable is an interrupt mask for events detected by the Clock Synthesis or the Parallel to Serial Converter block. When CSPI is a logic one, an interrupt is generated when events are detected, provided the associated enable in the CSPI Clock Synthesis Control, Status and Interrupt register is set.

Z0INS:

The Z0INS bit controls the values inserted in the transmit Z0 bytes when STS-3/3c (STM-1/AU3/AU4) mode is selected. When Z0INS is logic 1, the value contained in the TSOP Transmit Z0 register is inserted in the two Z0 bytes. When Z0INS is logic 0, the values 02H and 03H are inserted in Z0 byte of 2nd and 3rd STS-1 (STM-0/AU3) respectively. Note that values inserted using the transmit transport overhead port takes precedence.

RCP:

The RCP bit controls the enabling of the receive and transmit ring control ports. When RCP is a logic zero, the ring control ports are disabled, and the LOS, LAIS and LRDI outputs and the RLAIS, TLAIS, and TLRDI inputs are used to monitor alarm status and control maintenance signal insertion. When RCP is a logic one, the ring control ports are enabled, and alarm status and maintenance signal insertion control is provided by the RRCPCLK, RRCPFP, and RRCPDAT outputs and the TRCPCLK, TRCPFP, and TRCPDAT inputs.

Register Address 02H: SPECTRA-155 Section/Line Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CSPII	X
Bit 4	R	RASEI	X
Bit 3	R	CRSII	X
Bit 2	R	RSOPI	X
Bit 1	R	SSTBI	X
Bit 0	R	RLOPI	X

This register, together with the SPECTRA-155 Path/Mapper Interrupt Status register, the SPECTRA-155 Path Interrupt Status #1 register and the SPECTRA-155 Path Interrupt Status #2 register, allows the source of an active interrupt to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

RLOPI:

The RLOPI bit is set high when one or more of the maskable interrupt sources in the receive line overhead processor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RLOP Interrupt Enable and Status Register.

SSTBI:

The SSTBI bit is set high when one or more of the maskable interrupt sources in the section trace buffer has been activated. This register bit remains high until the interrupt is acknowledged by reading the SSTB Section Trace Status Register.

RSOPI:

The RSOPI bit is set high when one or more of the maskable interrupt sources in the receive section overhead processor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RSOP Interrupt Status Register.

CRSII:

The CRSII bit is set high when one or more of the maskable interrupt sources in the Clock Recovery Unit or the Serial to Parallel Converter block has been activated. This register bit remains high until the interrupt is acknowledged by reading the CRSI Clock Recovery Control/Status/Interrupt register.

RASEI:

The RASEI bit is set high when one or more of the maskable interrupt sources in the receive APS and synchronization extractor has been activated. This register bit remains high until the interrupt is acknowledged by reading the RASE Interrupt Status Register.

CSPII:

The CSPII bit is set high when one or more of the maskable interrupt sources in the Clock Synthesis or the Parallel to Serial Converter block has been activated. This register bit remains high until the interrupt is acknowledged by reading the CSPI Clock Synthesis Control, Status and Interrupt register.

Register Address 03H: SPECTRA-155 Reset, Identity, Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R/W	RESET_PATH	0
Bit 5		Unused	X
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

A write to this register initiates a transfer of all performance monitor counter values (PMON, B3, B2, B1, and REI registers) into holding registers.

ID[4:0]:

The version identification bits ID[4:0], are set to the value 02H, representing the version number of the SPECTRA-155.

RESET_PATH:

The RESET_PATH bit allows the path processing blocks of the SPECTRA-155 to be asynchronously reset independent of the transport processing blocks. When RESET_PATH is a logic one, the path processing blocks of the SPECTRA-155 are reset. When RESET is a logic zero, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

The path processing blocks of the SPECTRA-155 include the Transmit Path Overhead Processor (TPOP #1, #2, #3) blocks, the Transmit Telecom Aligner (TTAL #1, #2, #3) blocks, the Transmit Pointer Interpreter (TPIP #1, #2, #3) blocks, the DS3 Mapper ADD Side (D3MA #1, #2, #3) blocks, the Path Trace Buffer (SPTB #1, #2, #3) blocks, the Performance Monitor (PMON #1, #2, #3) blocks, the Receive Path Overhead Processor (RPOP #1, #2, #3) blocks, the Receive Telecom Aligner (RTAL #1, #2, #3) blocks, the DS3 Mapper DROP Side (D3MD #1, #2, #3) blocks, and the System Side Interface blocks (PRSG, PRSM). In addition, the following top level registers are also reset: 80H-8AH, E0H, E1H, EFH, F0H, 100H-109H.

RESET:

The RESET bit allows the SPECTRA-155 to be asynchronously reset. The software reset is equivalent to setting the RSTB input pin low. When RESET is a logic one, the SPECTRA-155 is reset. When RESET is a logic zero, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

Register Address 04H: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI:

The LRDI bit controls the insertion of transmit line remote defect indication (RDI). When LRDI is a logic one, line RDI is inserted into the transmit stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte. Line RDI may also be inserted using the TLRDI input (when the ring control ports are disabled) or using the transmit ring control port (when it is enabled). When LRDI is logic zero, bit 6, 7, and 8 of the K2 byte are not modified by the transmit line overhead processor.

Line RDI may also be inserted into the transmit stream, when receive line AIS is detected, by setting LAISINS bit to high in the SPECTRA-155 Line RDI Control register. Setting of this register bit is also required for line RDI insertion via the transmit ring control port.

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, the transmit APS channel is inserted from the bit serial input TOH which is shifted in on the rising edge of TOHCLK. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Reserved:

The Reserved bits must be set low for proper operation of SPECTRA-155.

Register Address 05H: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DB2	0

DB2:

The DB2 bit controls the insertion of bit errors continuously in each of the line BIP-8 bytes (B2 bytes). When DB2 is set high, each bit of every B2 byte is inverted.

Register Address 06H: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register Address 07H: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register Address 08H: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	LAISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	BLKREI	0
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is set high when line RDI is detected. Line RDI is detected when a 110 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the LRDIDET bit in this register). Line RDI is removed when any pattern other than 110 is detected for three or five consecutive frames. This alarm indication is also available on output LRDI.

LAISV:

The LAISV bit is set high when line AIS is detected. Line AIS is detected when a 111 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the LAISDET bit in this register). Line AIS is removed when any pattern other than 111 is detected for three or five consecutive frames. This alarm indication is also available on output LAIS.

BLKREI:

The BLKREI bit controls the accumulation of REI's. When BLKREI is logic 1, the REI event counter is incremented only once per non zero, valid REI codeword. When BLKREI is logic 0, the REI event counter is incremented for each and every REI indication as indicated by a valid REI codeword (i.e. the counter can be incremented up to 8xN times, for N=1,3). The REI counter is not incremented for invalid REI codewords.

BLKBIPO:

The BLKBIPO bit controls the indication of B2 errors (REI) to the far end. When BLKBIPO is logic one, indications are asserted once per frame

whenever one or more B2 bit errors occur during that frame. When BLKBIPO is logic zero, indications are asserted once for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently from the indications to the far end, and is controlled by the BLKBIP register bit.

If the AUTOLREI register bit is a logic one and the RINGEN register bit is a logic zero, the number of block errors sent to the far end in the line REI bits equals the number of B2E assertions. If BLKBIPO is a logic one, the REI transmitted in the Z2/M1 byte may only contain 00H or 01H.

LRDIDET:

The LRDIDET bit determines the line RDI alarm detection algorithm. When LRDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

LAISDET:

The LAISDET bit determines the line AIS alarm detection algorithm. When LAISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LAISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically overwriting the SONET/SDH frame with all-ones whenever line AIS is detected. When ALLONES is set to logic one, the SONET/SDH frame is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the SONET/SDH frame is immediately returned to carrying the receive stream. When ALLONES is set to logic zero, the outputs carry the receive stream regardless of the state of the line AIS alarm.

BLKBIP:

The BLKBIP bit controls the accumulation of B2 errors. When BLKBIP is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BLKBIP is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 8xN times per frame, for N=1 or 3).

Register Address 09H: RLOP Interrupt Enable and Status

Bit	Type	Function	Default
Bit 7	R/W	LREIE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	LREII	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is set high when line RDI is declared or removed. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

LAISI:

The LAISI bit is set high when line LAIS is declared or removed. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

BIPEI:

The BIPEI bit is set high when a line BIP error is detected. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

LREII:

The LREII bit is set high when a line REI error is detected. This bit is cleared when the RLOP Interrupt Enable and Status Register is read.

LRDIE:

The line RDI interrupt enable is an interrupt mask for line RDI. When LRDIE is a logic one, a line interrupt is generated when line RDI is declared or removed.

LAISE:

The LAIS interrupt enable is an interrupt mask for line AIS. When LAISE is a logic one, a line interrupt is generated when line AIS is declared or removed.

BIPEE:

The line BIP error interrupt enable is an interrupt mask for line BIP error events. When BIPEE is a logic one, a line interrupt is generated when a line BIP error (B2) is detected.

LREIE:

The line remote error indication interrupt enable is an interrupt mask for line REI events. When LREIE is a logic one, a line interrupt is generated when a line REI indication is detected.

Register Address 0AH: RLOP B2 Error Count #1

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Register Address 0BH: RLOP B2 Error Count #2

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

Register Address 0CH: RLOP B2 Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	BE[19]	X
Bit 2	R	BE[18]	X
Bit 1	R	BE[17]	X
Bit 0	R	BE[16]	X

BE[19:0]:

Bits BE[19] through BE[0] represent the number of line bit-interleaved parity errors that have been detected since the last accumulation interval. The error counters are polled by writing to the SPECTRA-155 Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the RLOP B2 Error Count Registers may be read.

Register Address 0DH: RLOP REI Error Count #1

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register Address 0EH: RLOP REI Error Count #2

Bit	Type	Function	Default
Bit 7	R	FE[15]	X
Bit 6	R	FE[14]	X
Bit 5	R	FE[13]	X
Bit 4	R	FE[12]	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

Register Address 0FH: RLOP REI Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	FE[19]	X
Bit 2	R	FE[18]	X
Bit 1	R	FE[17]	X
Bit 0	R	FE[16]	X

FE[19:0]:

Bits FE[19] through FE[0] represent the number of line remote error indications that have been detected since the last accumulation interval. The error counters are polled by writing to the SPECTRA-155 Reset and Identity Register. Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the RLOP REI Error Count Registers may be read.

Register Address 10H: RSOP Control

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOF interrupt enable is an interrupt mask for out of frame. When OOFE is a logic one, a section interrupt is generated when OOF is declared or removed.

LOFE:

The LOF interrupt enable is an interrupt mask for loss of frame. When LOFE is a logic one, a section interrupt is generated when LOF is declared or removed.

LOSE:

The LOS interrupt enable is an interrupt mask for loss of signal. When LOSE is a logic one, a section interrupt is generated when LOS is declared or removed.

BIPEE:

The section BIP interrupt enable is an interrupt mask for section BIP (B1) error events. When BIPE is a logic one, a section interrupt is generated when a section BIP error is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to confirm and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the last A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the

framing pattern regardless of the STS mode; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined. This algorithm examines all 16 bits of the framing pattern in STS-1 (STM-0/AU3) mode, and all 48 bits of the framing pattern in STS-3/3c (STM-1/AU3/AU4) mode.

FOOF:

When a logic one is written to the force out-of-frame (FOOF) bit location, the SPECTRA-155 is forced out-of-frame at the next frame boundary, regardless of the framing byte values. The out-of-frame event results in the assertion of the OOF output and the OOFV register bit. The FOOF bit is a write only bit; an RSOP Control register read may yield a logic one or a logic zero in this bit position.

DDS:

The disable descrambling (DDS) bit controls the descrambling of the receive stream. When a logic one is written to the DDS bit position, the descrambler is disabled. When a logic zero is written to the DDS bit position, the descrambler is enabled.

BLKBIP:

The BLKBIP bit position enables the accumulating of section block BIP errors. When a logic one is written to the BLKBIP bit position, one or more errors in the BIP-8 byte result in a single error accumulated in the B1 error counter. When a logic zero is written to the BLKBIP bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Register Address 11H: RSOP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is set high when out of frame is declared. OOF is declared (OOFV is high) while the SPECTRA-155 is unable to find a valid framing pattern (A1, A2) in the incoming stream. OOF is removed when a valid framing pattern is detected. This alarm indication is also available on output SALM.

LOFV:

The LOFV bit is set high when loss of frame is declared. LOF is declared (LOFV is high) when an out of frame state persists for 3 ms. LOF is removed when an in frame state persists for 3 ms. This alarm indication is also available on output LOF.

LOSV:

The LOSV bit is set high when loss of signal is declared. LOS is declared (LOSV is high) when 20 ± 2.5 µs of consecutive all zeros patterns is detected in the incoming stream. LOS is removed when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all zeros patterns is observed. This alarm indication is also available on output LOS.

OOFI:

The OOFI bit is set high when out of frame is declared or removed. This bit is cleared when the RSOP Interrupt Status Register is read.

LOFI:

The LOFI bit is set high when loss of frame is declared or removed. This bit is cleared when the RSOP Interrupt Status Register is read.

LOSI:

The LOSI bit is set high when loss of signal is declared or removed. This bit is cleared when the RSOP Interrupt Status Register is read.

BIPEI:

The BIPEI bit is set high when a section BIP error is detected. This bit is cleared when the RSOP Interrupt Status Register is read.

Register Address 12H: RSOP B1 Error Count #1

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Register Address 13H: RSOP B1 Error Count #2

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

BE[15:0]:

Bits BE[15] through BE[0] represent the number of section bit-interleaved parity errors that have been detected since the last accumulation interval. The error counters are polled by writing to the SPECTRA-155 Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the RSOP B1 Error Count Registers may be read.

Register Address 14H: SPECTRA-155 Output Port

Bit	Type	Function	Default
Bit 7	R/W	SCPO_TS	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SCPO[1]	0
Bit 0	R/W	SCPO[0]	0

SCPO[1:0]:

The values written to the SCPO[1:0] bit in the output port register directly correspond to the states set on the SCPO[1:0] output pins. This provides a generic port useful for controlling up to 2 signals.

SCPO_TS:

The serial control port output tristate bit along with input TRIS_OHB controls tristating of the SCPO[1:0] outputs. If TRIS_OHB is set high, SCPO_TS is ignored and the outputs are driven. When TRIS_OHB is low and SCPO_TS is set high, outputs SCPO[1:0] are tristate.

SCPO_TS defaults to logic one so that SCPO[1:0] are tristate after reset.

Register Address 15H: SPECTRA-155 Input Port Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SCPIFE[1]	0
Bit 2	R/W	SCPIFE[0]	0
Bit 1	R/W	SCPIRE[1]	0
Bit 0	R/W	SCPIRE[0]	0

SCPIRE[1:0], SCPIFE[1:0]

The SCPIRE[1:0] and SCPIFE[1:0] bits are interrupt enables. When a logic one is written to these locations, the occurrence of an event on the corresponding SCPI[1:0] input activates the interrupt (INTB). The interrupt is cleared by reading the SPECTRA-155 Input Port Status/Value Register. When a logic zero is written to these locations, the occurrence of an event on the corresponding SCPI[1:0] input is inhibited from activating the interrupt.

Register Address 17H: SPECTRA-155 Ring Control

Bit	Type	Function	Default
Bit 7	R/W	RINGEN	0
Bit 6	R	INSLRDI	X
Bit 5	R	INSLAIS	X
Bit 4	R/W	AUTOLREI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SLRDI	0
Bit 0	R/W	SLAIS	0

SLAIS:

The SLAIS bit controls the value of the SENDLAIS bit position in the receive ring control port stream. The SLAIS bit is used to cause a mate SPECTRA-155 to send the line AIS maintenance signal under software control.

SLRDI:

The SLRDI bit controls the value of the SENDLRDI bit position in the receive ring control port stream. The SENDLRDI bit value is determined by the logical OR of this register bit along with the line RDI insertion events programmed in the SPECTRA-155 line RDI Control register. The SLRDI bit is used to cause a mate SPECTRA-155 to send the line RDI maintenance signal under software control.

AUTOLREI:

The AUTOLREI bit enables the automatic insertion/indication of line REI events to the mate transmitter (local or remote). When AUTOLREI is a logic one and the local ring control port is disabled, receive B2 errors detected by the SPECTRA-155 are automatically inserted in the Z2/M1 byte of the transmit stream. When AUTOLREI is a logic one and the remote ring control port is enabled, received B2 errors are output on the ring control port for insertion in the Z2/M1 byte of the remote transmit stream.

When AUTOLREI is a logic zero, line REI events are not automatically inserted in the transmit stream nor indicated on the ring control port. A Z2/M1 byte inserted from the transmit transport overhead port (using the TTOHEN input) takes precedence over the automatic insertion of line REI events.

INSLAIS:

The INSLAIS bit reports the value of the SENDLAIS bit position in the transmit ring control port. When the ring control ports are enabled, a logic one in this bit position indicates that the SPECTRA-155 is inserting the line AIS maintenance signal.

INSLRDI:

The INSLRDI bit reports the value of the SENDLRDI bit position in the transmit ring control port. When the ring control ports are enabled, a logic one in this bit position indicates that the SPECTRA-155 is inserting the line RDI maintenance signal.

RINGEN:

The RINGEN bit controls the operation of the transmit ring control port when the ring control ports are enabled by the RCP bit in the SPECTRA-155 Control/Enable Register. When RINGEN is a logic one, the automatic insertion of line RDI, line AIS, and line REI is controlled by bit positions in the transmit ring control port input stream.

When RINGEN is a logic zero, the insertion of line RDI is done automatically based on alarms detected by the receive portion of the SPECTRA-155. Also, line REI is inserted based on B2 errors detected by the receive portion of the SPECTRA-155.

Register 18H: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set high, the TSOP inserts line AIS into the transmit stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

Reserved:

The Reserved bits must be set low for proper operation of SPECTRA-155.

DS:

The disable scrambling (DS) bit controls the scrambling of the transmit stream. When a logic one is written to the DS bit position, the scrambler is disabled. When a logic zero is written to the DS bit position, the scrambler is enabled.

Register 19H: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. If DFP is set high the A1 bytes are set to 76H instead of F6H.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B1 section overhead byte. When DBIP8 is set high the B1 byte value is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit outgoing stream. When DLOS is set high the transmit serial stream (TXD+/-) is forced low.

Register 1AH: SPECTRA-155 Transmit Z1/S1

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1[7]	0
Bit 6	R/W	Z1/S1[6]	0
Bit 5	R/W	Z1/S1[5]	0
Bit 4	R/W	Z1/S1[4]	0
Bit 3	R/W	Z1/S1[3]	0
Bit 2	R/W	Z1/S1[2]	0
Bit 1	R/W	Z1/S1[1]	0
Bit 0	R/W	Z1/S1[0]	0

Z1/S1[7:0]:

The value written to these bit positions is inserted in the first Z1/S1 byte position of the transmit stream. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The TTOHEN input takes precedence over the contents of this register.

Register 1BH: TSOP Transmit Z0

Bit	Type	Function	Default
Bit 7	R/W	Z0[7]	1
Bit 6	R/W	Z0[6]	1
Bit 5	R/W	Z0[5]	0
Bit 4	R/W	Z0[4]	0
Bit 3	R/W	Z0[3]	1
Bit 2	R/W	Z0[2]	1
Bit 1	R/W	Z0[1]	0
Bit 0	R/W	Z0[0]	0

Z0[7:0]:

Z0[7:0] contains the value inserted in Z0 bytes for STS-1 (STM-0/AU3) #2 and #3 in the transmit STS-3 (STM-1/AU3) stream when the Z0INS bit in the SPECTRA-155 Control/Enable register are both logic 1. Z0[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z0[0] is the least significant bit, corresponding to bit 8, the last bit transmitted.

Register 1CH: SPECTRA-155 Overhead Unused Bytes Control

Bit	Type	Function	Default
Bit 7	R/W	UNUSED_EN	0
Bit 6	R/W	UNUSED_V	0
Bit 5	R/W	NAT_EN	0
Bit 4	R/W	NAT_V	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

NAT_V:

The NAT_V bit determines the value of the national use transport overhead bytes when overwrite is enabled using the NAT_EN bit. When NAT_V is set high, the national use transport overhead bytes are set to FFH. When NAT_V is set low, the national use transport overhead bytes are set to 00H. Please refer to the NAT_EN bit description for the list of national use bytes affected.

NAT_EN:

The NAT_EN bit enables overwriting the national use transport overhead bytes with an all ones or all zeros pattern. When NAT_EN is set high, the F1 #2 (S{2,8,1}), F1 #3 (S{2,9,1}), the E2 #2 (S{9,8,1}) and E2 #3 (S{9,9,1}) bytes are overwritten with an all ones pattern or all zeros pattern as controlled by the NAT_V bit. When NAT_EN is set low, the national use transport overhead bytes are controlled by the TTOHEN input and the TLOP block. When NAT_EN and TTOHEN are both high, the NAT_EN has precedence.

Note, national use bytes Z0 #2 (S{1,8,1}) and Z0 #3 (S{1,9,1}) are not affected by the NAT_EN bit. These bytes can be controlled using the Z0INS bit in the SPECTRA-155 Section/Line Control/Enable register.

UNUSED_V:

The UNUSED_V bit determines the value of the unused transport overhead bytes when overwrite is enabled using the UNUSED_EN bit. When UNUSED_V is set high, the unused transport overhead bytes are set to FFH. When UNUSED_V is set low, the unused transport overhead bytes are set to

00H. Please refer to the UNUSED_EN bit description for the list of the unused bytes affected.

UNUSED_EN:

The UNUSED_EN bit enables overwriting the unused transport overhead bytes with an all ones or all zeros pattern. When UNUSED_EN is set high, the unused transport overhead bytes are overwritten with an all ones pattern or all zeros pattern as controlled by the UNUSED_V bit. When UNUSED_EN is set low, the unused transport overhead bytes are controlled by the TTOHEN input and the TLOP and TSOP blocks. When UNUSED_EN and TTOHEN are both high, the UNUSED_EN has precedence.

The unused bytes are illustrated below.

Table 26 - Transport overhead National and Unused bytes.

A1	A1	A1	A2	A2	A2	J0	N*	N*
B1	U	U	E1	U	U	F1	N	N
D1	U	U	D2	U	U	D3	U	U
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1	U	U	K2	U	U
D4	U	U	D5	U	U	D6	U	U
D7	U	U	D8	U	U	D9	U	U
D10	U	U	D11	U	U	D12	U	U
S1	U	U	U	U	M1	E2	N	N

N - National use byte.

N* - National use byte, controlled by the Z0INS bit in the SPECTRA-155 Section/Line Control/Enable register.

U - Unused byte.

Register Address 1DH: SPECTRA-155 Receive Line AIS Control

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	RTIMINS	0
Bit 2	R/W	RTIUINS	0
Bit 1		Unused	X
Bit 0	R/W	DCCAIS	0

DCCAIS:

The DCCAIS bit enables the insertion of all ones in the section DCC (RSLD) and the line DCC (RLD) when loss of frame (LOF) or LOS is declared. When DCCAIS is a logic 1, all ones is inserted in RSLD and RLD when LOF or LOS is declared.

RTIUINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The RTIUINS bit enables the insertion of path AIS in the DROP direction upon the declaration of section trace unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register). If RTIUINS is a logic 1, path AIS is inserted into the SONET/SDH frame when the current received section trace identifier message has not matched the previous message for eight consecutive messages. Path AIS is terminated when the current message becomes the accepted message.

RTIMINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The RTIMINS bit enables the insertion of path AIS in the DROP direction upon the declaration of section trace mismatch. If RTIMINS is a logic 1, path AIS is inserted into the SONET/SDH frame when the accepted identifier message differs from the expected message. Path AIS is terminated when the accepted message matches the expected message.

LOSINS:

The LOSINS bit enables the insertion of path AIS in the DROP direction upon the declaration of loss of signal (LOS). If LOSINS is a logic 1, path AIS is inserted into the SONET/SDH frame when LOS is declared. Path AIS is terminated when LOS is removed.

LOFINS:

The LOFINS bit enables the insertion of path AIS in the DROP direction upon the declaration of loss of frame (LOF). If LOFINS is a logic 1, path AIS is inserted into the SONET/SDH frame when LOF is declared. Path AIS is terminated when LOF is removed.

SFINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SFINS bit enables the insertion of path AIS in the DROP direction upon the declaration of signal fail (SF). If SFINS is a logic 1, path AIS is inserted into the SONET/SDH frame when SF is declared. Path AIS is terminated when SF is removed.

SDINS:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SDINS bit enables the insertion of path AIS in the DROP direction upon the declaration of signal degrade (SD). If SDINS is a logic 1, path AIS is inserted into the SONET/SDH frame when SD is declared. Path AIS is terminated when SD is removed.

Register Address 1EH: SPECTRA-155 Line RDI Control

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	RTIMINS	0
Bit 2	R/W	RTIUINS	0
Bit 1	R/W	LAISINS	1
Bit 0		Unused	X

LAISINS:

The LAISINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of line AIS. When LAISINS is a logic 1, the detection of line AIS results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

RTIUINS:

The RTIUINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of section trace unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register). When RTIUINS is a logic 1, the detection of section trace unstable results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

RTIMINS:

The RTIMINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of section trace mismatch. When RTIMINS is a logic 1, the detection of section trace mismatch results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

LOSINS:

The LOSINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of loss of signal. When LOSINS is a logic 1, the detection of LOS results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

LOFINS:

The LOFINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of loss of frame. When LOFINS is a logic 1, the detection of LOF results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

SFINS:

The SFINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of signal failure. When SFINS is a logic 1, the detection of SF results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

SDINS:

The SDINS bit enables the insertion of line RDI in the transmit stream or the receive ring control port upon the declaration of signal degrade. When SDINS is a logic 1, the detection of SD results in the insertion of line RDI in the transmit stream (when the ring control ports are disabled), or in the insertion of a logic 1 in the SENDLRDI bit position in the receive ring control port (when the ring control ports are enabled).

Register Address 1FH: SPECTRA-155 Input Port Status/Value

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	SCPIV[1]	X
Bit 4	R	SCPIV[0]	X
Bit 3	R/W	SCPIFI[1]	X
Bit 2	R/W	SCPIFI[0]	X
Bit 1	R/W	SCPIRI[1]	X
Bit 0	R/W	SCPIRI[0]	X

The interrupt bits in this register are write clearable. To clear, a logic one must be written to the corresponding bit position.

SCPIRI[1:0]:

The SCPIRI[1:0] bits are interrupt indications. A logic one in any bit location indicates that an event has occurred on the corresponding SCPI[1:0] input. More specifically, a logic one in any of the SCPIRI[1:0] bit locations indicates that the signal on the corresponding SCPI[1:0] input has transition from a logic zero to logic one (i.e. rising edge detect). The SCPIRI[1:0] bits are cleared by writing a one to the corresponding bit. These register bits function independently from the SPECTRA-155 Input Port Enable register bits; the SCPIRI[1:0] bits will indicate events occurring on the SCPI[1:0] inputs regardless of whether or not these events are enabled to generate an interrupt.

SCPIFI[1:0]:

The SCPIFI[1:0] bits are interrupt indications. A logic one in any bit location indicates that an event has occurred on the corresponding SCPI[1:0] input. More specifically, a logic one in any of the SCPIFI[1:0] bit locations indicates that the signal on the corresponding SCPI[1:0] input has transition from a logic one to logic zero (i.e. falling edge detect). The SCPIFI[1:0] bits are cleared by writing a one to the corresponding bit. These register bits function independently from the SPECTRA-155 Input Port Enable register bits; the SCPIFI[1:0] bits will indicate events occurring on the SCPI[1:0] inputs regardless of whether or not these events are enabled to generate an interrupt.

SCPIV[1:0]:

The SCPIV[1:0] bits are real-time input port state indications. A logic one in any bit location indicates that the signal on the corresponding SCPI[1:0] input is a logic one. A logic zero in any bit location indicates that the signal on the corresponding SCPI[1:0] input is a logic zero. The state of the SCPI[1:0] inputs are latched and held during a microprocessor read of this register.

Register 20H: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1/S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

SDBERE:

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Z1/S1E:

The Z1/S1 interrupt enable is an interrupt mask for changes in the received synchronization status. When Z1/S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1/S1 register.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the RASE Receive K1 and RASE Receive K2 registers.

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

Register 21H: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1/S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames have been received without three consecutive frames containing identical K1 bytes. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers.

SDBERI:

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Z1/S1I:

The Z1/S1I bit is set high when a new synchronization status message has been extracted into the RASE Receive Z1/S1 register. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the RASE Receive K1 and RASE Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Register 22H: RASE Configuration/Control

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1_CAP3	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Unused	X

SDCMODE:

The SDCMODE alarm bit selects the RASE window size to use for clearing the SD alarm. When SDCMODE is a logic 0 the RASE clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic 1 the RASE clears the SD alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SD Accumulation Period registers.

SDSMODE:

The SDSMODE bit selects the RASE saturation mode. When SDSMODE is a logic 0 the RASE limits the number of B2 errors accumulated in one frame period to the RASE SD Saturation Threshold register value. When SDSMODE is a logic 1 the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SD Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SD Accumulation Period register value.

SDBERTEN:

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the RASE. When SDBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SDBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE:

The SFCMODE alarm bit selects the RASE window size to use for clearing the SF alarm. When SFCMODE is a logic 0 the RASE clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic 1 the RASE clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SF Accumulation Period registers.

SFSMODE:

The SFSMODE bit selects the RASE saturation mode. When SFSMODE is a logic 0 the RASE limits the number of B2 errors accumulated in one frame period to the RASE SF Saturation Threshold register value. When SFSMODE is a logic 1 the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SF Accumulation Period register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the RASE. When SFBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SFBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1/S1_CAP3:

The Z1/S1_CAP3 bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP3 is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for three consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP3 is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

Register 23H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Register 24H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Register 25H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 26H: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Register 27H: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 28H: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Register 29H: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 2AH: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Register 2BH: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 2CH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Register 2DH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Register 2EH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]:

The SDSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SD alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Register 2FH: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Register 30H: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]:

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 31H: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Register 32H: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]:

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operations section for the recommended settings.

Register 33H: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Register 34H: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]:

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operations section for the recommended settings.

Register Address 35H: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register Address 36H: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 37H: RASE Receive Z1/S1

Bit	Type	Function	Default
Bit 7	R	Z1/S1[7]	X
Bit 6	R	Z1/S1[6]	X
Bit 5	R	Z1/S1[5]	X
Bit 4	R	Z1/S1[4]	X
Bit 3	R	Z1/S1[3]	X
Bit 2	R	Z1/S1[2]	X
Bit 1	R	Z1/S1[1]	X
Bit 0	R	Z1/S1[0]	X

Z1/S1[3:0]:

The lower nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1/S1E bit in the RASE Interrupt Enable Register). In addition, debouncing can be performed where the register is not loaded until three of the same consecutive nibbles are received. Debouncing is controlled using the Z1/S1_CAP3 bit in the RASE Configuration/Control register.

Z1/S1[7:4]:

The upper nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. No interrupt is asserted on the change of this nibble. In addition, when the Z1/S1_CAP3 bit in the RASE Configuration/Control register selects debouncing, the upper nibble is only updated when three of the same consecutive lower nibbles are received.

Register 38H: SSTB Section Trace Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes. When LEN16 is set high, the section trace message length is 16 bytes. When LEN16 is set low, the section trace message length is 64 bytes.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer are ignored and all-zeros bytes are optionally inserted into the J0 byte. When TNULL is set low the contents of the transmit section trace buffer is optionally inserted into the J0 byte. . TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive section trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, section trace identifier message state changes will not affect INTB.

RTIUIE:

The receive section trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for six consecutive messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received section trace identifier message stable/unstable state will activate the interrupt (INTB) output. When RTIUIE is set low, section trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the section trace buffers. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN:

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZEROs section trace message string. When ZEROEN is set high, all ZEROs section trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs section trace message strings are ignored. TIU assertion and removal are not affected by setting this register bit.

Register 39H: SSTB Section Trace Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace status.

RTIMV:

The receive section trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message. If the accepted section trace message string is all-ZEROs, the mismatch/match is not declared unless the ZEROEN bit in the SSTB Control register is set.

RTIMI:

The receive section trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV:

The receive section trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. RTIUV is set high when the current received section trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is set low when the current message becomes the accepted message.

RTIUI:

The receive section trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer

changes state. This bit (and the interrupt) are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SSTB Section Trace Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the SSTB Section Trace Indirect Data register. The maximum latency for BUSY to return low is 10 µs.

Register 3AH: SSTB Section Trace Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the section trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the J0 byte of the transmit stream. Addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SSTB Section Trace Indirect Data register. When RWB is set low, a write access is initiated. The data in the SSTB Section Trace Indirect Data register will be written to the addressed location in the static page.

Register 3BH: SSTB Section Trace Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 40H: CRSI Clock Recovery Control, Status and Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	ROOLI	X
Bit 5	R	DOOLI	X
Bit 4	R	ROOLV	X
Bit 3	R	DOOLV	X
Bit 2	R/W	ROOLE	0
Bit 1	R/W	DOOLE	0
Bit 0	R/W	REFSEL	0

This register controls the clock recovery and reports the state of the receive phase locked loop.

REFSEL:

The reference select (REFSEL) bit determines the expected frequency of the reference clock as selected using the RREFSRC bit in the SPECTRA-155 Clock Recovery Source Select register. If REFSEL is a logic 0, the correct line clock frequency is synthesized if the reference frequency is 19.44 MHz. If REFSEL is a logic 1, the reference frequency must be 6.48 MHz.

DOOLE:

The DOOLE bit is an interrupt enable for the recovered data out of lock status. When DOOLE is set to logic one, a maskable interrupt is generated when the DOOLV bit changes state.

ROOLE:

The ROOLE bit is an interrupt enable for the reference out of lock status. When ROOLE is set to logic one, an interrupt is generated when the ROOLV bit changes state.

DOOLV:

The recovered data out of lock status indicates the clock recovery phase lock loop is unable to recover and lock to the input data stream. DOOLV is a logic one if the divided down recovered clock frequency is not within 488 ppm of the reference frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bits.

ROOLV:

The reference out of lock status indicates the clock recovery phase lock loop is unable to lock to the reference clock. ROOLV is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the reference frequency. At startup, ROOLV may remain set to logic 1 for several hundreds of milliseconds. ROOLV is undefined if the reference clock is absent.

DOOLI:

The DOOLI bit is the data out of lock interrupt status bit. DOOLI is set high when the DOOLV bit of this register changes state, indicating that either the CRU has locked to the incoming data stream or has gone out of lock. DOOLI is cleared when this register is read. If the DOOLE interrupt enable is set, the INTB output is also asserted.

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOLV bit of this register changes state, indicating that either the CRU has locked to the reference clock or has gone out of lock. ROOLI is cleared when this register is read. If the ROOLE interrupt enable is set, the INTB output is also asserted. ROOLI is undefined if the reference clock is absent.

Reserved:

The Reserved bit is an internal test bit. The default value of this bit is not correct. For all SPECTRA-155 applications, Reserved must be written to logic one after reset to ensure correct operation of the clock recovery circuit.

Register 41H: CRSI Phase Lock Loop Mode Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	WANLANB	1

This register selects the CRU operation mode.

WANLANB:

The WANLANB bit is used to control the current level of the charge pump in the CRU. This bit should be set to logic 1 for WAN mode and logic 0 for LAN mode.

Reserved:

The Reserved bits must be set high for the correct operation of the SPECTRA-155.

Register 42H: CSPI Clock Synthesis Control, Status and Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	ROOLI	X
Bit 4		Unused	X
Bit 3	R	ROOLV	X
Bit 2		Unused	X
Bit 1	R/W	ROOLE	0
Bit 0	R/W	REFSEL	0

This register controls the clock synthesis and reports the state of the transmit phase locked loop.

REFSEL:

The reference select (REFSEL) bit determines the expected frequency of the reference clock as selected using the TREFSRC bit in the SPECTRA-155 Clock Synthesis Source Select register. If REFSEL is a logic 0, the correct line clock frequency is synthesized if the reference frequency is 19.44 MHz. If REFSEL is a logic 1, the reference frequency must be 6.48 MHz.

ROOLE:

The ROOLE bit is an interrupt enable for the reference out of lock status. When ROOLE is set to logic one, an interrupt is generated when the ROOLV bit changes state.

ROOLV:

The transmit reference out of lock status indicates the clock synthesis phase lock loop is unable to lock to the reference clock. ROOLV is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the reference clock frequency. At startup ROOLV may remain set to logic 1 for several hundred milliseconds. ROOLV is undefined if the reference clock is absent.

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOLV bit of this register changes state, indicating that either the PLL is locked to the reference clock or is out of lock. ROOLI is cleared

when this register is read. If the ROOLE interrupt enable is set, the INTB output is also asserted. ROOLI is undefined if the reference clock is absent.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155.

Register 78H: SPECTRA-155 PRS Generator Control

Bit	Type	Function	Default
Bit 7	R/W	ABUS_EN	0
Bit 6	R/W	ABUS_MODE	0
Bit 5	R/W	ABUS_FSEN	0
Bit 4	R/W	ABUS_ER	0
Bit 3	R/W	DBUS_EN	0
Bit 2	R/W	DBUS_MODE	0
Bit 1	R/W	DBUS_FSEN	0
Bit 0	R/W	DBUS_ER	0

For proper operation of the DROP bus PRBS generator, the DISV1 bit in the SPECTRA-155 Path/Mapper Configuration register must be set high.

For proper operation of the ADD bus PRBS generator, only the C1 and J1 indication should be present on the AC1J1V1 input.

DBUS_ER:

The DROP bus error (DBUS_ER) bit is used to generate bit errors in the generated pseudo random stream inserted into the DROP bus. A sequence consisting of a logic one followed by a logic zero written to this bit will induce a single bit error in the pseudo random stream.

DBUS_FSEN:

The DROP bus fix stuff enable (DBUS_FSEN) bit determines whether the pseudo random sequence is inserted into the fixed stuff columns of a STS-1 (STM-0/AU3) stream. When a logic one is written to this bit, the pseudo random sequence is inserted into the fixed stuff columns. When a logic zero is written to this bit, the pseudo random sequence is not inserted into the fixed stuff columns.

DBUS_MODE:

The DROP bus mode (DBUS_MODE) bit determines the location of the SONET/SDH payload the pseudo random bit sequence is mapped into. When a logic one is written to this bit, the H1, H2 pointer values are forced to zero with a non active NDF indication. In addition, the transport overhead bytes and the path overhead bytes are forced to 00H. When a logic zero is

written to this bit, the pseudo random bit sequence is mapped into the payload as received off the line.

DBUS_EN:

The DROP bus enable (DBUS_EN) bit controls overwriting of the SONET/SDH payload with a x^23 pseudo random bit sequence. The payload is identified using the DBUS_MODE bit. When DBUS_EN is set high, the DROP side output SONET/SDH payload is overwritten with the pseudo random sequence. When DBUS_EN is set low, no overwriting occurs.

Note, pseudo random overwriting is only supported for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) byte and nibble Telecombus operation.

ABUS_ER:

The ADD bus error (ABUS_ER) bit is used to generate bit errors in the generated pseudo random stream inserted into the ADD bus. A sequence consisting of a logic one followed by a logic zero written to this bit will induce a single bit error in the pseudo random stream.

ABUS_FSEN:

The ADD bus fix stuff enable (ABUS_FSEN) bit determines whether the pseudo random sequence is inserted into the fixed stuff columns of a STS-1 (STM-0/AU3) stream. When a logic one is written to this bit, the pseudo random sequence is inserted into the fixed stuff columns. When a logic zero is written to this bit, the pseudo random sequence is not inserted into the fixed stuff columns.

ABUS_MODE:

The ADD bus mode (ABUS_MODE) bit determines the location of the SONET/SDH payload the pseudo random bit sequence is mapped into. When a logic one is written to this bit, the H1, H2 pointer values are forced to zero. When a logic zero is written to this bit, the pseudo random bit sequence is mapped into the payload as received off the ADD bus.

ABUS_EN:

The ADD bus enable (ABUS_EN) bit controls overwriting of the SONET/SDH payload with a x^23 pseudo random bit sequence. The payload is identified using the ABUS_MODE bit. When ABUS_EN is set high, the incoming SONET/SDH payload is overwritten with the pseudo random sequence and transmitted. When ABUS_EN is set low, no overwriting occurs.

Note, pseudo random overwriting is only supported for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) byte and nibble Telecombus operation.

Register 79H: SPECTRA-155 PRS Monitor DROP Control

Bit	Type	Function	Default
Bit 7	R/W	DBUS_EN	0
Bit 6	R	DBUS_SYNCV	X
Bit 5	R/W	DBUS_SYNCE	0
Bit 4	R/W	DBUS_RES	0
Bit 3	R/W	DBUS_FSEN	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

For proper operation of the DROP bus PRBS monitor, the DISV1 bit in the SPECTRA-155 Path/Mapper Configuration register must be set high.

DBUS_FSEN:

The DROP bus fix stuff enable (DBUS_FSEN) bit determines whether the DROP bus monitor looks for the pseudo random sequence in the fixed stuff columns of a STS-1 (STM-0/AU3) stream. When a logic one is written to this bit, the fixed stuff columns are assumed to contain the pseudo random sequence. When a logic zero is written to this bit, the monitor ignores the fixed stuff columns.

DBUS_RES:

The DROP bus resync (DBUS_RES) bit allows a force resync of the DROP bus pseudo random monitor. A sequence consisting of a logic one followed by a logic zero written to this bit will force the pseudo random monitor to re-synchronize to the DROP bus SONET/SDH payload

DBUS_SYNCE:

The DROP bus synchronize interrupt enable (DBUS_SYNCE) bit allows an interrupt to be asserted on INTB. When DBUS_SYNCE is set high, a change in synchronization states of the DROP bus monitor will trigger an interrupt. When DBUS_SYNCE is set low, no interrupt is reported.

DBUS_SYNCV:

The DROP bus synchronize value (DBUS_SYNCV) bit indicates if the DROP side monitor has locked onto the pseudo random sequence. When DBUS_SYNCV is low, the monitor has not locked onto the pseudo random

stream. When DBUS_SYNCV is high, the monitor has locked onto the DROP side pseudo random sequence.

DBUS_EN:

The DROP bus enable (DBUS_EN) bit enables monitoring of the receive DROP side for the pseudo random pattern. When DBUS_EN is set low, monitoring is disabled. When DBUS_EN is set high, the SONET/SDH payload on the DROP bus is monitored for the pseudo random bit sequence.

Register 7AH: SPECTRA-155 PRS Monitor ADD Control

Bit	Type	Function	Default
Bit 7	R/W	ABUS_EN	0
Bit 6	R	ABUS_SYNCV	X
Bit 5	R/W	ABUS_SYNCE	0
Bit 4	R/W	ABUS_RES	0
Bit 3	R/W	ABUS_FSEN	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

For proper operation of the ADD bus PRBS monitor, only the C1 and J1 indication should be present on the AC1J1V1 input.

ABUS_FSEN:

The ADD bus fix stuff enable (ABUS_FSEN) bit determines whether the ADD bus monitor looks for the pseudo random sequence in the fixed stuff columns of a STS-1 (STM-0/AU3) stream. When a logic one is written to this bit, the fixed stuff columns are assumed to contain the pseudo random sequence. When a logic zero is written to this bit, the monitor ignores the fixed stuff columns.

ABUS_RES:

The ADD bus resync (ABUS_RES) bit allows a force resync of the ADD bus pseudo random monitor. A sequence consisting of a logic one followed by a logic zero written to this bit will force the pseudo random monitor to re-synchronize to the ADD bus SONET/SDH payload

ABUS_SYNCE:

The ADD bus synchronize interrupt enable (ABUS_SYNCE) bit allows an interrupt to be asserted on INTB. When ABUS_SYNCE is set high, a change in synchronization states of the ADD bus monitor will trigger an interrupt. When ABUS_SYNCE is set low, no interrupt is reported.

ABUS_SYNCV:

The ADD bus synchronize value (ABUS_SYNCV) bit indicates if the ADD side monitor has locked onto the pseudo random sequence. When ABUS_SYNCV is low, the monitor has not locked onto the pseudo random

stream. When ABUS_SYNCV is high, the monitor has locked onto the ADD side pseudo random sequence.

ABUS_EN:

The ADD bus enable (ABUS_EN) bit enables monitoring of the transmit ADD side for the pseudo random pattern. When ABUS_EN is set low, monitoring is disabled. When ABUS_EN is set high, the SONET/SDH payload on the ADD bus is monitored for the pseudo random bit sequence.

Register 7BH: SPECTRA-155 PRS Monitor Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	DBUS_SYNCI	X
Bit 0	R	ABUS_SYNCI	X

ABUS_SYNCI:

The ADD bus synchronize interrupt status (ABUS_SYNCI) bit indicates a change of synchronization states of the ADD bus monitor. When ABUS_SYNCI is set high, the ADD bus monitor has either transition from the in synchronize to out of synchronize state or vice versa. This bit is cleared when this register is read.

DBUS_SYNCI:

The DROP bus synchronize interrupt status (DBUS_SYNCI) bit indicates a change of synchronization states of the DROP bus monitor. When DBUS_SYNCI is set high, the DROP bus monitor has either transition from the in synchronize to out of synchronize state or visa versa. This bit is cleared when this register is read.

Register 7CH: SPECTRA-155 PRS Monitor DROP Count

Bit	Type	Function	Default
Bit 7	R	DPRSE[7]	X
Bit 6	R	DPRSE[6]	X
Bit 5	R	DPRSE[5]	X
Bit 4	R	DPRSE[4]	X
Bit 3	R	DPRSE[3]	X
Bit 2	R	DPRSE[2]	X
Bit 1	R	DPRSE[1]	X
Bit 0	R	DPRSE[0]	X

Register 7DH: SPECTRA-155 PRS Monitor DROP Count

Bit	Type	Function	Default
Bit 7	R	DPRSE[15]	X
Bit 6	R	DPRSE[14]	X
Bit 5	R	DPRSE[13]	X
Bit 4	R	DPRSE[12]	X
Bit 3	R	DPRSE[11]	X
Bit 2	R	DPRSE[10]	X
Bit 1	R	DPRSE[9]	X
Bit 0	R	DPRSE[8]	X

DPRSE[15:0]:

Bits DPRSE[15] through DPRSE[0] represent the number of DROP bus pseudo random errors that have been detected since the last accumulation interval. The error counters are polled by writing to the SPECTRA-155 Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the registers may be read.

Register 7EH: SPECTRA-155 PRS Monitor ADD Count

Bit	Type	Function	Default
Bit 7	R	APRSE[7]	X
Bit 6	R	APRSE[6]	X
Bit 5	R	APRSE[5]	X
Bit 4	R	APRSE[4]	X
Bit 3	R	APRSE[3]	X
Bit 2	R	APRSE[2]	X
Bit 1	R	APRSE[1]	X
Bit 0	R	APRSE[0]	X

Register 7FH: SPECTRA-155 PRS Monitor ADD Count

Bit	Type	Function	Default
Bit 7	R	APRSE[15]	X
Bit 6	R	APRSE[14]	X
Bit 5	R	APRSE[13]	X
Bit 4	R	APRSE[12]	X
Bit 3	R	APRSE[11]	X
Bit 2	R	APRSE[10]	X
Bit 1	R	APRSE[9]	X
Bit 0	R	APRSE[8]	X

APRSE[15:0]:

Bits APRSE[15] through APRSE[0] represent the number of ADD bus pseudo random errors that have been detected since the last accumulation interval. The error counters are polled by writing to the SPECTRA-155 Reset and Identity Register (03H). Such a write transfers the internally accumulated error count to the registers within 7µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7µs period has elapsed, the registers may be read.

Register 80H: SPECTRA-155 Clock Control

Bit	Type	Function	Default
Bit 7	R/W	TXCEN	0
Bit 6	R/W	RXCEN	0
Bit 5	R/W	RCLKEN	0
Bit 4	R/W	TCLKEN	0
Bit 3	R/W	TDLVAL	0
Bit 2	R/W	DS3TICLKB	0
Bit 1		Unused	X
Bit 0		Unused	X

DS3TICLKB:

The DS3 TICLK invert (DS3TICLKB) bit controls the edge of DS3TICLK[3:1] used to sample DS3TDAT[3:1]. When DS3TICLKB is set low, DS3TDAT[3:1] are sampled on the rising edge of DS3TICLK[3:1]. When DS3TICLKB is set high, DS3TDAT[3:1] is sampled on the falling edge of DS3TICLK[3:1].

TDLVAL:

The transmit data line value (TDLVAL) bit selects the value of the section data link (D1, D2, D3). TDLVAL is only used when TDLSEL is high in the SPECTRA-155 Transmit Overhead Input Control register.

TCLKEN:

The TCLK enable (TCLKEN) bit controls gating of the TCLK output. When TCLKEN is set low, the TCLK output is held low. When TCLKEN is set high, the TCLK output is allowed to oscillate.

RCLKEN:

The RCLK enable (RCLKEN) bit controls gating of the RCLK output. When RCLKEN is set low, the RCLK output is held low. When RCLKEN is set high, the RCLK output is allowed to oscillate.

TXCEN:

The TXC enable (TXCEN) bit controls gating of the TXC output. When TXCEN is set low, the TXC output is held low. When TXCEN is set high, the TXC output is allowed to oscillate.

RXCEN:

The RXC enable (RXCEN) bit controls gating of the RXC output. When RXCEN is set low, the RXC output is held low. When RXCEN is set high, the RXC output is allowed to oscillate.

Register 81H: SPECTRA-155 Receive Overhead Output Control

Bit	Type	Function	Default
Bit 7	R/W	R64SEL	0
Bit 6	R/W	ROHSEL[2]	1
Bit 5	R/W	ROHSEL[1]	0
Bit 4	R/W	ROHSEL[0]	0
Bit 3	R/W	RDLSEL	0
Bit 2	R/W	RSLD_TS	1
Bit 1	R/W	ROH_TS	1
Bit 0		Unused	X

ROH_TS:

The receive overhead tristate (ROH_TS) bit along with input TRIS_OHB controls tristating of the RFP, ROH and ROHCLK outputs. If TRIS_OHB is set high, ROH_TS is ignored and the outputs are driven. When TRIS_OHB is low and ROH_TS is set low, the RFP, ROH and ROHCLK outputs are driven. When TRIS_OHB is low and ROH_TS is set high, the ROH and ROHCLK outputs are tristate.

ROH_TS defaults to logic one so that RFP, ROH and ROHCLK are tristate after reset.

RSLD_TS:

The receive section/line datalink tristate (RSLD_TS) bit along with input TRIS_OHB controls tristating of the RSLD and RSLDCLK outputs. If TRIS_OHB is set high, RSLD_TS is ignored and the outputs are driven. When TRIS_OHB is low and RSLD_TS is set low, the RSLD and RSLDCLK outputs are driven. When TRIS_OHB is low and RSLD_TS is set high, the RSLD and RSLDCLK outputs are tristate.

RSLD_TS defaults to logic one so that RSLD and RSLDCLK are tristate after reset.

RDLSEL:

The receive data line select (RDLSEL) bit determines the contents of the outgoing RSLD stream. When RDLSEL is low, the RSLD stream contains the section DCC (D1-D3). When RDLSEL is high, the RSLD stream contains the line DCC (D4-D12).

ROHSEL[2:0]:

The receive overhead select (ROHSEL[2:0]) bus determines the contents of the out going ROH stream. The valid ROHSEL codepoints are listed below.

Table 27 - ROHSEL[2:0] codepoints.

ROHSEL[2:0]	Contents
000	section orderwire (E1)
001	line user channel (F1)
010	line orderwire (E2)
011	Reserved
100	APS bytes (K1/K2)
others	Reserved

R64SEL:

The receive 64 select (R64SEL) bit determine the clock frequency for outputs ROWCLK and ROHCLK. When R64SEL is set low, ROWCLK and ROHCLK are gapped 72 KHz clocks. When R64SEL is set high, ROWCLK and ROHCLK are smooth 64 KHz clocks. Note, ROHCLK is always a gapped 144 KHz clock when ROHSEL=100.

Register 82H: SPECTRA-155 Transmit Overhead Input Control

Bit	Type	Function	Default
Bit 7	R/W	T64SEL	0
Bit 6	R/W	TOHSEL[2]	1
Bit 5	R/W	TOHSEL[1]	0
Bit 4	R/W	TOHSEL[0]	0
Bit 3	R/W	TDLSEL	0
Bit 2	R/W	TSLD_TS	1
Bit 1	R/W	TOH_TS	1
Bit 0	R/W	TAPSTAP	0

TAPSTAP:

The transmit APS transmit alarm port (TAPSTAP) bit selects the source of the transmit APS (K1/K2) bytes. When TAPSTAP is low, the APS bytes are sourced using TLOP registers or via the TTOH or TOH inputs. When TAPSTAP is high, the APS bytes are sourced from the transmit alarm port and has precedence over the ring control port.

TOH_TS:

The transmit overhead tristate (TOH_TS) bit along with input TRIS_OHB controls tristating of the TFP and TOHCLK outputs. If TRIS_OHB is set high, TOH_TS is ignored and the outputs are driven. When TOH_TS is set low, the TFP and TOHCLK outputs are driven. When TOH_TS is set high, the TFP and TOHCLK outputs are tristate.

TOH_TS defaults to logic one so that TFP and TOHCLK are tristate after reset.

TSLD_TS:

The transmit section/line datalink tristate (TSLD_TS) bit along with input TRIS_OHB controls tristating of the TSLDCLK output. If TRIS_OHB is set high, TSLD_TS is ignored and the output is driven. When TRIS_OHB is low and TSLD_TS is set low, the TSLDCLK output is driven. When TRIS_OHB is low and TSLD_TS is set high, the TSLDCLK output is tristate.

TSLD_TS defaults to logic one so that TSLDCLK is tristate after reset.

TDLSEL:

The transmit data line select (TDLSEL) bit determines the contents of the incoming TSLD stream. When TDLSEL is low, the TSLD stream contains the section DCC (D1-D3). When TDLSEL is high, the TSLD stream contains the line DCC (D4-D12) and the TLD input is ignored. When TDLSEL is high, section DCC (D1-D3) can be controlled using the TTOH input or can be forced to an all ones or all zeros pattern using the TDLVAL bit in the SPECTRA-155 Clock Control register.

TOHSEL[2:0]:

The transmit overhead select (TOHSEL[2:0]) bus determines the contents of the incoming TOH stream. The valid TOHSEL codepoints are listed below.

Table 28 - TOHSEL[2:0] codepoints.

TOHSEL[2:0]	Contents
000	section orderwire (E1)
001	line user channel (F1)
010	line orderwire (E2)
011	Reserved
100	APS bytes (K1/K2)
others	Reserved

T64SEL:

The transmit 64 select (T64SEL) bit determine the clock frequency for outputs TOWCLK and TOHCLK. When T64SEL is set low, TOWCLK and TOHCLK are gapped 72 KHz clocks. When T64SEL is set high, TOWCLK and TOHCLK are smooth 64 KHz clocks. Note, TOHCLK is always a gapped 144 KHz clock when TOHSEL=100.

Register 83H: SPECTRA-155 Section Alarm Output Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOFEN	0
Bit 1	R/W	LOSEN	0
Bit 0	R/W	OOFEN	1

OOFEN, LOSEN, LOFEN, LAISEN, LRDIEN:

The above enable bits allow the corresponding alarm indications (out of frame, loss of signal, loss of frame, line alarm indication signal, line remote defect indication) to be ORed into the SALM output. When the enable bit is high, the corresponding alarm indication is ORed with other alarm indications and output on SALM. When the enable bit is low, the corresponding alarm indication does not affect the SALM output.

Register 84H: SPECTRA-155 RALM[1] Output Control

Bit	Type	Function	Default
Bit 7	R/W	LOPCONEN	0
Bit 6	R/W	PAISCONEN	0
Bit 5		Unused	X
Bit 4	R/W	LOMEN	0
Bit 3	R/W	PERDIEN	0
Bit 2	R/W	PRDIEN	0
Bit 1	R/W	PAISEN	0
Bit 0	R/W	LOPEN	0

LOPEN, PAISEN, PRDIEN, PERDIEN, LOMEN, LOPCONEN , PAISCONEN :

The above enable bits allow the corresponding alarm indications (loss of [concatenated] pointer, path [concatenated] AIS, path RDI, path enhanced RDI, loss of multiframe) to be ORed into the RALM[1] output. When the enable bit is high, the corresponding alarm indication is ORed with other alarm indications and output on RALM[1]. When the enable bit is low, the corresponding alarm indication does not affect the RALM[1] output.

Register 85H: SPECTRA-155 RALM[2] Output Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	LOMEN	0
Bit 3	R/W	PERDIEN	0
Bit 2	R/W	PRDIEN	0
Bit 1	R/W	PAISEN	0
Bit 0	R/W	LOPEN	0

LOPEN, PAISEN, PRDIEN, PERDIEN, LOMEN:

The above enable bits allow the corresponding alarm indications (loss of pointer, path AIS, path RDI, path enhanced RDI, loss of multiframe) to be ORed into the RALM[2] output. When the enable bit is high, the corresponding alarm indication is ORed with other alarm indications and output on RALM[2]. When the enable bit is low, the corresponding alarm indication does not affect the RALM[2] output.

Register 86H: SPECTRA-155 RALM[3] Output Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	LOMEN	0
Bit 3	R/W	PERDIEN	0
Bit 2	R/W	PRDIEN	0
Bit 1	R/W	PAISEN	0
Bit 0	R/W	LOPEN	0

LOPEN, PAISEN, PRDIEN, PERDIEN, LOMEN:

The above enable bits allow the corresponding alarm indications (loss of pointer, path AIS, path RDI, path enhanced RDI, loss of multiframe) to be ORed into the RALM[3] output. When the enable bit is high, the corresponding alarm indication is ORed with other alarm indications and output on RALM[3]. When the enable bit is low, the corresponding alarm indication does not affect the RALM[3] output.

Register 87H: SPECTRA-155 Data Mode Configuration

Bit	Type	Function	Default
Bit 7	R/W	DS3_SEL52	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RDM_SCRMEN	0
Bit 4	R/W	RDM_FSEN	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TDM_SCRMEN	0
Bit 0	R/W	TDM_FSEN	0

For proper operation in byte or nibble data mode, the DISV1 bit in the SPECTRA-155 Path/Mapper Configuration register must be set low.

TDM_FSEN:

The transmit data mode fix stuff enable (TDM_FSEN) bit determines whether to use the STS-1 (STM-0/AU3) fixed stuff columns to carry payload. When TDM_FSEN is set low, the fixed stuff columns are treated like stuff columns and is not used to carry payload. When TDM_FSEN is set high, the fixed stuff columns are used to carry payload.

TDM_FSEN is only valid when the SPECTRA-155 is configured for Byte and Nibble Data mode.

TDM_SCRMEN:

The transmit scrambler enable (TDM_SCRMEN) bit determines whether to use the $X^{43}+1$ scrambler or not. When TDM_SCRMEN is set low, the payload is not scrambled when configured for Byte or Nibble Data Mode. When TDM_SCRMEN is set high, the payload is scrambled using the $x^{43}+1$ polynomial when configured for Byte or Nibble Data Mode.

RDM_FSEN:

The receive data mode fix stuff enable (RDM_FSEN) bit determines whether the STS-1 (STM-0/AU3) fixed stuff columns carry payload. When RDM_FSEN is set low, the fixed stuff columns are treated like stuff columns and are not processed. When RDM_FSEN is set high, the fixed stuff columns are assumed to carry payload and are processed.

RDM_FSEN is only valid when the SPECTRA-155 is configured for Byte and Nibble Data mode.

RDM_SCRMEN:

The receive descrambler enable (RDM_SCRMEN) bit determines whether to use the $X^{43}+1$ descrambler or not. When RDM_SCRMEN is set low, the payload is not descrambled when configured for Byte or Nibble Data Mode. When RDM_SCRMEN is set high, the payload is descrambled using the $x^{43}+1$ polynomial when configured for Byte or Nibble Data Mode.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155.

DS3_SEL52:

The DS3 select 52 clock (DS3_SEL52) bit selects the desynchronizer source clock used by the D3MD blocks. When DS3_SEL52 is set low, the DS3RICLK[3:1] inputs are used as the D3MD source clocks. When DS3_SEL52 is set high, an internal 51.84 MHz recovered line clock is used as the D3MD source clocks.

Register 88H: SPECTRA-155 Path and DS3 Receive AIS Control #1

Bit	Type	Function	Default
Bit 7	R/W	ALMAIS	0
Bit 6	R/W	PSLUDS3AIS	0
Bit 5	R/W	PSLMDS3AIS	0
Bit 4	R/W	LOPDS3AIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PAISDS3AIS	0
Bit 1	R/W	TIUDS3AIS	0
Bit 0	R/W	TIMDS3AIS	0

This register controls the auto assertion of DS3 AIS on output DS3RDAT[1] when the specified condition is present.

TIMDS3AIS:

When set high, the TIMDS3AIS bit enables DS3 AIS assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMDS3AIS is set low, trace identifier mismatch events have no effect on DS3 AIS.

TIUDS3AIS:

When set high, the TIUDS3AIS bit enables DS3 AIS assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUDS3AIS is set low, trace identifier unstable events have no effect on DS3 AIS.

PAISDS3AIS:

When set high, the PAISDS3AIS bit enables DS3 AIS assertion when path alarms are detected in the receive stream. When PAISDS3AIS is set low, path AIS alarms have no effect on DS3 AIS.

Reserved:

This Reserved bit must be set low for correct operation of the SPECTRA-155.

LOPDS3AIS:

When set high, the LOPDS3AIS bit enables DS3 AIS assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPDS3AIS is set low, loss of pointer events have no effect on DS3 AIS.

PSLMDS3AIS:

When set high, the PSLMDS3AIS bit enables DS3 AIS assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMDS3AIS is set low, path signal label mismatch events have no effect on DS3 AIS.

PSLUDS3AIS:

When set high, the PSLUDS3AIS bit enables DS3 AIS assertion when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUDS3AIS is set low, path signal label unstable events have no effect on DS3 AIS .

ALMAIS:

When set high, the ALMAIS bit enables path AIS and DS3 AIS assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMAIS is set low, the above events have no effect on path AIS nor DS3 AIS.

Register 89H: SPECTRA-155 Path and DS3 Receive AIS Control #2

Bit	Type	Function	Default
Bit 7	R/W	ALMAIS	0
Bit 6	R/W	PSLUDS3AIS	0
Bit 5	R/W	PSLMDS3AIS	0
Bit 4	R/W	LOPDS3AIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PAISDS3AIS	0
Bit 1	R/W	TIUDS3AIS	0
Bit 0	R/W	TIMDS3AIS	0

This register controls the auto assertion of DS3 AIS on output DS3RDAT[2] when the specified condition is present.

TIMDS3AIS:

When set high, the TIMDS3AIS bit enables DS3 AIS assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMDS3AIS is set low, trace identifier mismatch events have no effect on DS3 AIS.

TIUDS3AIS:

When set high, the TIUDS3AIS bit enables DS3 AIS assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUDS3AIS is set low, trace identifier unstable events have no effect on DS3 AIS.

PAISDS3AIS:

When set high, the PAISDS3AIS bit enables DS3 AIS assertion when path alarms are detected in the receive stream. When PAISDS3AIS is set low, path AIS alarms have no effect on DS3 AIS.

Reserved:

This Reserved bit must be set low for correct operation of the SPECTRA-155.

LOPDS3AIS:

When set high, the LOPDS3AIS bit enables DS3 AIS assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPDS3AIS is set low, loss of pointer events have no effect on DS3 AIS.

PSLMDS3AIS:

When set high, the PSLMDS3AIS bit enables DS3 AIS assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMDS3AIS is set low, path signal label mismatch events have no effect on DS3 AIS.

PSLUDS3AIS:

When set high, the PSLUDS3AIS bit enables DS3 AIS assertion when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUDS3AIS is set low, path signal label unstable events have no effect on DS3 AIS .

ALMAIS:

When set high, the ALMAIS bit enables path AIS and DS3 AIS assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMAIS is set low, the above events have no effect on path AIS nor DS3 AIS.

Register 8AH: SPECTRA-155 Path and DS3 Receive AIS Control #3

Bit	Type	Function	Default
Bit 7	R/W	ALMAIS	0
Bit 6	R/W	PSLUDS3AIS	0
Bit 5	R/W	PSLMDS3AIS	0
Bit 4	R/W	LOPDS3AIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PAISDS3AIS	0
Bit 1	R/W	TIUDS3AIS	0
Bit 0	R/W	TIMDS3AIS	0

This register controls the auto assertion of DS3 AIS on output DS3RDAT[3] when the specified condition is present.

TIMDS3AIS:

When set high, the TIMDS3AIS bit enables DS3 AIS assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMDS3AIS is set low, trace identifier mismatch events have no effect on DS3 AIS.

TIUDS3AIS:

When set high, the TIUDS3AIS bit enables DS3 AIS assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUDS3AIS is set low, trace identifier unstable events have no effect on DS3 AIS.

PAISDS3AIS:

When set high, the PAISDS3AIS bit enables DS3 AIS assertion when path alarms are detected in the receive stream. When PAISDS3AIS is set low, path AIS alarms have no effect on DS3 AIS.

Reserved:

This Reserved bit must be set low for correct operation of the SPECTRA-155.

LOPDS3AIS:

When set high, the LOPDS3AIS bit enables DS3 AIS assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPDS3AIS is set low, loss of pointer events have no effect on DS3 AIS.

PSLMDS3AIS:

When set high, the PSLMDS3AIS bit enables DS3 AIS assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMDS3AIS is set low, path signal label mismatch events have no effect on DS3 AIS.

PSLUDS3AIS:

When set high, the PSLUDS3AIS bit enables DS3 AIS assertion when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUDS3AIS is set low, path signal label unstable events have no effect on DS3 AIS .

ALMAIS:

When set high, the ALMAIS bit enables path AIS and DS3 AIS assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMAIS is set low, the above events have no effect on path AIS nor DS3 AIS.

Register 90H, 98H, A0H: D3MD Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DSCRMEN	0
Bit 1	R/W	GAPFS	0
Bit 0	R/W	DS3AISGEN	0

DS3AISGEN:

The active high DS3 Alarm Indication Signal enable bit (DS3AISGEN) configures the D3MD to generate a DS3 AIS signal. Any data on the STS-1 (STM-0/AU3) SPE is lost due to the assertion of DS3AISGEN. DS3AISGEN bit is logically ORed with the DS3RAIS input and internal alarm indications as controlled using the SPECTRA-155 Path and DS3 Receive AIS Control register.

DS3AISGEN is valid only in Serial DS3 mode as selected using the SMODE[2:0] inputs.

GAPFS:

The fixed stuff gapping configuration bit (GAPFS) configures the D3MD to gap out the two columns of fixed stuff bytes of the SPE when in Serial Data Mode as selected using the SS[2:0] inputs. If GAPFS is high, the fixed stuff columns in the STS-1 (STM-0/AU3) SPE are gapped. If GAPFS is low, the entire STS-1 (STM-0/AU3) SPE is used to carry payload.

DSCRMEN:

The active high descrambler enable bit (DSCRMEN) configures the D3MD to pass the serial data through a self synchronous descrambler ($X^{43}+1$ polynomial). DSCRMEN is only valid when in Serial Data Mode as selected using the SMODE[2:0] inputs.

Register 91H, 99H, A1H: D3MD Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read by the microprocessor interface.

UFLI

When set high, this bit indicates that an underflow condition has occurred in the D3MD elastic store. This error resets the elastic store's read and write addresses to 180° apart.

OFLI

When set high, this bit indicates that an overflow condition has occurred in the D3MD elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 92H, 9AH, A2H: D3MD Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

UFLIEN:

When set high, this bit enables generation of an interrupt if a D3MD elastic store underflow condition occurs (UFLI='1').

OFLIEN:

When set high, this bit enables generation of an interrupt if a D3MD elastic store overflow condition occurs (OFLI='1').

Register 94H, 9CH, A4H: D3MA Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GAPFS	0
Bit 2	R/W	SCRMEN	0
Bit 1	R/W	RBSO	0
Bit 0	R/W	DS3AISGEN	0

DS3AISGEN:

The active high DS3 Alarm Indication Signal enable bit (DS3AISGEN) configures the D3MA to generate a DS3 AIS signal. Any data on the STS-1 (STM-0/AU3) SPE is lost due to the assertion of DS3AISGEN. DS3AISGEN bit is logically ORed with the DS3TAIS input and internal alarm indications as controlled using the SPECTRA-155 DS3 Transmit AIS Control register.

DS3AISGEN is valid only in Serial DS3 mode as selected using the SMODE[2:0] inputs.

RBSO:

When RBSO is high, the R bits of the DS3 mapping or the STS-1 (STM-0/AU3) mapping are set to ‘1’s. If RBSO bit is Low, R bits are set to ‘0’s. This bit is valid for both Serial DS3 and Serial Data Mode operation.

SCRMEN:

The active high scrambler enable bit (SCRMEN) configures the D3MA to pass the serial data through a self synchronous scrambler (X^43+1 polynomial). SCRMEN is only valid in Serial Data Mode.

GAPFS:

The fix stuff gapping configuration bit (GAPFS) configures the D3MA to gap out the two columns of fixed stuff bytes of the STS-1 (STM-0/AU3) SPE when in Serial Data Mode. If GAPFS is high, the fixed stuff columns in the STS-1 (STM-0/AU3) SPE are gapped. If GAPFS is low, the entire STS-1 (STM-0/AU3) SPE is used to carry payload.

Register 95H, 9DH, A5H: D3MA Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read by the microprocessor interface.

UFLI

When set High, this bit indicates that an underflow condition has occurred in the D3MA elastic store. This error resets the elastic store's read and write addresses to 180° apart.

OFLI

When set High, this bit indicates that an overflow condition has occurred in the D3MA elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 96H, 9EH, A6H: D3MA Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

UFLIEN:

When set High, this bit enables generation of an interrupt if an elastic store underflow condition occurs (UFLI='1').

OFLIEN:

When set High, this bit enables generation of an interrupt if an elastic store overflow condition occurs (OFLI='1').

Register B0H, C0H, D0H: TPIP Status and Control (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	PAISCONV	X
Bit 3	R	PAISV	X
Bit 2		Unused	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding TPIP if the EXTD bit is set low in the TPIP Pointer MSB register.

NEWPTRE:

When a 1 is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output.

NEWPTRI:

The NEWPTRI bit is set to logic 1 when a new_point indication is received. This bit (and the interrupt) are cleared when this register is read.

PAISV:

The path AIS status bit (PAIS) indicates reception of path AIS alarm in the receive stream.

PAISCONV:

The concatenation path AIS status bit (PAISCON) indicates reception of path AIS alarm in the concatenation indicator in the receive stream.

LOPV:

The loss of pointer status bit (LOP) indicates entry to the LOP_state in the TPIP pointer interpreter state machine.

LOPCONV:

The concatenated loss of pointer status bit (LOPCON) indicates entry to LOP_state for the concatenated streams in the TPIP pointer interpreter.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-155.

Register B0H, C0H, D0H: TPIP Status and Control (EXTD=1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides configuration of the corresponding TPIP if the EXTD bit is set high in the TPIP Pointer MSB register.

IINVCNT:

When a 1 is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state, 3 x new point will reset the inv_point count. If this bit is set to 0, the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-155.

Register B1H, C1H, D1H: TPIP Alarm Interrupt Status (EXTD=0)

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	PAISCONI	X
Bit 3	R	PAISI	X
Bit 2		Unused	X
Bit 1	R	BIPEI	X
Bit 0	R	PREII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set low in the TPIP Pointer MSB register.

These bits (and the interrupt) are cleared when the Interrupt Status Register is read.

PREII

The PREI interrupt status bit (PREII) is set high when a path REI is detected.

BIPEI:

The BIP error interrupt status bit (BIPEI) is set high when a path BIP-8 error is detected.

PAISI, PAISCONI, LOPI, LOPCONI:

The PAISI, PAISCONI, LOPI and LOPCONI interrupt status bits are set high on assertion and removal of the corresponding alarm states.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

Register B2H, C2H, D2H: TPIP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	CONCATI	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	Reserved	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

These bits (and the interrupt) are cleared when this register is read.

NDFI:

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream.

PSEI, NSEI:

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the TPIP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

INVNDFI:

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream.

DISCOPAI:

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the TPIP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication).

ILLJREQI:

The illegal justification request interrupt status bit (ILLJREQI) is set high when the TPIP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable).

CONCATI:

The concatenation indication error interrupt status bit (CONCATI) is set high when the SPECTRA-155 is operating in concatenation mode and an error is detected in the concatenation indicators of STS-1 (STM-0/AU3) #2 and STS-1 (STM-0/AU3) #3.

Register B3H, C3H, D3H: TPIP Alarm Interrupt Enable (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	PREIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set low in the TPIP Pointer MSB register.

PREIE:

When a 1 is written to the PREIE interrupt enable bit position, the reception of one or more path REIs will activate the interrupt (INTB) output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt (INTB) output.

PAISE:

When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output.

PAISCONE:

When a 1 is written to the PAISCONE interrupt enable bit position, a change in the concatenation path AIS state will activate the interrupt (INTB) output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output.

LOPCONE:

When a 1 is written to the LOPCONE interrupt enable bit position, a change in the concatenation loss of pointer state will activate the interrupt (INT) output.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155.

Register B3H, C3H, D3H: TPIP Alarm Interrupt Enable (EXTD=1)

Bit	Type	Function	Default
Bit 7	R	LOPCONV#2	X
Bit 6	R	LOPCONV#3	X
Bit 5	R	PAISCONV#2	X
Bit 4	R	PAISCONV#3	X
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	Reserved	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set high in the TPIP Pointer MSB register.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-155.

LOPCONV#2:

The concatenated loss of pointer value bit (LOPCONV#2) indicates the LOP value for the STS-3c (STM-1/AU3 #2).

LOPCONV#3:

The concatenated loss of pointer value bit (LOPCONV#3) indicates the LOP value for the STS-3c (STM-1/AU3 #3).

PAISCONV#2:

The concatenated path AIS value bit (PAISCONV#2) indicates the PAIS value for the STS-3c (STM-1/AU3 #2).

PAISCONV#3:

The concatenated path AIS value bit (PAISCONV#3) indicates the PAIS value for the STS-3c (STM-1/AU3 #3).

Register B4H, C4H, D4H: TPIP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	CONCATE	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

NDFE:

When a 1 is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output.

PSEE:

When a 1 is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output.

NSEE:

When a 1 is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-155.

INVNDFE:

When a 1 is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output.

DISCOPAE:

When a 1 is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output.

CONCATE:

When a 1 is written to the CONCATE interrupt enable bit position, an invalid Concatenation Indicator event will activate the interrupt (INTB) output.

ILLJREQE:

When a 1 is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output.

Register B5H, C5H, D5H: TPIP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

The register reports the lower eight bits of the active offset.

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the TPIP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Register B6H, C6H, D6H: TPIP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	Reserved	0
Bit 4	R	CONCAT	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

Reserved:

The Reserved bit must be set low for the correct operation of the SPECTRA-155.

CONCAT:

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

EXTD:

The EXTD bit extends the TPIP registers to facilitate additional mapping. If this bit is set to logic 1 the register mapping, for the TPIP Status and Control

register, the TPIP Alarm Interrupt Status register and the TPIP Alarm Interrupt Enable registers are extended.

NDFPOR:

The NDFPOR (new data flag pointer of range) bit controls the definition of the NDF_enable indication for entry to the LOP state under 8xNDF_enable events. When NDFPOR is set high, for the purposes of detect of loss of events only, the definition of the NDF_enable indication does not require the pointer value to be within the range of 0 to 782. When NDFPOR is set low, NDF_enable indications require the pointer to be within 0 to 782.

Register B8H, C8H, D8H: TPIP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

This register reports the lower eight bits of the BIP-8 error counter.

Register B9H, C9H, D9H: TPIP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

This register reports the upper eight bits of the BIP-8 error counter.

BE[15:0]:

Bits BE[15:0] represent the number of path bit-interleaved parity errors that have been detected since the last time the path BIP-8 registers were polled by writing to the SPECTRA-155 Reset and Identity register. The write access transfers the internally accumulated error count to the path BIP-8 registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register BCH, CCH, DCH: TPIP Tributary Multiframe Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4	R/W	Reserved	0
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register reports the status of the multiframe framer and enables interrupts due to framer events.

Reserved:

The Reserved bits must be set low for correct operation of the SPECTRA-155.

COMAE:

The change of multiframe alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPECTRA-155 detect a change in the multiframe phase. When LOME is set high, an interrupt is generated upon change of multiframe alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI:

The change of multiframe alignment interrupt status bit (COMAI) is set high on changes in the multiframe alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

LOME:

The loss of multiframe interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of loss of multiframe indication (LOM). When LOME is set high, an interrupt is generated upon loss of multiframe. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV:

The loss of multiframe status bit (LOMV) reports the current state of the multiframe framer monitoring the receive stream. LOMV is set high when loss of multiframe is declared and is set low when multiframe alignment has been acquired.

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Register BDH, CDH, DDH: TPIP BIP Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

DISFS:

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU3 carrying a VC3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 (STM-0/AU3) stream. This bit is ignored when the SPECTRA-155 is processing an STS-3c (STM-1/AU4) stream.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated and reported on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic 1 is written to this bit, an incorrect SS bit pattern (i.e., $\neq$10) will prevent TPIP from issuing NDF_enable, inc_ind and dec_ind indications. When a logic 0 is written to this bit, the SS bits received do not affect active offset change events.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic 1 is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic 0 is written to this bit, pointer justification

indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Reserved:

The Reserved bits must be set to low for correct operation of SPECTRA-155.

Register E0H: SPECTRA-155 Clock Synthesis Source Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TREFSRC	0
Bit 0		Unused	X

TREFSRC:

The transmit reference source (TREFSRC) bit determines the expected source of the clock synthesis reference. If TREFSRC is a logic 0, the TRCLK+/- inputs are selected as the clock synthesis reference. If TREFSRC is a logic 1, the RRCLK+/- inputs are selected as the clock synthesis reference.

Register E1H: SPECTRA-155 Clock Recovery Source Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	RREFSRC	0
Bit 0		Unused	X

RREFSRC:

The receive reference source (RREFSRC) bit determines the expected source of the clock recovery reference. If RREFSRC is a logic 0, the RRCLK+/- inputs are selected as the clock recovery reference. If RREFSRC is a logic 1, the TRCLK+/- inputs are selected as the clock recovery reference.

Reserved:

The Reserved bit must be set to low for correct operation of SPECTRA-155.

Register E3H: SPECTRA-155 Transmit Path AIS Control #1

Bit	Type	Function	Default
Bit 7	R/W	LOPCONPAIS	0
Bit 6	R/W	PAISCONPAIS	0
Bit 5		UNUSED	0
Bit 4		UNUSED	0
Bit 3	R/W	LOPPAIS	0
Bit 2	R/W	LOMTUAIS	0
Bit 1	R/W	TPAIS_EN	0
Bit 0	R/W	PAISPAIS	0

This register controls the auto assertion of path/TU AIS. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register controls the assertion of path/TU AIS for the entire transmit stream. When configured for STS-3 (STM-1/AU3) mode, this register controls path/TU AIS assertion on the STS-1 (STM-0/AU3) #1 stream only.

PAISPAIS:

When set high, the PAISPAIS bit enables path AIS insertion on the transmit stream when path AIS is detected on the ADD bus. When PAISPAIS is set low, path AIS events have no effect on the transmit stream.

TPAIS_EN:

When set high, the TPAIS_EN bit enables path AIS insertion into the transmit stream via the DTPAIS[1] input signal. When TPAIS_EN is set low, it enables path AIS insertion into the STS-1 (STM-0/AU3) stream on the DROP bus via the DTPAIS[1] input signal. Only the TPAIS_EN bit is active for the STS-3c (STM-1/AU4) and STS-1 (STM-0/AU3) modes.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the transmit stream when loss of multiframe (LOM) events are detected on the ADD bus. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events have no effect on the transmit stream. LOMTUAIS must be set low when transmitting VT3 (TU3) payloads because the loss of multiframe condition does not exist.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the transmit stream when loss of pointer (LOP) events are detected on the ADD bus. When LOPPAIS is set low, loss of pointer events have no effect on the transmit stream.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enable path AIS insertion on the transmit stream when loss of concatenated pointer (LOPCON) event is detected on the ADD bus. When this bit is set low, the LOPCON event has no effect on the transmit stream.

This bit should only be used when the SPECTRA-155 is configured for STS-3c (STM-1/AU4) mode.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enable path AIS insertion on the transmit stream when path AIS concatenation event is detected on the ADD bus. When this bit is set low, the corresponding event has no effect on the transmit stream.

This bit should only be used when the SPECTRA-155 is configured for STS-3c (STM-1/AU4) mode.

Register E4H: SPECTRA-155 Transmit Path AIS Control #2

Bit	Type	Function	Default
Bit 7	R	SDBERV	X
Bit 6	R	SFBERV	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	LOPPAIS	0
Bit 2	R/W	LOMTUAIS	0
Bit 1	R/W	TPAIS_EN	0
Bit 0	R/W	PAISPAIS	0

This register controls the auto assertion of path/TU AIS. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used for PAIS assertion. When configured for STS-3 (STM-1/AU3) mode, this register controls path/TU AIS assertion on the STS-1 (STM-0/AU3) #2 stream only.

PAISPAIS:

When set high, the PAISPAIS bit enables path AIS insertion on the transmit stream when path AIS is detected on the ADD bus. When PAISPAIS is set low, path AIS events have no effect on the transmit stream.

TPAIS_EN:

When set high, the TPAIS_EN bit enables path AIS insertion into the transmit stream via the DTPAIS[2] input signal. When TPAIS_EN is set low, it enables path AIS insertion into the STS-1 (STM-0/AU3) stream on the DROP bus via the DTPAIS[2] input signal.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the transmit stream when loss of multiframe (LOM) events are detected on the ADD bus. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events have no effect on the transmit stream. LOMTUAIS must be set low when transmitting VT3 (TU3) payloads because the loss of multiframe condition does not exist.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the transmit stream when loss of pointer (LOP) events are detected on the ADD bus. When LOPPAIS is set low, loss of pointer events have no effect on the transmit stream.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers. This bit is the same as the SFBERV bit in the RASE Interrupt Status register.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers. This bit is the same as the SDBERV bit in the RASE Interrupt Status register.

Register E5H: SPECTRA-155 Transmit Path AIS Control #3 / Auxiliary Signal Interrupt Status

Bit	Type	Function	Default
Bit 7	W	SDI	X
Bit 6	W	SFI	X
Bit 5	R/W	SDIEN	0
Bit 4	R/W	SFIEN	0
Bit 3	R/W	LOPPAIS	0
Bit 2	R/W	LOMTUAIS	0
Bit 1	R/W	TPAIS_EN	0
Bit 0	R/W	PAISPAIS	0

This register controls the auto assertion of path/TU AIS and interrupt generation. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used for PAIS assertion. When configured for STS-3 (STM-1/AU3) mode, this register controls path/TU AIS assertion on the STS-1 (STM-0/AU3) #3 stream only.

PAISPAIS:

When set high, the PAISPAIS bit enables path AIS insertion on the transmit stream when path AIS is detected on the ADD bus. When PAISPAIS is set low, path AIS events have no effect on the transmit stream.

TPAIS_EN:

When set high, the TPAIS_EN bit enables path AIS insertion into the transmit stream via the DTPAIS[3] input signal. When TPAIS_EN is set low, it enables path AIS insertion into the STS-1 (STM-0/AU3) stream on the DROP bus via the DTPAIS[3] input signal.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the transmit stream when loss of multiframe (LOM) events are detected on the ADD bus. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events have no effect on the transmit stream. LOMTUAIS must be set low when transmitting VT3 (TU3) payloads because the loss of multiframe condition does not exist.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the transmit stream when loss of pointer (LOP) events are detected on the ADD bus. When LOPPAIS is set low, loss of pointer events have no effect on the transmit stream.

SFIEN, SDIEN:

The interrupt enable bits control interrupt generation on output INTB by the corresponding SFI and SDI bits. Note, these enable bits do not affect the actual interrupt bits.

SFI, SDI:

The signal fail interrupt (SFI) and signal degrade interrupt (SDI) bits indicate when the signal fail threshold and signal degrade thresholds have been crossed as controlled using RASE registers. These interrupt bits are the same as the SFBERI and SDBERI bits found in the RASE Interrupt Status register with the exception that they do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

Register E6H: SPECTRA-155 Auxiliary Section/Line Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	TROOLI	X
Bit 6	R/W	RDOOLI	X
Bit 5		Unused	X
Bit 4	R/W	OOFI	X
Bit 3	R/W	LRDII	X
Bit 2	R/W	LAISI	X
Bit 1	R/W	LOFI	X
Bit 0	R/W	LOSI	X

The SPECTRA-155 Auxiliary Section/Line Interrupt Status register replicates section and line interrupts that can be found in the CRU, CSU, RSOP and RLOP registers. However, unlike the above interrupt register bits that clear on reads, the SPECTRA-155 Auxiliary Section/Line Interrupt Status register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

LOSI:

The LOSI bit is set high when loss of signal is declared or removed.

LOFI:

The LOFI bit is set high when loss of frame is declared or removed.

LAISI:

The LAISI bit is set high when line LAIS is declared or removed.

LRDII:

The LRDII bit is set high when line RDI is declared or removed.

OOFI:

The OOFI bit is set high when out of frame is declared or removed.

RDOOLI:

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the DOOLV bit of the SPECTRA-155 CRSI Clock Recovery Control, Status and Interrupt register changes state. DOOLV is a logic one if

the divided down recovered clock frequency is not within 488 ppm of the RRCLK+/- (TRCLK+/-) frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods.

TROOLI:

The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is set high when the ROOLV bit of the SPECTRA-155 CSPI Clock Synthesis Control, Status and Interrupt register changes state. ROOLV indicates the clock synthesis phase locked loop is unable to lock to the reference on TRCLK+/- (RRCLK+/-) and is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the TRCLK+/- (RRCLK+/-) frequency.

Register E7H: SPECTRA-155 Auxiliary Path Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R/W	PRDII	X
Bit 6	R/W	PAISI	X
Bit 5	R/W	PSLUI	X
Bit 4	R/W	PSLMI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	TIUI	X
Bit 0	R/W	TIMI	X

The SPECTRA-155 Auxiliary Path Interrupt Status #1 register replicates path interrupts that can be found in the RPOP #1 and SPTB #1 registers. However, unlike the RPOP #1 and SPTB #1 interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

TIMI:

The path trace identifier mismatch interrupt status bit (TIMI) is set high on changes in the path trace identifier mismatch status.

TIUI:

The path trace identifier unstable interrupt status bit (TIUI) is set high on changes in the path trace identifier unstable status (mode 1).

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status.

LOPI:

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PSLMI:

The path signal label mismatch interrupt status bit (PSLMI) is set high on changes in the path signal label mismatch status.

PSLUI:

The path signal label unstable interrupt status bit (PSLUI) is set high on changes in the path signal label unstable status.

PAISI:

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

PRDII:

The path RDI interrupt status bit (PRDII) is set high on changes in the path remote defect indication status.

Register E8H: SPECTRA-155 Auxiliary Path Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R/W	PRDII	X
Bit 6	R/W	PAISI	X
Bit 5	R/W	PSLUI	X
Bit 4	R/W	PSLMI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	TIUI	X
Bit 0	R/W	TIMI	X

The SPECTRA-155 Auxiliary Path Interrupt Status #2 register replicates path interrupts that can be found in the RPOP #2 and SPTB #2 registers. However, unlike the RPOP #2 and SPTB #2 interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

TIMI:

The path trace identifier mismatch interrupt status bit (TIMI) is set high on changes in the path trace identifier mismatch status.

TIUI:

The path trace identifier unstable interrupt status bit (TIUI) is set high on changes in the path trace identifier unstable status (mode 1).

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status.

LOPI:

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PSLMI:

The path signal label mismatch interrupt status bit (PSLMI) is set high on changes in the path signal label mismatch status.

PSLUI:

The path signal label unstable interrupt status bit (PSLUI) is set high on changes in the path signal label unstable status.

PAISI:

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

PRDII:

The path RDI interrupt status bit (PRDII) is set high on changes in the path remote defect indication status.

Register E9H: SPECTRA-155 Auxiliary Path Interrupt Status #3

Bit	Type	Function	Default
Bit 7	R/W	PRDII	X
Bit 6	R/W	PAISI	X
Bit 5	R/W	PSLUI	X
Bit 4	R/W	PSLMI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	TIUI	X
Bit 0	R/W	TIMI	X

The SPECTRA-155 Auxiliary Path Interrupt Status #3 register replicates path interrupts that can be found in the RPOP #3 and SPTB #3 registers. However, unlike the RPOP #3 and SPTB #3 interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

TIMI:

The path trace identifier mismatch interrupt status bit (TIMI) is set high on changes in the path trace identifier mismatch status.

TIUI:

The path trace identifier unstable interrupt status bit (TIUI) is set high on changes in the path trace identifier unstable status (mode 1).

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status.

LOPI:

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PSLMI:

The path signal label mismatch interrupt status bit (PSLMI) is set high on changes in the path signal label mismatch status.

PSLUI:

The path signal label unstable interrupt status bit (PSLUI) is set high on changes in the path signal label unstable status.

PAISI:

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

PRDII:

The path RDI interrupt status bit (PRDII) is set high on changes in the path remote defect indication status.

Register EAH: SPECTRA-155 Auxiliary Path Enhanced Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	LOPCONI	X
Bit 6	R/W	PAISCONI	X
Bit 5	R/W	TIU2I#3	X
Bit 4	R/W	TIU2I#2	X
Bit 3	R/W	TIU2I#1	X
Bit 2	R/W	EPRDII#3	X
Bit 1	R/W	EPRDII#2	X
Bit 0	R/W	EPRDII#1	X

The SPECTRA-155 Auxiliary Path Enhanced Interrupt Status register replicates path interrupts that can be found in the RPOP #1, RPOP #2 and RPOP #3 registers. However, unlike the RPOP #1, RPOP #2 and RPOP #3 interrupt register bits that clear on reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

EPRDII#1, EPRDII#2, EPRDII#3:

The enhanced path remote defect indication interrupt (EPRDII) bits are set high when the corresponding RPOP #n detects a change in the enhanced path remote defect state.

TIU2I#1, TIU2I#2, TIU2I#3:

The path trace identifier unstable mode 2 interrupt status bit (TIU2I) is set high on changes in the path trace identifier unstable status for mode 2 operation.

PAISCONI:

The path AIS concatenation interrupt (PAISCONI) bit is set high when the SPECTRA-155 is configured for STS-3c (STM-1/AU4) mode and there is a change of the path AIS concatenation state. Please refer to the RPOP #1 Status and Control register for the new path AIS concatenation state.

LOPCONI:

The loss of pointer concatenation interrupt (LOPCONI) bit is set high when the SPECTRA-155 is configured for STS-3c (STM-1/AU4) mode and there is a change of the pointer concatenation state. Please refer to the RPOP #1 Status and Control register for the new pointer concatenation state.

Register EBH: SPECTRA-155 Trace Message Mode 2 Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	PTIU2IE#3	0
Bit 6	R/W	PTIU2IE#2	0
Bit 5	R/W	PTIU2IE#1	0
Bit 4	R/W	STIU2IE	0
Bit 5	R	PTIU2I#3	X
Bit 4	R	PTIU2I#2	X
Bit 3	R	PTIU2I#1	X
Bit 0	R	STIU2I	X

The SPECTRA-155 Trace Message Mode 2 Interrupt Status register indicates section trace message (J0 byte) and path trace message (J1 byte) unstable states changes when operating in mode 2.

STIU2I:

The section trace identifier message unstable mode 2 interrupt status bit is set high when stable/unstable status of the section trace identifier framer changes state. This bit and the interrupt are cleared when this register is read.

PTIU2I#1, PTIU2I#2, PTIU2I#3:

The path trace identifier message unstable mode 2 interrupt status bit is set high when stable/unstable status of the path trace identifier framer changes state. This bit and the interrupt are cleared when this register is read.

STIU2IE:

The section trace identifier message unstable interrupt enable bit controls the activation of the interrupt output when the receive section identifier message state changes from stable to unstable and vice versa. The stable state is entered when the same identifier byte is received for forty eight consecutive SONET/SDH frames. The unstable state is entered when one or more errors are detected in a sixteen byte window and three consecutive sixteen byte windows are in error. When STIU2IE is set high, changes in the receive section trace identifier message stable/unstable state will activate the interrupt (INTB) output. When STIU2IE is set low, section trace identifier state changes will not affect INTB.

PTIU2IE#1, PTIU2IE#2, PTIU2IE#3:

The path trace identifier message unstable interrupt enable bit controls the activation of the interrupt output when the receive path identifier message state changes from stable to unstable and vice versa. The stable state is entered when the same identifier byte is received for forty eight consecutive SONET/SDH frames. The unstable state is entered when one or more errors are detected in a sixteen byte window and three consecutive sixteen byte windows are in error. When PTIU2IE#n is set high, changes in the receive path trace identifier message stable/unstable state of STS-1#n will activate the interrupt (INTB) output. When PTIU2IE#n is set low, path trace identifier state changes of STS-1#n will not affect INTB.

Register ECH: SPECTRA-155 Trace Message Mode 2 Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	PTIU2V#3	X
Bit 2	R	PTIU2V#2	X
Bit 1	R	PTIU2V#1	X
Bit 0	R	STIU2V	X

The SPECTRA-155 Trace Message Mode 2 Status register indicates section trace message (J0 byte) and path trace message (J1 byte) unstable states when operating in mode 2. In mode 2 operation, a stable condition is considered as receiving the same byte (J0 or J1) for forty-eight consecutive SONET/SDH frame.

STIU2V:

The section trace identifier message unstable value bit reports the stable/unstable status of the section identifier message framer. When high, the corresponding message framer is in the unstable state. When low, the corresponding message framer is in the stable state.

PTIU2V#1, PTIU2V#2, PTIU2V#3:

The path trace identifier message unstable value bit reports the stable/unstable status of the path identifier message framer. When high, the corresponding message framer is in the unstable state. When low, the corresponding message framer is in the stable state.

Register EDH: SPECTRA-155 Auto Trace Message Mode 1/2 Control

Bit	Type	Function	Default
Bit 7	R/W	AUTOPTIU1#3	0
Bit 6	R/W	AUTOPTIU1#2	0
Bit 5	R/W	AUTOPTIU1#1	0
Bit 4	R/W	AUTOSTIU1	0
Bit 3	R/W	AUTOPTIU2#3	0
Bit 2	R/W	AUTOPTIU2#2	0
Bit 1	R/W	AUTOPTIU2#1	0
Bit 0	R/W	AUTOSTIU2	0

The SPECTRA-155 Auto Trace Message Mode 1/2 Control register along with individual alarm enable registers listed in the bit descriptions allow auto assertion of consequential actions based on mode 1 and mode 2 section trace message (J0 byte) and path trace message (J1 byte) unstable states.

AUTOSTIU2:

The auto section trace identifier unstable mode 2 bit controls auto assertion of a consequential action (receive Path AIS and/or Line RDI) due to the detection of a section mode 2 trace identifier unstable (TIU) state. When AUTOSTIU2 is set high, mode 2 TIU can automatically assert receive Line AIS as controlled by the RTIUINS bit in the SPECTRA-155 Receive Line AIS Control register or Line RDI as controlled using the RTIUINS bit in the SPECTRA-155 Receive Line RDI Control register. When AUTOSTIU2 is set low, mode 2 TIU does not affect consequential actions.

AUTOPTIU2#1, AUTOPTIU2#2, AUTOPTIU2#3:

The auto path trace identifier unstable mode 2 bit controls auto assertion of a consequential action (receive Path AIS, Path RDI, Enhanced Path RDI, and/or DS3 AIS) due to the detection of a path mode 2 trace identifier unstable (TIU) state.

When AUTOPTIU2 is set high, mode 2 TIU can automatically assert receive Path AIS as controlled by the corresponding TIUPAIS bit in the SPECTRA-155 Receive Path AIS Control (#1, #2, #3) registers or Path RDI as controlled using the corresponding TIUPRDI bit in the SPECTRA-155 Path REI/RDI Control (#1, #2, #3) registers or Enhanced Path RDI as controlled using the corresponding TIUEPRDI bit in the SPECTRA-155 Enhanced Path RDI Control (#1, #2, #3) registers or DS3 AIS as controlled using the

corresponding TIUDS3AIS bit in the SPECTRA-155 Path and DS3 Receive AIS Control (#1, #2, #3) registers. When AUTOPTIU2 is set low, mode 2 TIU does not affect consequential actions.

AUTOSTIU1:

The auto section trace identifier unstable mode 1 bit controls auto assertion of a consequential action (receive Path AIS and/or Line RDI) due to the detection of a section mode 1 trace identifier unstable (TIU) state. Mode 1 section trace is detected using the SSTB block. When AUTOSTIU1 is set high, mode 1 TIU can automatically assert receive Line AIS as controlled by the RTIUINS bit in the SPECTRA-155 Receive Line AIS Control register or Line RDI as controlled using the RTIUINS bit in the SPECTRA-155 Receive Line RDI Control register. When AUTOSTIU1 is set low, mode 1 TIU does not affect consequential actions.

AUTOPTIU1#1, AUTOPTIU1#2, AUTOPTIU1#3:

The auto path trace identifier unstable mode 1 bit controls auto assertion of a consequential action (receive Path AIS, Path RDI, Enhanced Path RDI, and/or DS3 AIS) due to the detection of a path mode 1 trace identifier unstable (TIU) state. Mode 1 path trace is detected using the three SPTB blocks.

When AUTOPTIU1 is set high, mode 1 TIU can automatically assert receive Path AIS as controlled by the corresponding TIUPAIS bit in the SPECTRA-155 Receive Path AIS Control (#1, #2, #3) registers or Path RDI as controlled using the corresponding TIUPRDI bit in the SPECTRA-155 Path REI/RDI Control (#1, #2, #3) registers or Enhanced Path RDI as controlled using the corresponding TIUEPRDI bit in the SPECTRA-155 Enhanced Path RDI Control (#1, #2, #3) registers or DS3 AIS as controlled using the corresponding TIUDS3AIS bit in the SPECTRA-155 Path and DS3 Receive AIS Control (#1, #2, #3) registers. When AUTOPTIU1 is set low, mode 1 TIU does not affect consequential actions.

Register EFH: SPECTRA-155 Receive Concat Path AIS, RDI and Enhanced RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPRDI	0
Bit 6	R/W	NOPAISCONEPRDI	0
Bit 5	R/W	PAISCONPAIS	0
Bit 4		Unused	X
Bit 3	R/W	LOPCONPAIS	0
Bit 2		Unused	X
Bit 1	R/W	UNEQPRDI	1
Bit 0	R/W	UNEQEPRDI	1

This register along with the SPECTRA-155 Receive Path AIS Control #1 register controls the auto assertion of path AIS on the DROP bus. This register along with the SPECTRA-155 Path REI/RDI Control #1 register controls the auto assertion of path RDI on the transmit stream. This register along with the SPECTRA-155 Enhanced Path RDI Control #1 register controls the auto assertion of path RDI on the transmit stream.

When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register controls the entire SONET/SDH stream. When configured for STS-3 (STM-1/AU3) mode, this register controls path AIS, path RDI and enhanced path RDI assertion on the STS-1 (STM-0/AU3) #1 only.

UNEQEPRDI:

When set high, the UNEQEPRDI bit enables enhanced path RDI assertion when the path signal label in the receive stream indicates unequipped status. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When UNEQEPRDI is set low, path signal label unequipped status has no effect on enhanced path RDI.

UNEQPRDI:

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enables path AIS insertion on the DROP bus when loss of pointer concatenation (LOPCON) events are detected in the receive STS-1 (STM-0/AU3) #2 or #3 streams. When LOPCONPAIS is set low, loss of pointer concatenation events have no effect on the DROP bus.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enables path AIS insertion on the DROP bus when Path AIS concatenation (PAISCON) events are detected in the receive STS-1 (STM-0/AU3) #2 or #3 streams. When PAISCONPAIS is set low, Path AIS concatenation events have no effect on the DROP bus.

NOPAISCONEPRDI:

When set high, the NOPAISCONEPRDI bit disables enhanced path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOPAISCONEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOPAISCONEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

PAISCONPRDI:

When set high, the PAISCONPRDI bit enables path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPRDI is set low, path AIS concatenation events have no effect on path RDI.

Register F0H: SPECTRA-155 Receive Path AIS Control #2

Bit	Type	Function	Default
Bit 7	R/W	RXSEL[1]	0
Bit 6	R/W	RXSEL[0]	0
Bit 5	R/W	PSLUPAIS	1
Bit 4	R/W	PSLMPAIS	1
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	LOMTUAIS	1
Bit 1	R/W	TIUPAIS	1
Bit 0	R/W	TIMPAIS	1

This register controls the auto assertion of path AIS on the DROP bus. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used except the LOMTUAIS bit (described below). When configured for STS-3 (STM-1/AU3) mode, this register controls path AIS assertion on the STS-1 (STM-0/AU3) #2 DROP bus stream only. In STS-3c (STM-1/AU4) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in TUG3 #2. In STS-3 (STM-1/AU3) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in VC-3 #2.

TIMPAIS:

When set high, the TIMPAIS bit enables path AIS insertion on the DROP bus when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

TIUPAIS:

When set high, the TIUPAIS bit enables path AIS insertion on the DROP bus when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUPAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the DROP bus when loss of multiframe (LOM) events are detected in the receive stream. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events

have no effect on the DROP bus. In STS-3c (STM-1/AU4) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in TUG3 #2. In STS-3 (STM-1/AU3) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in VC-3 #2. LOMTUAIS must be set low when processing TU3 or payload not requiring tributary multiframe alignment.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the DROP bus when loss of pointer (LOP) events are detected in the receive stream. When LOPPAIS is set low, loss of pointer events have no effect on the DROP bus.

PSLMPAIS:

When set high, the PSLMPAIS bit enables path AIS insertion on the DROP bus when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPAIS is set low, path signal label mismatch events have no effect on the DROP bus.

PSLUPAIS:

When set high, the PSLUPAIS bit enables path AIS insertion on the DROP bus when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUPAIS is set low, path signal label unstable events have no effect on the DROP bus.

RXSEL[1:0]:

The RXSEL[1:0] bits controls the source of the associated receive section of the transmit stream. When RXSEL[1:0] is set to 'b00, the receive section is chosen to be one in the local SPECTRA-155. The path REI count and path RDI status of the transmit stream is derived from the local RPOP. When RXSEL[1:0] is set to 'b01, a remote receive section is chosen and it reports the detected path BIP-8 error count and the path AIS status of its DROP bus via the transmit alarm port. The path status byte in the transmit stream carries the path REI and path RDI indications reported in the transmit alarm port. When RXSEL[1:0] is set to 'b10, inband error reporting is chosen. The associated receive section forms a new G1 byte reporting on the path BIP-8 errors detected and path AIS status. The SPECTRA-155 does not support inband error reporting of enhanced RDI codes. To enable inband reporting of non-enhanced RDI codes, the SPECTRA-155 must be configured to generate path AIS on the drop bus for all events which can cause RDI. The local transmit section pass the path REI and path RDI bits on the ADD bus to the transmit stream unmodified. When RXSEL[1:0] is set to 'b11, the path status byte in the transmit stream is not associate with any receive stream. No path REI nor path RDI will be reported.

Table 29 - RXSEL[1:0] codepoints for STS-1 #2.

RXSEL[1:0]	Source
00	local SPECTRA-155
01	remote receive (TAP port)
10	inband reporting
11	no reporting

Register F1H: SPECTRA-155 Receive Path AIS Control #3

Bit	Type	Function	Default
Bit 7	R/W	RXSEL[1]	0
Bit 6	R/W	RXSEL[0]	0
Bit 5	R/W	PSLUPAIS	1
Bit 4	R/W	PSLMPAIS	1
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	LOMTUAIS	1
Bit 1	R/W	TIUPAIS	1
Bit 0	R/W	TIMPAIS	1

This register controls the auto assertion of path AIS on the DROP bus. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used except the LOMTUAIS bit (described low). When configured for STS-3 (STM-1/AU3) mode, this register controls path AIS assertion on the STS-1 (STM-0/AU3) #3 DROP bus stream only. In STS-3c (STM-1/AU4) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in TUG3 #3. In STS-3 (STM-1/AU3) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in VC-3 #3.

TIMPAIS:

When set high, the TIMPAIS bit enables path AIS insertion on the DROP bus when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

TIUPAIS:

When set high, the TIUPAIS bit enables path AIS insertion on the DROP bus when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUPAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the DROP bus when loss of multiframe (LOM) events are detected in the receive stream. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events

have no effect on the DROP bus. In STS-3c (STM-1/AU4) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in TUG3 #3. In STS-3 (STM-1/AU3) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in VC-3 #3. LOMTUAIS must be set low when processing TU3 or payload not requiring tributary multiframe alignment.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the DROP bus when loss of pointer (LOP) events are detected in the receive stream. When LOPPAIS is set low, loss of pointer events have no effect on the DROP bus.

PSLMPAIS:

When set high, the PSLMPAIS bit enables path AIS insertion on the DROP bus when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPAIS is set low, path signal label mismatch events have no effect on the DROP bus.

PSLUPAIS:

When set high, the PSLUPAIS bit enables path AIS insertion on the DROP bus when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUPAIS is set low, path signal label unstable events have no effect on the DROP bus.

RXSEL[1:0]:

The RXSEL[1:0] bits controls the source of the associated receive section of the transmit stream. When RXSEL[1:0] is set to 'b00, the receive section is chosen to be one in the local SPECTRA-155. The path REI count and path RDI status of the transmit stream is derived from the local RPOP. When RXSEL[1:0] is set to 'b01, a remote receive section is chosen and it reports the detected path BIP-8 error count and the path AIS status of its DROP bus via the transmit alarm port. The path status byte in the transmit stream carries the path REI and path RDI indications reported in the transmit alarm port. When RXSEL[1:0] is set to 'b10, inband error reporting is chosen. The associated receive section forms a new G1 byte reporting on the path BIP-8 errors detected and path AIS status. The SPECTRA-155 does not support inband error reporting of enhanced RDI codes. To enable inband reporting of non-enhanced RDI codes, the SPECTRA-155 must be configured to generate path AIS on the drop bus for all events which can cause RDI. The local transmit section pass the path REI and path RDI bits on the ADD bus to the transmit stream unmodified. When RXSEL[1:0] is set to 'b11, the path status byte in the transmit stream is not associate with any receive stream. No path REI nor path RDI will be reported.

Table 30 - RXSEL[1:0] codepoints for STS-1 #3.

RXSEL[1:0]	Source
00	local SPECTRA-155
01	remote receive (TAP port)
10	inband reporting
11	no reporting

Register F2H: SPECTRA-155 Path REI/RDI Control #2

Bit	Type	Function	Default
Bit 7	R/W	AUTOPREI	0
Bit 6	R/W	ALMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	PSLMPRDI	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	UNEQPRDI	1
Bit 1	R/W	TIUPRDI	1
Bit 0	R/W	TIMPRDI	1

This register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP #2 or a mate TPOP #2 via the RAD PRDI5 bit position. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used. When configured for STS-3 (STM-1/AU3) mode, this register controls the assertion of path RDI for the STS-1 (STM-0/AU3) #2 only.

TIMPRDI:

When set high, the TIMPRDI bit enables path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPRDI is set low, trace identifier mismatch events have no effect on path RDI.

TIUPRDI:

When set high, the TIUPRDI bit enables path RDI assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUPRDI is set low, trace identifier mismatch events have no effect on path RDI.

UNEQPRDI:

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

LOPPRDI:

When set high, the LOPPRDI bit enables path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPRDI is set low, loss of pointer events have no effect on path RDI.

PSLMPRDI:

When set high, the PSLMPRDI bit enables path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPRDI is set low, path signal label mismatch events have no effect on path RDI.

PAISPRDI:

When set high, the PAISPRDI bit enables path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When PAISPRDI is set low, PAIS states have no effect on path RDI.

ALMPRDI:

When set high, the ALMPRDI bit enables path RDI assertion when loss of signal (LOS), loss of frame (LOF), line alarm indication signal (LAIS) events are detected in the receive stream. When ALMPRDI is set low, the above events have no effect on path RDI.

AUTOPREI:

The AUTOPREI bit enables the automatic insertion of path REI events in the local or mate transmitter. When AUTOPREI is a logic one, receive B3 errors detected by the SPECTRA-155 are automatically inserted in the G1 byte of the local transmit stream (as enabled using the RXSEL[1:0] bits in the SPECTRA-155 Path REI/RDI Control #2 register). In addition, REI events are indicated on the RAD[2] output. When AUTOPREI is a logic zero, path REI events are not automatically inserted in the local transmit stream. In addition, REI events are not indicated on the RAD[2] output.

Register F3H: SPECTRA-155 Path REI/RDI Control #3

Bit	Type	Function	Default
Bit 7	R/W	AUTOPREI	0
Bit 6	R/W	ALMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	PSLMPRDI	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	UNEQPRDI	1
Bit 1	R/W	TIUPRDI	1
Bit 0	R/W	TIMPRDI	1

This register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP #3 or a mate TPOP #3 via the RAD PRDI5 bit position. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used. When configured for STS-3 (STM-1/AU3) mode, this register controls the assertion of path RDI for the STS-1 (STM-0/AU3) #3 only.

TIMPRDI:

When set high, the TIMPRDI bit enables path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPRDI is set low, trace identifier mismatch events have no effect on path RDI.

TIUPRDI:

When set high, the TIUPRDI bit enables path RDI assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUPRDI is set low, trace identifier mismatch events have no effect on path RDI.

UNEQPRDI:

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

LOPPRDI:

When set high, the LOPPRDI bit enables path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPRDI is set low, loss of pointer events have no effect on path RDI.

PSLMPRDI:

When set high, the PSLMPRDI bit enables path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPRDI is set low, path signal label mismatch events have no effect on path RDI.

PAISPRDI:

When set high, the PAISPRDI bit enables path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When PAISPRDI is set low, PAIS states have no effect on path RDI.

ALMPRDI:

When set high, the ALMPRDI bit enables path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMPRDI is set low, the above events have no effect on path RDI.

AUTOPREI:

The AUTOPREI bit enables the automatic insertion of path REI events in the local or mate transmitter. When AUTOPREI is a logic one, receive B3 errors detected by the SPECTRA-155 are automatically inserted in the G1 byte of the local transmit stream (as enabled using the RXSEL[1:0] bits in the SPECTRA-155 Path REI/RDI Control #3 register). In addition, REI events are indicated on the RAD[3] output. When AUTOPREI is a logic zero, path REI events are not automatically inserted in the local transmit stream. In addition, REI events are not indicated on the RAD[3] output.

Register F4H: SPECTRA-155 Enhanced Path RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	EPRDI_EN	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	R/W	PSLMEPRDI	1
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	NOLOPCONEPRDI	0
Bit 1	R/W	TIUEPRDI	0
Bit 0	R/W	TIMEPRDI	1

This register and the SPECTRA-155 Path REI/RDI Control #1 register controls the auto assertion of enhanced path RDI (G1 bits 5,6,7) in the local TPOP #1 or a mate TPOP #1 via the RAD PRDI5, PRDI6 and PRDI7 bit positions. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register with it's companion register controls auto enhanced path RDI assertion on the entire transmit stream. When configured for STS-3 (STM-1/AU3) mode, this register controls the assertion of enhanced path RDI for the STS-1 (STM-0/AU3) #1 only.

TIMEPRDI:

When set high, the TIMEPRDI bit enables enhanced path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIMEPRDI is set low, trace identifier mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

TIUEPRDI:

When set high, the TIUEPRDI bit enables enhanced path RDI assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIUEPRDI is set low, trace identifier unstable events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOLOPCONEPRDI:

When set high, the NOLOPCONEPRDI bit disables enhanced path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOLOPCONEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOLOPCONEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

NOLOPEPRDI:

When set high, the NOLOPEPRDI bit disables enhanced path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOLOPEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOLOPEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

PSLMEPRDI:

When set high, the PSLMEPRDI bit enables enhanced path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLMEPRDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOPAISEPRDI:

When set high, the NOPAISEPRDI bit disables enhanced path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD

output PRDI7 bit position) is set high. NOPAISEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOPAISEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

NOALMEPRDI:

When set high, the NOALMEPRDI bit disables enhanced path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. If enabled, when these events occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOALMEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOALMEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

EPRDI_EN:

The EPRDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter or in a mate transmitter via the RAD output. When EPRDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register and in the SPECTRA-155 Path REI/RDI Control #1 register. When EPRDI_EN is a logic zero, enhanced path REI is not automatically inserted in the transmit stream.

Register F5H: SPECTRA-155 Enhanced Path RDI Control #2

Bit	Type	Function	Default
Bit 7	R/W	EPRDI_EN	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	R/W	PSLMEPRDI	1
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	UNEQEPRDI	1
Bit 1	R/W	TIUEPRDI	0
Bit 0	R/W	TIMEPRDI	1

This register and the SPECTRA-155 Path REI/RDI Control #2 register controls the auto assertion of enhanced path RDI (G1 bits 5,6,7) in the local TPOP #2 or a mate TPOP #2 via the RAD PRDI5, PRDI6 and PRDI7 bit positions. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used. When configured for STS-3 (STM-1/AU3) mode, this register controls the assertion of enhanced path RDI for the STS-1 (STM-0/AU3) #2 only.

TIMEPRDI:

When set high, the TIMEPRDI bit enables enhanced path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIMEPRDI is set low, trace identifier mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

TIUEPRDI:

When set high, the TIUEPRDI bit enables enhanced path RDI assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIUEPRDI is set low, trace identifier unstable events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

UNEQEPRDI:

When set high, the UNEQEPRDI bit enables enhanced path RDI assertion when the path signal label in the receive stream indicates unequipped status. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When UNEQEPRDI is set low, path signal label unequipped status has no effect on enhanced path RDI.

NOLOPEPRDI:

When set high, the NOLOPEPRDI bit disables enhanced path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOLOPEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOLOPEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

PSLMEPRDI:

When set high, the PSLMEPRDI bit enables enhanced path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLMEPRDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOPAISEPRDI:

When set high, the NOPAISEPRDI bit disables enhanced path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOPAISEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOPAISEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

NOALMEPRDI:

When set high, the NOALMEPRDI bit disables enhanced path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. If enabled, when these events occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOALMEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOALMEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

EPRDI_EN:

The EPRDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter or in a mate transmitter via the RAD output. When EPRDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register and in the SPECTRA-155 Path RDI Control #2 register. When EPRDI_EN is a logic zero, enhanced path REI is not automatically inserted in the transmit stream.

Register F6H: SPECTRA-155 Enhanced Path RDI Control #3

Bit	Type	Function	Default
Bit 7	R/W	EPRDI_EN	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	R/W	PSLMEPRDI	1
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	UNEQEPRDI	1
Bit 1	R/W	TIUEPRDI	0
Bit 0	R/W	TIMEPRDI	1

This register and the SPECTRA-155 Path REI/RDI Control #3 register controls the auto assertion of enhanced path RDI (G1 bits 5,6,7) in the local TPOP #3 or a mate TPOP #3 via the RAD PRDI5, PRDI6 and PRDI7 bit positions. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register is not used. When configured for STS-3 (STM-1/AU3) mode, this register controls the assertion of enhanced path RDI for the STS-1 (STM-0/AU3) #3 only.

TIMEPRDI:

When set high, the TIMEPRDI bit enables enhanced path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIMEPRDI is set low, trace identifier mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

TIUEPRDI:

When set high, the TIUEPRDI bit enables enhanced path RDI assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIUEPRDI is set low, trace identifier unstable events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

UNEQEPRDI:

When set high, the UNEQEPRDI bit enables enhanced path RDI assertion when the path signal label in the receive stream indicates unequipped status. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When UNEQEPRDI is set low, path signal label unequipped status has no effect on enhanced path RDI.

NOLOPEPRDI:

When set high, the NOLOPEPRDI bit disables enhanced path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOLOPEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOLOPEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

PSLMEPRDI:

When set high, the PSLMEPRDI bit enables enhanced path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLMEPRDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOPAISEPRDI:

When set high, the NOPAISEPRDI bit disables enhanced path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOPAISEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOPAISEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

NOALMEPRDI:

When set high, the NOALMEPRDI bit disables enhanced path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. If enabled, when these events occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. NOALMEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOALMEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

EPRDI_EN:

The EPRDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter or in a mate transmitter via the RAD output. When EPRDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register and in the SPECTRA-155 Path REI/RDI Control #3 register. When EPRDI_EN is a logic zero, enhanced path REI is not automatically inserted in the transmit stream.

Register F7H: SPECTRA-155 Auxiliary Section/Line Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	TROOLIEN	0
Bit 6	R/W	RDOOLIEN	0
Bit 5		Unused	X
Bit 4	R/W	OOFIEN	0
Bit 3	R/W	LRDIIEN	0
Bit 2	R/W	LAISIEN	0
Bit 1	R/W	LOFIEN	0
Bit 0	R/W	LOSIEN	0

LOSIEN, LOFIEN, LAISIEN, LRDIIEN, OOFIEN, RDOOLIEN, TROOLIEN:

The interrupt enable bits control interrupt generation on output INTB by the corresponding bit in the SPECTRA-155 Auxiliary Section/Line Interrupt Status register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-155 Auxiliary Section/Line Interrupt Status register.

Register F8H: SPECTRA-155 Auxiliary Path Interrupt Enable #1

Bit	Type	Function	Default
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PAISEN	0
Bit 5	R/W	PSLUIEN	0
Bit 4	R/W	PSLMIEN	0
Bit 3	R/W	LOPIEN	0
Bit 2	R/W	LOMIEN	0
Bit 1	R/W	TIUIEN	0
Bit 0	R/W	TIMIEN	0

TIMIEN, TIUIEN, LOMIEN, LOPIEN, PSLMIEN, PSLUIEN, PAISEN, PRDIEN:

The interrupt enable bits control interrupt generation on output INTB by the corresponding bit in the SPECTRA-155 Auxiliary Path Interrupt Status #1 register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-155 Auxiliary Path Interrupt Status #1 register. This register is associated with the STS-1 (STM-0/AU3) #1 of an STS-3 (STM-1/AU3) stream or an STS-3c (STM-1/AU4) stream or an STS-1 (STM-0/AU3) stream.

Register F9H: SPECTRA-155 Auxiliary Path Interrupt Enable #2

Bit	Type	Function	Default
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PAISEN	0
Bit 5	R/W	PSLUIEN	0
Bit 4	R/W	PSLMIEN	0
Bit 3	R/W	LOPIEN	0
Bit 2	R/W	LOMIEN	0
Bit 1	R/W	TIUIEN	0
Bit 0	R/W	TIMIEN	0

TIMIEN, TIUIEN, LOMIEN, LOPIEN, PSLMIEN, PSLUIEN, PAISEN, PRDIEN:

The interrupt enable bits control interrupt generation on output INTB by the corresponding bit in the SPECTRA-155 Auxiliary Path Interrupt Status #2 register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-155 Auxiliary Path Interrupt Status #2 register. This register is associated with the STS-1 (STM-0/AU3) #2 of an STS-3 (STM-1/AU3) stream. It is invalid when SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode.

Register FAH: SPECTRA-155 Auxiliary Path Interrupt Enable #3

Bit	Type	Function	Default
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PAISEN	0
Bit 5	R/W	PSLUIEN	0
Bit 4	R/W	PSLMIEN	0
Bit 3	R/W	LOPIEN	0
Bit 2	R/W	LOMIEN	0
Bit 1	R/W	TIUIEN	0
Bit 0	R/W	TIMIEN	0

TIMIEN, TIUIEN, LOMIEN, LOPIEN, PSLMIEN, PSLUIEN, PAISEN, PRDIEN:

The interrupt enable bits control interrupt generation on output INTB by the corresponding bit in the SPECTRA-155 Auxiliary Path Interrupt Status #3 register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-155 Auxiliary Path Interrupt Status #3 register. This register is associated with the STS-1 (STM-0/AU3) #3 of an STS-3 (STM-1/AU3) stream. It is invalid when SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode.

Register FBH: SPECTRA-155 Auxiliary Path Enhanced Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LOPCONIEN	0
Bit 6	R/W	PAISCONIEN	0
Bit 5	R/W	TIU2I#3EN	0
Bit 4	R/W	TIU2I#2EN	0
Bit 3	R/W	TIU2I#1EN	0
Bit 2	R/W	EPRDII#3EN	0
Bit 1	R/W	EPRDII#2EN	0
Bit 0	R/W	EPRDII#1EN	0

EPRDII#1EN, EPRDII#2EN, EPRDII#3EN, TIU2I#1EN, TIU2I#2EN, TIU2I#3EN, PAISCONIEN, LOPCONIEN:

The interrupt enable bits control interrupt generation on output INTB by the corresponding bit in the SPECTRA-155 Auxiliary Path Enhanced Interrupt Status register. Note, these enable bits do not affect the actual interrupt bits found in the SPECTRA-155 Auxiliary Path Enhanced Interrupt Status register.

Register FCH: SPECTRA-155 Auxiliary Path Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current filtered value of the enhanced RDI codepoint (G1 bits 5, 6, & 7). When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, ERDIV[2:0] is the filtered enhanced RDI codepoint for the SONET/SDH stream. When configured for STS-3 (STM-1/AU3) mode, ERDIV[2:0] is the filtered enhanced RDI codepoint for the STS-1 (STM-0/AU3) #1 stream.

Filtering is controlled using the RDI10 bit in the corresponding RPOP #n, Pointer MSB register. This register reflects the same ERDIV[2:0] value that can be found in the corresponding RPOP #n, Status and Control (EXTD=1) register. This register can be used for interrupt handling if it is undesirable to use the EXTD feature.

Register FDH: SPECTRA-155 Auxiliary Path Status #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current filtered value of the enhanced RDI codepoint (G1 bits 5, 6, & 7). When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, ERDIV[2:0] is invalid. When configured for STS-3 (STM-1/AU3) mode, ERDIV[2:0] is the filtered enhanced RDI codepoint for the STS-1 (STM-0/AU3) #2 stream.

Filtering is controlled using the RDI10 bit in the corresponding RPOP #n, Pointer MSB register. This register reflects the same ERDIV[2:0] value that can be found in the corresponding RPOP #n, Status and Control (EXTD=1) register. This register can be used for interrupt handling if it is undesirable to use the EXTD feature.

Register FEH: SPECTRA-155 Auxiliary Path Status #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current filtered value of the enhanced RDI codepoint (G1 bits 5, 6, & 7). When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, ERDIV[2:0] is invalid. When configured for STS-3 (STM-1/AU3) mode, ERDIV[2:0] is the filtered enhanced RDI codepoint for the STS-1 (STM-0/AU3) #3 stream.

Filtering is controlled using the RDI10 bit in the corresponding RPOP #n, Pointer MSB register. This register reflects the same ERDIV[2:0] value that can be found in the corresponding RPOP #n, Status and Control (EXTD=1) register. This register can be used for interrupt handling if it is undesirable to use the EXTD feature.

Register 100H: SPECTRA-155 Path/Mapper Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISJ1V1	0
Bit 4	R/W	MONRS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	DISV1	0
Bit 1	R/W	ALMJ1V1	0
Bit 0		Unused	X

This register allows the operational mode of the SPECTRA-155 Path and Mapper functions to be configured.

ALMJ1V1:

When set high, the ALMJ1V1 bit disables the realignment of the Telecombus DROP side J1 and V1 indication on DC1J1V1 when the RPOP blocks are in the LOP or PAIS state. The J1 and V1 pulses will flywheel at their previous position prior to entry to the LOP or PAIS state.

DISV1:

When set high, the DISV1 bit configures the DC1J1V1, and GC1J1V1 outputs to mark only the frame and synchronous payload envelope (virtual container) alignments (C1 and J1 bytes). DC1J1V1 and GC1J1V1 will not indicate the tributary multiframe alignment. When DISV1 is set low, DC1J1V1 and GC1J1V1 mark all three of the frame, payload envelope and tributary multiframe alignments.

The DISV1 bit must be set high when byte or nibble data mode as selected by the SMODE[2:0] inputs is in operation. The DISV1 bit must also be set high when the built-in DROP bus PRBS generator and monitor are used.

MONRS:

When set high, the MONRS selects the receive side pointer justification events counters to monitor the receive stream directly. When MONRS is set low, the counters accumulates pointer justification events on the DROP bus.

DISJ1V1:

When set high, the DISJ1V1 bit configures the SPECTRA-155 to only expect C1 byte indications on the AC1J1V1 input or the SAC1J1V1 input. When only C1 byte indications are provided, the SPECTRA-155 will interpret the pointer of the ADD bus to identify the J1 and V1 byte positions. When set low, the SPECTRA-155 expects the AC1J1V1 input or the SAC1J1V1 input to indicate C1, J1 and V1.

DISJ1V1 is only valid when configured for Telecombus operation.

Reserved:

The Reserved bits must be set low for the correct operation of the SPECTRA-155.

Register 101H: SPECTRA-155 Receive Path AIS Control #1

Bit	Type	Function	Default
Bit 7	R/W	RXSEL[1]	0
Bit 6	R/W	RXSEL[0]	0
Bit 5	R/W	PSLUPAIS	1
Bit 4	R/W	PSLMPAIS	1
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	LOMTUAIS	1
Bit 1	R/W	TIUPAIS	1
Bit 0	R/W	TIMPAIS	1

This register along with the SPECTRA-155 Receive Additional Path AIS Control #1 register controls the auto assertion of path AIS on the DROP bus. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register controls the assertion of path AIS for the entire SONET/SDH DROP bus stream. When configured for STS-3 (STM-1/AU3) mode, this register controls path AIS assertion on the STS-1 (STM-0/AU3) #1 DROP bus stream only. In STS-3c (STM-1/AU4) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in TUG3 #1. In STS-3 (STM-1/AU3) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in VC-3 #1.

TIMPAIS:

When set high, the TIMPAIS bit enables path AIS insertion on the DROP bus when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPAIS is set low, trace identifier mismatch events have no effect on the DROP bus.

TIUPAIS:

When set high, the TIUPAIS bit enables path AIS insertion on the DROP bus when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUPAIS is set low, trace identifier unstable events have no effect on the DROP bus.

LOMTUAIS:

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the DROP bus when loss of multiframe (LOM) events are detected in the receive stream. The path overhead (POH), the fixed stuff, and the pointer bytes (H1,

H2) are unaffected. When LOMTUAIS is set low, loss of multiframe events have no effect on the DROP bus. In STS-3c (STM-1/AU4) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in TUG3 #1. In STS-3 (STM-1/AU3) mode, the LOMTUAIS bit controls the insertion of tributary path AIS in VC-3 #1. LOMTUAIS must be set low when processing TU3 or payload not requiring tributary multiframe alignment.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion on the DROP bus when loss of pointer (LOP) events are detected in the receive stream. When LOPPAIS is set low, loss of pointer events have no effect on the DROP bus.

PSLMPAIS:

When set high, the PSLMPAIS bit enables path AIS insertion on the DROP bus when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPAIS is set low, path signal label mismatch events have no effect on the DROP bus.

PSLUPAIS:

When set high, the PSLUPAIS bit enables path AIS insertion on the DROP bus when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUPAIS is set low, path signal label unstable events have no effect on the DROP bus.

RXSEL[1:0]:

The RXSEL[1:0] bits controls the source of the associated receive section of the transmit stream. When RXSEL[1:0] is set to 'b00, the receive section is chosen to be one in the local SPECTRA-155. The path REI count and path RDI status of the transmit stream is derived from the local RPOP. When RXSEL[1:0] is set to 'b01, a remote receive section is chosen and it reports the detected path BIP-8 error count and the path AIS status of its DROP bus via the transmit alarm port. The path status byte in the transmit stream carries the path REI and path RDI indications reported in the transmit alarm port. When RXSEL[1:0] is set to 'b10, inband error reporting is chosen. The associated receive section forms a new G1 byte reporting on the path BIP-8 errors detected and path AIS status. The SPECTRA-155 does not support inband error reporting of enhanced RDI codes. To enable inband reporting of non-enhanced RDI codes, the SPECTRA-155 must be configured to generate path AIS on the drop bus for all events which can cause RDI. The local transmit section pass the path REI and path RDI bits on the ADD bus to the transmit stream unmodified. When RXSEL[1:0] is set to 'b11, the path status byte in the transmit stream is not associate with any receive stream. No path REI nor path RDI will be reported.

Table 31 - RXSEL[1:0] codepoints for STS-1 #1 and STS-3c.

RXSEL[1:0]	Source
00	local SPECTRA-155
01	remote receive (TAP port)
10	inband reporting
11	no reporting

Register 102H: SPECTRA-155 Path REI/RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	AUTOPREI	0
Bit 6	R/W	ALMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	PSLMPRDI	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	LOPCONPRDI	1
Bit 1	R/W	TIUPRDI	1
Bit 0	R/W	TIMPRDI	1

This register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP #1 or a mate TPOP #1 via the RAD PRDI5 bit position. When the SPECTRA-155 is configured for STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, this register controls the assertion of path RDI for the entire SONET/SDH stream. When configured for STS-3 (STM-1/AU3) mode, this register controls the assertion of path RDI for the STS-1 (STM-0/AU3) #1 only.

TIMPRDI:

When set high, the TIMPRDI bit enables path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPRDI is set low, trace identifier mismatch events have no effect on path RDI.

TIUPRDI:

When set high, the TIUPRDI bit enables path RDI assertion when path trace message unstable (mode 1 or mode 2 as controlled by the SPECTRA-155 Auto Trace Message Mode 1/2 Control register) events are detected in the receive stream. When TIUPRDI is set low, trace identifier unstable events have no effect on path RDI.

LOPCONPRDI:

When set high, the LOPCONPRDI bit enables path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When LOPCONPRDI is set low, loss of pointer concatenation events have no effect on path RDI.

LOPPRDI:

When set high, the LOPPRDI bit enables path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPRDI is set low, loss of pointer events have no effect on path RDI.

PSLMPRDI:

When set high, the PSLMPRDI bit enables path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPRDI is set low, path signal label mismatch events have no effect on path RDI.

PAISPRDI:

When set high, the PAISPRDI bit enables path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When PAISPRDI is set low, PAIS states have no effect on path RDI.

ALMPRDI:

When set high, the ALMPRDI bit enables path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When ALMPRDI is set low, the above events have no effect on path RDI.

AUTOPREI:

The AUTOPREI bit enables the automatic insertion of path REI events in the local or mate transmitter. When AUTOPREI is a logic one, receive B3 errors detected by the SPECTRA-155 are automatically inserted in the G1 byte of the local transmit stream (as enabled using the RXSEL[1:0] bits in the SPECTRA-155 Path REI/RDI Control #1 register). In addition, REI events are indicated on the RAD[1] output. When AUTOPREI is a logic zero, path REI events are not automatically inserted in the local transmit stream. In addition, REI events are not indicated on the RAD[1] output.

Register 103H: SPECTRA-155 Path/Mapper Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	TPIP3I	X
Bit 3	R	TPIP2I	X
Bit 2	R	TPIP1I	X
Bit 1	R	D3MA[3:1]I	X
Bit 0	R	D3MD[3:1]I	X

This register, together with the SPECTRA-155 Section/Line Interrupt Status register, the SPECTRA-155 Path Interrupt Status #1 register and the SPECTRA-155 Path Interrupt Status #2 register, allows the source of an active interrupt to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

These register bits are not cleared on read.

D3MD[3:1]I:

The D3MD[3:1]I bit is high when an interrupt request is active from any one of the D3MD blocks.

D3MA[3:1]I:

The D3MA[3:1]I bit is high when an interrupt request is active from any one of the D3MA block.

TPIPnI:

The TPIPnI bits are high when an interrupt request is active from the corresponding TPIP block.

Register 104H: SPECTRA-155 Path Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	DPAIS	X
Bit 6		Unused	X
Bit 5	R	RPOP3I	X
Bit 4	R	RPOP2I	X
Bit 3	R	RPOP1I	X
Bit 2	R	RTAL3I	X
Bit 1	R	RTAL2I	X
Bit 0	R	RTAL1I	X

This register, together with the SPECTRA-155 Section/Line Interrupt Status register, the SPECTRA-155 Path/Mapper Interrupt Status register and the SPECTRA-155 Path Interrupt Status #2 register, allows the source of an active interrupt to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

RTALnI:

The RTALnI bits are high when an interrupt request is active from the corresponding RTAL block.

RPOPnI:

The RPOPnI bits are high when an interrupt request is active from the corresponding RPOP block.

DPAIS:

The DROP bus alarm indication signal (DPAIS) bit is set high when path AIS is inserted in the DROP bus. In STS-3 (STM-1/AU3) mode, DPAIS is set high when path AIS is inserted in any of the three STS-1 (STM-0/AU3) streams. DROP bus Path AIS assertion can be automatic using the Receive Path AIS Control registers or manual using the RTAL Control registers. Note, DPAIS is not an interrupt bit.

These register bits are not cleared on read.

Register 105H: SPECTRA-155 Path Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	TPAIS	X
Bit 6		Unused	X
Bit 5	R	TTAL3I	X
Bit 4	R	TTAL2I	X
Bit 3	R	TTAL1I	X
Bit 2	R	SPTB3I	X
Bit 1	R	SPTB2I	X
Bit 0	R	SPTB1I	X

This register, together with the SPECTRA-155 Section/Line Interrupt Status register, the SPECTRA-155 Path/Mapper Interrupt Status register and the SPECTRA-155 Path Interrupt Status #1 register, allows the source of an active interrupt to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

These register bits are not cleared on read.

SPTBnI:

The SPTBnI bits are high when an interrupt request is active from the corresponding SPTB block.

TTALnI:

The TTALnI bits are high when an interrupt request is active from the corresponding TTAL block.

TPAIS

The transmit stream alarm indication signal (TPAIS) bit is set high when path AIS is inserted in the transmit stream. In STS-3 (STM-1/AU3) mode, TPAIS is set high when path AIS is inserted in any of the three STS-1 (STM-0/AU3) streams. Transmit bus Path AIS assertion is controlled using the TTAL Control registers or the TPOP Control registers. Note, TPAIS is not an interrupt bit.

Register 106H: SPECTRA-155 Path Transmit Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	TDIS3	0
Bit 4	R/W	TDIS2	0
Bit 3	R/W	TDIS1	0
Bit 2	R/W	TPTB3EN	0
Bit 1	R/W	TPTB2EN	0
Bit 0	R/W	TPTB1EN	0

This register controls the insertion of path overhead in the transmit stream.

TPTBnEN:

The TPTBnEN bits controls whether the path trace message stored in the TPTB block is inserted in the transmit stream. When TPTBnEN is set high, the message in the corresponding transmit path trace buffer (TPTB) is inserted in the transmit stream. When TPTBnEN is set low, the path trace message is supplied by the TPOP block or via the corresponding TPOH input. The TPTBnEN bits must be set low and the serial TPOH stream must be disable to prevent path trace insertion at intermediate tandem connection nodes.

TDISn:

The TDISn bits controls the insertion of path overhead bytes in the transmit stream. When TDIS is set high, the path overhead bytes of the corresponding transmit stream is sourced from the ADD bus. Serial path overhead insertion and corruption via the TPOH input is still available. However, setting TPOHEN high during the B3 byte field corrupts the transmitted byte in an unpredictable fashion. All other POH bytes may be modified via the TPOH inputs as controlled by the TPOP source control register bits and the TPOHEN input normally. When TDIS is set low, path overhead is processed normally. The TDISn bits must be set high and the TPOHEN[3:1] inputs set low to disable path overhead insertion at intermediate tandem connection and at line (multiplexed section) terminating nodes.

Register 107H: SPECTRA-155 Path Loopback, ADD Bus Control

Bit	Type	Function	Default
Bit 7	R/W	ADDUEV	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	SLLBEN	0
Bit 3		Unused	X
Bit 2	R/W	ADDUE3	0
Bit 1	R/W	ADDUE2	0
Bit 0	R/W	ADDUE1	0

This register provides control of line and diagnostic loopback of the SPECTRA-155.

ADDUEn:

When set high, the ADDUEn bits configure the corresponding STS-1 (STM-0/AU3) stream in the ADD bus as unequipped. Payload bytes from that STS-1 (STM-0/AU3) stream are overwritten with all ones or all zeros as controlled using the ADDUEV bit. When ADDUEn is set low, the STS-1 (STM-0/AU3) stream is equipped and carrying valid data.

SLLBEN:

When set high, the system side line loopback enable bit (SLLBEN) activates line loopback in the SPECTRA-155. Data from the receive stream propagates to the DROP bus and replaces the data on the ADD bus. When SLLBEN is set low, system side line loopback is disabled, data on the ADD bus is transmitted on the transmit stream. SLLBEN must be set low when operating in DS3 mode, in Serial Datacom or in Serial Telecom mode.

ADDUEV:

When set high, the ADDUEV bit selects the all ones pattern as the overwrite pattern when payload overwrite is enabled using the ADDUEn bits. When set low, the ADDUEV bit selects the all zeros pattern as the overwrite pattern when payload overwrite is enabled using the ADDUEn bits.

Register 108H: SPECTRA-155 Signal Activity Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	ADA	X
Bit 4	R	ACA	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	DCKA	X
Bit 0	R	ACKA	X

This register provides activity monitoring on major SPECTRA-155 inputs for byte and nibble Telecombus operation (SMODE=000,001). When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

ACKA:

The ACK active (ACKA) bit monitors for low to high transitions on the ACK input. ACKA is set high on a rising edge of ACK, and is set low when this register is read.

DCKA:

The DCK active (DCKA) bit monitors for low to high transitions on the DCK input. DCKA is set high on a rising edge of DCK, and is set low when this register is read.

ACA:

The ADD bus control active (ACA) bit monitors for low to high transitions on the APL, AC1J1V1 and ADP inputs. ACA is set high when rising edges have been observed on all three signals, and is set low when this register is read.

ADA:

The ADD bus data active (ADA) bit monitors for low to high transitions on the AD[7:0] bus when configured for Byte Telecombus mode or on the AD[3:0] bus when configured for Nibble Telecombus mode. ADA is set high when

rising edges have been observed on all the signals in AD[7:0] or AD[3:0], and is set low when this register is read.

Register 109H: SPECTRA-155 Parity Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	API	X
Bit 4	R/W	APE	0
Bit 3	R/W	ODDPG	0
Bit 2	R/W	ODDPC	0
Bit 1	R/W	INCPL	0
Bit 0	R/W	INCC1J1V1	0

This register allows the parity insertion in the ADD and GENERATED busses of the SPECTRA-155 to be configured.

INCC1J1V1:

The INCC1J1V1 bit controls the whether the composite timing signals (AC1J1V1, DC1J1V1, GC1J1V1) in the ADD, DROP and GENERATED busses are used to calculate the corresponding parity signals (ADP, DDP, GDP). When INCC1J1V1 is set high, the parity signal set includes the C1J1V1 signal. When INCC1J1V1 is set low, parity is calculated without regard to the state of the corresponding C1J1V1 signal on the three busses.

INCPL:

The INCPL bit controls the whether the payload active signal (APL, DPL, GPL) in the ADD, DROP and GENERATED busses are used to calculate the corresponding parity signals (ADP, DDP, and GDP, respectively). When INCPL is set high, the parity signal set includes the PL signal. When INCPL is set low, parity is calculated without regard to the state of the corresponding PL signal on the three busses.

ODDPC:

The ODDPC bit controls the parity expected on the ADD bus parity signal (ADP). When set high, the ODDPC bit configures the bus parity including the corresponding parity signal to be odd. When set low, the ODDPC bit configures the bus parity to be even.

ODDPG:

The ODDPG bit controls the parity placed on the DROP bus and GENERATED bus parity signals (DDP, GDP). When set high, the ODDPG bit configures the bus parity including the corresponding parity signal to be odd. When set low, the ODDPG bit configures the bus parity to be even.

APE:

The APE bit controls the assertion of interrupts when a parity error is detected in the ADD bus. When APE is set high, an interrupt will be asserted (INTB set low) when a parity error has been detected in the ADD bus. When APE is set low, ADD bus parity errors will not affect the interrupt output.

API:

The ADD bus parity interrupt status bit (API) reports the status of the ADD bus parity interrupt. API is set high on detection of a parity error event (transition to good or bad parity) on the ADD bus. This bit and the interrupt are cleared when this register is read. Note, API is only valid when operating in Telecombus byte or nibble mode. The occurrence of parity error events is usually an indication of mis-configured parity generation/detection or actual hardware problem at the ADD bus input.

Register 110H, 150H, 190H: RPOP Status and Control (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	PAISCONV	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding RPOP if the EXTD bit is set low in the RPOP Pointer MSB register.

NEWPTRE:

When a 1 is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output.

NEWPTRI:

The NEWPTRI bit is set to logic 1 when a new_point indication is received. This bit (and the interrupt) are cleared when this register is read.

PRDIV:

The path RDI status bit (PRDI) indicates reception of path RDI alarm in the receive stream.

PAISV:

The path AIS status bit (PAISV) indicates reception of path AIS alarm in the receive stream.

PAISCONV:

The concatenation path AIS status bit (PAISCONV) indicates reception of path AIS alarm in the concatenation indicator in the receive stream.

LOPV:

The loss of pointer status bit (LOPV) indicates entry to the LOP_state in the RPOP pointer interpreter state machine.

LOPCONV:

The concatenated loss of pointer status bit (LOPCONV) indicates entry to LOP_state for the concatenated streams in the RPOP pointer interpreter.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-155.

Register 110H, 150H, 190H: RPOP Status and Control (EXTD=1)

Bit	Type	Function	Default
Bit 7	R/W	TCDLT	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	PSL5	0
Bit 4	R/W	V1DISLOP	0
Bit 3		Unused	
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

This register provides configuration and reports the status of the corresponding RPOP if the EXTD bit is set high in the RPOP Pointer MSB register.

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current state of the detected enhanced RDI, (filtered G1 bits 5, 6, & 7).

V1DISLOP:

When a 1 is written to the V1DISLOP bit (V1 Disable in LOP), the RPOP and the DROP bus will flywheel on the last known multiframe position prior to entering LOP. When a 0 is written to this bit, while in LOP the RPOP will continue to track the receive J1 and V1 positions and indicate these positions to downstream blocks.

PSL5:

The PSL5 bit controls the filtering of the path signal label (PSL) byte (C2). When a 1 is written to PSL5, the PSL is updated when the same value is received for 5 consecutive frames. When a 0 is written to PSL5, the PSL is updated when the same value is received for 3 consecutive frames.

IINVCNT:

When a 1 is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state, 3 x new point will reset the inv_point count. If this bit is set to 0, the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected.

TCDLT:

When a 1 is written to the TCDLT (Tandem Connection Data Link Transparent) bit, the data link field of the Z5 byte will be passed transparently if no data is inserted via the tandem connection overhead data signal (TCOH). If this bit is set to 0, all ones will be inserted into the data link field of the Z5 byte, provided no data is inserted via the tandem connection overhead data signal (TCOH).

Register 111H, 151H, 191H: RPOP Alarm Interrupt Status (EXTD=0)

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	PAISCONI	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	PREII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set low in the RPOP Pointer MSB register.

These bits (and the interrupt) are cleared when the this register is read.

PREII

The PREI interrupt status bit (PREII) is set high when a path REI is detected.

BIPEI:

The BIP error interrupt status bit (BIPEI) is set high when a path BIP-8 error is detected.

PRDII:

The PRDII interrupt status bit is set high on assertion and removal of the path RDI alarm (bit 5 of G1) or when a change is detected in bit 6 of G1.

PAISI, PAISCONI, LOPI, LOPCONI:

The PRDII, PAISI, PAISCONI, LOPI and LOPCONI interrupt status bits are set high on assertion and removal of the corresponding alarm states.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

Register 111H, 151H, 191H: RPOP Alarm Interrupt Status (EXTD=1)

Bit	Type	Function	Default
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	ERDII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set high in the RPOP Pointer MSB register.

These bits (and the interrupt) are cleared when the Interrupt Status Register is read.

ERDII:

The ERDII bit is set to logic 1 when a change is detected in the received enhanced RDI state.

Register 112H, 152H, 192H: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	CONCATI	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	Reserved	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

These bits (and the interrupt) are cleared when this register is read.

NDFI:

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream.

PSEI, NSEI:

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the RPOP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream.

Reserved:

The Reserved bit is an interrupt status bit and must be ignored when this register is read.

INVNDFI:

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream.

DISCOPAI:

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the RPOP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication).

ILLJREQI:

The illegal justification request interrupt status bit (ILLJREQI) is set high when the RPOP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable).

CONCATI:

The concatenation indication error interrupt status bit (CONCATI) is set high when the SPECTRA-155 is operating in concatenation mode and an error is detected in the concatenation indicators of STS-1 (STM-0/AU3) #2 and STS-1 (STM-0/AU3) #3.

Register 113H, 153H, 193H: RPOP Alarm Interrupt Enable (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	PREIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set low in the RPOP Pointer MSB register.

PREIE:

When a 1 is written to the PREIE interrupt enable bit position, the reception of one or more path REIs will activate the interrupt (INTB) output.

BIPEE:

When a 1 is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt (INTB) output.

PRDIE:

When a 1 is written to the PRDIE interrupt enable bit position, a change in the path RDI state (bit 5 of G1) will activate the interrupt (INTB) output.

PAISE:

When a 1 is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output.

PAISCONE:

When a 1 is written to the PAISCONE interrupt enable bit position, a change in the concatenation path AIS state will activate the interrupt (INTB) output.

LOPE:

When a 1 is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output.

LOPCONE:

When a 1 is written to the LOPCONE interrupt enable bit position, a change in the concatenation loss of pointer state will activate the interrupt (INT) output.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155.

Register 113H, 153H, 193H: RPOP Alarm Interrupt Enable (EXTD=1)

Bit	Type	Function	Default
Bit 7	R	LOPCONV#2	X
Bit 6	R	LOPCONV#3	X
Bit 5	R	PAISCONV#2	X
Bit 4	R	PAISCONV#3	X
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	ERDIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set high in the RPOP Pointer MSB register.

ERDIE:

When a 1 is written to the RDIE interrupt enable bit position, a change in the enhanced path RDI state. will activate the interrupt (INT) output.

LOPCONV#2:

The concatenated loss of pointer value bit (LOPCONV#2) indicates the LOP value for the STS-3c (STM-1/AU3 #2).

LOPCONV#3:

The concatenated loss of pointer value bit (LOPCONV#3) indicates the LOP value for the STS-3c (STM-1/AU3 #3).

PAISCONV#2:

The concatenated path AIS value bit (PAISCONV#2) indicates the PAIS value for the STS-3c (STM-1/AU3 #2).

PAISCONV#3:

The concatenated path AIS value bit (PAISCONV#3) indicates the PAIS value for the STS-3c (STM-1/AU3 #3).

Register 114H, 154H, 194H: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	CONCATE	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

NDFE:

When a 1 is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output.

PSEE:

When a 1 is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output.

NSEE:

When a 1 is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output.

Reserved:

The Reserved bit must be programmed to logic zero for proper operation of the SPECTRA-155.

INVNDFE:

When a 1 is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output.

DISCOPAE:

When a 1 is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output.

CONCATE:

When a 1 is written to the CONCATE interrupt enable bit position, an invalid Concatenation Indicator event will activate the interrupt (INTB) output.

ILLJREQE:

When a 1 is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output.

Register 115H, 155H, 195H: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

The register reports the lower eight bits of the active offset.

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Register 116H, 156H, 196H: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	RDI10	0
Bit 4	R	CONCAT	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

CONCAT:

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

RDI10:

The RDI10 bit controls the filtering of the remote defect indication, the auxiliary remote defect indication and the enhanced remote defect indication. When RDI10 is set high, the RDI and ERDI status is updated when the same value is received in the corresponding bit/bits of the G1 byte for 10 consecutive frames. When RDI10 is set low, the RDI and ERDI status is updated when the same value is received for 5 consecutive frames.

EXTD:

The EXTD bit extends the RPOP registers to facilitate additional mapping. If this bit is set to logic 1 the register mapping, for the RPOP Status and Control register, the RPOP Alarm Interrupt Status register and the RPOP Alarm Interrupt Enable registers are extended.

NDFPOR:

The NDFPOR (new data flag pointer of range) bit controls the definition of the NDF_enable indication for entry to the LOP state under 8xNDF_enable events. When NDFPOR is set high, for the purposes of detect of loss of events only, the definition of the NDF_enable indication does not require the pointer value to be within the range of 0 to 782. When NDFPOR is set low, NDF_enable indications require the pointer to be within 0 to 782.

Register 117H, 157H, 197H: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register reports the path label byte in the receive stream..

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three or five consecutive frames as selected using the PSL5 bit in the RPOP Status and Control (EXTD=1) register.

Register 118H, 158H, 198H: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Register 119H, 159H, 199H: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

BE[15:0]:

Bits BE[15:0] represent the number of path bit-interleaved parity errors that have been detected since the last time the path BIP-8 registers were polled by writing to the SPECTRA-155 Reset and Identity register. The write access transfers the internally accumulated error count to the path BIP-8 registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 11AH, 15AH, 19AH: RPOP Path REI LSB

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register 11BH, 15BH, 19BH: RPOP Path REI MSB

Bit	Type	Function	Default
Bit 7	R	FE[15]	X
Bit 6	R	FE[14]	X
Bit 5	R	FE[13]	X
Bit 4	R	FE[12]	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[15:0]:

Bits FE[15:0] represent the number of path remote error indications that have been received since the last time the Path REI registers were polled by writing to the SPECTRA-155 Reset and Identity register. The write access transfers the internally accumulated error count to the path REI registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 11CH, 15CH, 19CH: RPOP Tributary Multiframe Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4	R/W	BLKREI	0
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register reports the status of the multiframe framer and enables interrupts due to framer events.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155 device.

COMAE:

The change of multiframe alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPECTRA-155 detect a change in the multiframe phase. When LOME is set high, an interrupt is generated upon change of multiframe alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI:

The change of multiframe alignment interrupt status bit (COMAI) is set high on changes in the multiframe alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

BLKREI:

When set high, the block REI bit (BLKREI) indicates that path REI counts are to be reported and accumulated on a block basis. A single REI error is accumulated if the received REI code is between 1 and 8 inclusive. When BLKREI is set low, REI errors are accumulated literally.

LOME:

The loss of multiframe interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of loss of multiframe indication (LOM). When LOME is set high, an interrupt is generated upon loss of multiframe. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV:

The loss of multiframe status bit (LOMV) reports the current state of the multiframe framer monitoring the receive stream. LOMV is set high when loss of multiframe is declared and is set low when multiframe alignment has been acquired.

LOMI:

The loss of multiframe interrupt status bit (LOMI) is set high on changes in the loss of multiframe status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Register 11DH, 15DH, 19DH: RPOP Tandem Connection and Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	CDIFF	0
Bit 1	R/W	ISF	0
Bit 0	R/W	OTCTE	0

This register contains tandem connection and ring control bits.

OTCTE:

When set high, the OTCTE bit configures the RPOP to operates as a piece of originating TCTE (tandem connection terminating equipment). RPOP will place the receive BIP-8 error count from the previous frame on the IEC field and source the tandem path data link presented on the corresponding RTCOH input in the DL field of the tandem connection maintenance byte (Z5) on the DROP bus. The BIP-8 byte (B3) is updated to reflect the current and all previous modifications of the Z5 byte. When a loss of pointer (LOP) or path AIS event is detected in the receive stream, RPOP will maintain the previous pointer on the H1, H2 bytes, and set the IEC field to indicate ISF (IEC = 'b1111). Correct B3 and Z5 bytes, and all ones on remaining synchronous payload envelope (virtual container) bytes will be placed on the DROP bus. When OTCTE is set high, the H4BYP bit in the RTAL Control register must be set high. The LOPPAIS bit in SPECTRA-155 Receive Path AIS Control register must be set high for LOP detection in originating TCTE mode. The When OTCTE is set low, RPOP is not an originating TCTE; payload data in receive stream is placed on the DROP bus unmodified.

ISF:

The ISF bit controls the insertion of incoming signal failure codes in the SPE bytes. When ISF is set high, the IEC field of the Z5 byte is set to indicated ISF ('b1111). The tandem connection data link remains active. An error-free path BIP is inserted in the B3 byte. All remaining SPE bytes are set to all-ones. When ISF is set low, data is processed normally. ISF is ignored when OTCTE is set low.

CDIFF:

The CDIFF bit controls the method of accumulating incoming error counts. When CDIFF is set low, the Tandem Connection IEC Count registers accumulate the counts reported in the IEC field of the Z5 byte directly. When CDIFF is set high, the Tandem Connection IEC Count registers accumulate the absolute value of the difference between the number of BIP errors detected in the current frame and the IEC count value.

BLKBIPO:

When set high, the block BIP-8 output bit (BLKBIPO) indicates that path BIP-8 errors are to be reported on a block basis. A single BIP error is reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. In inband error reporting mode, the REI count of the G1 byte is set on a block basis. When BLKBIPO is set low, BIP-8 errors are reported on a bit basis. In inband error reporting mode, the REI count of the G1 byte is set on a bit basis.

DISFS:

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU3 carrying a VC3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 (STM-0/AU3) stream. This bit is ignored when the SPECTRA-155 is processing an STS-3c (STM-1/AU4) stream.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic 1 is written to this bit, an incorrect SS bit pattern (i.e., b'10) will prevent RPOP from issuing NDF_enable, inc_ind and dec_ind indications. When a logic 0 is written to this bit, the SS bits received do not affect active offset change events.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic 1 is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least

three frame ago. When a logic 0 is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Register 11EH, 15EH, 19EH: RPOP Tandem Connection IEC Count LSB

Bit	Type	Function	Default
Bit 7	R	IEC[7]	X
Bit 6	R	IEC[6]	X
Bit 5	R	IEC[5]	X
Bit 4	R	IEC[4]	X
Bit 3	R	IEC[3]	X
Bit 2	R	IEC[2]	X
Bit 1	R	IEC[1]	X
Bit 0	R	IEC[0]	X

Register 11FH, 15FH, 19FH: RPOP Tandem Connection IEC Count MSB

Bit	Type	Function	Default
Bit 7	R	IEC[15]	X
Bit 6	R	IEC[14]	X
Bit 5	R	IEC[13]	X
Bit 4	R	IEC[12]	X
Bit 3	R	IEC[11]	X
Bit 2	R	IEC[10]	X
Bit 1	R	IEC[9]	X
Bit 0	R	IEC[8]	X

IEC[15:0]:

Bits IEC[15:0] represent the sum of the tandem connection incoming error counts that have been detected since the last time the tandem connection incoming error count registers were polled by writing to the SPECTRA-155 Identity and Reset register. The write access transfers the internally accumulated error count to the tandem connection incoming error count registers within 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 124H, 164H, 1A4H: PMON Receive Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RPJE[7]	X
Bit 6	R	RPJE[6]	X
Bit 5	R	RPJE[5]	X
Bit 4	R	RPJE[4]	X
Bit 3	R	RPJE[3]	X
Bit 2	R	RPJE[2]	X
Bit 1	R	RPJE[1]	X
Bit 0	R	RPJE[0]	X

This register reports the number of positive pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate positive pointer justifications in the receive stream when the MONRS bit in the SPECTRA-155 Path/Mapper Configuration register is set high, and to accumulate justifications on the DROP bus when MONRS is set low.

RPJE[7:0]:

Bits RPJE[7:0] represent the number of positive pointer justification events observed on the receive stream since the RPJE register was polled by writing to SPECTRA-155 Identity and Reset register. The write access transfers the internally accumulated error count to the RPJE register within 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 125H, 165H, 1A5H: PMON Receive Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RNJE[7]	X
Bit 6	R	RNJE[6]	X
Bit 5	R	RNJE[5]	X
Bit 4	R	RNJE[4]	X
Bit 3	R	RNJE[3]	X
Bit 2	R	RNJE[2]	X
Bit 1	R	RNJE[1]	X
Bit 0	R	RNJE[0]	X

This register reports the number of negative pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate negative pointer justifications in the receive stream when the MONRS bit in the SPECTRA-155 Identity and Reset register is set high, and to accumulate justifications on the DROP bus when MONRS is set low.

RNJE[7:0]:

Bits RNJE[7:0] represent the number of negative pointer justification events observed on the receive side since the RNJE register was polled by writing to SPECTRA-155 Identity and Reset register. The write access transfers the internally accumulated error count to the RNJE register within 7µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 126H, 166H, 1A6H: PMON Transmit Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TPJE [7]	X
Bit 6	R	TPJE [6]	X
Bit 5	R	TPJE [5]	X
Bit 4	R	TPJE [4]	X
Bit 3	R	TPJE [3]	X
Bit 2	R	TPJE [2]	X
Bit 1	R	TPJE [1]	X
Bit 0	R	TPJE [0]	X

This register reports the number on positive pointer justification events that occurred on the transmit stream in the previous accumulation interval.

TPJE[7:0]:

Bits TPJE[7:0] represent the number of positive pointer justification events inserted in the transmit stream since the TPJE register was polled by writing to SPECTRA-155 Identity and Reset register. The write access transfers the internally accumulated error count to the TPJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 127H, 167H, 1A7H: PMON Transmit Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TNJE [7]	X
Bit 6	R	TNJE [6]	X
Bit 5	R	TNJE [5]	X
Bit 4	R	TNJE [4]	X
Bit 3	R	TNJE [3]	X
Bit 2	R	TNJE [2]	X
Bit 1	R	TNJE [1]	X
Bit 0	R	TNJE [0]	X

This register reports the number of negative pointer justification events that occurred on the transmit stream in the previous accumulation interval.

TNJE[7:0]:

Bits TNJE[7:0] represent the number of negative pointer justification events inserted in the transmit stream since the TNJE register was polled by writing to SPECTRA-155 Identity and Reset register. The write access transfers the internally accumulated error count to the TNJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 128H, 168H, 1A8H: RTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	SSS	1
Bit 3	R/W	ISFE	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	DPJEE	0
Bit 0	R/W	IPAIS	0

This register allows the operation of the Receive Telecombus Aligner to be configured.

IPAIS:

The insert path alarm indication signal (IPAIS) bit controls the insertion of PAIS in the DROP bus. When IPAIS is set high, path AIS is inserted in the DROP bus. The pointer bytes (H1, H2 and H3) and the entire SPE (VC) are set to all-ones. Path RDI indication is reported in the receive alarm port and to the companion TPOP in the SPECTRA-155. Normal operation resumes when the IPAIS bit is set low.

DPJEE:

The DROP bus pointer justification event interrupt enable bit (DPJEE) controls the activation of the interrupt output when a pointer justification is inserted in the DROP bus. When DPJEE is set high, insertion of pointer justification events in the DROP bus will activate the interrupt (INTB) output. When DPJEE is set low, insertion of pointer justification events in the DROP bus will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events affect the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

ISFE:

The incoming signal failure interrupt enable bit (ISFE) controls the activation of the interrupt output when the status of the ISF code in the tandem connection maintenance byte changes to indicate failure or to indicate normal operation.

SSS:

The set ss bit (SSS) controls the value of the ss field in the H1 pointer byte in the DROP bus. When SSS is set high, the ss bits are set to 'b10. When SSS is set low, the ss bits are set to 'b00.

CLRFS:

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns in virtual tributary (low order tributary) mappings to zero. When a logic 1 is written to CLRFS, the fixed stuff column data are set to 00H. When a logic 0 is written to CLRFS, the fixed stuff column data from the receive stream is placed on the DROP bus unchanged. The location of the fixed stuff columns in the synchronous payload envelope (virtual container) is dependent on the whether the SPECTRA-155 is processing concatenated payload.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the RTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the receive stream is placed on the DROP bus unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multiframe is synchronized by the multiframe framer in the RPOP block. In originating tandem connection terminating equipment mode (OTCTE set high in RPOP Tandem Connection and Ring Control register), H4BYP must be set high for proper operation of the SPECTRA-155.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155.

Register 129H, 169H, 1A9H: RTAL Interrupt Status and Control

Bit	Type	Function	Default
Bit 7	R/W	DOPJ[1]	0
Bit 6	R/W	DOPJ[0]	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	DLOP	0

This register allows the control of the DROP bus interface and sensing of interrupt status.

DLOP:

The diagnose loss of pointer control bit (DLOP) allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the payload pointer inserted in the DROP bus is inverted causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

NPJI:

The DROP bus negative pointer justification interrupt status bit (NPJI) is set high when the RTAL inserts a positive pointer justification event on the DROP bus.

PPJI:

The DROP bus positive pointer justification interrupt status bit (PPJI) is set high when the RTAL inserts a positive pointer justification event on the DROP bus.

ESEI:

The DROP bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in RTAL underflows or overflows.

ESD0- ESD1:

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds. I.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 32 - Receive ESD[1:0] codepoints.

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definitions:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing negative justifications at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the RTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the RTAL will start generates outgoing positive justification at the rate of 1 in every 4 frames).

DOPJ0- DOPJ1:

The diagnose pointer justification bits (DOPJ[1:0]) allow downstream pointer processing elements to be diagnosed for correct reaction to pointer justification events. Setting DOPJ[1] high and DOPJ[0] low, forces the RTAL to generate positive stuff justification events on the DROP bus at the rate of one every four frames regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to overflow. Setting DOPJ[1] low and DOPJ[0] high, forces the RTAL to generate negative stuff justification events at the rate of one every four frames, regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to underflow. Setting both DOPJ[1] and DOPJ[0] high disables the RTAL from generating pointer justification events. If the incoming and outgoing clocks have a frequency offset, the internal FIFO may under/overflow depending on the relative frequencies of the clocks. Pointer justification events are generated based on the current depth of the internal FIFO when DOPJ[1] and DOPJ[0] are both set low. When DOPJ[1:0] is set to values other than 'b00, the detection of elastic store over/underflow is disabled.

The interrupt bits (and the interrupt) are cleared when this register is read.

Register 12AH, 16AH, 1AAH: RTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	ISFV	X
Bit 6	R	ISFI	X
Bit 5	R/W	H4AISB	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	FISF	0
Bit 2	R/W	TTCTE	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register reports alarms and controls diagnostics on the DROP bus.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the DROP bus. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the DROP bus when a FIFO underflow or overflow has been detected in the elastic store . When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the DROP bus for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

TTCTE:

The TTCTE bit controls whether the RTAL is terminating a tandem connection. When TTCTE is set high, Incoming Signal Failure codes (ISF) in the Incoming Error Count field (IEC) of the tandem connection maintenance byte (Z5) is translated into path AIS in the DROP bus. Z5 bytes carrying a normal IEC value are cleared to zero, and the B3 byte is update to reflect the change to Z5. When TTCTE is set low, the RTAL is not terminating a tandem connection. The B3 and Z5 bytes are not modified by the RTAL.

FISF:

The FISF bit controls the filtering of ISF codes in the receive stream in terminating tandem connection terminating equipment mode (TTCTE high). When FISF is set high, the ISF state is entered after receiving an active ISF code ('b1111) for three consecutive frames. Similarly, path AIS is removed after detection of inactive ISF codes for three consecutive frames. When FISF is set low, the ISF state is asserted immediately on detection of active ISF and removal occurs immediately on detection of inactive ISF.

ITUAIS:

The insert tributary path AIS bits controls the insertion of Tributary Path AIS on the DROP bus for VT1.5 (TU11), VT2 (TU12), VT3 and VT6 (TU2) payloads. When ITUAIS is set high, columns in the DROP bus carrying tributary traffic are set to all ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low. The ITUAIS bit is not applicable for TU3 tributary payloads and the ITUAIS bit must be set low.

H4AISB:

The insert H4 AIS bits controls the insertion of the all-ones AIS pattern in the H4 byte. When H4AISB is set low, the H4 byte will be over-written with 'hFF when path AIS is inserted in the DROP bus. When H4AISB is set high, the H4 byte is not over-written during path AIS insertion.

ISFI:

The incoming signal failure alarm interrupt status bit (ISFI) is set high when the RTAL detects a change in the ISF state (from normal to signal failure, or vice versa). This bit is cleared when this register is read. This bit is only active when TTCTE is set high. When TTCTE is set low, this bit should be ignored.

ISFV:

The incoming signal failure alarm status bit (ISFV) reports the status of the ISF state derived from the ISF code in the tandem connection maintenance byte (Z5) of the receive stream. This bit is only active when TTCTE is set high. When TTCTE is set low, this bit should be ignored.

Register 130H, 170H, 1B0H: TPOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EPRDIEN	0
Bit 5	R/W	EPRDISRC	0
Bit 4	R/W	PERSIST	0
Bit 3	R/W	EXCFS	0
Bit 2	R/W	DH4	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

The register controls the operation of the transport overhead processor for downstream diagnostics and tandem connection applications.

PAIS:

The PAIS bit controls the insertion of path alarm indication signal in the transmit stream. When a logic one is written to this bit, the synchronous payload envelope and the pointer bytes (H1 - H3) are set to all-ones. When a logic zero is written to this bit, the SPE and pointer bytes are processed normally. Upon de-activation of path AIS, a new data flag accompanies the first valid pointer.

DB3:

The diagnose BIP-8 enable bit (DB3) controls the inversion of the path BIP-8 byte (B3) in the transmit stream. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame. This bit overrides the state of the B3 error insertion mask controlled by the corresponding TPOHEN primary input.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the transmit stream. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

EXCFS:

The fixed stuff column BIP-8 exclusion bit (EXCFS) controls the inclusion of bytes in the fixed stuff columns of the STS-1 (STM-0/AU3) payload carrying tributaries in path BIP-8 calculations. When EXCFS is set high, the value of bytes in the fixed stuff columns do not affect the path BIP-8 byte (B3). When EXCFS is set low, data in the fixed stuff bytes are included in path BIP-8 calculations. This bit has no effect when the SPECTRA-155 is processing an STS-3c (STM-1/AU4) stream.

PERSIST:

The path far end receive failure alarm persistence bit (PERSIST) controls the persistence of the RDI asserted into the transmit stream. When PERSIST is a logic one, the RDI code inserted into the transmit stream as a result of consequential actions is asserted for a minimum of 20 frames in non-enhanced RDI mode, or the last valid RDI code before an idle code (idle codes are when bits 5,6,7 are 000, 001, or 011) is asserted for 20 frames in enhanced RDI mode. When PERSIST is logic zero, the transmit RDI code changes immediately based on received alarm conditions.

EPRDISRC:

The enhanced path remote defect indication source (EPRDISRC) bit controls the source of the enhanced path RDI code. When EPRDISRC is set high, the enhanced path RDI code is sourced from internal receive side alarms as controlled by the SPECTRA-155 Path RDI Control register. When EPRDISRC is set low, the enhanced path RDI code is sourced from the TPOP Path Status register.

EPRDIEN:

The enhanced path remote defect indication enable (EPRDIEN) bit controls path RDI insertion. When EPRDIEN is set high, enhanced path RDI assertion (bits 5,6,7 of the G1 byte) is enabled while normal path RDI (bit 5 of the G1 byte) and auxiliary path RDI (bit 6 of the G1 byte) are disabled. When EPRDIEN is set low, enhanced path RDI assertion is disabled while normal path RDI and auxiliary path RDI are enabled.

Register 131H, 171H, 1B1H: TPOP GENERATED Bus Control

Bit	Type	Function	Default
Bit 7	R/W	H1LOAD	0
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved1	0

This registers controls the active offset on the GENERATED bus.

Reserved1:

The Reserved1 bit must be written to logic 0 for proper operation of the SPECTRA-155.

PSE:

The positive stuff enable bit (PSE) controls the generation of positive pointer movements in the GENERATED bus. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the GENERATED bus. This register bit is automatically cleared after the pointer movement is inserted. If the NSE and PSE register bits are both asserted, no pointer movement is generated, but the PSE and NSE bits are cleared anyway.

NSE:

The negative stuff enable bit (NSE) controls the generation of negative pointer movements in the GENERATED bus. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the GENERATED bus. This register bit is automatically cleared after the pointer movement is inserted. If the NSE and PSE register bits are both asserted, no pointer movement is generated, but the PSE and NSE bits are cleared anyway.

NDF:

The NDF insert bit (NDF) controls the insertion of new data flags in the payload pointer. When a logic one is written to this bit, the pattern contained

in the NDF[3:0] bits in the TPOP Payload Pointer MSB register is inserted continuously in the payload pointer of the transmit stream. When a logic zero is written to this bit, the normal pattern ('b0110) is inserted in the payload pointer.

PLD:

The payload pointer load enable bit (PLD) controls the loading of the pointer value contained in the Payload Pointer registers. If a legal value (i.e., 0 ≤ pointer value ≤ 782) is found in the TPOP Payload Pointer registers, writing a one to this bit causes the J1 indication pulse on GC1J1V1 pulse to immediately jump to the corresponding byte position. If a value greater than 782 is found in the TPOP Payload Pointer registers, GC1J1V1 pulses will retain the previous alignment. This bit is automatically cleared after the new payload pointer has been loaded. The J1 indicator will not track changes in GFP. To maintain a constant J1 offset with respect to GFP, PLD must be reasserted each time the GFP changes position.

SOS:

The stuff opportunity spacing control bit (SOS) bit controls the spacing between consecutive SPE positive or negative stuff events on the GENERATED bus. When a logic 0 is written to this bit, stuff events may be generated every frame as controlled by the PSE, and NSE register bits. When a logic 1 is written to this bit, no positive or negative stuffs occur within three frames of the latest pointer movement (including an arbitrary movement). An arbitrary pointer movement can still occur in any frame.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated. If FTPTR is set to logic 1, the APTR[9:0] bits of the TPOP Payload Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. When FTPTR is set and immediately reset at least one Arbitrary Pointer substitution is guaranteed to be sent . If FTPTR is a logic 0, a valid pointer is inserted.

H1LOAD:

The H1 load bit (H1LOAD) controls the periodic updating of the payload pointer which is used to establish the timing on the GENERATE bus. When H1LOAD is logic one, the payload pointer is updated with an adjusted arbitrary payload pointer at every occurrence of the H1 byte. This allows the payload frame and multiframe (J1 and V1 in GC1J1V1) to follow movements in GFP. This adjusted arbitrary payload pointer value is reset with the

contents of the TPOP Arbitrary Pointer Register by writing to the PLD and is adjusted as controlled by the NSE and PSE bits. When H1LOAD is logic zero, the payload pointer is only updated with the value in the TPOP Arbitrary Pointer Registers by writing to the PLD bit in the TPOP Pointer Control Register. The payload frame and multiframe will only react to changes in GFP after writing to the PLD bit.

Register 133H, 173H, 1B3H: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

Register 134H, 174H, 1B4H: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:0]:

The CPTR[9:0] bits reflect the value of the active offset on the transmit stream as indicated by pulses on the AC1J1V1 signal. It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 135H, 175H, 1B5H: TPOP Payload Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

Register 136H, 176H, 1B6H: TPOP Payload Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

APTR[9:0]:

The APTR[9:0] bits are used to set an arbitrary active offset value on the GENERATED bus. The arbitrary pointer value is transferred by writing a logic one to the PLD bit in the TPOP GENERATE Bus Control Register. A legal value (i.e. $0 \leq$ pointer value ≤ 782) results in the J1 pulse on the GC1J1V1 signal shifting to the corresponding byte position. A value of greater than 782 has no effect. For diagnostic purposes, the APTR[9:0] bits can also be forced onto the transmit stream by writing to the FTPTR bit in the TPOP GENERATED Bus Control register.

S1-S0:

The payload pointer size bits (S[1:0]) are inserted in the S[1:0] bit positions in the payload pointer in the transmit stream.

NDF[3:0]:

The new data flag bits (NDF[3:0]) are inserted in the NDF bit positions when the TPOP makes a discontinuous change in active offset or when the NDF bit in the TPOP GENERATE Bus Control register is set to logic one.

Register 137H, 177H, 1B7H: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register contains the value to be inserted in the path trace byte (J1) of the transmit stream when the Transmit Path Trace Buffer block is disabled (TPTBxEN set low).

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream when the associated SPTB block is disabled and corresponding TPOHEN input is low during the path trace bit positions in the path overhead input stream, TPOH.

Register 138H, 178H, 1B8H: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register contains the value to be inserted in the path signal label byte (C2) of the transmit stream.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream when the corresponding TPOHEN input is low during the path signal label bit positions in the path overhead input stream, TPOH. Upon reset, the register value defaults to 01H, which represents "Equipped - Non Specific Payload."

Register 139H, 179H, 1B9H: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	PREI[3]	0
Bit 6	R/W	PREI[2]	0
Bit 5	R/W	PREI[1]	0
Bit 4	R/W	PREI[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	EPRDI6	0
Bit 1	R/W	EPRDI7	0
Bit 0	R/W	G1[0]	0

This register reflects the value inserted in the path status byte (G1) of the transmit stream.

G1[0]:

The G1[0] bit is inserted in the unused bit positions in the path status byte the corresponding TPOHEN input is low during the unused bit positions in the corresponding path overhead input stream, TPOH.

EPRDI6, EPRDI7:

The EPRDI6 and EPRDI7 bits control the insertion of the STS path receive defect indication alarm (PRDI6 and PRDI7, respectively) when EPRDIEN is logic one, and are inserted in the unused bit positions G1[2:1] in the path status byte when EPRDIEN is logic zero, or when the primary input TPOHEN is low during the unused bit positions in the path overhead input stream, TPOH. The function is described in the table below.

Table 31 - Transmit RDI control

TPOHEN	EPRDIEN	IBER	EPRDISRC	Tx G1 bit 5	tx G1 bit 6	tx G1 bit 7
0	0	0	0	PRDI5+Reg[3]	Reg[2]	Reg[1]
0	0	0	1	PRDI5+Reg[3]	Reg[2]	Reg[1]
0	0	1	0	SPE_G1[5]+Reg[3]	Reg[2]	Reg[1]
0	0	1	1	SPE_G1[5]+Reg[3]	Reg[2]	Reg[1]
0	1	0	0	Reg[3]	Reg[2]	Reg[1]
0	1	0	1	PRDI5	PRDI6	PRDI7
0	1	1	0	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
0	1	1	1	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
1	0	0	0	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	0	0	1	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	0	1	0	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	0	1	1	TPOH_G1[5]	TPOH_G1[6]	TPOH_G1[7]
1	1	0	0	Reg[3]	Reg[2]	Reg[1]
1	1	0	1	PRDI5	PRDI6	PRDI7
1	1	1	0	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
1	1	1	1	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]

Table 31 Notes:

1. IBER = 1 when inband reporting is enabled. Inband error reporting is enabled when RXSEL[1:0] = ”10” in the SPECTRA-155 Receive Path AIS Control #1, #2, and #3 registers (bits 7:6 in registers 101H, F0H, F1H).
2. SPE_G1[7:5] = bits 7 through 5 of the G1 byte on the ADD bus
3. PRDI7, PRDI6, PRDI5 = bits 7 through 5 of the G1 byte from the associated RPOP or the transmit alarm port of the SPECTRA-155
4. Reg[3:1] = PRDI, EPRDI6, EPRDI7 register bit values, respectively
5. TPOH_G1[7:5] = the TPOH port values during the time slots reserved for bits 7 through 5 of the G1 byte

PRDI:

The PRDI bit controls the insertion of the STS path receive defect indication alarm. The function is described in the table above. This bit has no effect when the primary input TPOHEN is high during the path PRDI alarm bit position in the path overhead input stream, TPOH, in which case the value to taken from TPOH.

PREI[3:0]:

The path remote error indication count (PREI[3:0]) is inserted in the path REI bit positions in the path status byte when the corresponding TPOHEN input is low during the path status REI bit positions in the corresponding path

overhead input stream, TPOH. The value contained in PREI[3:0] is cleared after being inserted in the path status byte. Any non-zero PREI[3:0] value overwrites the value that would normally have been inserted based on the number of PREIs accumulated from the BIP-8 errors detected by the companion RPOP in the SPECTRA-155 during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Register 13AH, 17AH, 1BAH: TPOP Path User Channel

Bit	Type	Function	Default
Bit 7	R/W	F2[7]	0
Bit 6	R/W	F2[6]	0
Bit 5	R/W	F2[5]	0
Bit 4	R/W	F2[4]	0
Bit 3	R/W	F2[3]	0
Bit 2	R/W	F2[2]	0
Bit 1	R/W	F2[1]	0
Bit 0	R/W	F2[0]	0

This register contains the value to be inserted in the path user channel byte (F2) of the transmit stream.

F2[7:0]:

The F2[7:0] bits are inserted in the F2 byte position in the transmit stream when the corresponding TPOHEN input is low during the path user channel bit positions in the corresponding path overhead input stream, TPOH.

Register 13BH, 17BH, 1BBH: TPOP Path Growth #1

Bit	Type	Function	Default
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

This register contains the value to be inserted in the path growth byte #1 (Z3) of the transmit stream.

Z3[7:0]:

The Z3[7:0] bits are inserted in the Z3 byte position in the transmit stream when the corresponding TPOHEN input is low during the path growth #1 bit positions in the corresponding path overhead input stream, TPOH.

Register 13CH, 17CH, 1BCH: TPOP Path Growth #2

Bit	Type	Function	Default
Bit 7	R/W	Z4[7]	0
Bit 6	R/W	Z4[6]	0
Bit 5	R/W	Z4[5]	0
Bit 4	R/W	Z4[4]	0
Bit 3	R/W	Z4[3]	0
Bit 2	R/W	Z4[2]	0
Bit 1	R/W	Z4[1]	0
Bit 0	R/W	Z4[0]	0

This register contains the value to be inserted in the path growth byte #2 (Z4) of the transmit stream.

Z4[7:0]:

The Z4[7:0] bits are inserted in the Z4 byte position in the transmit stream when the corresponding TPOHEN input is low during the path growth #2 bit positions in the corresponding path overhead input stream, TPOH.

Register 13DH, 17DH, 1BDH: TPOP Tandem Connection Maintenance

Bit	Type	Function	Default
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

This register contains the value to be inserted in the tandem connection maintenance byte (Z5) of the transmit stream.

Z50-Z57:

The Z5[7:0] bits are inserted in the Z5 byte position in the transmit stream when the corresponding TPOHEN input is low during the tandem connection maintenance byte positions in the corresponding path overhead input stream, TPOH.

Register 13EH: TPOP Concatenation LSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[7]	1
Bit 6	R/W	CONCAT[6]	1
Bit 5	R/W	CONCAT[5]	1
Bit 4	R/W	CONCAT[4]	1
Bit 3	R/W	CONCAT[3]	1
Bit 2	R/W	CONCAT[2]	1
Bit 1	R/W	CONCAT[1]	1
Bit 0	R/W	CONCAT[0]	1

Register 13FH: TPOP Concatenation MSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[15]	1
Bit 6	R/W	CONCAT[14]	0
Bit 5	R/W	CONCAT[13]	0
Bit 4	R/W	CONCAT[12]	1
Bit 3	R/W	CONCAT[11]	0
Bit 2	R/W	CONCAT[10]	0
Bit 1	R/W	CONCAT[9]	1
Bit 0	R/W	CONCAT[8]	1

The TPOP Concatenation LSB and MSB Registers controls the value inserted in the concatenation indicators in the transmit stream.

CONCAT[15:0]:

The CONCAT[15:0] bits control the value inserted in the second and third H1 and H2 byte positions when transmitting an STS-3c (STM-1/AU4) stream. The value written to CONCAT[15:8] is inserted in the H1 byte position of STS-1 (STM-0/AU3) #2 and STS-1 (STM-0/AU3) #3 in the concatenated transmit stream. The value written to CONCAT[7:0] is inserted in the H2 byte position of STS-1 (STM-0/AU3) #2 and STS-1 (STM-0/AU3) #3 in the concatenated transmit stream. The default values represent the normal concatenation indication (all ones in the pointer bits, zeros in the unused bits,

and NDF enabled indication). CONCAT[15:0] is not used when transmitting an STS-1 (STM-0/AU3) or an STS-3 (STM-1/AU3) stream.

Register 140H, 180H, 1C0H: TTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved3	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	Reserved2	1
Bit 3	R/W	ISFE	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	PJEE	0
Bit 0	R/W	Reserved1	0

This register allows the operation of the Transmit Telecombus Aligner to be configured.

Reserved1:

The reserved1 bit must be set low for correct operation of the SPECTRA-155.

PJEE:

The pointer justification event interrupt enable bit (PJEE) controls the activation of the interrupt output when a pointer justification is inserted in the transmit stream. When PJEE is set high, insertion of pointer justification events in the transmit stream will activate the interrupt (INTB) output. When PJEE is set low, insertion of pointer justification events in the transmit stream will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events will affect the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

ISFE:

The incoming signal failure interrupt enable bit (ISFE) controls the activation of the interrupt output when the ISF state in the tandem connection maintenance byte changes to indicate failure or to indicate normal operation.

Reserved2:

The reserved2 bit must be set high for correct operation of the SPECTRA-155.

CLRFS:

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns in virtual tributary (low order tributary) mappings to zero. When a logic 1 is written to CLRFS, the fixed stuff column data are set to 00H. When a logic 0 is written to CLRFS, the fixed stuff column data from the ADD bus is placed on the transmit stream unchanged. The location of the fixed stuff columns in the synchronous payload envelope (virtual container) is dependent on the whether the SPECTRA-155 is processing concatenated payload.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the TTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the ADD bus is placed in the transmit stream unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multiframe is synchronized by the V1 pulse in AC1J1V1 input.

Reserved3:

The Reserved3 bit must be set low for correct operation of the SPECTRA-155.

Register 141H, 181H, 1C1H: TTAL Interrupt Status and Control

Bit	Type	Function	Default
Bit 7	R/W	DOPJ[1]	0
Bit 6	R/W	DOPJ[0]	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	Reserved	0

This register allows the control of the transmit stream and sensing of interrupt status.

The interrupt bits (and the interrupt) are cleared when this register is read.

Reserved:

The Reserved bit must be set low for correct operation of the SPECTRA-155.

NPJI:

The transmit stream negative pointer justification interrupt status bit (NPJI) is set high when the TTAL inserts a negative pointer justification event in the transmit stream.

PPJI:

The transmit stream positive pointer justification interrupt status bit (PPJI) is set high when the TTAL inserts a positive pointer justification event in the transmit stream.

ESEI:

The DROP bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in TTAL underflows or overflows.

ESD0- ESD1:

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds ie., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 33 - Transmit ESD[1:0] codepoints.

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definition:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing negative justification at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the TTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the TTAL will start generates outgoing positive justification at the rate of in 1 every 4 frames).

DOPJ0- DOPJ1:

The diagnose pointer justification bits (DOPJ[1:0]) allow downstream pointer processing elements to be diagnosed for correct reaction to pointer justification events. Setting DOPJ[1] high and DOPJ[0] low, forces the TTAL to generate positive stuff justification events in the transmit stream at the rate of one every four frames regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to overflow. Setting DOPJ[1] low and DOPJ[0] high, forces the TTAL to generate negative stuff justification events at the rate of one every four frames, regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to underflow. Setting both DOPJ[1] and DOPJ[0] high disables the TTAL from generating pointer justification events. If the incoming and outgoing clocks have a frequency offset, the internal FIFO may under/overflow depending on the relative frequencies of the clocks. Pointer justification events are generated based on the current depth of the internal FIFO when DOPJ[1] and DOPJ[0] are both set low. When DOPJ[1:0] is set to values other than 'b00, the detection of elastic store over/underflow is disabled.

Register 142H, 182H, 1C2H: TTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	ISFV	X
Bit 6	R	ISFI	X
Bit 5	R/W	Reserved2	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	FISF	0
Bit 2	R/W	TTCTE	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register controls the tributary format on the transmit stream.

DH4:

The diagnose multiframe indicator enable bit (DH4) controls the inversion of the multiframe indicator (H4) byte in the TRANSMIT stream. This bit may be used to cause an out of multiframe alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic 0 is written to this bit position, the H4 byte is unmodified. When a logic 1 is written to this bit position, the H4 byte is inverted.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the transmit stream when a FIFO underflow or overflow has been detected in the elastic store . When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the transmit stream for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

TTCTE:

The TTCTE bit controls whether the TTAL is terminating a tandem connection. When TTCTE is set high, Incoming Signal Failure codes (ISF) in the Incoming Error Count field (IEC) of the tandem connection maintenance byte (Z5) is translated into path AIS in the transmit stream. For normal IEC values, the Z5 byte is cleared to zero and the B3 byte is updated to reflect the change to Z5. When TTCTE is set low, the TTAL is not terminating a tandem connection. The Z5 and B3 bytes are not modified by the TTAL.

FISF:

The FISF bit controls the filtering of ISF codes in the receive stream. When FISF is set high, path AIS will only be inserted in the transmit stream after detection of active ISF in three consecutive frames. Similarly, path AIS is removed after detection of inactive ISF in three consecutive frames. When FISF is set low, path AIS insertion occurs immediately on detection of active ISF and removal occurs immediately on detection of inactive ISF.

ITUAIS:

The insert tributary path AIS bits controls the insertion of Tributary Path AIS in the transmit stream when transmitting VT11 (TU11), VT12 (TU12) and VT2 (TU2) payloads. When ITUAIS is set high, columns in the transmit stream carrying tributary traffic are set to all ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low. The ITUAIS bit does not work for VT3 (TU3) tributary payloads and the ITUAIS bit must be set low.

Reserved2:

The Reserved bit must be set to logic 0 for correct operation of the SPECTRA-155.

ISFI:

The incoming signal failure alarm interrupt status bit (ISFI) is set high when the TTAL detects a change in the ISF state (from normal to signal failure, or vice versa). This bit is cleared when this register is read. This bit is only active when TTCTE is set high. When TTCTE is set low, this bit should be ignored.

ISFV:

The incoming signal failure alarm status bit (ISFV) reports the status of the ISF state derived from the ISF code in the tandem connection maintenance byte (Z5) of the ADD bus. This bit is only active when TTCTE is set high. When TTCTE is set low, this bit should be ignored.

Register 148H, 188H, 1C8H: SPTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SPTB.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes. When LEN16 is set high, the path trace message length is 16 bytes. When LEN16 is set low, the path trace message length is 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignore and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit path trace buffer is sent to TPOP. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive path trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, path trace identifier message state changes will not affect INTB.

RTIUIE:

The receive path trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for eight messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received path trace identifier message stable/unstable state of will activate the interrupt (INTB) output. When RTIUIE is set low, path trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the SPECTRA-155. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN:

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZEROs path trace message string. When ZEROEN is set high, all ZEROs path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs path trace message strings are ignored. TIU assertion and removal are not affected by setting this register bit.

Register 149H, 189H, 1C9H: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5	R	UNEQI	X
Bit 4	R	UNEQV	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV:

The receive path trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message. If the accepted path trace message string is all-ZEROs, the mismatch is not declared unless the ZEROEN bit in the SPTB Control register is set.

RTIMI:

The receive path trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV:

The receive path trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. An unstable counter is increment when the current message differs from its immediate predecessor. RTIUV is set high when the unstable count reaches eight. RTIUV is set low when the current message becomes the accepted message.

RTIUI:

The receive path trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

UNEQV:

The receive path signal label unequipped status bit (UNEQV) reports the unequipped status of the path signal label. UNEQV is set high when the filtered path signal label indicates unequipped. UNEQV is set low when the filtered path signal label does not indicate unequipped.

UNEQI:

The receive path signal label unequipped interrupt status bit (UNEQI) is set high when equipped/unequipped status of the path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SPTB Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the SPTB Indirect Data register. The maximum latency for BUSY to return low is 10 μs.

Register 14AH, 18AH, 1CAH: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the path trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the J1 bytes of the transmit stream. Addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the path trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the path trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SPTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the SPTB Indirect Data register will be written to the addressed location in the static page.

Register 14BH, 18BH, 1CBH: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 14CH, 18CH, 1CCH: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This register contains the expected path signal label byte in the receive stream.

EPSL[7:0]:

The EPSL[7:0] bits contain the expected path signal label byte (C2). EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if the accepted PSL differs from the expected PSL. Path AIS may be optionally inserted in the DROP bus when PSLM is declared. If enabled, an interrupt is asserted upon declaration and removal of PSLM.

Register 14DH, 18DH, 1CDH: SPTB Path Signal Label Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5	R/W	UNEQIE	0
Bit 4		Unused	X
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

This register reports the path signal label status of the SPTB.

RPSLMV:

The receive path signal label mismatch status bit (RPSLMV) reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is set high when the accepted PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL.

RPSLMI:

The receive path signal label mismatch interrupt status bit (RPSLMI) is set high when the match/mismatch status between the accepted and the expected path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

RPSLUV:

The receive path signal label unstable status bit (RPSLUV) reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is set high when the current received C2 byte differs from the previous C2 byte for five consecutive frames. RPSLUV is set low when the same PSL code is received for five consecutive frames.

RPSLUI:

The receive path signal label unstable interrupt status bit (RPSLUI) is set high when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

UNEQIE:

The receive path signal label unequipped interrupt enable bit (UNEQIE) controls the activation of the interrupt output when the path signal label changes from path signal label unequipped to any other value or vice versa. When UNEQIE is set high, changes of the filtered path signal label changes from unequipped to equipped and vice versa activates the interrupt (INTB) output. When UNEQIE is set low, changes in the filtered path signal will not affect INTB.

RPSLMIE:

The receive path signal label mismatch interrupt enable bit (RPSLMIE) controls the activation of the interrupt output when the comparison between accepted and the expected path signal label changes state from match to mismatch and vice versa. When RPSLMIE is set high, changes in match state activates the interrupt (INTB) output. When RPSLMIE is set low, path signal label state changes will not affect INTB.

RPSLUIE:

The receive path signal label unstable interrupt enable bit (RPSLUIE) controls the activation of the interrupt output when the received path signal label changes state from stable to unstable and vice versa. When RPSLUIE is set high, changes in stable state activates the interrupt (INTB) output. When RPSLUIE is set low, path signal label state changes will not affect INTB.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB, and WRB inputs in Motorola mode, as well as having MBEB input set high, causes all output pins, and the data bus to be held in a high-impedance state. This test feature may be used for board or module level testing.

Test mode registers are used to apply test vectors during production testing of the SPECTRA-155. Test mode registers (as opposed to normal mode registers) are selected when A[9] is high.

Test mode registers may also be used for board or module level testing. When all of the constituent TSBs within the SPECTRA-155 are placed in test mode 0, device inputs may be observed, and device outputs may be controlled via the microprocessor interface (refer to the "Test Mode 0" section below for details).

11.1 Test Mode Register Address Map

Table 34 - Test mode register address map.

Address A[9:0]	Register
000H-1FFH	SPECTRA-155 Normal mode registers
200H	SPECTRA-155 Master Test register
201H	SPECTRA-155 Analog Test Access register
202H-203H	Reserved
204H-207H	TLOP test registers (0-3)
208H-20BH	RLOP test registers (0-3)
20CH-20FH	Reserved
210H-213H	RSOP test registers (0-3)
214H-217H	Reserved
218H-21BH	TSOP test registers (0-3)
21CH-21FH	Reserved
220H-223H	RASE test registers (0-3)
224H-237H	Reserved
238H-239H	SSTB test registers (0-1)
23AH-23FH	Reserved

Address A[9:0]	Register
240H-241H	CRSI test registers (0-1)
242H-243H	CSPI test registers (0-1)
250H-26FH	SPECTRA-155 test registers (0-31)
270H-28FH	Reserved
290H-293H	D3MD#1 test registers (0-3)
294H-297H	D3MA#1 test registers (0-3)
298H-29BH	D3MD#2 test registers (0-3)
29CH-29FH	D3MA#2 test registers (0-3)
2A0H-2A3H	D3MD#3 test registers (0-3)
2A4H-2A7H	D3MA#3 test registers (0-3)
2A8H-2AFH	Reserved
2B0H-2B6H	TPIP#1 test registers (0-6)
2B7H-2BFH	Reserved
2C0H-2C6H	TPIP#2 test registers (0-6)
2C7H-2CFH	Reserved
2D0H-2D6H	TPIP#3 test registers (0-6)
2D7H-30FH	Reserved
310H-316H	RPOP#1 test registers (0-6)
317H-31FH	Reserved
320H-321H	PMON#1 test registers (0-1)
322H-327H	Reserved
328H-32BH	RTAL#1 test registers (0-3)
32AH-32FH	Reserved
330H-334H	TPOP#1 test registers (0-4)
335H-33FH	Reserved
340H-343H	TTAL#1 test registers (0-3)
344H-347H	Reserved
348H-349H	SPTB#1 test registers (0-1)
34AH-34FH	Reserved

Address A[9:0]	Register
350H-356H	RPOP#2 test registers (0-6)
357H-35FH	Reserved
360H-361H	PMON#2 test registers (0-1)
362H-367H	Reserved
368H-36BH	RTAL#2 test registers (0-3)
36CH-36FH	Reserved
370H-374H	TPOP#2 test registers (0-4)
375H-37FH	Reserved
380H-383H	TTAL#2 test registers (0-3)
384H-387H	Reserved
388H-389H	SPTB#2 test registers (0-1)
38AH-38FH	Reserved
390H-396H	RPOP#3 test registers (0-6)
397H-39FH	Reserved
3A0H-3A1H	PMON#3 test registers (0-1)
3A2H-3A7H	Reserved
3A8H-3ABH	RTAL#3 test registers (0-3)
3ACH-3AFH	Reserved
3B0H-3B4H	TPOP#3 test registers (0-4)
3B5H-3BFH	Reserved
3C0H-3C3H	TTAL#3 test registers (0-3)
3C4H-3C7H	Reserved
3C8H-3C9H	SPTB#3 test registers (0-1)
3CAH-3FFH	Reserved

Notes on Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Register Address 200H: SPECTRA-155 Master Test

Bit	Type	Function	Default
Bit 7	R/W	ATST	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	MOTOTST	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable SPECTRA-155 test features. All bits, except PMCTST, are reset to zero by a reset of the SPECTRA-155.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the SPECTRA-155. While the HIZIO bit is a logic one, all output pins of the SPECTRA-155 except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the SPECTRA-155 for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

MOTOTST:

The MOTOTST bit is used to test the MOTOROLA interface. When MOTOTST is logic one and the MBEB input is logic zero the SCPI[1] and SCPI[0] inputs are used to replace the function of E and RWB, respectively. This is done because the fixed waveform shapes assigned to the RDB/E and WRB/RWB inputs can not be used to test MOTOROLA type microprocessor interface logic. This mode is also used to test the D.C. drive capability of the D[7:0] device pins.

PMCTST:

The PMCTST bit is used to configure the SPECTRA-155 for PMC's manufacturing tests. When PMCTST is set to logic one, the SPECTRA-155 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic one or by writing a logic zero.

ATST:

The ATST bit is used to configure the SPECTRA-155 for PMC's manufacturing tests. When ATST is set to logic one, the SPECTRA-155 is configured for analog production tests.

11.2 Test Mode 0

In test mode 0, the SPECTRA-155 allows the logic levels on the device inputs to be observed through the microprocessor interface, and allows the device outputs to be controlled to either logic level through the microprocessor interface.

Test mode 0 is enabled by resetting the device (using the RSTB input, or the SPECTRA-155 reset and identity register), and then setting the IOTST bit in the SPECTRA-155 Master Test register. The following addresses must then be written with the value 00H: 205H, 209H, 211H, 219H, 221H, 239H, 241H, 243H, 251H, 291H, 295H, 299H, 29DH, 2A1H, 2A5H, 2B1H, 2C1H, 2D1H, 311H, 321H, 329H, 331H, 341H, 349H, 351H, 361H, 369H, 371H, 381H, 389H, 391H, 3A1H, 3A9H, 3B1H, 3C1H, 3C9H.

The following registers can be read to sense primary input pins of the SPECTRA-155.

Table 35 - Test mode 0 primary input read registers.

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01FH			SCPI[1]	SCPI[0]				
204H	TTOHEN[1]	TLOW	TLD/ TSLD[2]		TOH		TTOH1[1]	
207H					RLAIS[3]	TLAIS/ TLRDI[4]		
218H	TSUC[5]	TSOW[5]						
240H			RBYP					RXD
241H				ALOS				
242H					TBYP			
256H[6]		SS[34]	SS[33]	SS[32]				

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
257H							TAD	TAFP
260H[8]						SMODE [2]	SMODE [1]	SMODE [0]
261H			SS[1][8]					
262H							SS[26][10]	
263H[7]			SS[18]	SS[17]	SS[16]	SS[24]	SS[23]	SS[22]
264H[7]		SS[25]	SS[15]	SS[14]	SS[13]	SS[21]	SS[20]	SS[19]
268H[9]						SS[3]	SS[2]	SS[0]
310H			RTCEN[1]	RTCOH[1]				
350H			RTCEN[2]	RTCOH[2]				
390H			RTCEN[3]	RTCOH[3]				
333H	TACK[11]							
333H							TPOH[1] 12	TPOHEN [1]
373H							TPOH[2] 13	TPOHEN [2]
3B3H							TPOH[3] 14	TPOHEN [3]

Notes:

1. One TCK cycle is required before the read.
2. TSLD input whenTLDSEL='1' in normal register 082H, otherwise TLD input.
3. RCP bit normal register 001H and RINGEN bit in normal register 017H must both be set to '1'. The inverse of RLAIS input is seen.
4. RCP bit normal register 001H and RINGEN bit in normal register 017H must both be set to '1'. TLAIS input is seen when TLRDI input is held at logic zero, and the inverse of TLRDI is seen when TLAIS is held at logic one.
5. The TLOP OWCLK must be toggled in TLOP test register 0 (bit 4) to sample these inputs. These inputs are sampled on the rising edge of TLOP OWCLK.
6. SMODE input set to "000".
7. SPECTRA-155 test register 25AH bit 0 must be set to logic one.
8. SPECTRA-155 test register 25AH bit 1 must be set to logic one.

9. SPECTRA-155 test register 25AH bit 1 must be set to logic one and SMODE input set to "010".

10. SPECTRA-155 test register 25AH bit 6 must be set to logic one.

11. The inverse of the TACK input is seen when bits 7:6 (RXSEL) of normal register 101H are set to "01".

12. The TPOHEN[1] input must be set to logic one.

13. The TPOHEN[2] input must be set to logic one.

14. The TPOHEN[3] input must be set to logic one.

A write to one of the following locations forces each output to the value in the corresponding bit position.

Table 36 - Test mode 0 primary output write registers.

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
014H							SCPO[1]	SCPO[0]
204H[1]			TOHCLK	TOWCLK	TLDCLK			
208H[1]	ROH			LRDI	LAIS	RFP		
20AH[1]				ROHCLK	RLD	RLDCLK	RLOW	ROWCLK
210H[1]			LOF	SALM	LOS			
212H[1]			RSOW		RSLD	RSLDCLK	RSUC	
213H[1]						RTOHFP	RTOHCLK	RTOH1
218H[1]					TSLDCLK			
21AH[1]								TFP
241H		SS[0][2]	RXC[3]					
258H	RAD							
25EH								TTOHCLK[4]
25FH								TTOHFP[4]
260H	SS[31][5]	SS[30][5]/ SS[12][6]	SS[11][6]	SS[10][6]				
261H[6]	SS[9]	SS[8]	SS[7]	SS[6]	SS[5]	SS[4]	SS[3]	SS[2]
296H							SS[27][7]	
29EH							SS[28][7]	
2A6H							SS[29][7]	

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
312H			RALM[1][8]			B3E[1]		
313H						RPOHFP [1]	RPOH[1]	RPOHCLK [1]
333H					TPOHCLK [1]	TPOHFP [1]		
352H			RALM[2][8]			B3E[2]		
353H						RPOHFP [2]	RPOH[2]	RPOHCLK [2]
373H					TPOHCLK [2]	TPOHFP [2]		
392H			RALM[3][8]			B3E[3]		
393H						RPOHFP [3]	RPOH[3]	RPOHCLK [3]
3B3H					TPOHCLK [3]	TPOHFP [3]		

Notes:

1. One TCK cycle is required after the write.
2. SMODE input must be set to "011" and SPECTRA-155 test register 25BH bit 1 set to logic one. SPECTRA-155 test register 260H bit 7 set to logic one. ss[27] input set to logic zero. The inverse logic level is provided at ss[0].
3. SPECTRA-155 normal register 000H must be set 00H and SPECTRA-155 normal register 080H bit 6 must be set to logic one.
4. SPECTRA-155 test register 250H bit 3 must be set to logic one.
5. SPECTRA-155 test register 25BH bit 6 must be set to logic one and SMODE input set to "000".
6. SPECTRA-155 test register 25BH bit 1 must be set to logic one and SMODE input set to "000". ss[0] input set to logic zero.
7. SMODE input must be set to "101"
8. SPECTRA-155 normal register 000H bit 1 must be set to logic one. SPECTRA-155 normal registers 084H, 085H and 086H bit 0 must be set to logic one. One TCK cycle is required after the write.

11.3 JTAG Test Port

The SPECTRA-155 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 37 - JTAG Instruction Register Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 2H

Part Number - 5342H

Manufacturer's identification code - 0CDH

Device identification - 253420CDH

Boundary Scan Register

The boundary scan register is made up of TBD boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells form the ID code register, and carry the code 253420CDH. The cells are arranged as follows:

Table 38 - Boundary scan register.

Pin/ Enable	Reg Bit	Cell Type	I.D. Bit	Pin/ Enable	Reg Bit	Cell Type	I.D. Bit
SCPI[0:1]	172:171	IN_CELL	00	RLD	81	OUT_CELL	
RSTB	170	IN_CELL	1	RLDCLK	80	OUT_CELL	
ALE	169	IN_CELL	0	RTOH1	79	OUT_CELL	
A[0:9]	168:159	IN_CELL	0101001101	RTOHCLK	78	OUT_CELL	
MBEB	158	IN_CELL	0	RTOHFP	77	OUT_CELL	
CSB	157	IN_CELL	0	RFP	76	OUT_CELL	
RDB_E	156	IN_CELL	0	ROH_TS2 (5)	75	OUT_CELL	
WRB_RWB	155	IN_CELL	0	RPOH[1:3]	74:72	OUT_CELL	
SS[1]	154	IN_CELL	1	RPOHCLK[1:3]	71:69	OUT_CELL	
SS[13:25]	153:141	IN_CELL	0000011001101	RPOHFP[1:3]	68:66	OUT_CELL	
SS[26]	140	IN_CELL		RALM[1:3]	65:63	OUT_CELL	
SS[32:34]	139:137	IN_CELL		B3E[1:3]	62:60	OUT_CELL	
SMODE[0:2]	136:134	IN_CELL		RAD	59	OUT_CELL	
TPOHEN[1:3]	133:131	IN_CELL		TFP	58	OUT_CELL	
TPOH[1:3]	130:128	IN_CELL		TOH_TS1 (6)	57	OUT_CELL	
TTOHEN	127	IN_CELL		TOWCLK	56	OUT_CELL	
TTOH	126	IN_CELL		TOHCLK	55	OUT_CELL	
TLAIS_TRCPDAT	125	IN_CELL		TOH_TS (7)	54	OUT_CELL	
TLRDI_TRCPFP	124	IN_CELL		TLDCLK	53	OUT_CELL	
TSLD	123	IN_CELL		TSLDCLK	52	OUT_CELL	
TLD	122	IN_CELL		TSLD_TS (8)	51	OUT_CELL	
TOH	121	IN_CELL		TTOHCLK	50	OUT_CELL	
TACK	120	IN_CELL		TTOHFP	49	OUT_CELL	
TAFP	119	IN_CELL		TPOHCLK[1:3]	48:46	OUT_CELL	
TAD	118	IN_CELL		TPOHFP[1:3]	45:43	OUT_CELL	
TLOW	117	IN_CELL		HIZ (9)	42	OUT_CELL	
TSUC	116	IN_CELL		SS[4:12]	41:33	OUT_CELL	
TSOW	115	IN_CELL		SS[28:31]	32:29	OUT_CELL	
RTCOH[3:1]	114:112	IN_CELL		SS[0]	28	IO_CELL	
RTCEN[3:1]	111:109	IN_CELL		SS_IO_OENB[0] (10)	27	OUT_CELL	

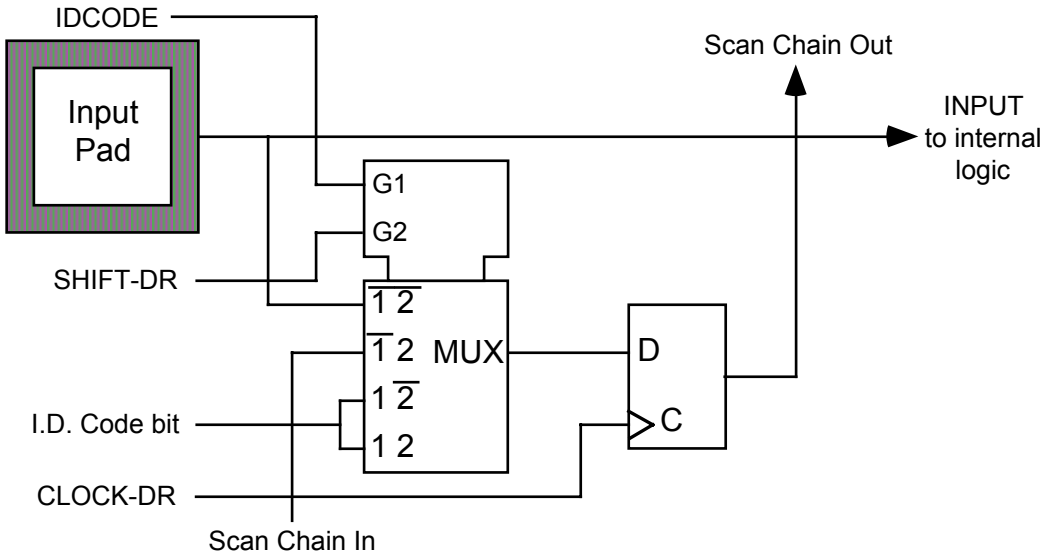
Pin/ Enable	Reg Bit	Cell Type	I.D. Bit	Pin/ Enable	Reg Bit	Cell Type	I.D. Bit
TRIS_OHB	108	IN_CELL		SS[2]	26	IO_CELL	
RLAIS_TRCPCLK	107	IN_CELL		SS_IO_OENB[2] (11)	25	OUT_CELL	
RBYP	106	IN_CELL		SS[3]	24	IO_CELL	
TBYP	105	IN_CELL		SS_IO_OENB[3] (12)	23	OUT_CELL	
TXDP	104	OUT_CELL		SS[27]	22	IO_CELL	
TXDN	103	OUT_CELL		SS_IO_OENB[27] (13)	21	OUT_CELL	
TXC	102	OUT_CELL		INTB	20	OUT_CELL	
TCLK	101	OUT_CELL		D[0]	19	IO_CELL	
RCLK	100	OUT_CELL		OENB7 (14)	18	OUT_CELL	
RXC	99	OUT_CELL		D[1]	17	IO_CELL	
LOF	98	OUT_CELL		OENB6 (15)	16	OUT_CELL	
LOS_RRCPFP	97	OUT_CELL		D[2]	15	IO_CELL	
LRDI_RRCPCLK	96	OUT_CELL		OENB5 (16)	14	OUT_CELL	
LAIS_RRCPDAT	95	OUT_CELL		D[3]	13	IO_CELL	
SALM	94	OUT_CELL		OENB4 (17)	12	OUT_CELL	
ROWCLK	93	OUT_CELL		D[4]	11	IO_CELL	
RLOW	92	OUT_CELL		OENB3 (18)	10	OUT_CELL	
RSOW	91	OUT_CELL		D[5]	9	IO_CELL	
RSUC	90	OUT_CELL		OENB2 (19)	8	OUT_CELL	
ROHCLK	89	OUT_CELL		D[6]	7	IO_CELL	
ROH_TS1 (1)	88	OUT_CELL		OENB1 (20)	6	OUT_CELL	
ROH	87	OUT_CELL		D[7]	5	IO_CELL	
ROH_TS (2)	86	OUT_CELL		OENB (21)	4	OUT_CELL	
RSLD	85	OUT_CELL		SCPO[0]	3	OUT_CELL	
RSLD_TS1 (3)	84	OUT_CELL		SCPO_TS1 (22)	2	OUT_CELL	
RSLDCLK	83	OUT_CELL		SCPO[1]	1	OUT_CELL	
RSLD_TS (4)	82	OUT_CELL		SCPO_TS (23)	0	OUT_CELL	

NOTES:

1. ROH_TS1 is the active low output enable for ROHCLK
2. ROH_TS is the active low output enable for ROH
3. RSLD_TS1 is the active low output enable for RSLD
4. RSLD_TS is the active low output enable for RSLDCLK
5. ROH_TS2 is the active low output enable for RFP
6. TOH_TS1 is the active low output enable for TFP
7. TOH_TS is the active low output enable for TOHCLK
8. TSLD_TS is the active low output enable for TSLDCLK
9. HIZ is the active low output enable for all other outputs not listed here
10. SS_IO_OENB[0] selects the direction of SS[0]
11. SS_IO_OENB[2] selects the direction of SS[2]
12. SS_IO_OENB[3] selects the direction of SS[3]
13. SS_IO_OENB[27] selects the direction of SS[27]
14. OENB7 selects the direction of D[0]
15. OENB6 selects the direction of D[1]
16. OENB5 selects the direction of D[2]
17. OENB4 selects the direction of D[3]
18. OENB3 selects the direction of D[4]
19. OENB2 selects the direction of D[5]
20. OENB1 selects the direction of D[6]
21. OENB selects the direction of D[7]
22. SCPO_TS1 is the active low output enable for SCPO[0]
23. SCPO_TS is the active low output enable for SCPO[1]

24. SCPI[0] IS the first bit of the scan chain (closest to TDI).

Figure 20 - Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 21 - Output Cell (OUT_CELL)

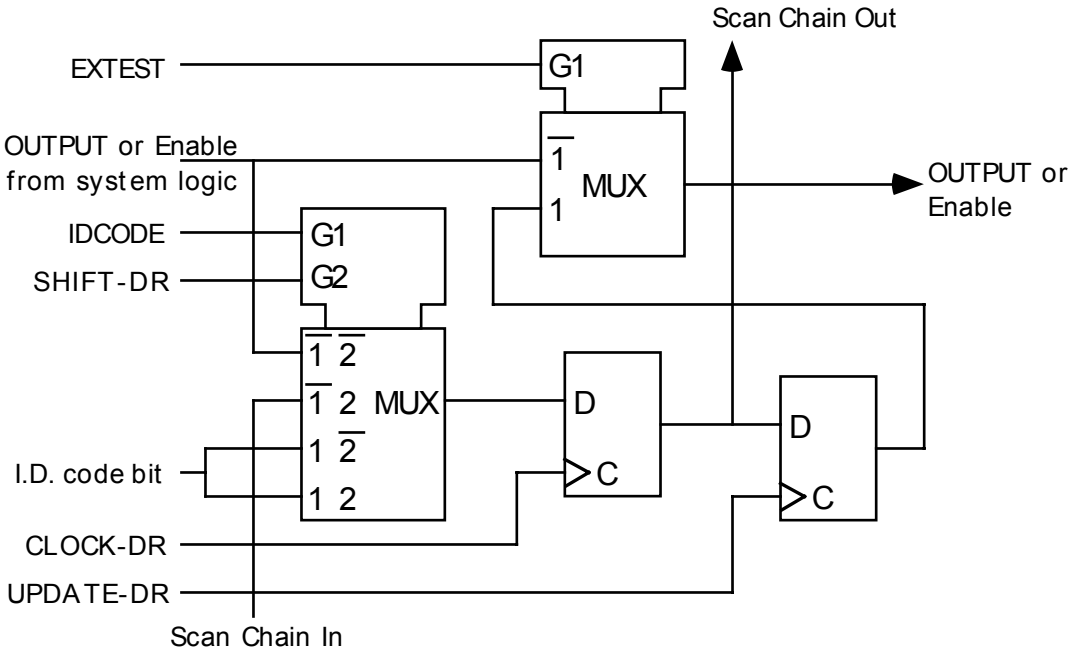


Figure 22 - Bidirectional Cell (IO_CELL)

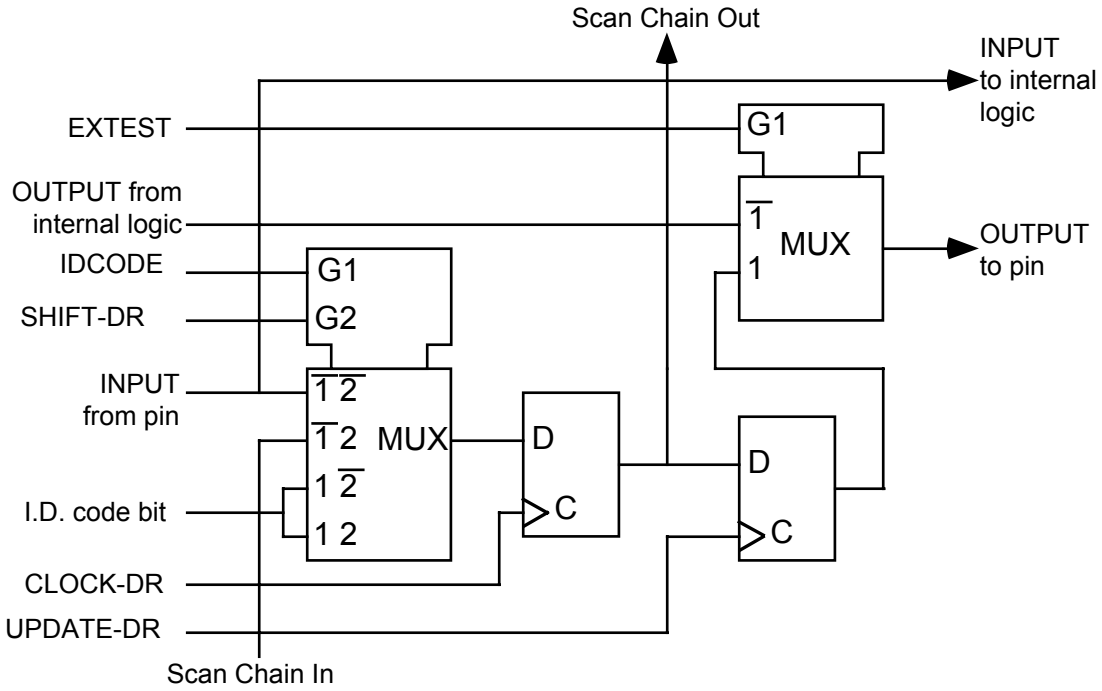
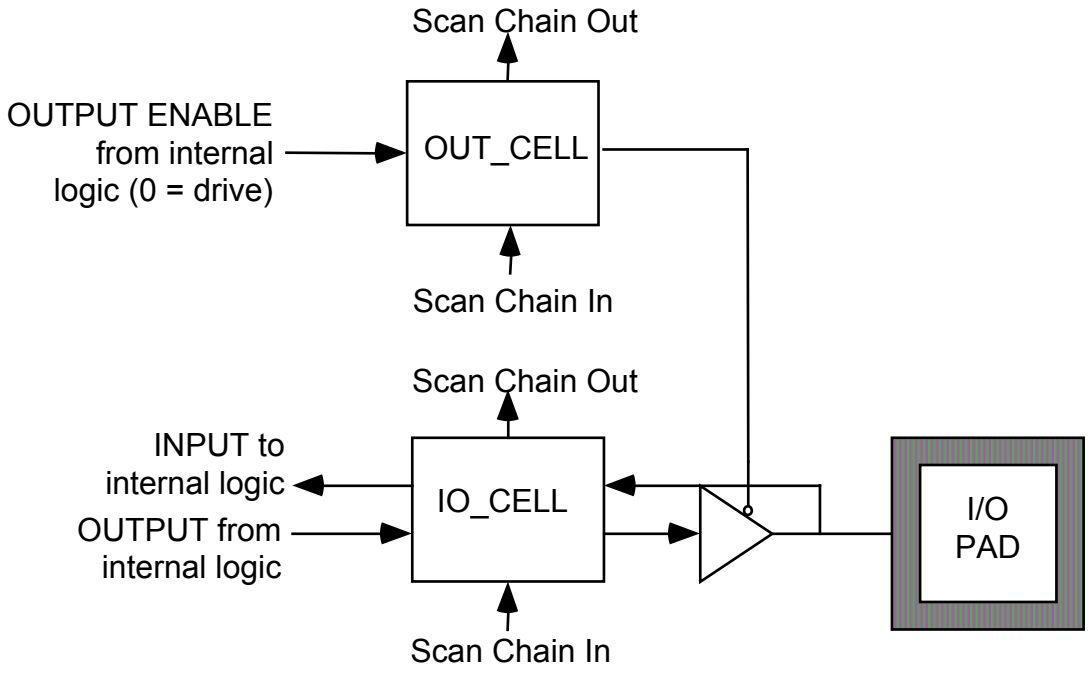


Figure 23 - Layout of Output Enable and Bidirectional Cells



12 OPERATION

This section presents Configuration Options, PCB design recommendations, operating details for the JTAG boundary scan feature and interface details for system side devices.

The SPECTRA-155 is a SONET/SDH PAYLOAD EXTRACTOR/ALIGNER device. It processes the section, line, path overhead of an STS-1 (STM-0/AU3), an STS-3c (STM-1/AU4) or an STS-3 (STM-1/AU3) stream. The SPECTRA-155 supports a rich set of line and system configuration options.

12.1 Line Configuration Options

12.1.1 STS-1 (STM-0/AU3) Mode

The SPECTRA-155 terminates and sources the path payload of a duplex STS-1 (STM-0/AU3) stream.

12.1.2 STS-3 (STM-1/AU3) Mode

The SPECTRA-155 terminates and sources the path payload of a duplex STS-3 (STM-1/AU3) stream. The path overhead of the three multiplexed STS-1 (STM-0/AU3) streams are processed independently.

12.1.3 STS-3c (STM-1/AU4) Mode

The SPECTRA-155 terminates and sources the path payload of a duplex STS-3c (STM-1/AU4) stream.

12.1.4 Originating TCTE Mode

The SPECTRA-155 receive section originates a tandem connection. Incoming BIP-8 errors and a data link are inserted in the tandem connection maintenance byte (Z5) of the DROP bus. The remaining path overhead bytes are unchanged, except under path AIS conditions. The SPECTRA-155 transmit section operates independently in any applicable mode with transmit TCTE bypass mode being most likely.

12.1.5 Transmit TCTE Terminating Mode

The SPECTRA-155 transmit section terminates a tandem connection. Incoming signal failure indication (ISF) generated by the originating TCTE triggers path AIS

insertion in the transmit stream. The SPECTRA-155 receive section operates independently in any applicable mode.

12.1.6 Path and TCTE Terminating Mode

The SPECTRA-155 receive section is simultaneously terminating a path payload and a tandem connection. The incoming error count (IEC) in the tandem connection maintenance byte (Z5) is accumulated and the data link serialized on the low speed RPOH output. Received incoming signal failure code (ISF) will trigger path AIS insertion in the DROP bus. The transmit section of the SPECTRA-155 is unlikely to be in any of the TCTE modes.

12.2 System Configuration Options

12.2.1 Byte Telecombus Mode

The Byte Telecombus mode can be configured by setting inputs SMODE[2:0]=000B. When operating in Byte Telecombus mode, system data can be source to the SPECTRA-155 via an eight bit ADD bus and sourced by the SPECTRA-155 via an eight bit DROP bus. For the ADD bus, the SPECTRA-155 requires either a composite C1, J1, V1 input or optionally a C1 signal coupled with a valid H1, H2 pointer.

The ADD and DROP buses can be either STS-1 (STM-0/AU3), STS-3 (STM-1/AU3) or STS-3c (STM-1/AU4) streams. Both the ADD bus and the DROP bus timing domains can be different from one another as well as different from the SPECTRA-155. The SPECTRA-155 will compensate for timing differences via pointer justifications.

12.2.2 Nibble Telecombus Mode

The Nibble Telecombus mode can be configured by setting inputs SMODE[2:0]=001B. Nibble Telecombus mode is the same as Byte Telecombus mode except that both the ADD and DROP buses are only four bits wide.

12.2.3 Serial Telecombus Mode

The Serial Telecombus mode can be configured by setting inputs SMODE[2:0]=010B. When configured for Serial Telecombus mode, three independent Serial ADD buses and three independent Serial DROP buses are provided. For the ADD buses, the SPECTRA-155 requires either a composite C1, J1, V1 input or optionally a C1 signal coupled with a valid H1, H2 pointer.

Only STS-1 (STM-0/AU3) streams are supported on the ADD and DROP buses. The ADD buses and the DROP buses can all have different timing domains. The SPECTRA-155 will compensate for timing differences via pointer justifications. If configured for STS-1 (STM-0/AU3) mode, the SPECTRA-155 will only use stream #1 on the ADD and DROP buses. If configured for STS-3 (STM-1/AU3) mode, the SPECTRA-155 will multiplex/demultiplex the three serial ADD/DROP bus streams into/out of the SONET/SDH stream.

12.2.4 Byte Data Mode

The Byte Data mode can be configured by setting inputs SMODE[2:0]=011B. For Byte Data Mode operation, the SPECTRA-155 is the clock master and "pulls" data from the system in the transmit direction and "pushes" data to the system in the receive direction.

Only STS-1 (STM-0/AU3) and STS-3c (STM-1/AU4) line side streams are supported for Byte Data mode.

12.2.5 Nibble Data Mode

The Nibble Data mode can be configured by setting inputs SMODE[2:0]=100B. For Nibble Data Mode operation, the SPECTRA-155 is the clock master and "pulls" data from the system in the transmit direction and "pushes" data to the system in the receive direction.

Only STS-1 (STM-0/AU3) and STS-3c (STM-1/AU4) line side streams are supported for Nibble Data mode.

12.2.6 Serial Data Mode

The Serial Data mode can be configured by setting inputs SMODE[2:0]=101B. When configured for Serial Data mode, three independent transmit buses and three independent receive buses are provided. As in other data modes, the SPECTRA-155 is the clock master and "pulls" data from the system in the transmit direction and "pushes" data to the system in the receive direction.

Only STS-1 (STM-0/AU3) and STS-3 (STM-1/AU3) line side streams are supported.

12.2.7 Serial DS3 Mode

The Serial DS3 mode can be configured by setting inputs SMODE[2:0]=110B. When configured for Serial DS3 mode, three independent transmit buses and three independent receive buses are provided. In the transmit direction, the DS3

mapper/synchronizer expects the DS3 source clock to be provided externally. In the receive direction, the DS3 desynchronizer/mapper provides a DS3 output clock which is a gapped version of the receive SONET line clock or a gapped version of an externally provided 44.928 MHz clock.

Only STS-1 (STM-0/AU3) and STS-3 (STM-1/AU3) line side streams are supported.

12.3 Bit Error Rate Monitor

The Receive APS, Synchronization Extractor and Bit Error (RASE) block counts and monitors line BIP errors over programmable periods of time (window size). The RASE contains two Bit Error Rate Monitors (BERM), one monitors the signal fail threshold crossing alarm, and the other monitors the signal degrade threshold crossing alarm.

The tables below give calculated values that are appropriate for both the SF BERM and SD BERM. Typically, the SF threshold will be configured for a BER of 10^{-3} or 10^{-4} and the SD threshold will be configured between 10^{-5} and 10^{-9}. For all of the tables below, the saturation threshold should be disabled by setting SMODE=0.

All of the recommended values below meet the various requirements for detection/clearing and (where applicable) false detection/clearing. In the case of the SDH recommendations, the detection (clearing) thresholds were chosen between the minimum and maximum values established by the detection and false detection requirements. In the case of the Sonet recommendations, the detection thresholds were chosen at their maximum value, and the clearing thresholds at their minimum.

The CMODE column corresponds to the values that should be written to the SFCMODE and SDCMODE bits in the RASE Configuration/Control register. The Accumulation Period column represents the values that should be written to the RASE SF Accumulation Registers and the RASE SD Accumulation Period Registers. . The Detection Threshold column represents the values that should be written to the RASE SF Detection Threshold Registers and the RASE SD Detection Threshold Registers. The Clearing Threshold column represents the values that should be written to the RASE SF Clearing Threshold Registers and the RASE SD Clearing Threshold Period Registers.

Table 39 - RASE-BERM Configuration for SDH STM-0

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.01	0	00000A	0D7	04A
1.0E-04	0.1	0	000064	0D7	04A
1.0E-05	1	0	0003E8	0D7	04A
1.0E-06	10	0	002710	0D7	04A
1.0E-07	100	0	0186A0	0D7	04A
1.0E-08	1000	0	0F4240	0D7	04A
1.0E-09	10000	0	989680	0D7	04A

Table 40 - RASE-BERM Configuration for SDH STM-1

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.01	0	00000A	2A2	0CA
1.0E-04	0.1	0	000064	2A2	0CA
1.0E-05	1	0	0003E8	2A2	0CA
1.0E-06	10	0	002710	2A2	0CA
1.0E-07	100	0	0186A0	2A2	0CA
1.0E-08	1000	0	0F4240	2A2	0CA
1.0E-09	10000	0	989680	2A2	0CA

Table 41 - RASE-BERM Configuration for Sonet STS-1

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.01*	1	00000A	0D9	1B5
1.0E-04	0.04	1	000028	0A7	0B8
1.0E-05	0.3	1	00012C	084	08E
1.0E-06	3	1	000BB8	084	08E
1.0E-07	30	1	007530	084	08E
1.0E-08	250	1	03D090	06D	078
1.0E-09	2000	1	1E8480	055	061

*Detection time objectives and false detection objectives cannot be met simultaneously for STS-1 with a 10^{-3} bit error rate. The given values meet the detection time requirements with a 0.999 probability, and also meet the false detection objectives.

Table 42 - RASE-BERM Configuration for Sonet STS-3

BER	Evaluation Period (s)	CMODE (SFCMODE/ SDCMODE)	Accumulation Period (SFSAP/SDSAP)	Detection Threshold (SFDTH/SDDTH)	Clearing Threshold (SFCTH/SDCTH)
1.0E-03	0.008	1	000008	245	3BE
1.0E-04	0.013	1	00000D	0A3	0B4
1.0E-05	0.1	1	000064	084	08E
1.0E-06	1	1	0003E8	084	08E
1.0E-07	10	1	002710	084	08E
1.0E-08	83	1	014438	06D	077
1.0E-09	667	1	0A2D78	055	061

12.4 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines *must* be followed in order to ensure proper operation.

1. In a noisy board environment, separate digital and analog ground planes should be provided and connected together at the power entry point. Otherwise, a single, solid ground plane is acceptable. Avoid "chopping up" the ground plane, as it often increases power supply noise.

2. In a noisy board environment, separate analog and digital +5 volt planes should be provided and connected together at the power entry point (separate regulation of the analog and digital supplies may also be necessary). Otherwise, a single, solid +5 volt plane, filtered to the appropriate ground planes, is acceptable. Avoid "chopping up" the power plane, as it often increases power supply noise.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistor does not lower the supply voltage below the recommended operating voltage.

4. Separate high-frequency decoupling capacitors are recommended for each analog power pin. These capacitors should be placed as close to the SPECTRA-155 power pin as possible. To prevent noise from coupling between power pins, each of the following sets of pins be decoupled separately:

   Set #1: TAVD2
   Set #2: RAVD2
   Set #3: TAVD1, TAVD3, TAVD4
   Set #4: RAVD1, RAVD3
   Set #5: QAVD1, QAVD2, QAVD3

5. The high speed serial streams (TXD+/- and RXD+/-) must be routed with controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

12.5 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. The recommended power supply sequencing is as follows:

1. To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDD power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification (20 mA).

2. Analog power supplies and VDD must be applied together. To prevent forward biasing the ESD protection diode between AVD supplies and VDD, the differential voltage measured between these power supplies must be less than 0.5 volt. This recommended differential voltage is to include peak to peak noise on the VDD power supply as digital noise will otherwise be coupled into the analog circuitry.

3. Analog power supplies and VDD must be powered down together. Small offsets in VDD and AVD discharge times will not damage the device.

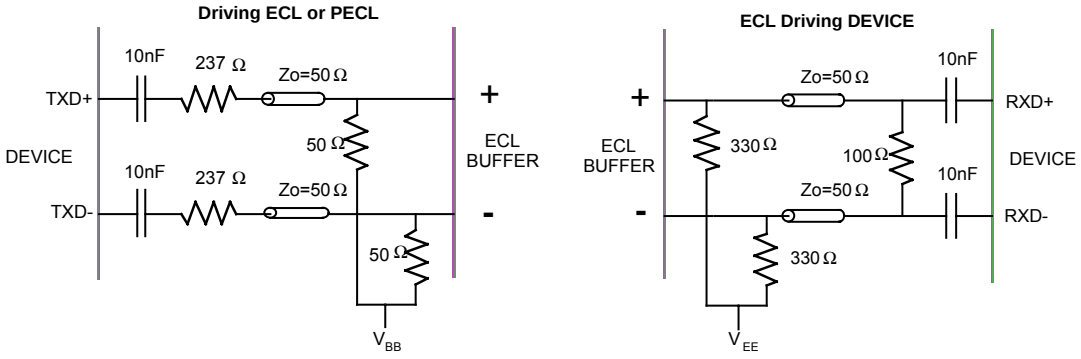
12.6 Interfacing to ECL or PECL Devices

Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. The figure below illustrates the recommended configuration. The capacitors AC couple the outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the 237 Ω and 50 Ω resistors divide the voltage down to a nominally 800mV swing. The 50 Ω resistors also terminate the signals.

Similarly, the RXD+/- inputs to the SPECTRA-155 are AC coupled as shown below. The SPECTRA-155 inputs are self-biasing to improve operating speed and waveform symmetry. For this reason, the DC blocking capacitors are always required, even when interfacing to PECL drivers.

Ceramic coupling capacitors are recommended.

Figure 24 - Interfacing SPECTRA-155 to ECL or PECL



In the recommended TXD+/- termination shown in Figure 24, the TXD +/- outputs are required to drive PECL or ECL inputs and therefore do not have to meet TTL drive specifications. Because they do not have to meet TTL drive specifications,

the TXD+/- outputs can draw more current than their specified 8 mA output rating.

12.7 Driving Differential Inputs Single Ended

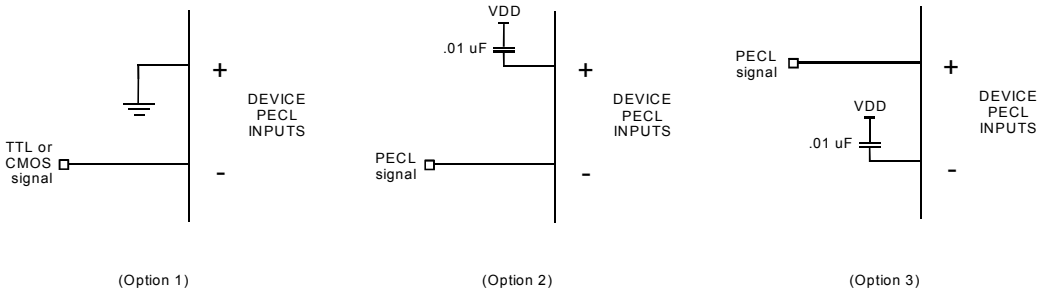
In some applications, it may be more cost effective or technically desirable to drive the ALOS+/-, RRCLK+/- or TRCLK+/- inputs with a single ended TTL, single ended CMOS, or single ended PECL signal. The RXD+/- inputs do not support single ended operation and must be driven by a differential source.

The hardware configurations to drive the ALOS+/- input with a single ended TTL, CMOS or PECL signal are shown in Figure 25.

Option 1 shows the single ended TTL or CMOS configuration; the positive input is grounded and the negative input is DC coupled to the input signal. Using option 1, the input signal is logically inverted (TTL or CMOS signal tied to logic zero indicates analog loss of signal).

Option 2 and option 3 show the two permissible single ended PECL configurations. In option 2, the positive input is tied to VDD through a DC blocking capacitor and the negative input is DC coupled to the input signal. Using option 2, the input signal is logically inverted (PECL signal tied to logic zero indicates analog loss of signal). In option 3, the negative input is tied to VDD through a DC blocking capacitor and the positive input is DC coupled to the input signal. Using option 3, the input signal is not inverted.

Figure 25 - Single Ended Driving Differential ALOS+/- Inputs



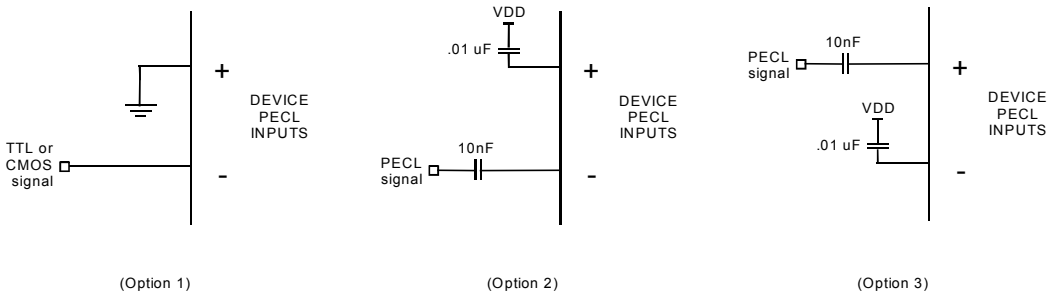
The hardware configurations to drive the RRCLK+/- or TRCLK+/- with a single ended TTL, CMOS or PECL signal are shown in Figure 26. Option 1 and option 2 invert the input signal; option 3 does not. The RRCLK+/- and TRCLK+/- inputs can only be driven with a single ended 19.44 MHz or a 6.48 MHz reference clock. The RRCLK+/- and TRCLK+/- inputs can not be driven with a single ended high-speed input (155.52MHz or 51.84 MHz when in clock recovery or clock synthesis is bypassed). When clock recovery or clock synthesis is

bypassed, the respective RRCLK+/- or TRCLK+/- input must be driven with a differential signal.

For TTL or CMOS signals (option 1), the positive input must be grounded and the negative input must be DC coupled to the TTL or CMOS signal as shown. TTL and CMOS input signals must be connected directly to the negative PECL input with no DC blocking capacitor.

For PECL signals, the option 2 or option 3 configurations are permissible. Using option 2, the positive input must be tied to VDD through a DC blocking capacitor and the negative PECL input must be AC coupled as shown. Using option 3, the negative input must be tied to VDD through a DC blocking capacitor and the positive PECL input must be AC coupled as shown. For PECL input signals, the SPECTRA-155 inputs are self biasing to improve operating signal speed and waveform symmetry. For this reason, when option 2 or option 3 are used, the DC blocking capacitors between the PECL signal and the SPECTRA-155 inputs are always required even when interfacing to PECL drivers. Ceramic coupling capacitors are recommended.

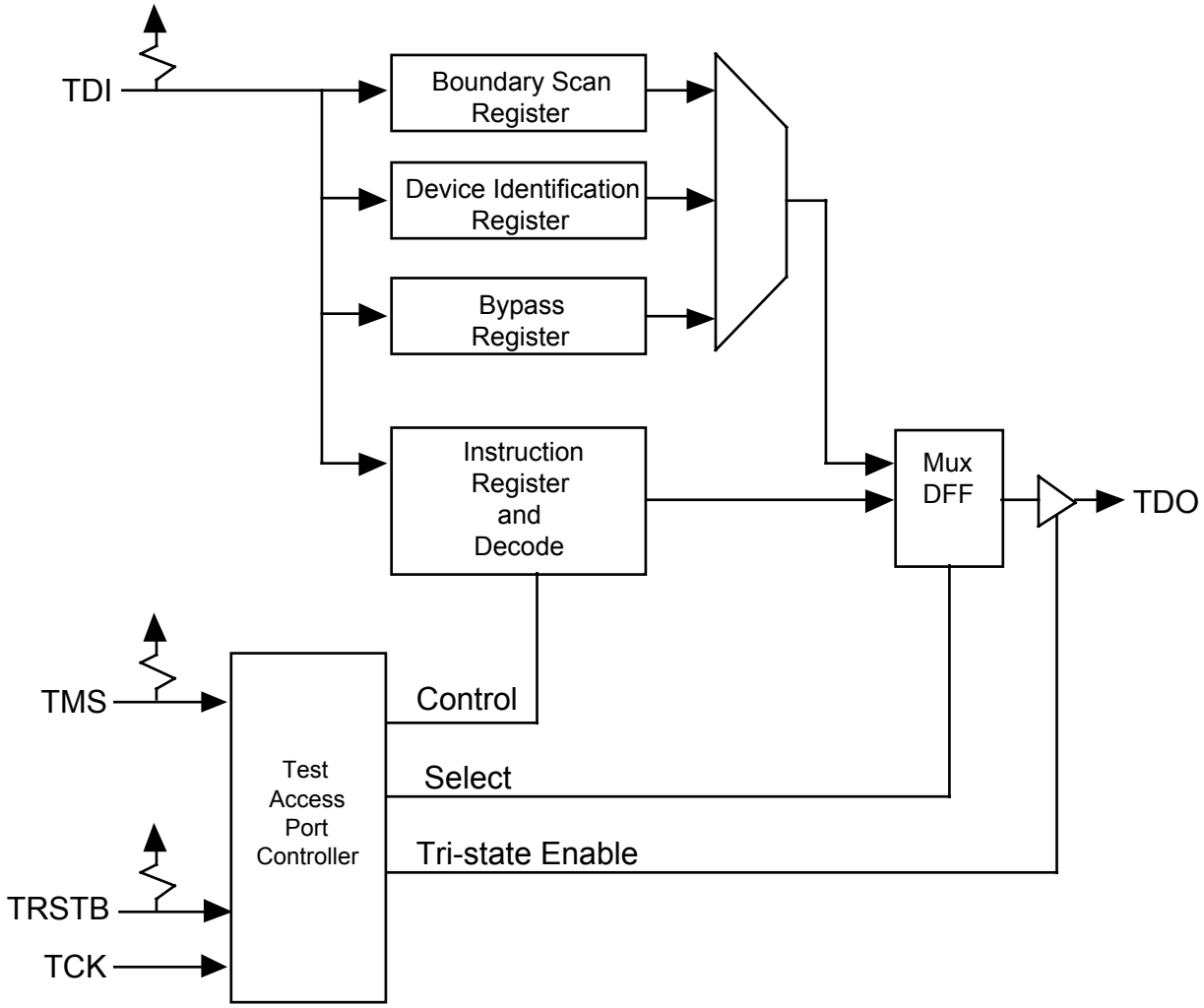
Figure 26 - Single Ended Driving Differential RRCLK+/- or TRCLK+/- Inputs



12.8 JTAG Support

The SPECTRA-155 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 27 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

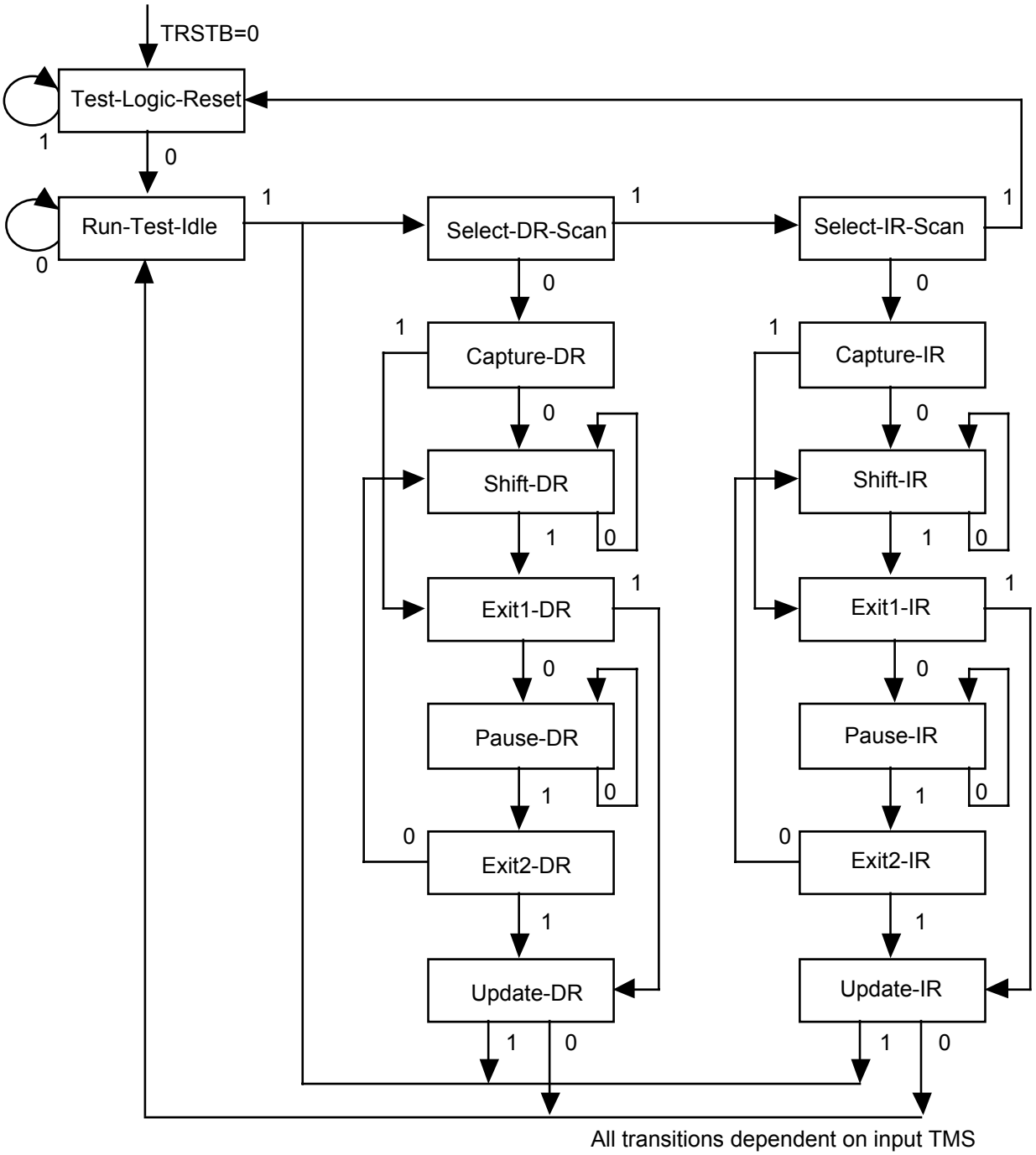
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 28 - TAP Controller Finite State Machine



Test-Logic-Reset The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is

entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle — The run test/idle state is used to execute tests.

Capture-DR — The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR — The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR — The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR — The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR — The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR — The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS — The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST — The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE — The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE — The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST — The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out on output, TDO using the Shift-DR state.

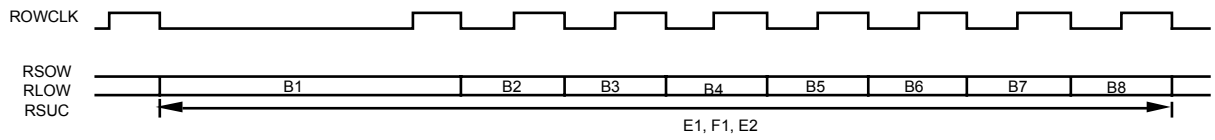
INTEST — The internal test instruction is used to exercise the device's internal core logic. When this instruction is the current

instruction, the boundary scan register is connected between TDI and TDO. During the Update-DR state, patterns shifted in on input, TDI are used to drive primary inputs. During the Capture-DR state, primary outputs are sampled and loaded into the boundary scan register.

13 FUNCTIONAL TIMING

13.1 Transport Overhead Extraction and Insertion

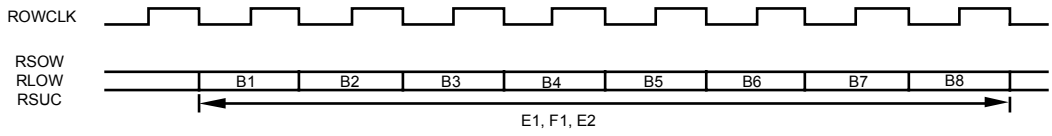
Figure 29 - Receive Overhead Clock and Data Alignment (R64SEL=0)



The receive overhead clock and data alignment timing diagram above shows the relationship between the RSOW, RSUC and RLOW serial data outputs and their associated clock ROWCLK. When register bit R64SEL is set low, ROWCLK is a 72 KHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. The E1, F1 and E2 bytes are shifted out on RSOW, RSUC and RLOW respectively. Output data is updated on the falling edge of ROWCLK.

Bit 1 can be identified using the RFP output. RFP pulses high approximately 650 ns after the falling edge of ROWCLK which updates bit 1.

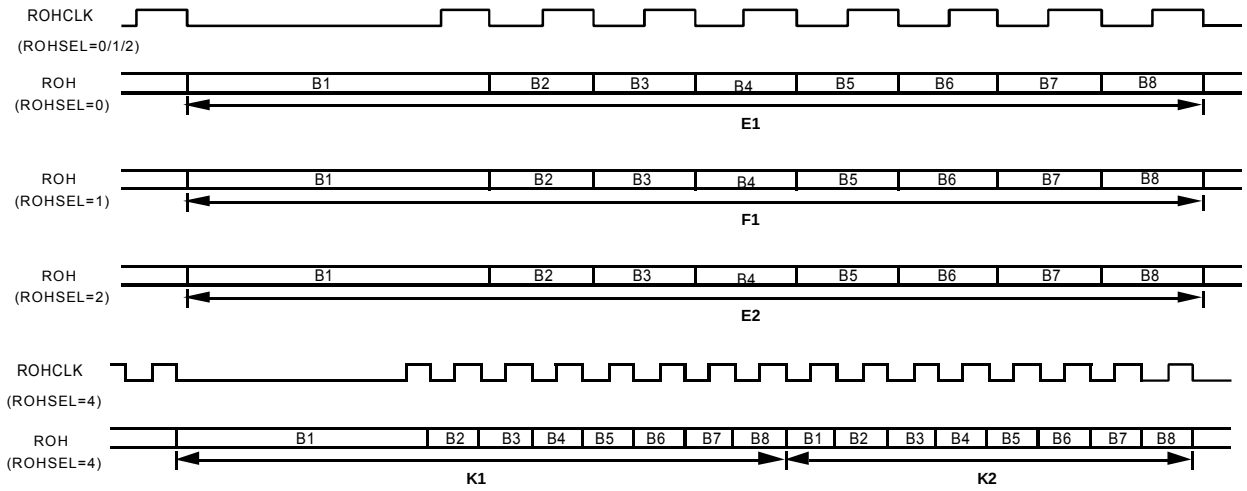
Figure 30 - Receive Overhead Clock and Data Alignment (R64SEL=1)



The receive overhead clock and data alignment timing diagram above shows the relationship between the RSOW, RSUC, RLOW and ROWCLK. When register bit R64SEL is set high, ROWCLK is a 64 KHz 50% duty cycle clock. The E1, F1 and E2 bytes are shifted out on RSOW, RSUC and RLOW respectively. Output data is updated on the falling edge of ROWCLK.

Bit 1 can be identified using the RFP output. RFP pulses high aligned with the falling edge of ROWCLK which updates bit 1.

Figure 31 - Receive Selectable Overhead Clock and Data Alignment (R64SEL=0)



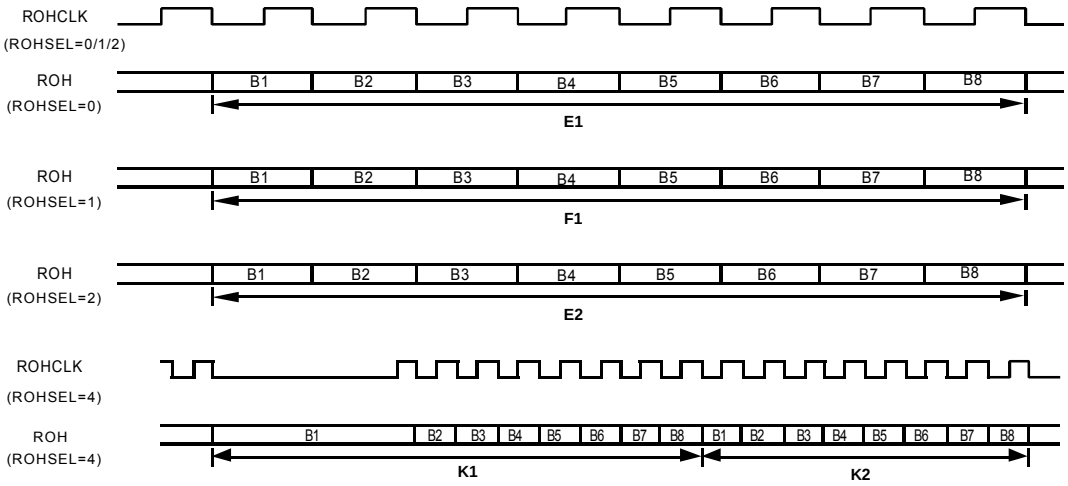
The receive selectable overhead clock and data alignment timing diagram above shows the relationship between the ROH serial data output and its associated clock ROHCLK when register bit R64SEL is set low.

For ROHSEL={0,1,2}, ROHCLK will be a 72 KHz 50% duty cycle clock that is gapped to produce a 64 KHz nominal rate and is aligned as shown in the timing diagram. The E1, F1 and E2 bytes may be shifted out on the ROH as selected by ROHSEL.

For ROHSEL={4}, ROHCLK will be a 144 KHz clock gapped to produce a 128 KHz nominal rate. The K1 and K2 bytes are shifted out on the ROH in the order as illustrated. Output data is updated on the falling edge of ROHCLK.

Bit 1 can be identified using the RFP output. RFP pulses high approximately 650 ns after the falling edge of ROHCLK which updates bit 1 when ROHSEL=0,1,2,4.

Figure 32 - Receive Selectable Overhead Clock and Data Alignment (R64SEL=1)



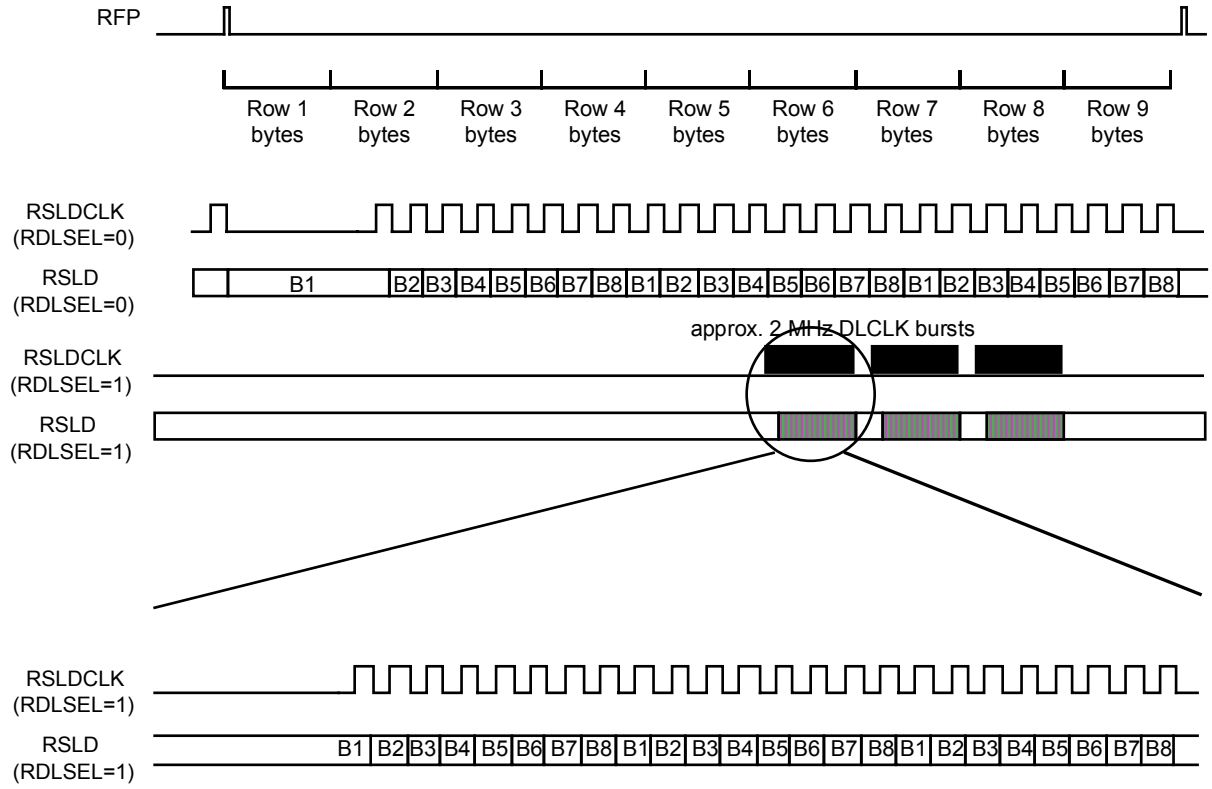
The receive selectable overhead clock and data alignment timing diagram above shows the relationship between the ROH serial data output and its associated clock ROHCLK when register bit R64SEL is set high.

For ROHSEL={0,1,2}, ROHCLK will be a 64 KHz 50% duty cycle clock and is aligned as shown in the timing diagram. The E1, F1 and E2 bytes may be selectively shifted out on the ROH.

For ROHSEL={4}, the ROHCLK will be a 144 KHz 50% duty cycle clock gapped to produce a 128 KHz nominal rate. The K1 and K2 bytes are shifted out on the ROH in the order as illustrated. Output data is updated on the falling edge of ROHCLK.

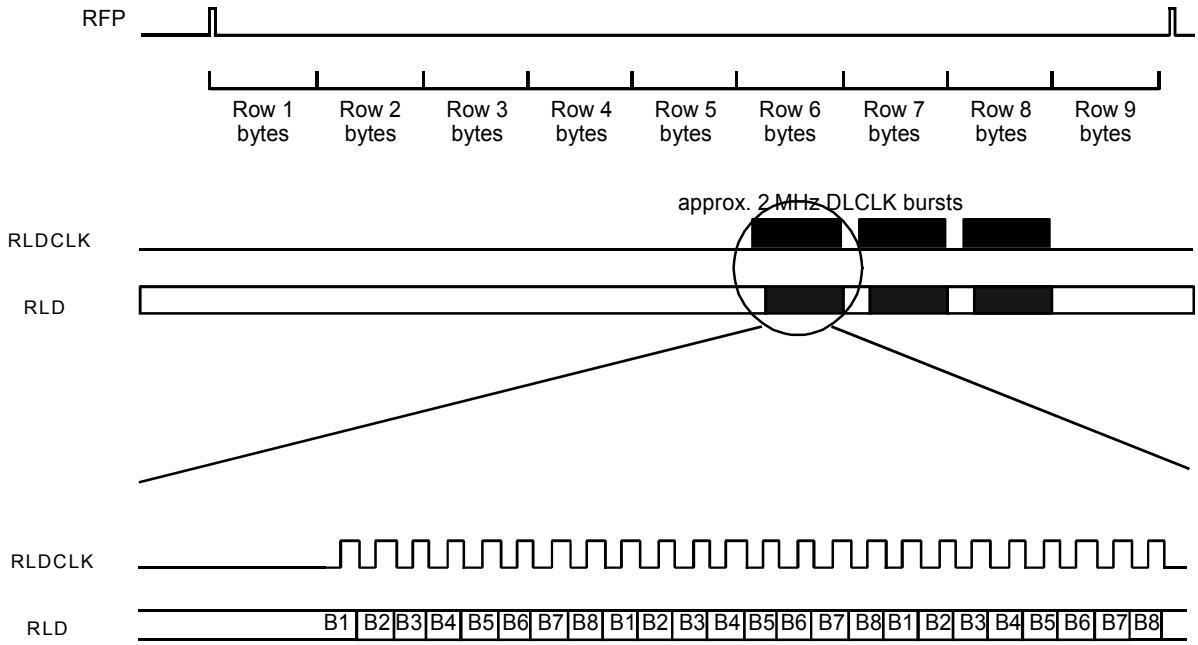
Bit 1 can be identified using the RFP output. RFP pulses high aligned with the falling edge of ROHCLK which updates bit 1 when ROHSEL=0,1,2. When ROHSEL=4, RFP pulses high approximately 650 ns after the falling edge of ROHCLK.

Figure 33 - Receive Section/Line DCC Clock and Data Alignment



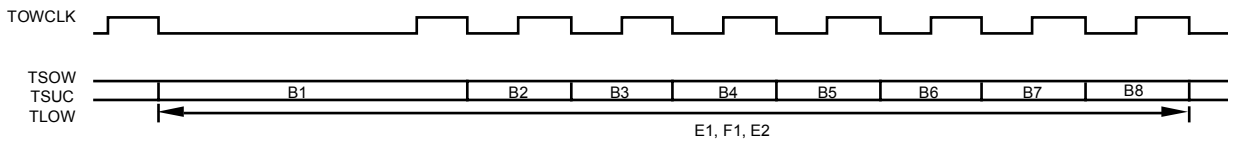
The receive section/line DCC clock and data alignment timing diagram above shows the relationship between the RSLD serial data output and its associated clock, RSLDCLK. When register bit RDLSEL is low, the RSLDCLK is a 216 KHz, 50% duty cycle clock gapped to produce a 192 KHz nominal rate and is aligned with RFP as shown in the timing diagram. The section DCC, D1-D3, bytes are shifted out on the RSLD output. When register bit RDLSEL is high, the RSLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock gapped to produce a 576 KHz nominal rate and is aligned with RFP as shown in the timing diagram. The line DCC, D4-D12, bytes are shifted out on the RSLD output. RSLD is updated on the falling RSLDCLK edge.

Figure 34 - Receive Line DCC Clock and Data Alignment



The receive line DCC clock and data alignment timing diagram above shows the relationship between the RLD serial data output and its associated clock, RLDCLK. The line DCC, D4-D12, bytes are shifted out on the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock. RLD is updated on the falling RLDCLK edge.

Figure 35 - Transmit Overhead Clock and Data Alignment (T64SEL=0)

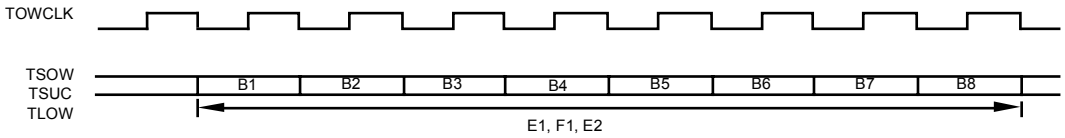


The transmit overhead clock and data alignment timing diagram above shows the relationship between the TSOW, TSUC and TLOW serial data inputs and their associated clock, TOWCLK. When register bit R64SEL is set low, TOWCLK is a 72 KHz 50% duty cycle clock that is gapped to produce a 64 KHz nominal rate. The E1, F1 and E2 bytes are shifted in on TSOW, TSUC and TLOW respectively. Input data is sampled on the rising edge of TOWCLK.

External sourcing of E1, F1 and E2 via the TSOW, TSUC and TLOW can be overridden using the TOHSEL register bit.

Bit 1 can be identified using the TFP output. TFP pulses high approximately 650 ns after the falling edge of TOWCLK which updates bit 1.

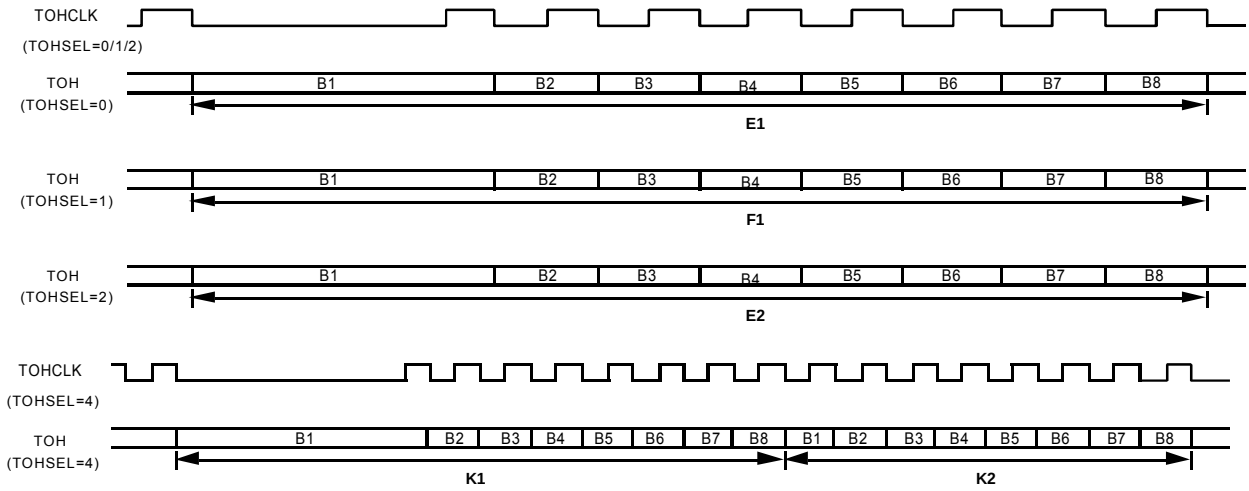
Figure 36 - Transmit Overhead Clock and Data Alignment (T64SEL=1)



The transmit overhead clock and data alignment timing diagram above shows the relationship between the TSOW, TSUC, TLOW and TOWCLK. When register bit T64SEL is set high, TOWCLK is a 64 KHz 50% duty cycle clock. The E1, F1 and E2 bytes are shifted in on TSOW, TSUC and TLOW respectively. Input data is sampled on the rising edge of TOWCLK.

Bit 1 can be identified using the TFP output. TFP pulses high aligned to the falling edge of TOWCLK which updates bit 1.

Figure 37 - Transmit Selectable Overhead Clock and Data Alignment (T64SEL=0)



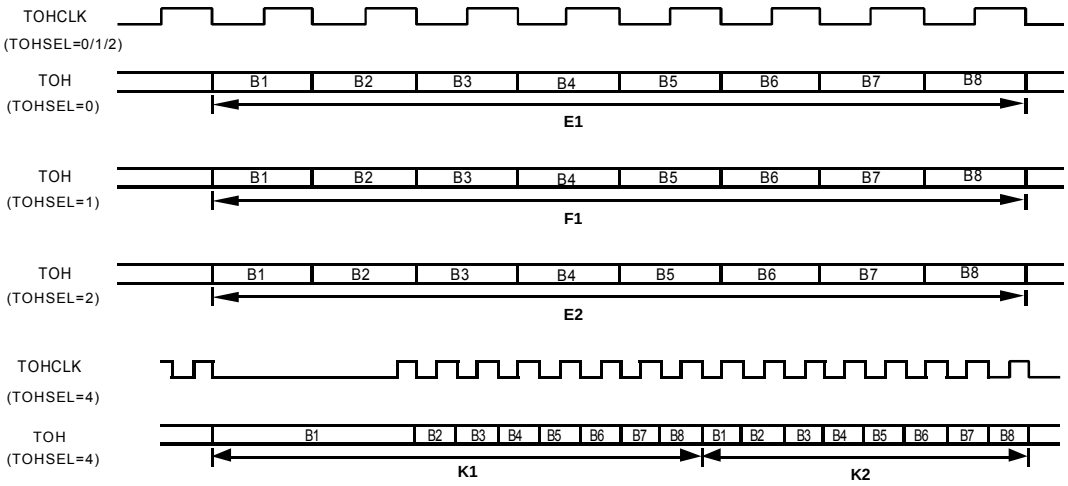
The transmit overhead clock and data alignment timing diagram above shows the relationship between the TOH serial data input and its associated clock, TOHCLK when T64SEL is set low. The T64SEL and TOHSEL settings determine the characteristic of TOHCLK and the interpretation of the input data.

For TOHSEL={0,1,2}, TOHCLK is a 72 KHz 50% duty cycle clock that is gapped to produce a 64 KHz nominal rate. The input data shifted in on the TOH is interpreted as the E1, F1 or E2 bytes according to the TOHSEL setting. In addition, the corresponding stream on the TSOW, TSUC or TLOW input is ignored.

For TOHSEL={4}, TOHCLK will be a 144 KHz 50% duty cycle clock that is gapped to produce a 128 KHz nominal rate. The input data shifted in on the TOH is interpreted as the K1 and K2 bytes in the order as illustrated.

Bit 1 can be identified using the TFP output. TFP pulses high approximately 650 ns after the falling edge of TOHCLK which updates bit 1 when TOHSEL=0,1,2,4

Figure 38 - Transmit Selectable Overhead Clock and Data Alignment (T64SEL=1)



The transmit overhead clock and data alignment timing diagram above shows the relationship between the TOH serial data input and its associated clock, TOHCLK when register bit T64SEL is set high.

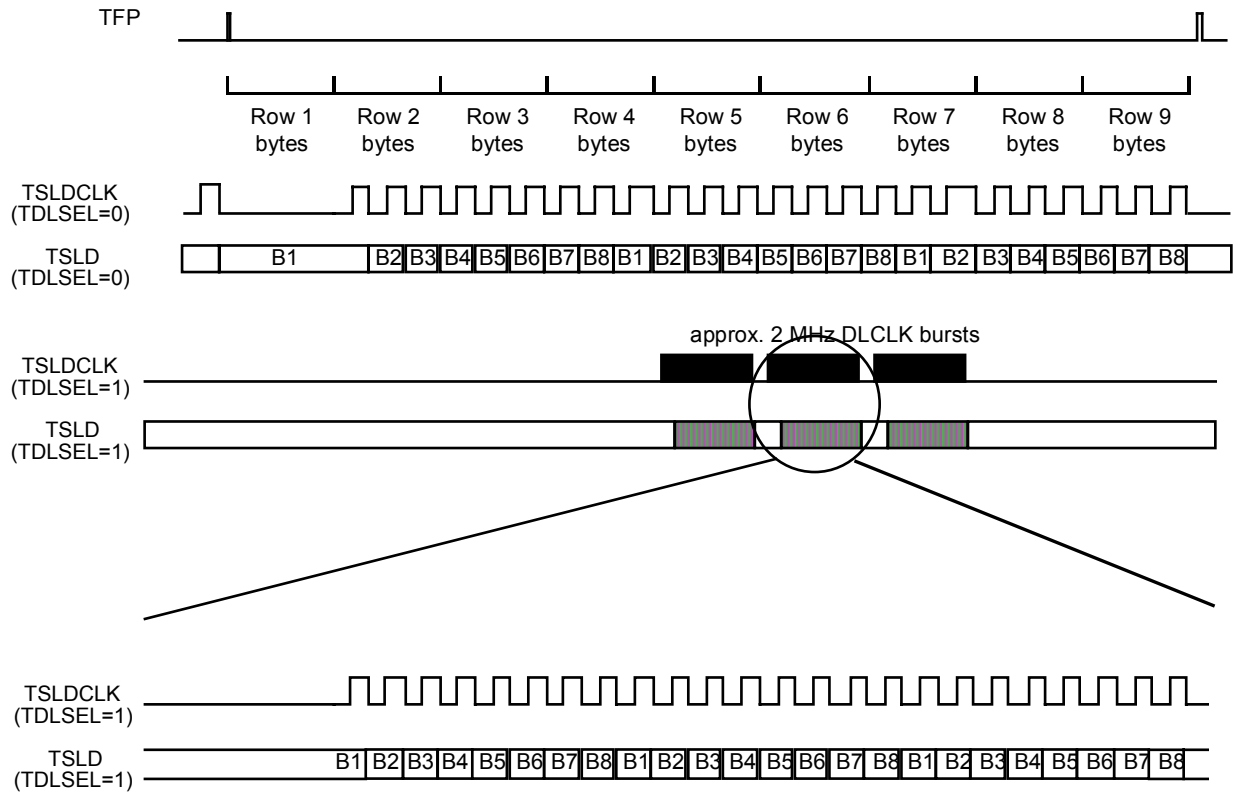
For TOHSEL={0,1,2}, TOHCLK will be a 64 KHz 50% duty cycle clock. In addition, the corresponding stream on the TSOW, TSUC or TLOW input is ignored.

For TOHSEL={4}, TOHCLK will be a 144 KHz 50% duty cycle clock that is gapped to produce a 128 KHz nominal rate.

The input data shifted in on the TOH is interpreted as E1, F1, E2 or K1 and K2 bytes according to the TOHSEL setting.

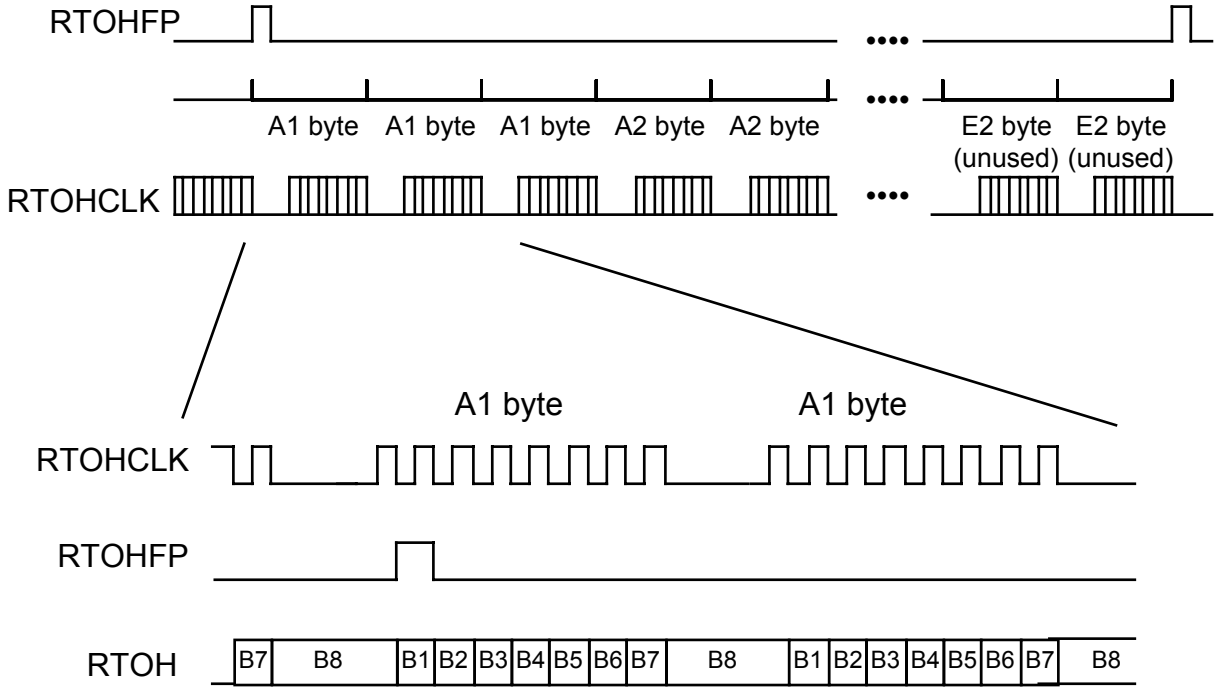
Bit 1 can be identified using the TFP output. TFP pulses high aligned to the falling edge of TOHCLK which updates bit 1 when TOHSEL=0,1,2. When TOHSEL=4, TFP pulses high approximately 650 ns after the falling edge of TOHCLK.

Figure 39 - Transmit Data Link Clock and Data Alignment



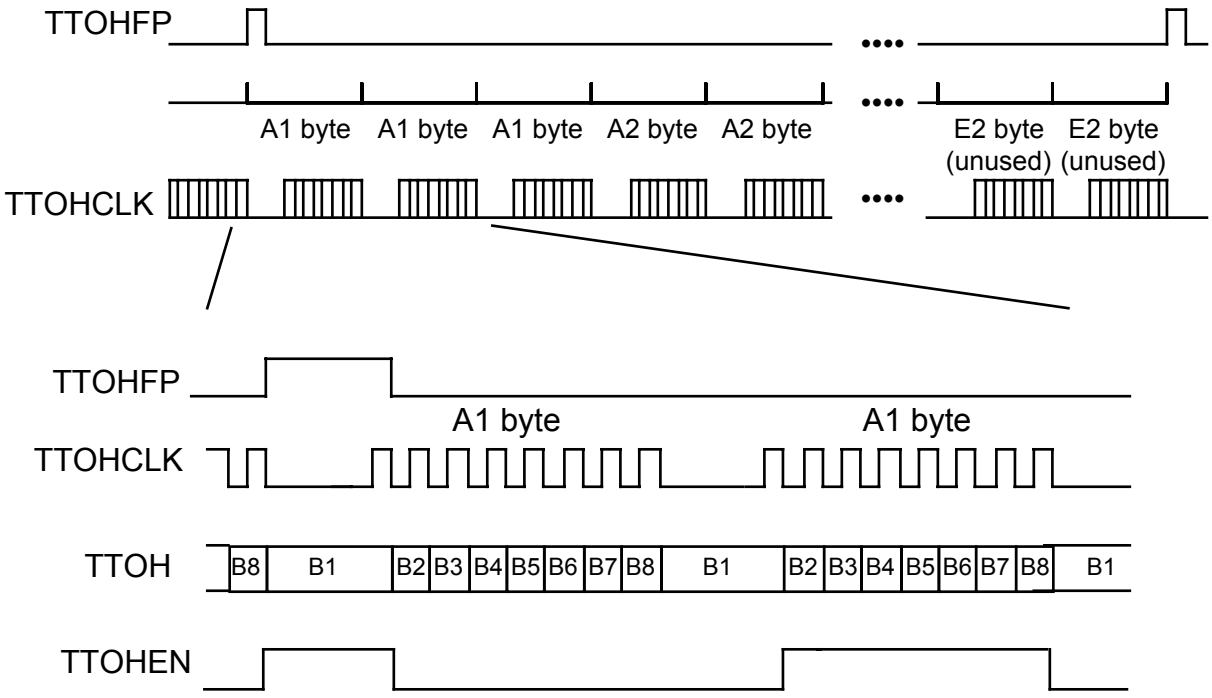
The transmit data link clock and data alignment timing diagram above shows the relationship between the TSLD serial data input and its associated clock, TSLDCLK. When register bit TDLSEL is set low, TSLDCLK is a 216 KHz, 50% duty cycle clock gapped to produce a 192 KHz nominal rate that is aligned with TFP as shown in the timing diagram. The section DCC bytes, D1-D3 are sourced from the TSLD input. When register bit TDLSEL is set high, TSLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock gapped to produce a 576 KHz nominal rate that is aligned with TFP as shown in the timing diagram. The line DCC bytes, D4-D12 are sourced from the TSLD input. All input data on TSLD is sampled on the rising edge of TSLDCLK.

Figure 40 - Transport Overhead Extraction (STS-3/3c)



The transport overhead extraction timing diagram above illustrates the transport overhead extraction interface for STS-3/3c (STM-1/AU3/AU4). The transport overhead extraction clock, RTOHCLK is nominally a 5.184 MHz clock (1.728 MHz for an STS-1 (STM-0/AU3) stream), and is derived from the receive line clock, RCLK. The entire transport overhead (the complete 9 row by 9 column structure) is extracted for the STS-3/3c (STM-1/AU3/AU4) stream and is serialized on RTOH over a frame period (125 µs). For STS-1 (STM-0/AU3), the transport overhead structure of 9 rows by 3 columns is serialized in a similar way on RTOH over a frame period (125 µs).

Figure 41 - Transport Overhead Insertion (STS-3/3c)

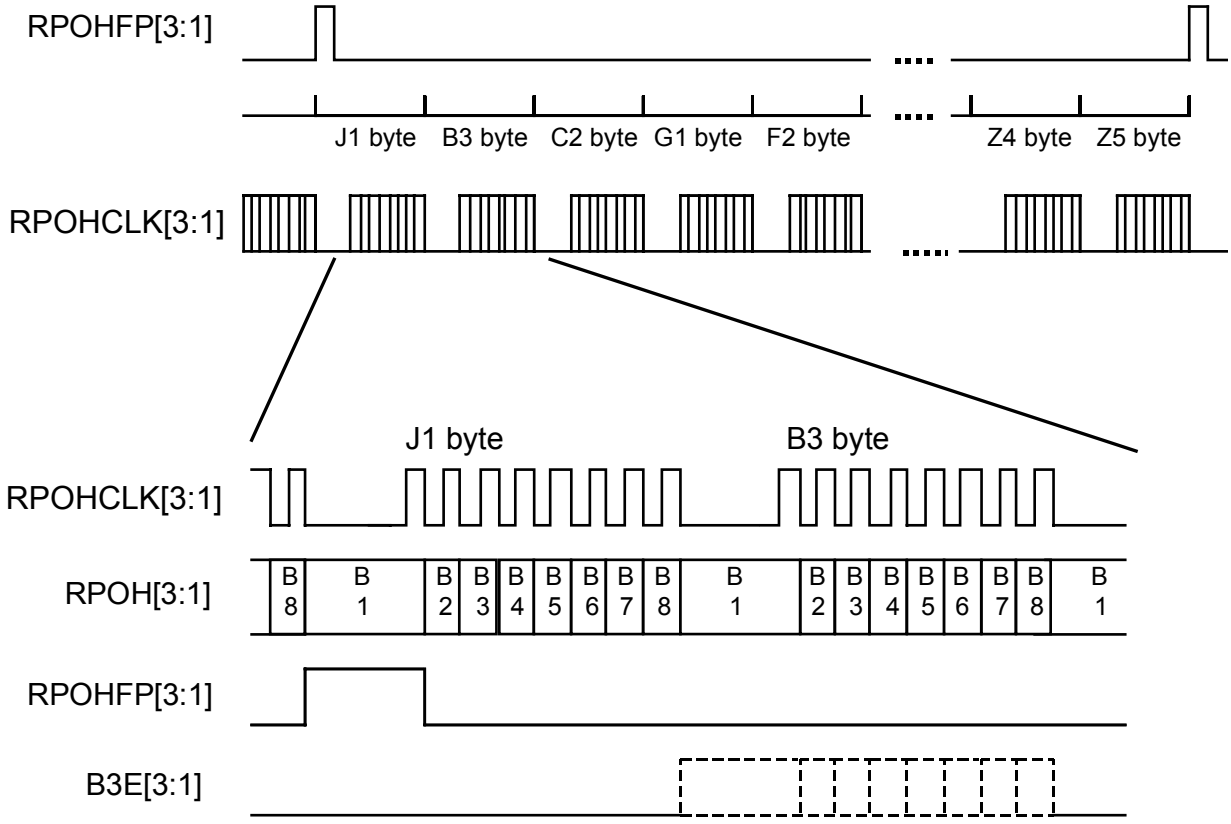


The transport overhead insertion timing diagram above illustrates the transport overhead insertion interface. Output TTOHCLK is nominally a 5.184 MHz clock (1.728 MHz for an STS-1 (STM-0/AU3) stream), and is used to update output TTOHFP, and to sample input TTOH and TTOHEN. The value sampled on TTOHEN during the first overhead bit position of a given overhead byte determines whether the byte sampled on TTOH is inserted in the STS-3/3c (STM-1/AU3/AU4) stream. TTOHEN is held high during the bit 1 position of the first A1 byte in the TTOH stream. The eight bit values sampled on input TTOH during the first A1 byte period are inserted in the first A1 byte position in the STS-3/3c (STM-1/AU3/AU4) stream. Similarly, TTOHEN is held low during the bit 1 position of the second A1 byte. The default value (F6H) is inserted in the second A1 byte position in the STS-3/3c (STM-1/AU3/AU4) stream ignoring the contents of TTOH

An error insertion feature is also provided for the B1, and B2 byte positions. When TTOH is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the STS-3/3c (STM-1/AU3/AU4) stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

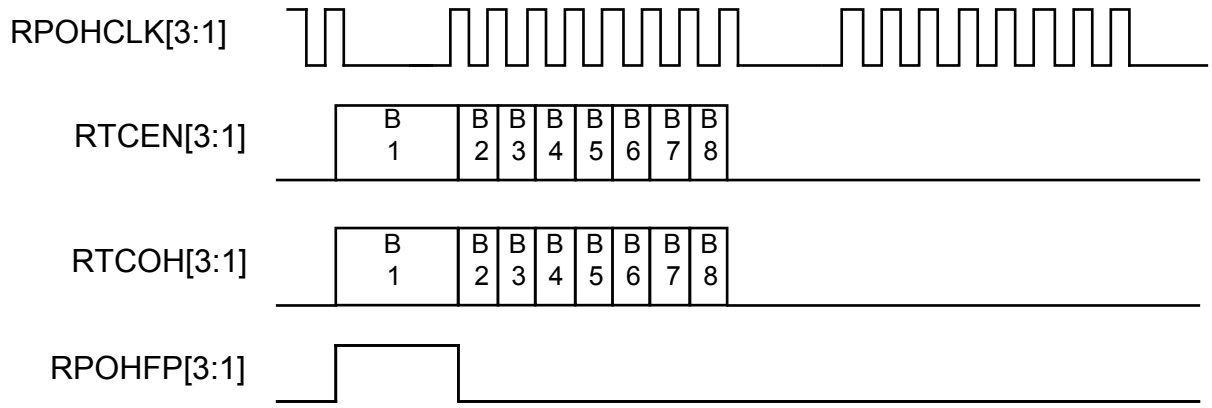
13.2 Path Overhead Extraction and Insertion

Figure 42 - Receive Path Overhead Extraction Timing



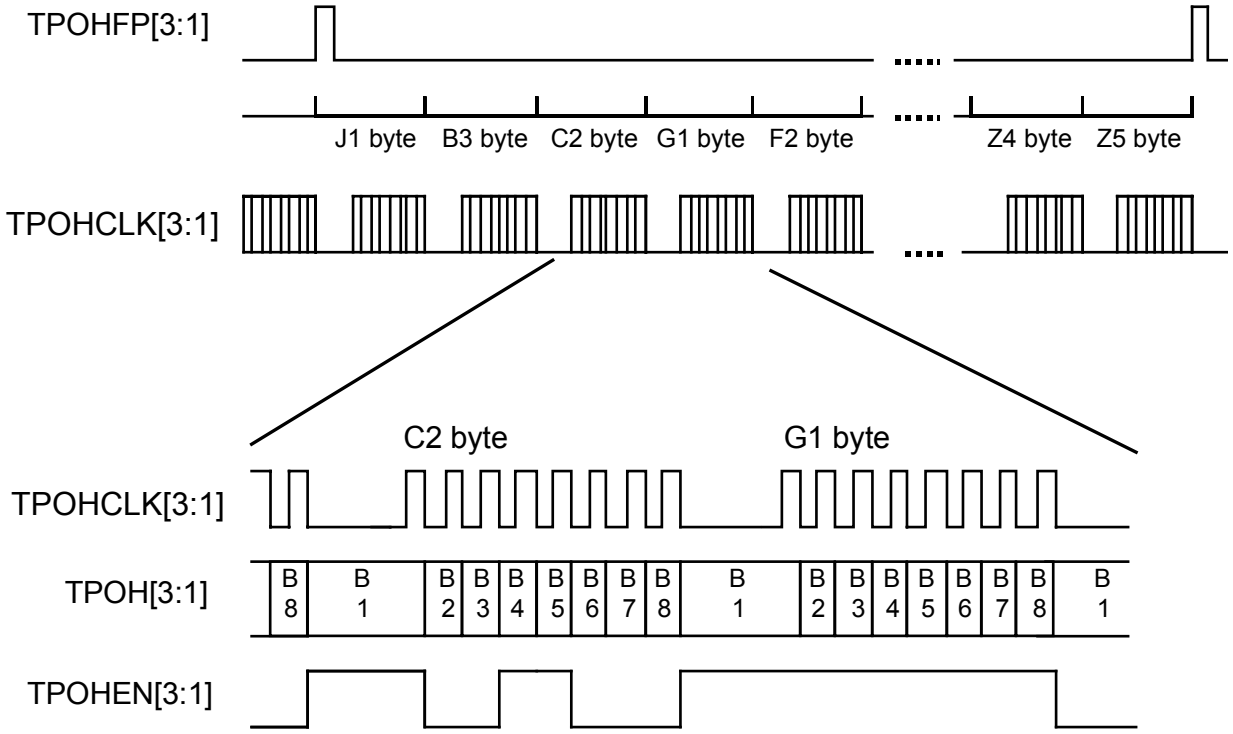
The figure above shows the receive path overhead extraction to a low speed serial stream. RPOHCLK[3:1] are nominally 576 KHz clocks. The entire path overhead (J1, B3, C2, G1, F2, H4, Z3, Z4, Z5 bytes) is extracted, serialized and placed on RPOH[3:1] over a frame period. For each byte, the most significant bit is transmitted first. RPOHFP[3:1] mark the most significant bit of the J1 byte. B3E[3:1] identify the bits within the B3 bytes containing a parity error. The index in the signal names refer to the STS-1 (STM-0/AU3) stream number within the receive STS-3 (STM-1/AU3) stream. I.e., signals carrying an index of 1 reflect the status of STS-1 (STM-0/AU3) #1, those with index of 2 reflect STS-1 (STM-0/AU3) #2, and those with index of 3 reflect STS-1 (STM-0/AU3) #3. In STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, only RPOHCLK[1], RPOH[1], RPOHFP[1] and B3E[1] are active. The remaining outputs are set low.

Figure 43 - Receive Tandem Connect Maintenance Insertion Timing



The figure above illustrates the Receive Tandem Connection Maintenance Insertion interface. RTCOH[3:1] carries the data to be inserted in the tandem connection maintenance byte (Z5) in the DROP bus. RTCOH[1] and RTCEN[1] are associated with STS-1 (STM-0/AU3) #1, RTCOH[2] and RTCEN[2] with STS-1 (STM-0/AU3) #2, and RTCOH[3] and RTCEN[3] with STS-1 (STM-0/AU3) #3. The first bit on RTCOH (B1) corresponds to the most significant bit of Z5. The RTCEN[3:1] signal controls whether the corresponding bit in RTCOH[3:1] is inserted in the Z5 byte. The data bit on RTCOH[3:1] is inserted in the Z5 byte if the corresponding bit of RTCEN[3:1] is high. The incoming error count or a logic one data link bit is placed on the Z5 byte if the corresponding bit in RTCEN[3:1] is low.

Figure 44 - Transmit Path Overhead Insertion Timing

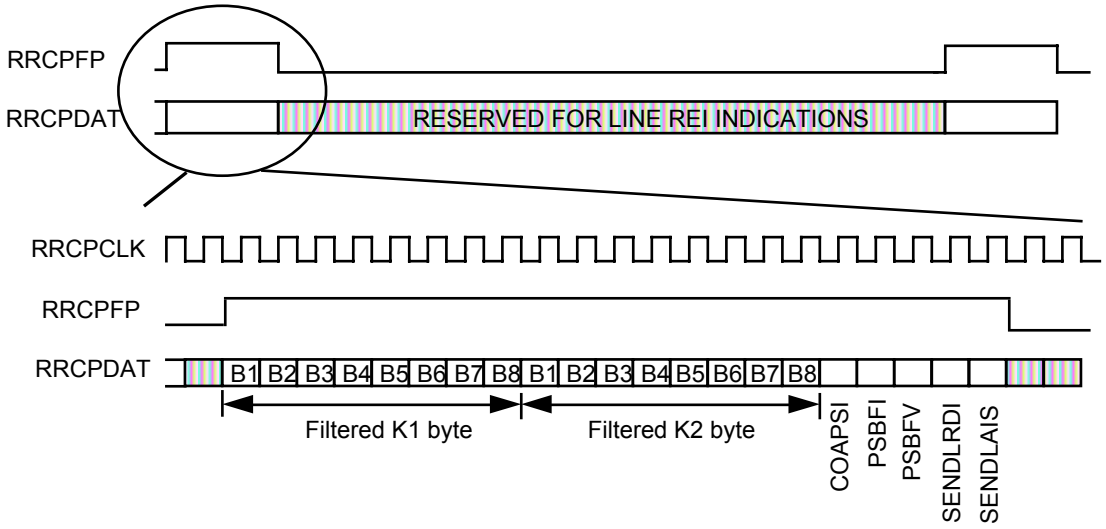


The figure above shows the transmit path overhead insertion from a low speed serial stream. TPOHCLK[3:1] are nominally 576 KHz clocks. The entire path overhead, except B3 and H4, (J1, C2, G1, F2, Z3, Z4, Z5 bytes) can be inserted into the transmit stream via TPOH[3:1] over a frame period. In each byte, the most significant bit is transmitted first. TPOHFP[3:1] mark the most significant bit of the J1 byte. TPOHEN[3:1] control the insertion of data on TPOH[3:1] on a bit-by-bit basis. The data on TPOH is inserted in the path overhead of the transmit stream if TPOHEN is set high at the corresponding bit position. TPOHEN is set high during bits 1, 4 and 5 of the C2 byte and the entire G1 byte. For this sample configuration, the G1 byte and bits 1, 4 and 5 of the C2 byte will be taken from TPOH while the remaining bits (2, 3, 6, 7 and 8) retain their default values. The index in the signal names refer to the STS-1 (STM-0/AU3) stream number within the receive STS-3 (STM-1/AU3) stream. I.e., signals carrying an index of 1 are associated with STS-1 (STM-0/AU3) #1, those with index of 2 with STS-1 (STM-0/AU3) #2, and those with index of 3 with STS-1 (STM-0/AU3) #3. In STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, only TPOHCLK[1], TPOH[1], TPOHFP[1] and TPOHEN[1] are active. The remaining outputs are set low and inputs are ignored.

An error insertion feature is provided for the B3 or H4 byte. When TPOHEN and TPOH are both set high, the corresponding path BIP bit or tributary multiframe sequence bit will be inverted before insertion in the transmit stream.

13.3 Mate SPECTRA-155 Interfaces

Figure 45 - Receive Ring Control Port



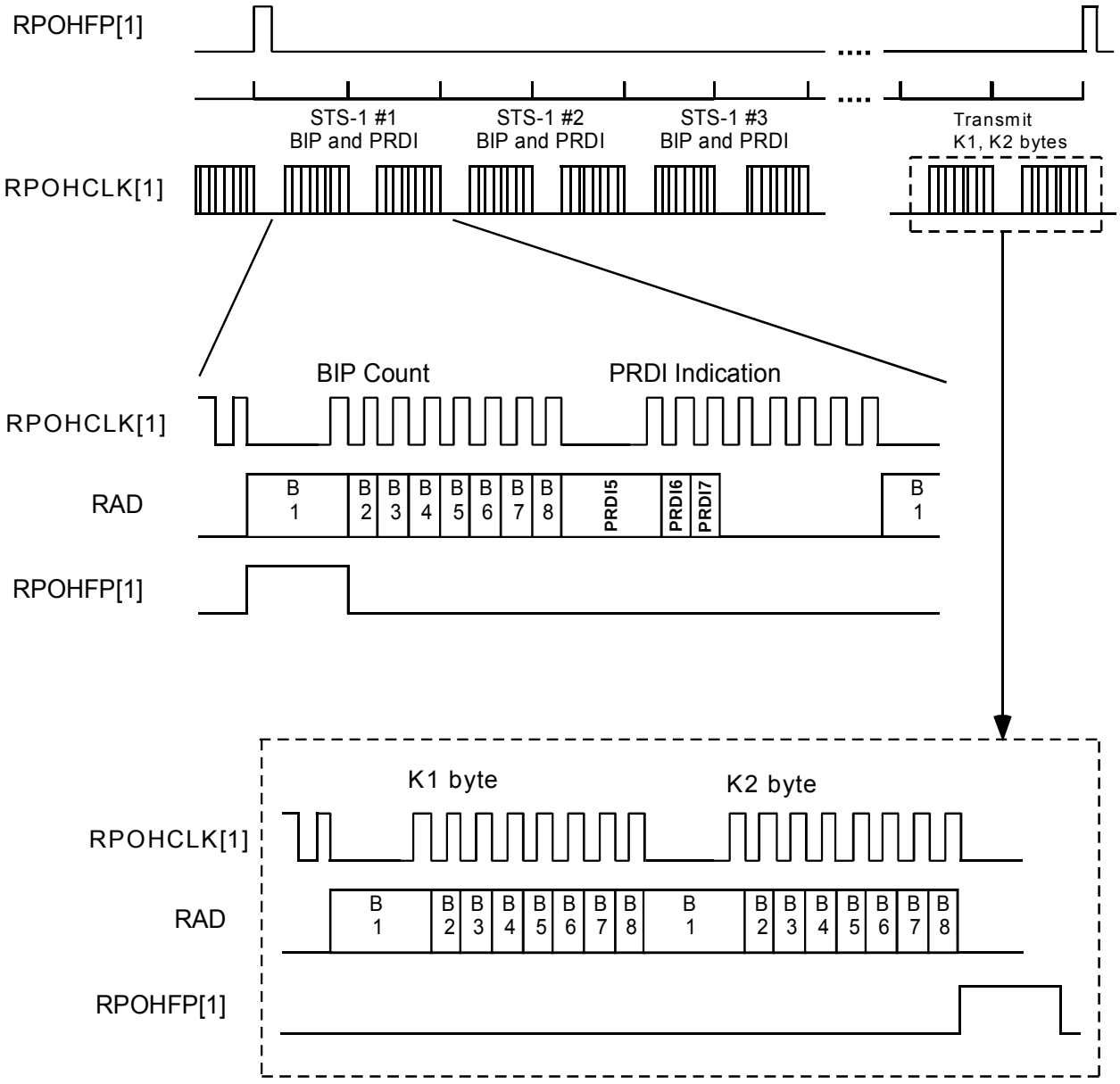
The Receive Ring Control Port timing diagram above illustrates the operation of the receive ring control port when the ring control ports are enabled (using the RCP bit in the Control/Enable Register). The control port timing is provided by the RRCPCLK input. RRCPFP and RRCPDAT are updated on the falling edge of RRCPCLK. RRCPFP is used to distinguish the bit positions carrying alarm status and maintenance signal control information (RRCPFP is high) from the bit positions carrying line REI indications (RRCPFP is low). RRCPFP is high for 21 bit positions once per 125 µs frame. Note, REI indications are enabled using the AUTOREI bit in the SPECTRA-155 Ring Control register.

The first 16 bit positions contain the APS channel byte values after filtering (the K1 and K2 values have been identical for at least three consecutive frames). The 17th bit position, COAPSI, is high for one frame when a new APS channel byte value (after filtering) is received. The 18th and 19th bit positions contain the current protection switch byte failure alarm status. PSBFI is high for one frame when a change in the protection switch byte failure alarm state is detected. PSBFV contains the real-time active high state value of the protection switch byte failure alarm. The 20th and 21st bit positions control the insertion of the line AIS and line RDI maintenance signals in a mate device. The SENDLRDI bit position is controlled by the logical OR of the section/line alarms as enabled by the SPECTRA-155 Line RDI Control register, or by the SRDI bit in the

SPECTRA-155 Ring Control Register. The SENDLAIS bit position is controlled by the SAIS bit in the SPECTRA-155 Ring Control Register.

While RRCPFP is low, RRCPDAT is high for one RRCPCLK cycle for each received REI indication.

Figure 46 - Receive Path Alarm Port Timing



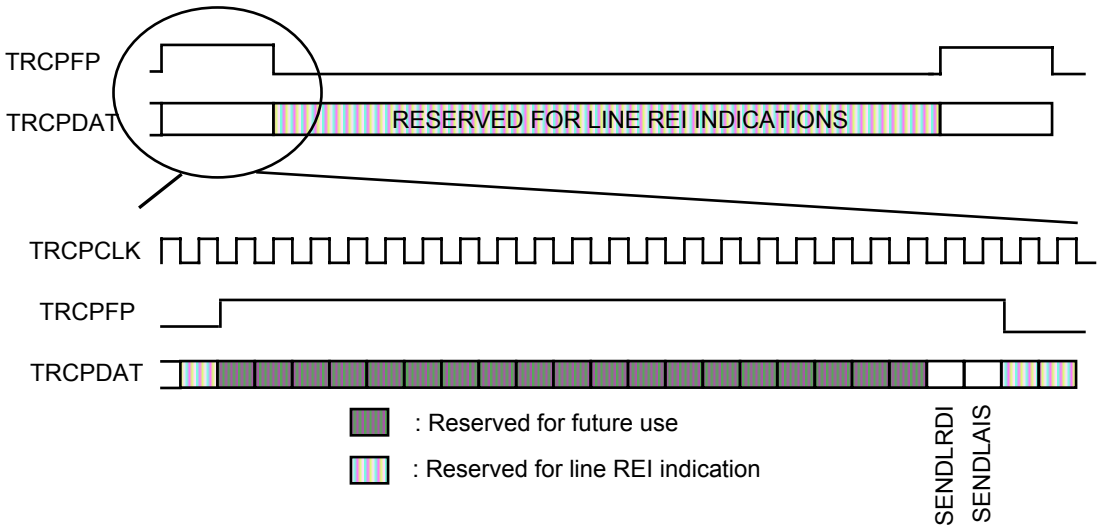
The figure above shows the format of the path receive path alarm port. The path BIP-8 counts from all three STS-1 (STM-0/AU3) streams are serialized in the receive alarm data output (RAD) and clocked out by RPOHCLK[1]. The eight BIP count bit positions for each STS-1 (STM-0/AU3) are left justified. If there are eight BIP errors in the corresponding STS-1 (STM-0/AU3) stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions

corresponding to the number of detected errors are set high, the remainder are set low. The PRDI bits are set when receive alarm conditions are asserted for the corresponding STS-1 (STM-0/AU3) stream. Note, BIP error indications are enabled using the AUTOPREI bit in the SPECTRA-155 Path REI/RDI registers. The PRDI5 indications are enabled using bits in the SPECTRA-155 Path REI/RDI registers. The PRDI6 and PRDI7 bits are enabled using bits in the SPECTRA-155 Enhanced Path RDI Control registers.

The transmit APS channel, K1 and K2, bytes are also serialized on the RAD during the last two byte position in the output bit stream. The transmit K1 and K2 bytes can be sourced from the TTOH input, the TOH input or via the TLOP Transmit K1/K2 registers in order of precedence.

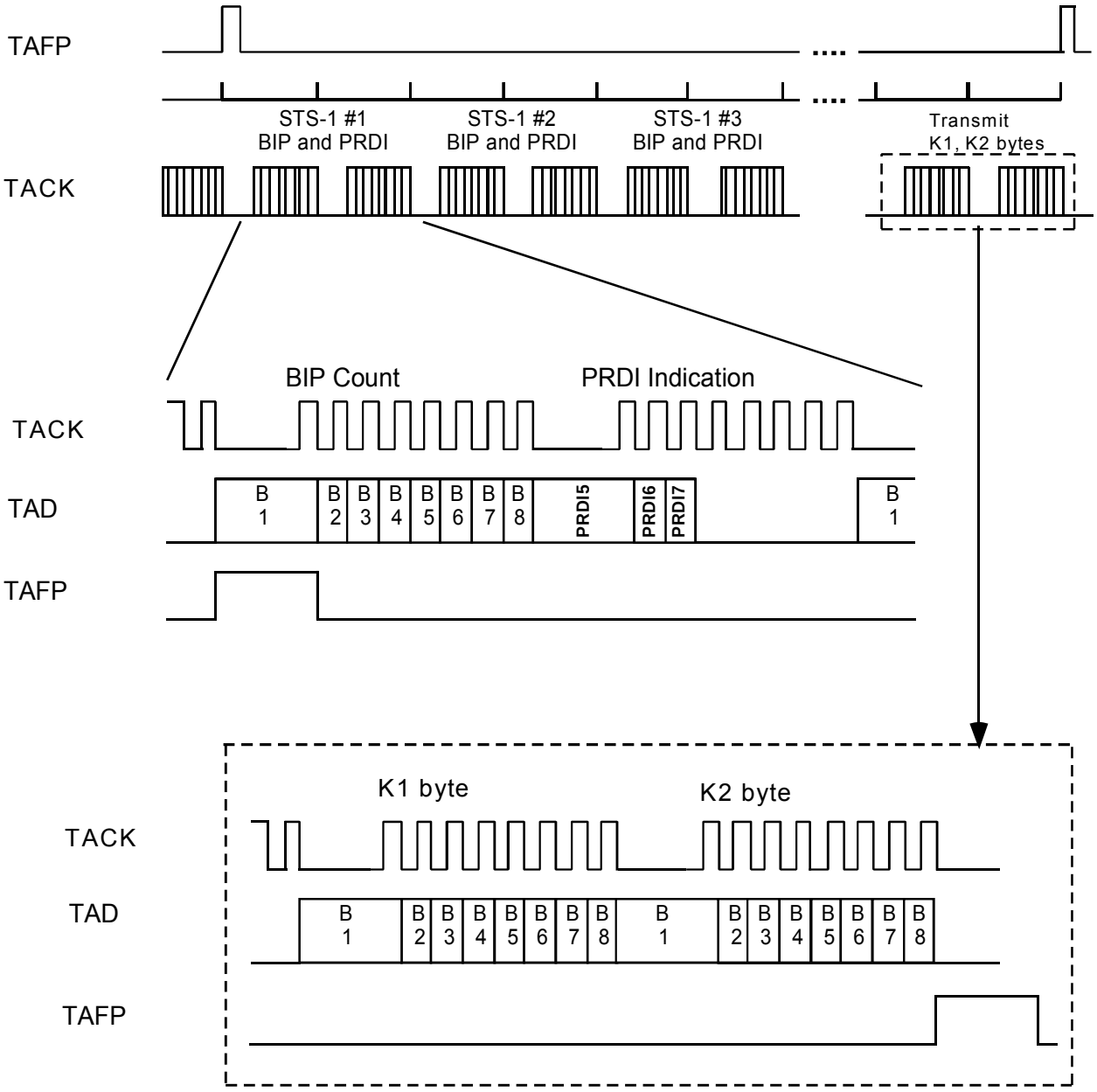
Output data is updated on the falling edge of RPOHCLK[1]. In STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, only the bit positions assigned to STS-1 (STM-0/AU3) #1 are active, those assigned to streams #2, and #3 are set low.

Figure 47 - Transmit Ring Control Port



The Transmit Ring Control Port timing diagram above illustrates the operation of the transmit ring control port when the ring control ports are enabled (using the RCP bit in the Control/Enable Register). The control port timing is provided by the TRCPCLK input. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK. TRCPFP is used to distinguish the bit positions carrying maintenance signal control information (TRCPFP is high) from the bit positions carrying line REI indications (TRCPFP is low). TRCPFP is high for 21 bit positions once per frame 125 µs). Currently, only the last two bit positions are used. These bit positions control the insertion of line RDI and line AIS maintenance signals as illustrated. The remaining 19 bit positions are reserved for future feature enhancements.

Figure 48 - Transmit Alarm Port Timing



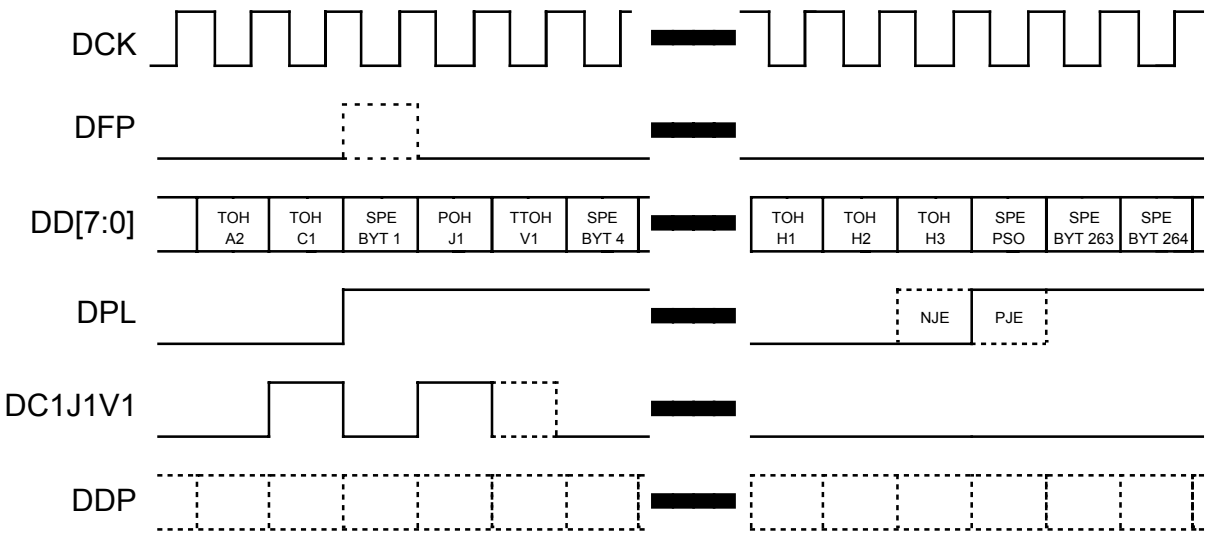
The figure above shows the format of the transmit path alarm port. The path RDI counts from all three STS-1 (STM-0/AU3) streams are serialized in the transmit alarm data input (TAD) and clocked in by TACK. The eight BIP count bit positions for each STS-1 (STM-0/AU3) are left justified. If there are eight BIP errors in the corresponding STS-1 (STM-0/AU3) stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions corresponding to the number of

detected errors are set high, the remainder are set low. The PRDI bits (PRDI5, PRDI6, PRDI7) are set accordingly when the corresponding STS-1 (STM-0/AU3) stream in the peer receive section inserts an RDI condition to be relayed back to the far end. The transmit APS channel, K1 and K2, bytes can also be sourced from TAD stream during the last two byte position in the input bit stream. Input data is sampled on the rising edge of TACK. In STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) mode, only the bit positions assigned to STS-1 (STM-0/AU3) #1 are active, those assigned to streams #2, and #3 are ignored.

13.4 Telecom Bus System Side

13.4.1 DROP Bus

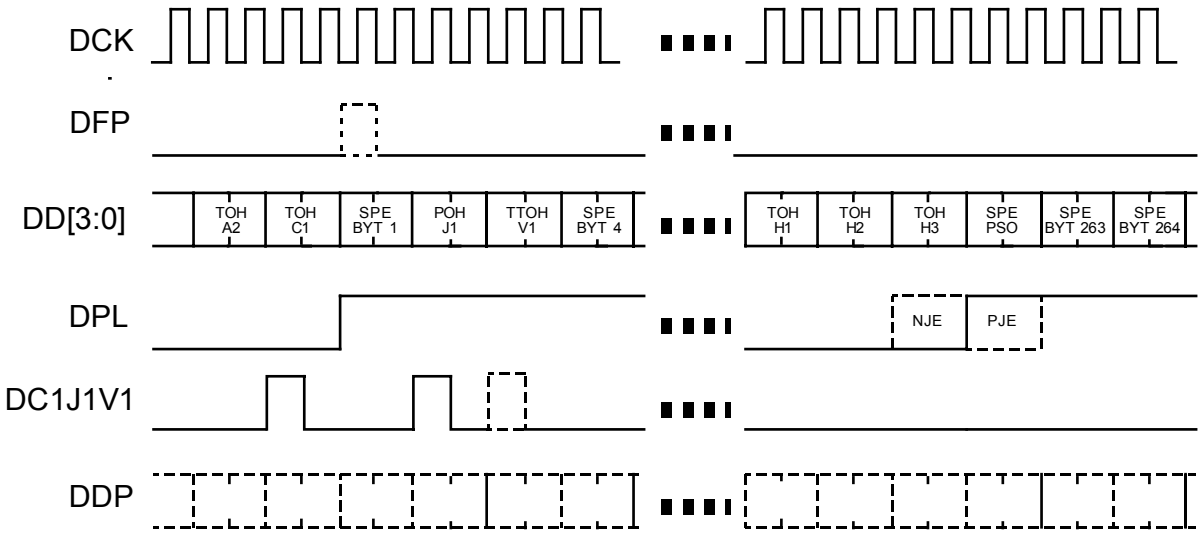
Figure 49 - STS-1 (STM-0/AU3) Byte Mode DROP Bus Timing



The figure above shows the STS-1 (STM-0/AU3) byte mode DROP bus timing. DCK is a 6.48 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte in the STS-1 (STM-0/AU3) frame on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labeled NJE), DPL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labeled PJE), DPL is set low during the PSO byte to indicate that payload data is not available. The DROP bus composite timing signal DC1J1V1 is set high when DPL is set low to mark the C1 byte. DC1J1V1 is set high when DPL is also set high to mark the J1 byte.

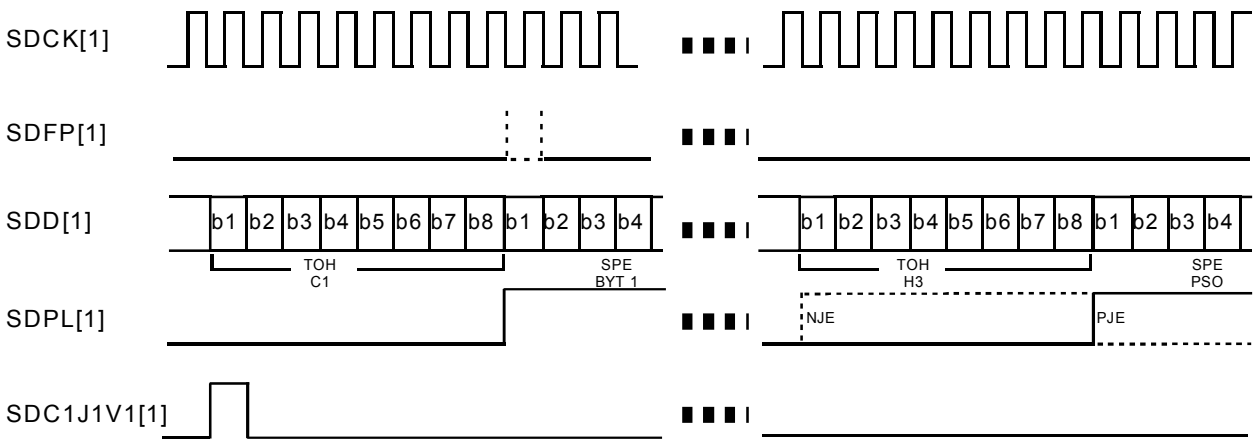
Optionally, DC1J1V1 is set high on the first payload byte after J1 once every multiframe to mark the first frame of the DROP bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP reports the parity of DD[7:0] and optionally includes DPL and DC1J1V1.

Figure 50 - STS-1 (STM-0/AU3) Nibble Mode DROP Bus Timing



The figure above shows the STS-1 (STM-0/AU3) nibble mode DROP bus timing of the same STS-1 (STM-0/AU3) output sequence as the byte mode illustration. DCK is a 12.96 MHz clock. Each byte in an STS-1 (STM-0/AU3) stream , including overhead and payload, is transferred as nibbles with the upper nibble in each byte being driven onto DD[3:0] first. The frame pulse DFP marks the upper nibble of the first synchronous payload envelope byte in an STS-1 (STM-0/AU3) frame. This position is maintained by an internal fly-wheel counter thus DFP need not be asserted on every frame. The DPL signal marks the nibbles of each payload byte. The composite signal DC1J1V1 which marks the C1, J1 and optionally, the V1 byte positions in an STS-1 (STM-0/AU3) stream is asserted when the upper nibbles of these bytes are driven out on DD[3:0]. The DROP bus parity output DDP reports the parity of DD[3:0] and optionally includes DPL and DC1J1V1.

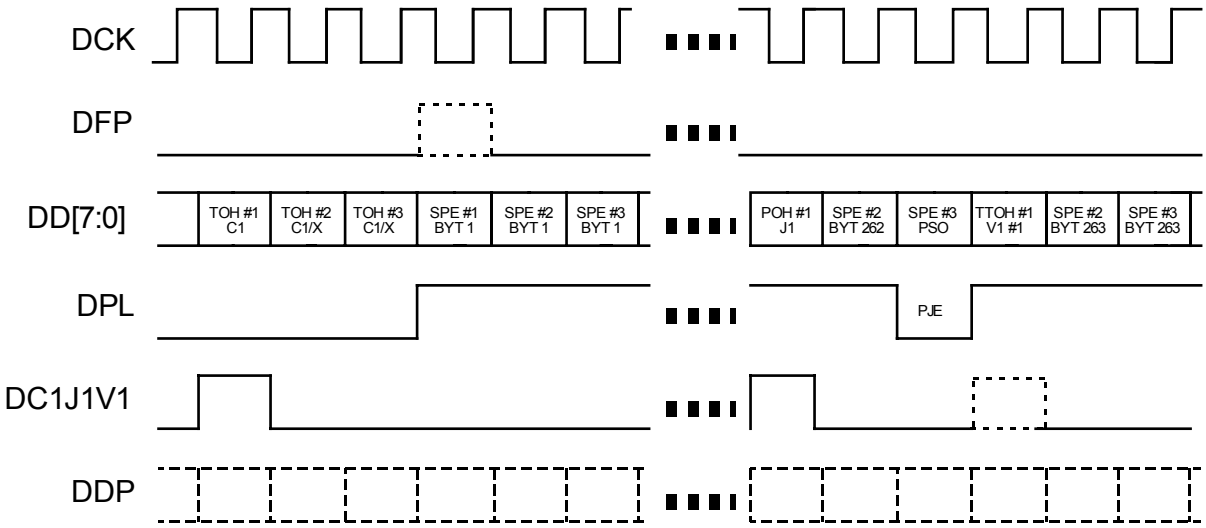
Figure 51 - STS-1/3 (STM-0/AU3, STM-1/AU3) Serial Mode DROP Bus Timing



The figure above shows the STS-1/3 (STM-0/AU3, STM-1/AU3) serial mode DROP bus timing for the same STS-1 (STM-0/AU3) output sequence as the byte mode illustration. SDCK[1] is a 51.84 MHz clock. Each byte in the STS-1 (STM-0/AU3) stream, including overhead and payload, is transferred as a serial stream. The most significant bit b1 in each byte is driven onto SDD[1] first. The frame pulse SDFP[1] marks the b1 position of the first synchronous payload envelope byte in an STS-1 (STM-0/AU3) frame. This position is maintained by an internal fly-wheel counter thus SDFP[1] need not be asserted on every frame. The SDPL[1] signal marks all bits of each payload byte in the serial output stream. It is also asserted during a negative stuff byte (H3) if such an event exists. The SDPL[1] will not be asserted during a positive stuff byte. The composite signal SDC1J1V1[1] which marks the C1, J1 and optionally, the V1 byte positions in an STS-1 (STM-0/AU3) stream is asserted only when the most significant bit b1 of these bytes are driven out on SDD[1].

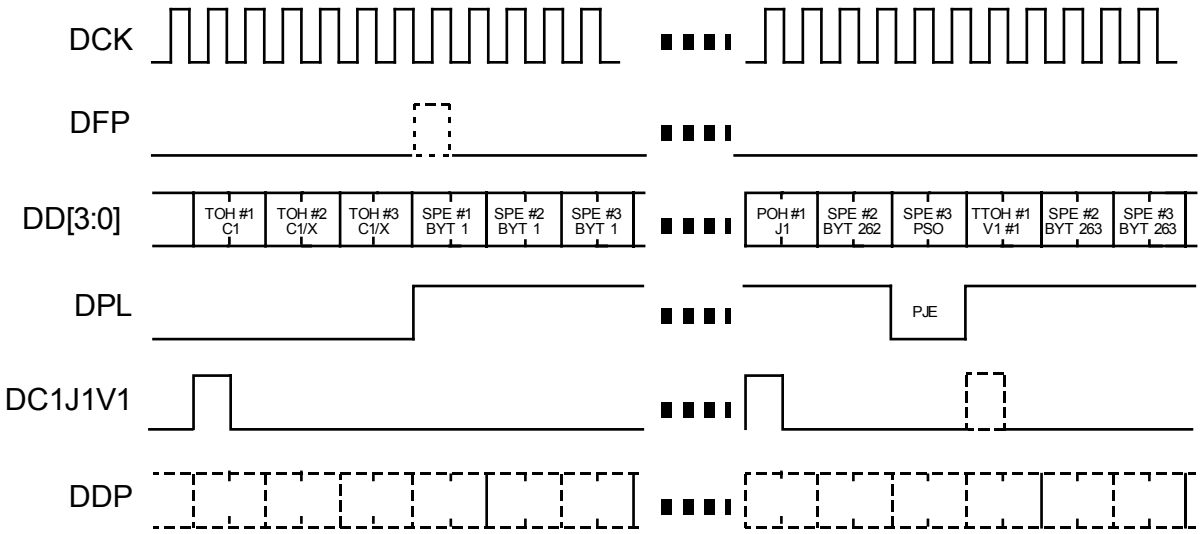
For an STS-3 (STM-1/AU3) stream, the above illustration applies to the serial mode DROP bus timing for its STS-1 (STM-0/AU3) #1 stream. The DROP bus timing for STS-1 (STM-0/AU3) #2 and #3 streams in the STS-3 (STM-1/AU3) stream are similar. The STS-1 (STM-0/AU3) #2 stream is transferred via SDD[2], SDPL[2] and SDC1J1V1[2]. The DROP bus clock is SDCK[2] and the synchronous payload envelopes (SPE) in the STS-1 (STM-0/AU3) #2 stream are aligned by frame pulses asserted on SDFP[2]. The STS-1 (STM-0/AU3) #3 stream is transferred out on the serial DROP bus comprising SDCK[3], SDFP[3], SDD[3], SDPL[3] and SDC1J1V1[3] signals. The three serial DROP buses for the individual STS-1 (STM-0/AU3) streams in an STS-3 (STM-1/AU3) stream operate independently of each other.

Figure 52 - STS-3 (STM-1/AU3) Byte Mode DROP Bus Timing



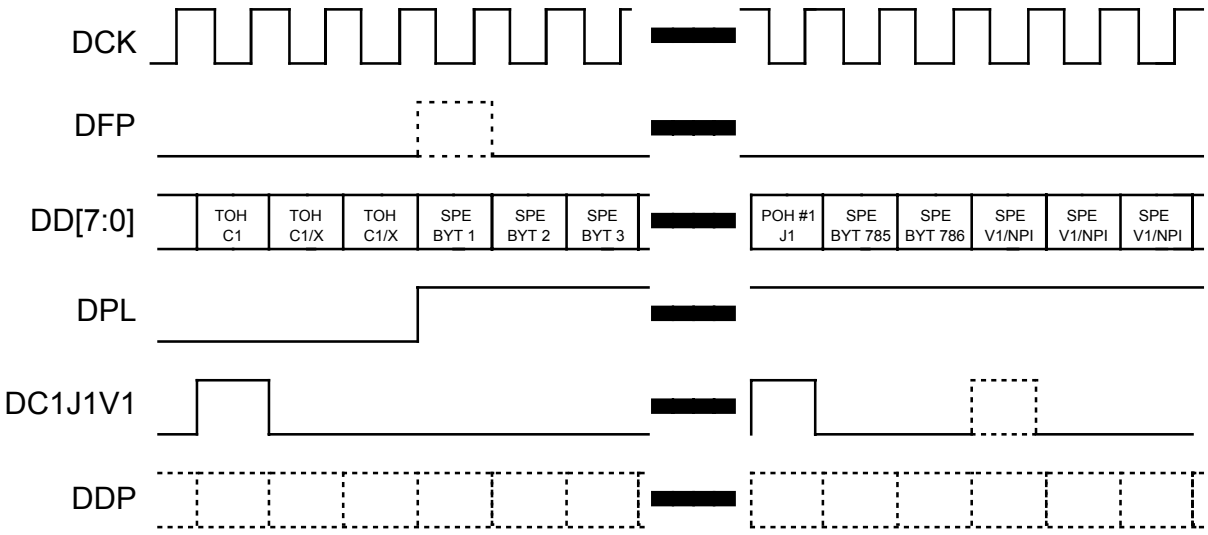
The figure above shows the STS-3 (STM-1/AU3) byte mode DROP bus timing. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte in the STS-3 (STM-1/AU3) frame on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 (STM-0/AU3) #3. A stuff byte is place in the positive stuff opportunity byte and DPL is set low to indicate that data is not available. The DROP bus composite timing signal DC1J1V1 is set high when DPL is set low to mark the C1 byte. DC1J1V1 is set high when DPL is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU3) streams. Optionally, DC1J1V1 is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP reports the parity of DD[7:0] and optionally includes DPL and DC1J1V1.

Figure 53 - STS-3 (STM-1/AU3) Nibble Mode DROP Bus Timing



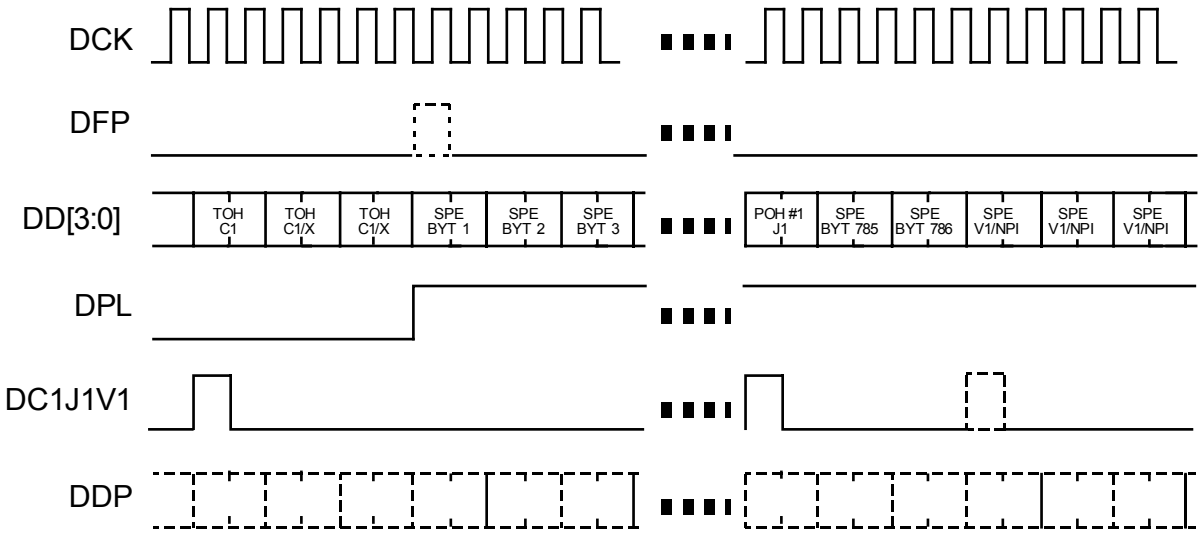
The figure above shows the STS-3 (STM-1/AU3) nibble mode DROP bus timing of an equivalent STS-3 (STM-1/AU3) output sequence as in the byte mode illustration. DCK is a 38.88 MHz clock. Each byte in each of the three STS-1 (STM-0/AU3) streams, including overhead and payload, is transferred as nibbles with the upper nibble in each byte being driven onto DD[3:0] first. The frame pulse DFP marks the upper nibble of the first synchronous payload envelope byte in the STS-1 (STM-0/AU3) #1 frame. This position is maintained by an internal fly-wheel counter thus DFP need not be asserted on every frame. The DPL signal marks both nibbles of each payload byte. A positive pointer justification event for STS-1 (STM-0/AU3) #3 is indicated by a de-asserted DPL signal at the position of the stuff byte. The composite signal DC1J1V1 which marks the C1, J1 and optionally, the V1 byte positions in an STS-1 (STM-0/AU3) stream is asserted when the upper nibbles of these bytes are driven out on DD[3:0]. Only the C1 byte of STS-1 (STM-0/AU3) #1 will be indicated. The J1 and V1 (if required) bytes in each of the three STS-1 (STM-0/AU3) streams will be indicated. In case of V1, only the V1 byte position in the first frame of a tributary multiframe will be indicated. The DROP bus parity output DDP reports the parity of DD[3:0] and optionally includes DPL and DC1J1V1.

Figure 54 - STS-3c (STM-1/AU4) Byte Mode DROP Bus Timing



The figure above shows the STS-3c (STM-1/AU4) byte mode DROP bus timing. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first synchronous payload envelope byte on DD[7:0]. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. The DROP bus composite timing signal DC1J1V1 is set high when DPL is set low to mark the C1 byte. DC1J1V1 is set high when DPL is also set high to mark the J1 byte of the STS-3c (STM-1/AU4) streams. Optionally, DC1J1V1 is set high once every multiframe to mark the first frame of the DROP bus tributary multiframe. When processing an STS-3c (STM-1/AU4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c (STM-1/AU4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The DROP bus parity output DDP reports the parity of DD[7:0] and optionally includes DPL and DC1J1V1.

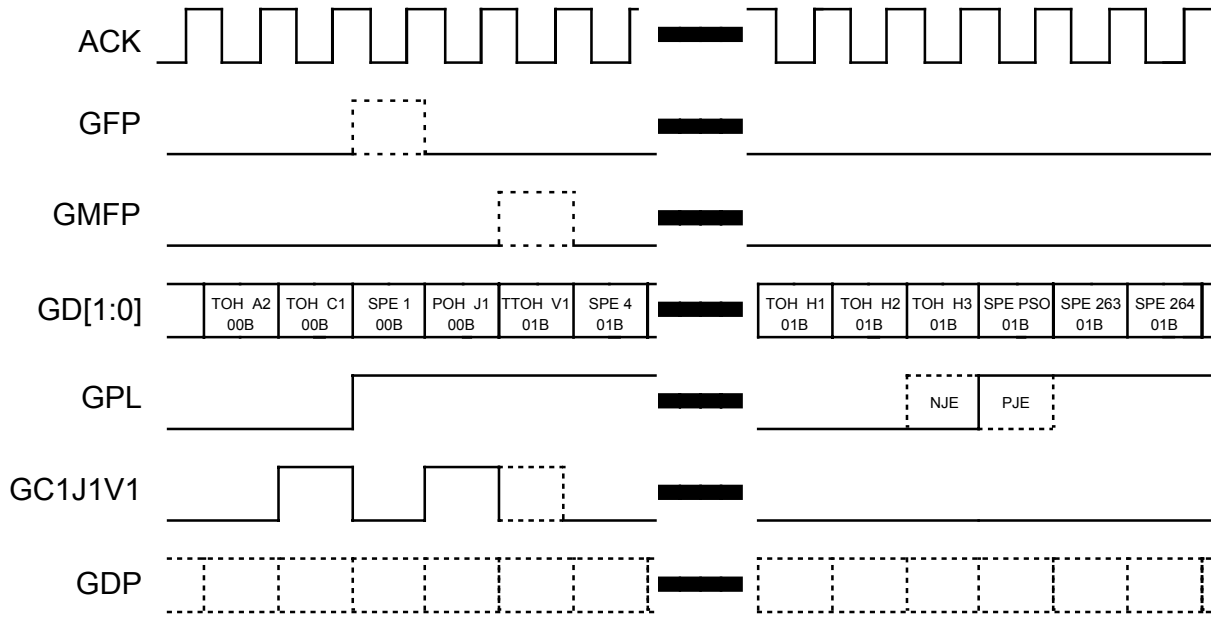
Figure 55 - STS-3c (STM-1/AU4) Nibble Mode DROP Bus Timing



The figure above shows the STS-3c (STM-1/AU4) nibble mode DROP bus timing of an equivalent STS-3c (STM-1/AU4) output sequence as in the byte mode illustration. DCK is a 38.88 MHz clock. Each byte in the STS-3c (STM-1/AU4) stream, including overhead and payload, is transferred as nibbles with the upper nibble in each byte being driven onto DD[3:0] first. The frame pulse DFP marks the upper nibble of the first synchronous payload envelope byte in the STS-3c (STM-1/AU4) frame. This position is maintained by an internal fly-wheel counter thus DFP need not be asserted on every frame. The DPL signal marks both nibbles of each payload byte. The composite signal DC1J1V1 which marks the C1, J1 and optionally, the V1 byte positions in an STS-3c (STM-1/AU4) stream is asserted when the upper nibbles of these bytes are driven out on DD[3:0]. Only the first C1 byte position in an STS-3c (STM-1/AU4) frame and the V1 (if required) byte position in the first frame of a tributary multiframe will be indicated. For STS-3c (STM-1/AU4), the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI). The DROP bus parity output DDP reports the parity of DD[3:0] and optionally includes DPL and DC1J1V1.

13.4.2 GENERATED Bus

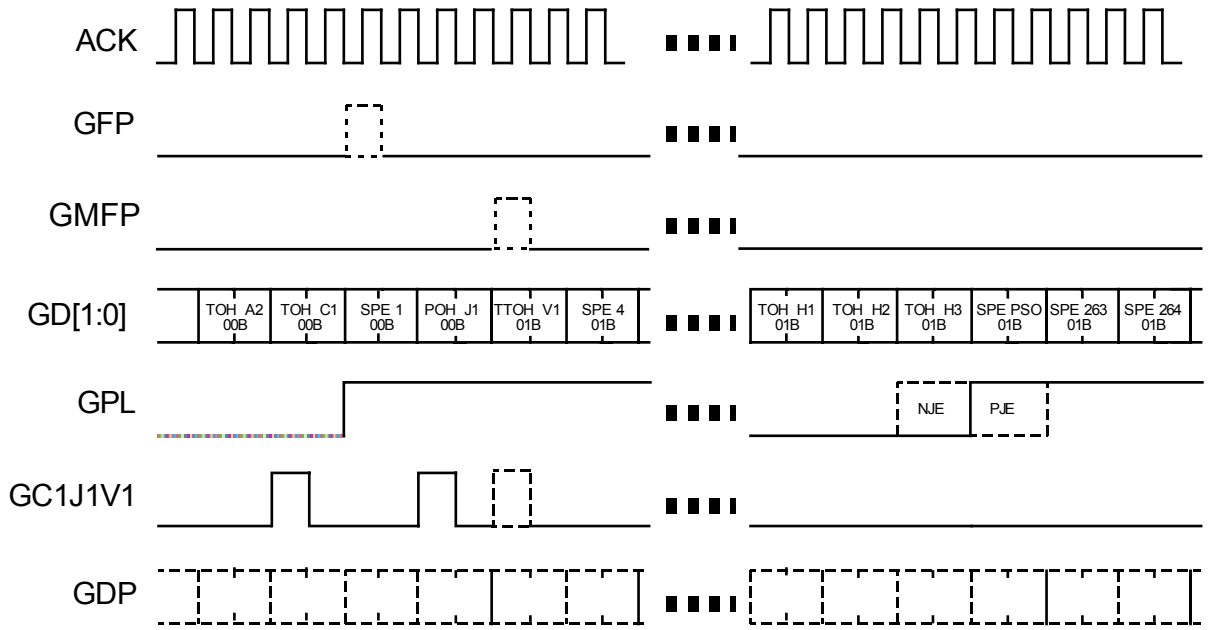
Figure 56 - STS-1 (STM-0/AU3) Byte Mode GENERATED Bus Timing



The figure above shows the STS-1 (STM-0/AU3) byte mode GENERATED bus timing. ACK is a 6.48 MHz clock. The frame pulse GFP marks the first synchronous payload envelope byte in the STS-1 (STM-0/AU3) frame on GD[1:0]. The tributary multiframe frame pulse GMFP marks the byte after J1 of the first frame in a tributary multiframe on GD[1:0]. It is not necessary for GFP or GMFP to be present at every opportunity. Internal counters fly-wheel based on the most recent GFP and GMFP received. In the first frame of a tributary multiframe, GD[1:0] is set to 01B. The data on GD[1:0] is update once per frame on the byte after the J1 byte in the sequence of 01B, 10B, 11B and 00B. Transport overhead and payload bytes are distinguished by the GPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labeled NJE), GPL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labeled PJE), GPL is set low during the PSO byte to indicate that payload data is not available. The GENERATED bus composite timing signal GC1J1V1 is set high when GPL is set low to mark the C1 byte. GC1J1V1 is set high when GPL is also set high to mark the J1 byte. Optionally, GC1J1V1 is set high on the first payload byte after J1 to mark the first frame of the GENERATED bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The GENERATED bus

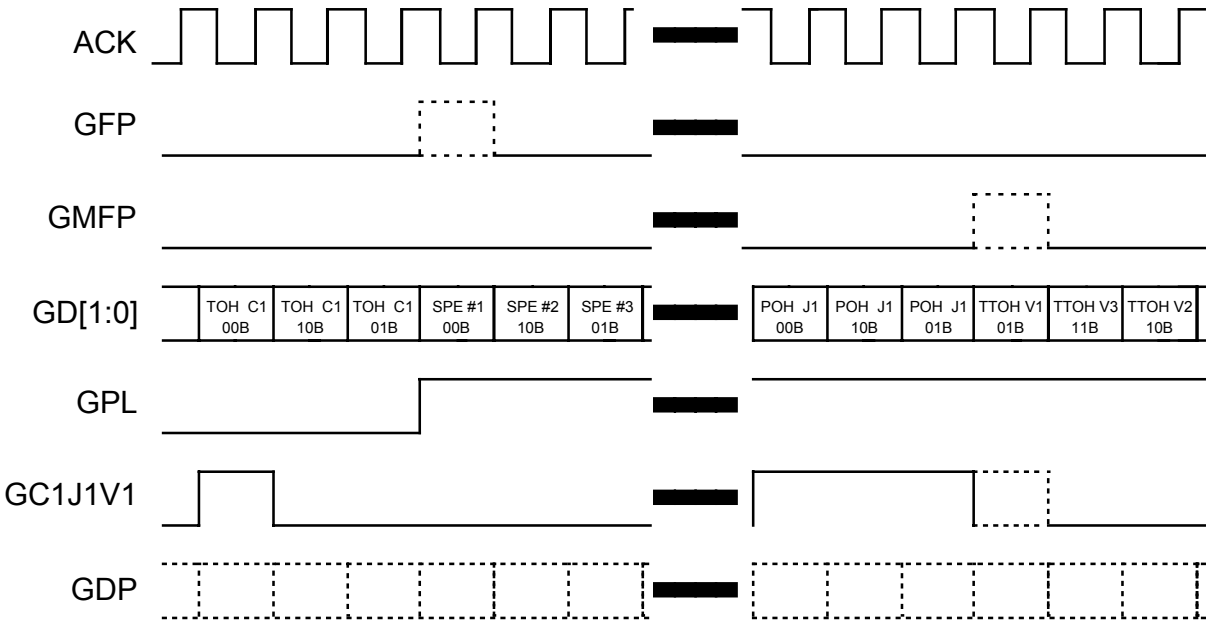
parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

Figure 57 - STS-1 (STM-0/AU3) Nibble Mode GENERATED Bus Timing



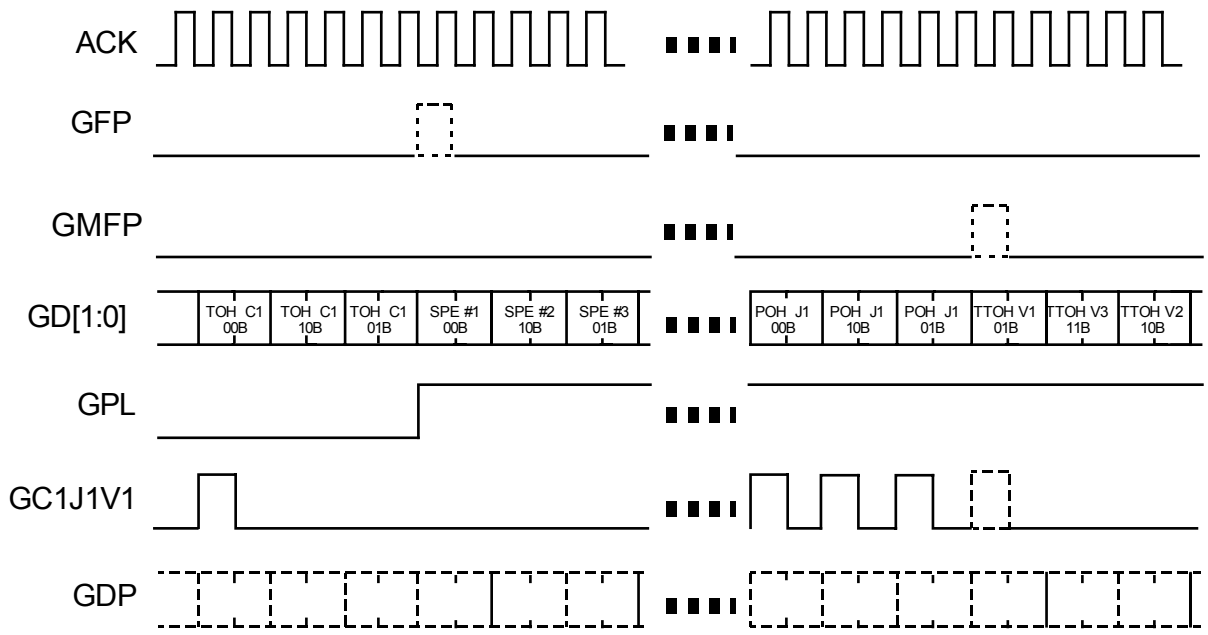
The figure above shows the STS-1 (STM-0/AU3) nibble mode GENERATED bus timing of an equivalent STS-1 (STM-0/AU3) sequence as in the byte mode illustration. ACK is a 12.96 MHz clock. The frame pulse GFP marks the upper nibble of the first synchronous payload envelope byte in the STS-1 (STM-0/AU3) frame. The tributary multiframe frame pulse GMFP marks the upper nibble after the J1 byte in the first frame of a multiframe sequence. The respective positions marked by GFP and GMFP are maintained by internal fly-wheel counters thus they need not be asserted on every frame. The GD[1:0] signals sequence through 01B, 10B, 11B and 00B and changing values on the byte immediately after the J1 byte in each STS-1 (STM-0/AU3) frame. This is to indicate (control) the current tributary multiframe sequence with 01B indicating the first frame. The GPL signal marks both nibbles of each payload byte in an STS-1 (STM-0/AU3) stream. The composite signal GC1J1V1 which marks the C1, J1 and optionally, the V1 byte positions in an STS-1 (STM-0/AU3) stream is asserted when the upper nibbles of these bytes are transferred. The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

Figure 58 - STS-3 (STM-1/AU3) Byte Mode GENERATED Bus Timing



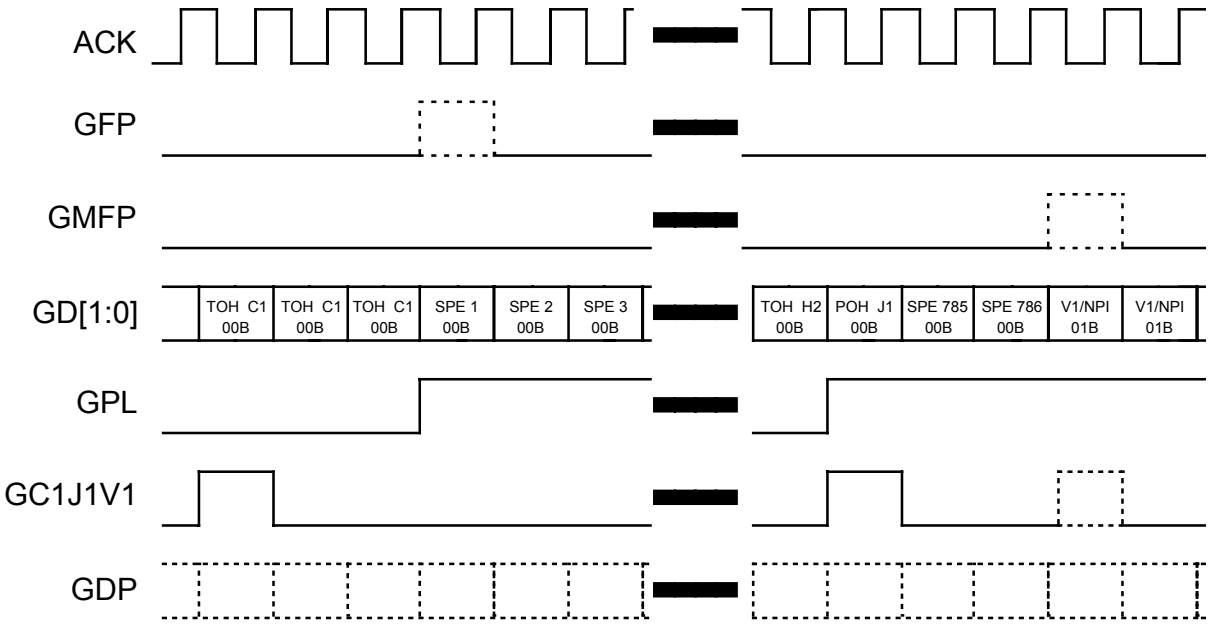
The figure above shows the STS-3 (STM-1/AU3) byte mode GENERATED bus timing. ACK is a 19.44 MHz clock. The frame pulse GFP marks the first synchronous payload envelope byte in the STS-3 (STM-1/AU3) frame on GD[1:0]. The tributary multiframe frame pulse GMFP marks the byte after J1 of the first frame in a tributary multiframe of each STS-1 (STM-0/AU3) stream. It is not necessary for GFP or GMFP to be present at every opportunity. Internal counters fly-wheel based on the most recent GFP and GMFP received. Transport overhead and payload bytes are distinguished by the GPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. All three synchronous payload envelops are shown to have the same active offset for illustration only; any combination of active offsets are possible. The tributary multiframe alignments of the three STS-1 (STM-0/AU3) streams are independent. The value on GD[1:0] reflect the different alignments. The GENERATED bus composite timing signal GC1J1V1 is set high when GPL is set low to mark the C1 byte. GC1J1V1 is set high when GPL is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU3) streams. Optionally, GC1J1V1 is set high once every multiframe to mark the first frame of the GENERATED bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

Figure 59 - STS-3 (STM-1/AU3) Nibble Mode GENERATED Bus Timing



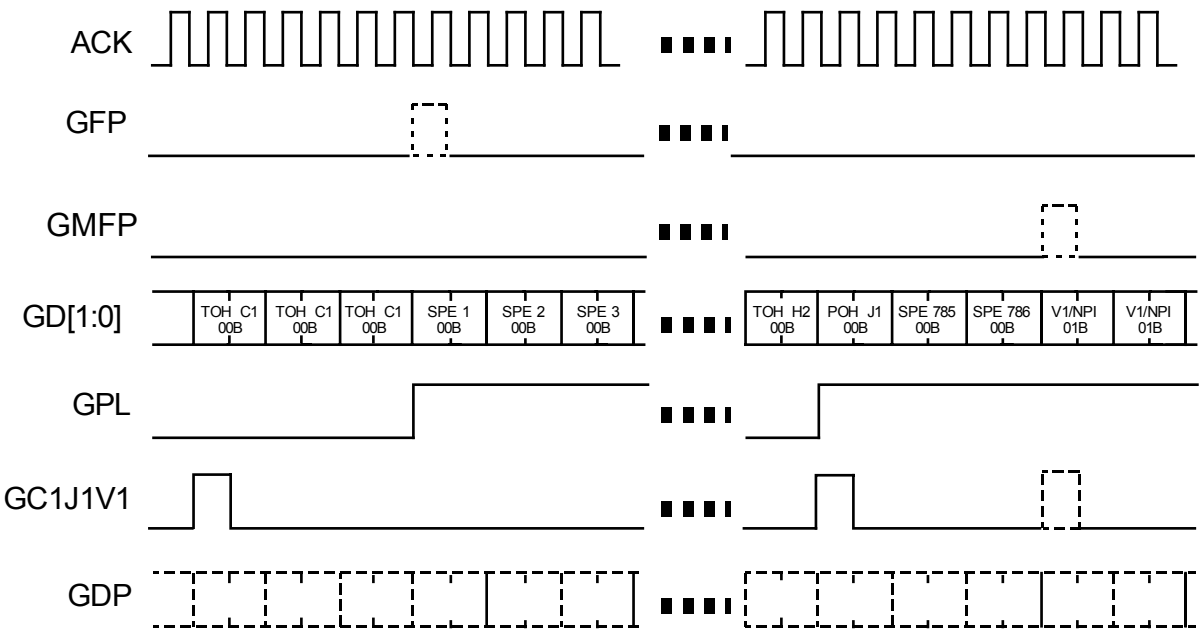
The figure above shows the STS-3 (STM-1/AU3) nibble mode GENERATED bus timing of an equivalent STS-3 (STM-1/AU3) sequence as in the byte mode illustration. ACK is a 38.88 MHz clock. The frame pulse GFP marks the upper nibble of the first synchronous payload envelope byte in the STS-3 (STM-1/AU3) frame. The tributary multiframe frame pulse GMFP marks the upper nibble after the J1 byte in the first frame of a multiframe sequence in each STS-1 (STM-0/AU3) stream. The respective positions marked by GFP and GMFP are maintained by an internal fly-wheel counters thus they need not be asserted on every frame. The GD[1:0] signals sequence through 01B, 10B, 11B and 00B and changing values on the byte immediately after the J1 byte in each STS-1 (STM-0/AU3) stream. This is to indicate (control) the current tributary multiframe sequence in each STS-1 (STM-0/AU3) stream with 01B indicating the first frame. The tributary multiframe alignments of the three STS-1 (STM-0/AU3) streams are independent and different as illustrated. The GPL signal marks both nibbles of each payload byte in each STS-1 (STM-0/AU3) stream. The composite signal GC1J1V1 which marks the C1, J1 and optionally, the V1 byte positions in the STS-1 (STM-0/AU3) streams is asserted when the upper nibbles of these bytes are transferred. Only the C1 byte of STS-1 (STM-0/AU3) #1 will be indicated. If required, the J1 and V1 bytes in each of the three STS-1 (STM-0/AU3) streams will be indicated. For V1, only the V1 byte position in the first frame of a tributary multiframe will be indicated. The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

Figure 60 - STS-3c (STM-1/AU4) Byte Mode GENERATED Bus Timing



The figure above shows the STS-3c (STM-1/AU4) byte mode GENERATED bus timing. ACK is a 19.44 MHz clock. The frame pulse GFP marks the first synchronous payload envelope byte in the STS-3c (STM-1/AU4) frame on GD[1:0]. The tributary multiframe frame pulse GMFP marks the third byte after J1 of the first frame in a tributary multiframe on GD[1:0]. It is not necessary for GFP or GMFP to be present at every opportunity. Internal counters fly-wheel based on the most recent GFP and GMFP received. Transport overhead and payload bytes are distinguished by the GPL output which is set low to mark transport overhead bytes and set high to mark payload bytes. The GENERATED bus composite timing signal GC1J1V1 is set high when GPL is set low to mark the C1 byte. GC1J1V1 is set high when GPL is also set high to mark the J1 byte of the STS-3c (STM-1/AU4) streams. Optionally, GC1J1V1 is set high once every multiframe to mark the first frame of the GENERATED bus tributary multiframe. When processing an STS-3c (STM-1/AU4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. A negative justification event (NJE) is shown. Prior to the NJE, the alignment of the transport frame and the synchronous payload envelope corresponds to an active offset of 0. After the event, the active offset will be 782. The active offsets shown are for illustration only; other alignments are possible. The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

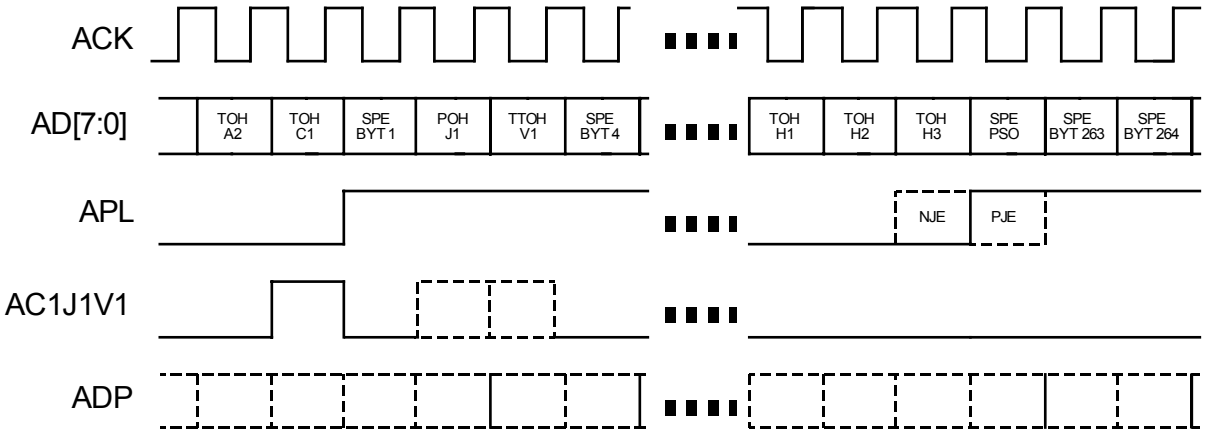
Figure 61 - STS-3c (STM-1/AU4) Nibble Mode GENERATED Bus Timing



The figure above shows the STS-3c (STM-1/AU4) nibble mode GENERATED bus timing of an equivalent STS-3c (STM-1/AU4) sequence as in the byte mode illustration. ACK is a 38.88 MHz clock. The frame pulse GFP marks the upper nibble of the first synchronous payload envelope byte in the STS-3c (STM-1/AU4) frame. The tributary multiframe frame pulse GMFP marks the upper nibble of the third byte after the J1 byte, in the first frame of a multiframe sequence, in an STS-3c (STM-1/AU4) stream. The respective positions marked by GFP and GMFP are maintained by an internal fly-wheel counters thus they need not be asserted on every frame. The GD[1:0] signals sequence through 01B, 10B, 11B and 00B and changing values on the third byte following the J1 byte in the STS-3c (STM-1/AU4) stream. This is to indicate (control) the current tributary multiframe sequence in the STS-3c (STM-1/AU4) stream with 01B indicating the first frame. The GPL signal marks both nibbles of each payload byte in the STS-3c (STM-1/AU4) stream. The composite signal GC1J1V1 which marks the C1, J1 and optionally, the V1 byte positions in the STS-3c (STM-1/AU4) stream is asserted when the upper nibbles of these bytes are transferred. Only the first C1 byte in an STS-3c (STM-1/AU4) frame will be indicated. For STS-3c (STM-1/AU4), only the first V1 (if required) byte in the first STS-3c (STM-1/AU4) frame of a tributary multiframe will be indicated. For STS-3c (STM-1/AU4), the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI). The GENERATED bus parity output GDP reports the parity of GD[1:0] and optionally includes GPL and GC1J1V1.

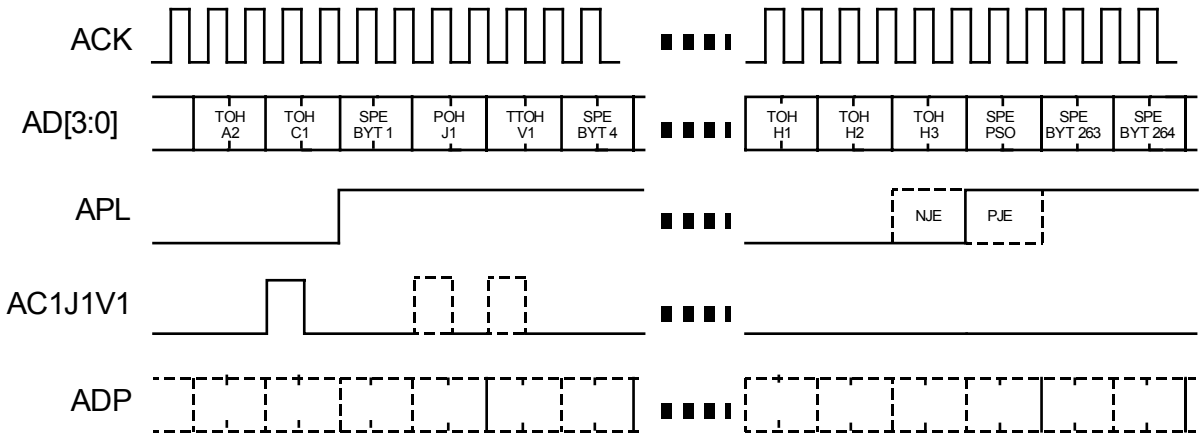
13.4.3 ADD Bus

Figure 62 - STS-1 (STM-0/AU3) Byte Mode ADD Bus Timing



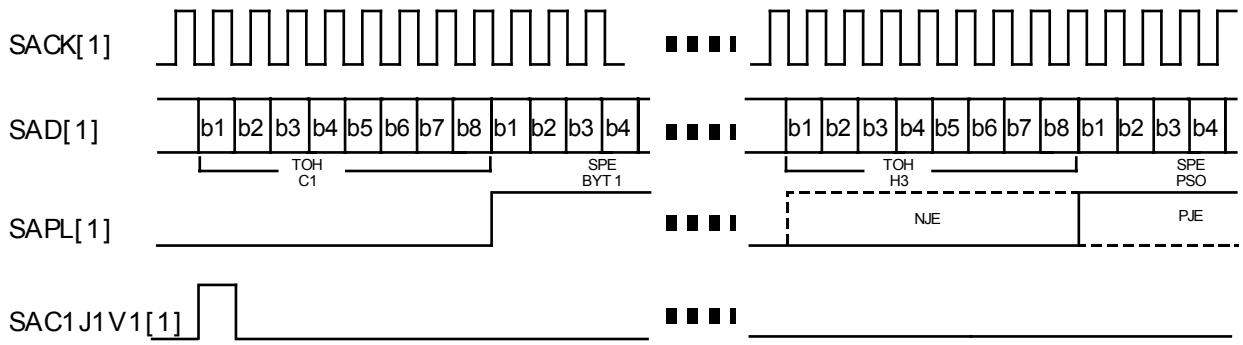
The figure above shows the STS-1 (STM-0/AU3) byte mode ADD bus timing. ACK is a 6.48 MHz clock. Transport overhead and payload bytes are distinguished by the APL input which is set low to mark transport overhead bytes and set high to mark payload bytes. During a negative justification event (labeled NJE), APL is set high during the H3 byte to indicate that payload data is available. During a positive justification event (labeled PJE), APL is set low during the PSO byte to indicate that payload data is not available. The ADD bus composite timing signal AC1J1V1 is set high when APL is set low to mark the C1 byte. AC1J1V1 is optionally set high when APL is also set high to mark the J1 byte. Optionally, AC1J1V1 is set high on the first payload byte after J1 once every multiframe to mark the first frame of the ADD bus tributary multiframe. The alignment of the transport frame and the synchronous payload envelope shown corresponds to an active offset of 523 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP carries the parity of AD[7:0] and optionally includes APL and AC1J1V1.

Figure 63 - STS-1 (STM-0/AU3) Nibble Mode ADD Bus Timing



The figure above shows the STS-1 (STM-0/AU3) nibble mode ADD bus timing of the same STS-1 (STM-0/AU3) input sequence as the byte mode illustration. ACK is a 12.96 MHz clock. Each byte in an STS-1 (STM-0/AU3) stream, including overhead and payload, is transferred as nibbles with the upper nibble in each byte being driven onto AD[3:0] first. The APL signal marks both nibbles of each payload byte. A negative justification event (NJE) will be indicated by an APL assertion during the H3 byte. A positive justification event (PJE) will be indicated by a de-asserted APL signal during the PSO byte. The composite signal AC1J1V1 which marks the C1, optionally the J1 and optionally the V1 byte positions in an STS-1 (STM-0/AU3) stream is asserted when the upper nibbles of these bytes are provided on AD[3:0]. Only the V1 byte in the first STS-1 (STM-0/AU3) frame of a tributary multiframe sequence is indicated if required. The ADD bus parity input ADP reports the parity of AD[3:0]. The APL and AC1J1V1 signals are optionally included in the parity checking.

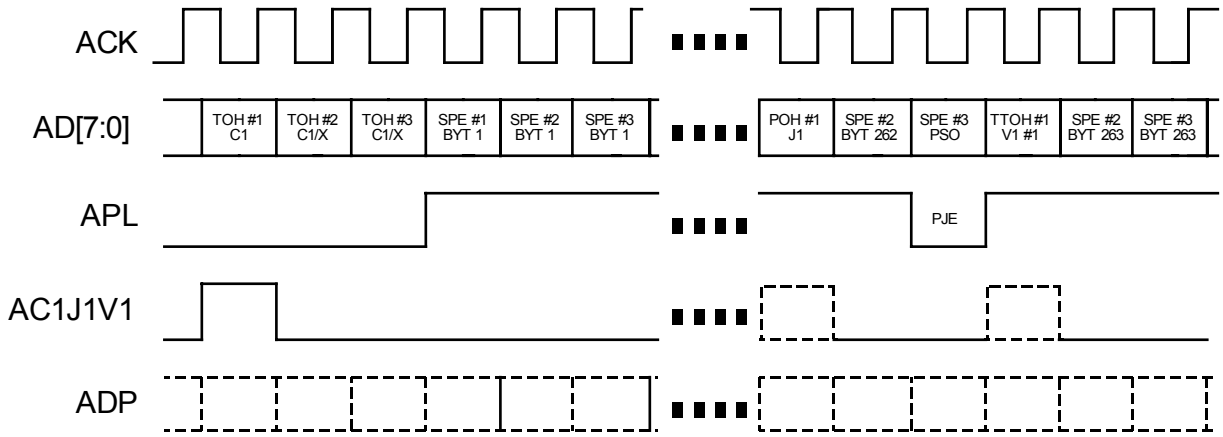
Figure 64 - STS-1/3 (STM-0/AU3, STM-1/AU3) Serial Mode ADD Bus Timing



The figure above shows the STS-1/3 (STM-0/AU3, STM-1/AU3) serial mode ADD bus timing of an equivalent STS-1 (STM-0/AU3) input sequence as in the byte mode illustration. SACK[1] is a 51.84 MHz clock. Each byte in an STS-1 (STM-0/AU3) stream, including overhead and payload, is transferred as a serial stream. The most significant bit b1 in each byte is driven onto SAD[1] first. The SAPL[1] signal marks all 8 bits of each payload byte in the serial input stream. It is also asserted during a negative stuff byte (H3) if such an event exists. A positive stuff event is indicated by a de-asserted SAPL[1] signal during that payload stuff opportunity (PSO) byte. The composite signal SAC1J1V1[1] which marks the C1, optionally the J1 and optionally the V1 byte positions in an STS-1 (STM-0/AU3) stream is only asserted when the most significant bit b1 of these bytes are provided on SAD[1]. Only the V1 byte in the first STS-1 (STM-0/AU3) frame of a tributary multiframe sequence is indicated if required.

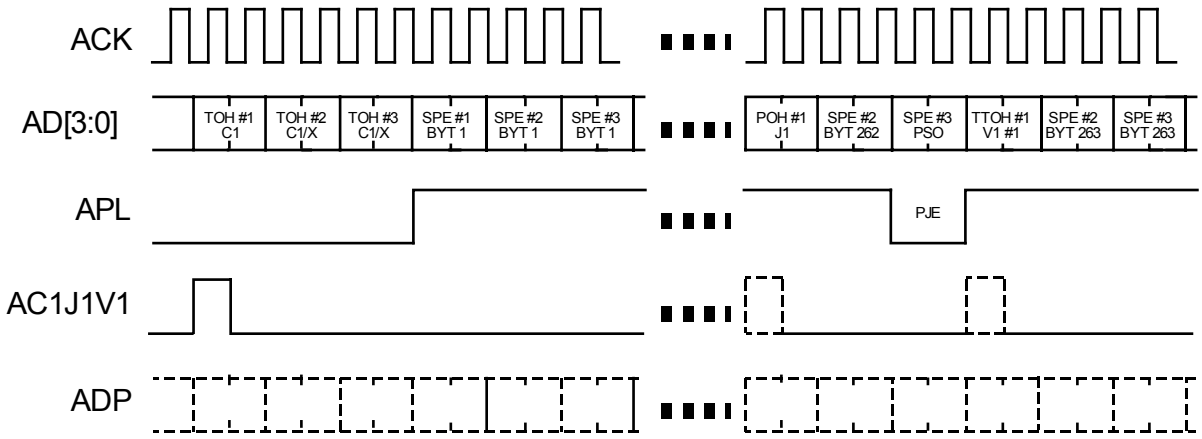
For an STS-3 (STM-1/AU3) stream, the above serial mode ADD bus timing applies to its STS-1 (STM-0/AU3) #1 stream. The ADD bus timing for STS-1 (STM-0/AU3) #2 and #3 streams in the STS-3 (STM-1/AU3) stream are similar. The STS-1 (STM-0/AU3) #2 stream is transferred via SAD[2], SAPL[2] and SAC1J1V1[2]. The ADD bus clock is SACK[2]. The STS-1 (STM-0/AU3) #3 stream is transferred on the serial ADD bus comprising the SACK[3], SAD[3], SAPL[3] and SAC1J1V1[3] signals. The three serial ADD buses for the individual STS-1 (STM-0/AU3) streams, which will be aligned and multiplexed into an STS-3 (STM-1/AU3) stream, operate independently of each other.

Figure 65 - STS-3 (STM-1/AU3) Byte Mode ADD Bus Timing



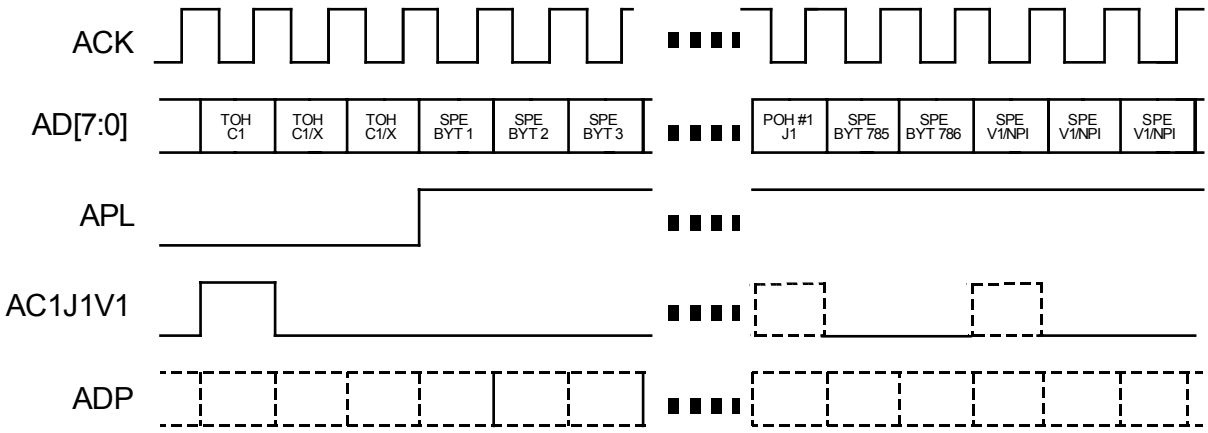
The figure above shows the STS-3 (STM-1/AU3) ADD bus timing. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL input which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 (STM-0/AU3) #3. A stuff byte is place in the positive stuff opportunity byte and APL is set low to indicate that data is not available. The ADD bus composite timing signal AC1J1V1 is set high when APL is set low to mark the C1 byte. Optionally, AC1J1V1 is set high when APL is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU3) streams. Optionally, AC1J1V1 is set high once every multiframe to mark the first frame of the ADD bus tributary multiframe in each STS-1 (STM-0/AU3) stream. The alignment of the transport frame and the synchronous payload envelope of STS-1 (STM-0/AU3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP carries the parity of AD[7:0] and optionally includes APL and AC1J1V1.

Figure 66 - STS-3 (STM-1/AU3) Nibble Mode ADD Bus Timing



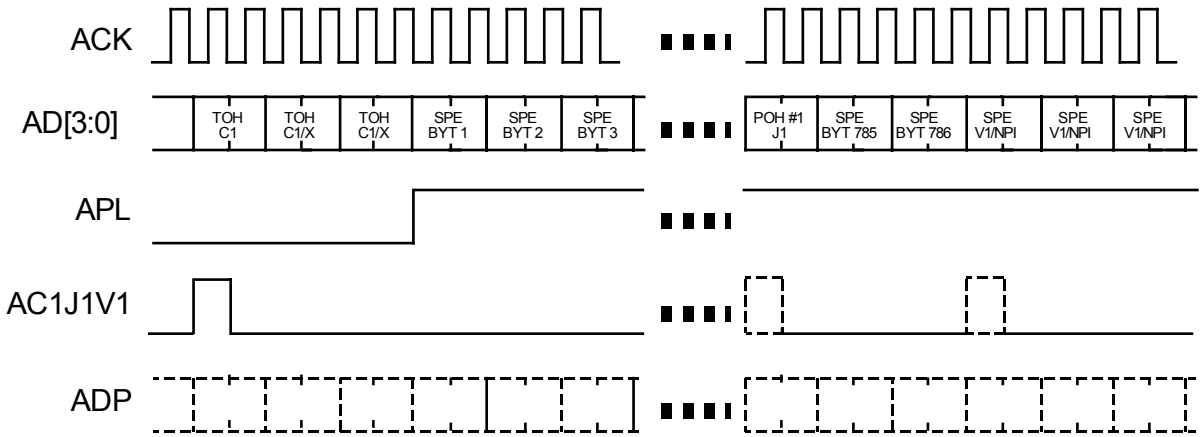
The figure above shows the STS-3 (STM-1/AU3) nibble mode ADD bus timing of the same STS-3 (STM-1/AU3) input sequence as in the byte mode illustration. ACK is a 38.88 MHz clock. Each byte in each of the three STS-1 (STM-0/AU3) streams, including overhead and payload, is transferred as nibbles with the upper nibble in each byte being driven onto AD[3:0] first. The APL signal marks both nibbles of each payload byte. A positive pointer justification event for STS-1 (STM-0/AU3) #3 is indicated by a de-asserted APL signal during the stuff byte. The composite signal AC1J1V1 which marks the C1, optionally the J1 and optionally the V1 byte positions in an STS-1 (STM-0/AU3) stream is only asserted when the upper nibbles of these bytes are provided on AD[3:0]. Only the C1 byte of STS-1 (STM-0/AU3) #1 will be indicated. Optionally the J1 and V1 bytes in each of the three STS-1 (STM-0/AU3) streams will be indicated. In case of V1, only the V1 byte position in the first frame of a tributary multiframe will be indicated. The ADD bus parity input ADP reports the parity of AD[3:0]. The APL and AC1J1V1 signals are optionally included in the parity checking.

Figure 67 - STS-3c (STM-1/AU4) Byte Mode ADD Bus Timing



The figure above shows the STS-3c (STM-1/AU4) ADD bus timing. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL input which is set low to mark transport overhead bytes and set high to mark payload bytes. The ADD bus composite timing signal AC1J1V1 is set high when APL is set low to mark the C1 byte. Optionally, AC1J1V1 is set high when APL is also set high to mark the J1 byte. Optionally, AC1J1V1 is set high once every multiframe to mark the first frame of the ADD bus tributary multiframe. When processing an STS-3c (STM-1/AU4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multiframe. The alignment of the transport frame and the synchronous payload envelope of STS-3c (STM-1/AU4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The ADD bus parity input ADP carries the parity of AD[7:0] and optionally includes APL and AC1J1V1.

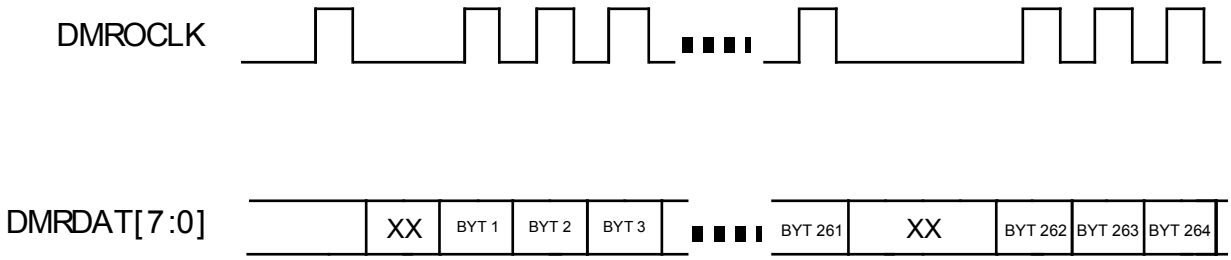
Figure 68 - STS-3c (STM-1/AU4) Nibble Mode ADD Bus Timing



The figure above shows the STS-3c (STM-1/AU4) nibble mode ADD bus timing of an equivalent STS-3c (STM-1/AU4) input sequence as in the byte mode illustration. ACK is a 38.88 MHz clock. Each byte in the STS-3c (STM-1/AU4) stream, including overhead and payload, is transferred as nibbles with the upper nibble in each byte being driven onto AD[3:0] first. The APL signal marks both nibbles of each payload byte. The composite signal AC1J1V1 which marks the C1, optionally the J1 and optionally the V1 byte positions in an STS-3c (STM-1/AU4) stream is asserted when the upper nibbles of these bytes are provided on AD[3:0]. Only the first C1 byte position in an STS-3c (STM-1/AU4) frame and the V1 (if required) byte position in the first frame of a tributary multiframe will be indicated. For STS-3c (STM-1/AU4), the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI). The ADD bus parity input ADP reports the parity of AD[3:0]. The APL and AC1J1V1 signals are optionally included in the parity checking.

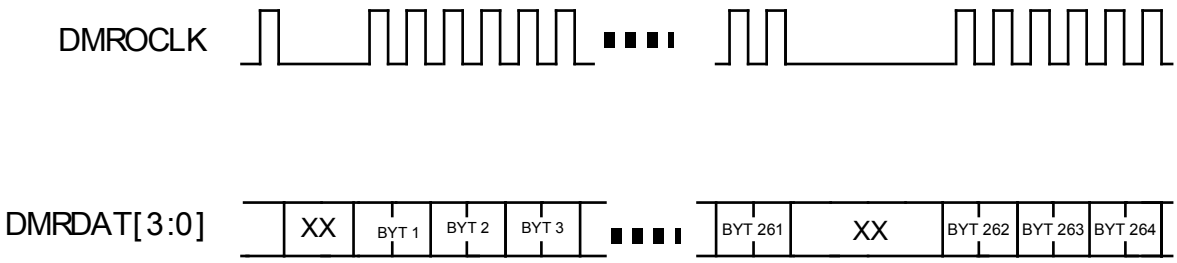
13.5 Data Mode System Side

Figure 69 - STS-1/3c (STM-0/AU3, STM-1/AU4) Byte Data Mode Receive Bus Timing



The figure above shows the STS-1/3c (STM-0/AU3, STM-1/AU4) byte data mode Receive bus timing. DMROCLK is a gapped clock. Data bytes on the DMRDAT[7:0] bus are updated on the falling edge of DMROCLK. In STS-1 (STM-0/AU3) data mode, the gapped clock is generated using a 6.48 MHz clock. The nominal frequency of DMROCLK is 6.048 MHz if payload data is not carried in the two fixed stuff columns. Otherwise, the nominal frequency of DMROCLK is 6.192 MHz. In STS-3c (STM-1/AU4) data mode, the gapped clock is generated using a 19.44 MHz clock. The nominal frequency of DMROCLK is 18.72 MHz.

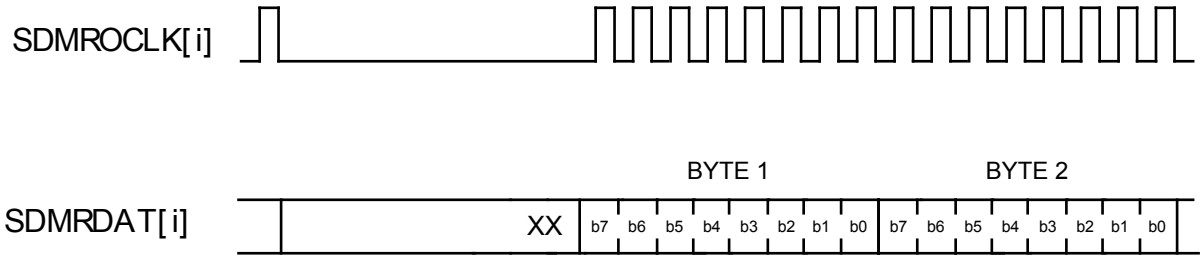
Figure 70 - STS-1/3c (STM-0/AU3, STM-1/AU4) Nibble Data Mode Receive Bus Timing



The figure above shows the STS-1/3c (STM-0/AU3, STM-1/AU4) nibble data mode Receive bus timing. DMROCLK is a gapped clock. Data nibbles on the DMRDAT[3:0] bus are updated on the falling edge of DMROCLK. The upper nibble of a data byte is always driven onto DMRDAT[3:0] bus first followed by the lower nibble. Nibble positions are indicated by the SPECTRA-155 RCLK output (not shown, see AC Timing for nibble data mode). In STS-1 (STM-0/AU3) data mode, the gapped clock is generated using a 12.96 MHz clock. The nominal frequency of DMROCLK is 12.096 MHz if payload data is not carried in the two

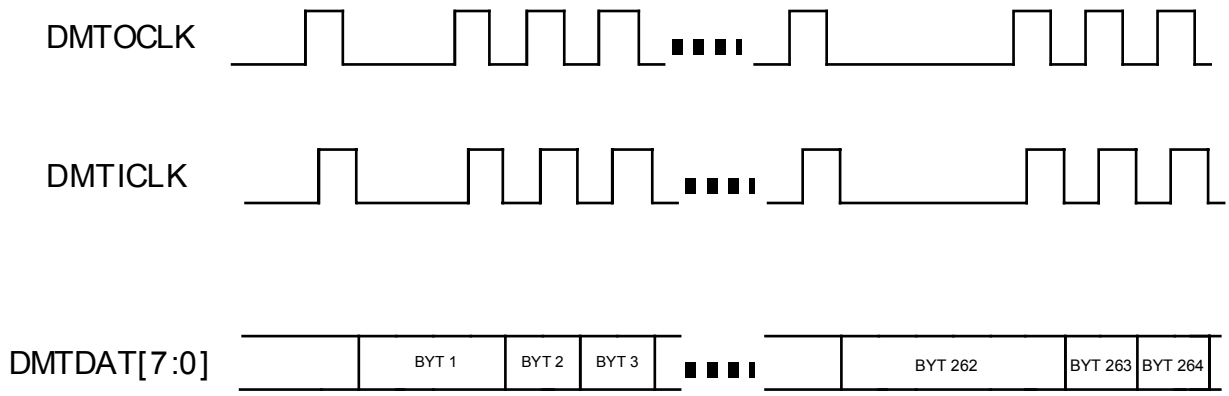
fixed stuff columns. Otherwise, the nominal frequency of DMROCLK is 12.384 MHz. In STS-3c (STM-1/AU4) data mode, the gapped clock is generated using a 38.88 MHz clock. The nominal frequency of DMROCLK is 36.44 MHz.

Figure 71 - STS-1/3 (STM-0/AU3, STM-1/AU3) Serial Data Mode Receive Bus Timing



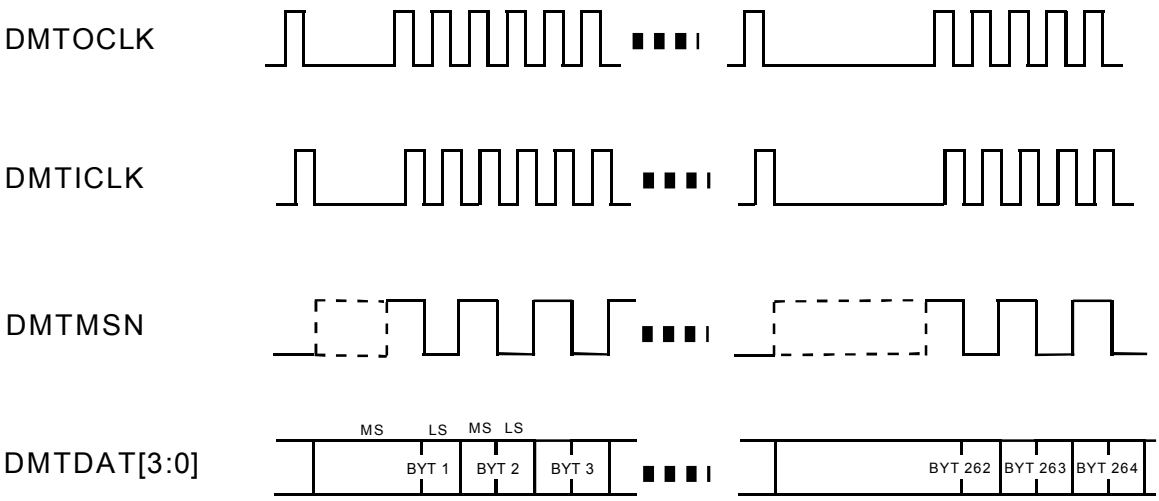
The figure above shows the STS-1/3 (STM-0/AU3, STM-1/AU3) serial data mode Receive bus timing. SDMROCLK[i] is a gapped clock of serial bus #i where i = {1,2,3}. Data bits on the SDMRDAT[i] bus are updated on the falling edge of SDMROCLK[i]. The most significant bit b7 (msb) of a data byte is always driven onto SDMRDAT[i] bus first followed by the less significant bits. The gapped clock is generated using a 51.84 MHz clock. The nominal frequency of SDMROCLK[i] is 48.384 MHz if payload data is not carried in the two fixed stuff columns. Otherwise, the nominal frequency of SDMROCLK[i] is 49.536 MHz. In STS-1 (STM-0/AU3) mode, only serial bus #1 will be active. In STS-3 (STM-1/AU3) mode, all three serial buses operate independently of each other.

Figure 72 - STS-1/3c (STM-0/AU3, STM-1/AU4) Byte Data Mode Transmit Bus Timing



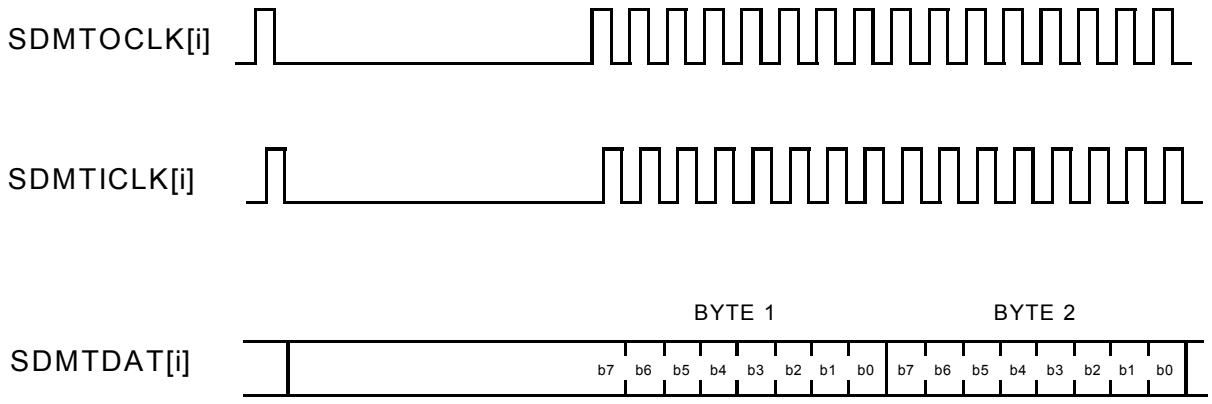
The figure above shows the STS-1/3c (STM-0/AU3, STM-1/AU4) byte data mode Transmit bus timing. DMTOCLK is a gapped clock used to fetch input data from a data source. DMTOCLK is normally fed back to the SPECTRA-155 as DMTICLK. Data bytes on the DMTDAT[7:0] bus are sampled on the rising edge of DMTICLK. In STS-1 (STM-0/AU3) data mode, the gapped clock is generated using a 6.48 MHz clock. The nominal frequency of DMTOCLK is 6.048 MHz if payload data is not carried in the two fixed stuff columns. Otherwise, the nominal frequency of DMTOCLK is 6.192 MHz. In STS-3c (STM-1/AU4) data mode, the gapped clock is generated using a 19.44 MHz clock. The nominal frequency of DMTOCLK is 18.72 MHz.

Figure 73 - STS-1/3c (STM-0/AU3, STM-1/AU4) Nibble Data Mode Transmit Bus Timing



The figure above shows the STS-1/3c (STM-0/AU3, STM-1/AU4) nibble data mode Transmit bus timing. DMTOCLK is a gapped clock used to fetch input data from a data source. DMTOCLK is normally fed back to the SPECTRA-155 as DMTICLK. Data nibbles on the DMTDAT[3:0] bus are sampled on the rising edge of DMTICLK. The more significant nibble of a data byte is driven onto DMTDAT[3:0] bus first followed by the less significant nibble. The nibble positions must be indicated using the DMTMSN input continuously as shown. The more significant nibble of a data byte is indicated by setting DMTMSN to high. The TCLK output of SPECTRA-155 should be used as the DMTMSN signal. In STS-1 (STM-0/AU3) data mode, the gapped clock is generated using a 12.96 MHz clock. The nominal frequency of DMTOCLK is 12.096 MHz if payload data is not carried in the two fixed stuff columns. Otherwise, the nominal frequency of DMTOCLK is 12.384 MHz. In STS-3c (STM-1/AU4) data mode, the gapped clock is generated using a 38.88 MHz clock. The nominal frequency of DMTOCLK is 36.44 MHz.

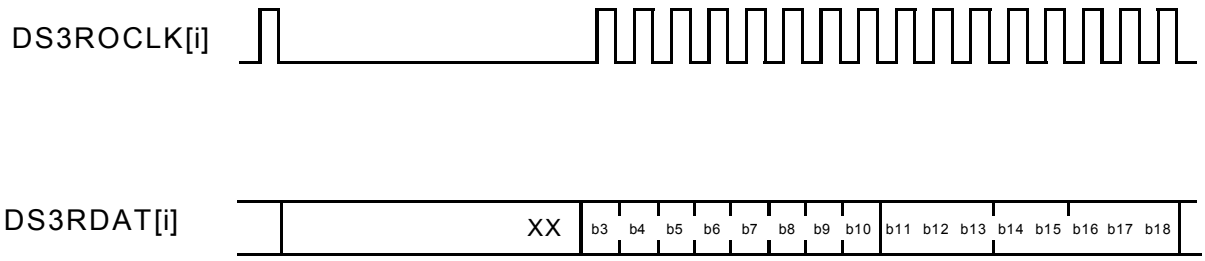
Figure 74 - STS-1/3 (STM-0/AU3, STM-1/AU3) Serial Data Mode Transmit Bus Timing



The figure above shows the STS-1/3 (STM-0/AU3, STM-1/AU3) serial data mode Transmit bus timing. SDMTOCLK[i] is a gapped clock of serial bus #i where i = {1,2,3}. SDMTOCLK[i] is a gapped clock used to fetch input data from a data source. SDMTOCLK[i] is normally fed back to the SPECTRA-155 as SDMTICLK[i]. Data bits on the SDMTDAT[i] bus are sampled on the rising edge of SDMTICLK[i]. The most significant bit b7 (the first transmitted bit of a SONET/SDH serial word) of a data byte is always driven onto SDMTDAT[i] bus first followed by the less significant bits. The gapped clock is generated using a 51.84 MHz clock. The nominal frequency of SDMTOCLK[i] is 48.384 MHz if payload data is not carried in the two fixed stuff columns. Otherwise, the nominal frequency of DMTOCLK is 49.536 MHz. In STS-1 (STM-0/AU3) data mode, only bus #1 will be active. In STS-3 (STM-1/AU3) data mode, all three serial buses operate independently of each other.

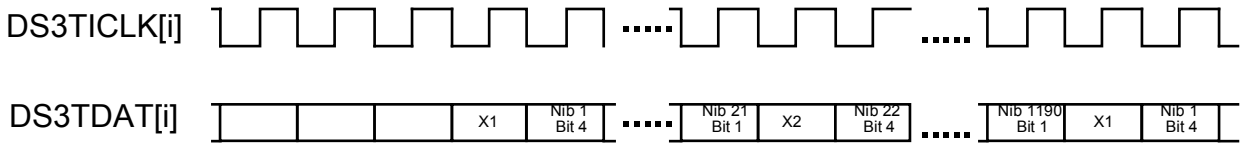
13.6 DS3 Mode System Side

Figure 75 - STS-1/3 (STM-0/AU3, STM-1/AU3) DS3 Mode Receive Bus Timing



The figure above shows the STS-1/3 (STM-0/AU3, STM-1/AU3) DS3 mode Receive bus timing. DS3ROCLK[i] is a gapped clock of serial bus #i where i = {1,2,3}. Data bits on the DS3RDAT[i] bus are updated on the falling edge of DS3ROCLK[i]. The gapped clock is generated using either an internal 51.84 MHz clock or an external 44.928 MHz clock (DS3RICLK[i]). The nominal frequency of DS3ROCLK[i] is 44.736 MHz for either clock sources. In STS-1 (STM-0/AU3) mode, only serial bus #1 will be active. In STS-3 (STM-1/AU3) mode, all three serial buses operate independently of each other.

Figure 76 - STS-1/3 (STM-0/AU3, STM-1/AU3) DS3 Mode Transmit Bus Timing



The figure above shows the STS-1/3 (STM-0/AU3, STM-1/AU3) DS3 mode Transmit bus timing. DS3TICLK[i] is a 44.736 MHz input clock of serial bus #i where i = {1,2,3}. Data bits on the DS3TDAT[i] bus are sampled on the rising edge of DS3TICLK[i]. In STS-1 (STM-0/AU3) mode, only bus #1 will be active. In STS-3 (STM-1/AU3) mode, all three serial buses operate independently of each other.

14 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias -40°C to +85°C

Storage Temperature -40°C to +125°C

Supply Voltage -0.5V to +6.0V

Voltage on Any Pin -0.5V to V_{DD}+0.5V

Static Discharge Voltage ±1000 V

Latch-Up Current ±100 mA

DC Input Current ±20 mA

Lead Temperature +230°C

Absolute Maximum Junction Temperature +150°C

15 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 43 - D.C. Characteristics.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.5	5	5.5	Volts	Note 4.
A_{VD}	Power Supply	4.5	5	5.5	Volts	Note 4.
V_{IL} (TTL)	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage for TTL inputs.
V_{PIL}	Input Low Voltage (ALOS+/- PECL mode only)	A_{VD} - 1.8		A_{VD} - 1.6	Volts	Input LOW Voltage referenced to RAVD3. Note 6
V_{IH} (TTL)	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage for TTL inputs.
V_{PIH}	Input High Voltage (ALOS+/- PECL mode only)	A_{VD} - 1.0		A_{VD} - 0.8	Volts	Input HIGH Voltage referenced to RAVD3. Note 6
V_{PSWG}	Input Voltage Swing (RXD+/-, RRCLK+/-, TRCLK+/- Only)	550			mV	$\|V_{PIH} - V_{PIL}\|$. Only valid for AC coupling.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	I_{OL} = -2 mA for outputs: RAD, B3E[3:1], RALM[3:1], RPOH[3:1], RPOHFP[3:1], RFP, LOF, SALM, LOS_RRCPFP, ROHCLK, RLDCLK, ROH, RLD, RLOW, RSUC, RSLDCLK, ROWCLK, RSLD, RSOW, LAIS_RRCPDAT, LRDI_RRCPCLK, RTOHFP, RTOHCLK, RTOH, TOWCLK, TLDCLK, TTOHCLK, TOHCLK, TSLDCLK, TTOHFP, TFP, TPOHFP[3:1], and SCPO[1:0]. I_{OL} = -4 mA for outputs: TDO, RPOHCLK[3:1], RXC, RCLK, TCLK, D[7:0], INTB, TPOHCLK[3:1], SS[31:27], SS[12:2] and SS[0]. I_{OL} = -8 mA for outputs: TXDN, TXDP and TXC. Notes 3, 4.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output or Bidirectional High Voltage	V_{DD} - 1.0	4.7		Volts	I_{OL} = +2 mA for outputs: RAD, B3E[3:1], RALM[3:1], RPOH[3:1], RPOHFP[3:1], RFP, LOF, SALM, LOS_RRCPFP, ROHCLK, RLDCLK, ROH, RLD, RLOW, RSUC, RSLDCLK, ROWCLK, RSLD, RSOW, LAIS_RRCPDAT, LRDI_RRCPCLK, RTOHFP, RTOHCLK, RTOH, TOWCLK, TLDCLK, TTOHCLK, TOHCLK, TSLDCLK, TTOHFP, TFP, TPOHFP[3:1], and SCPO[1:0]. I_{OL} = +4 mA for outputs: TDO, RPOHCLK[3:1], RXC, RCLK, TCLK, D[7:0], INTB, TPOHCLK[3:1], SS[31:27], SS[12:2] and SS[0]. I_{OL} = +8 mA for outputs: TXDN, TXDP and TXC. Notes 3, 4.
V_{TXOL}	Output Low Voltage (TXD+/- Only)			0.4	Volts	I_{OL} = -6 mA for TXD+, and TXD-, Note 5.
V_{TXOH}	Output High Voltage (TXD+/- Only)	3.9			Volts	I_{OH} = 6 mA for TXD+, and TXD-, Note 5.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{T+}	Schmitt TTL Input High Voltage	2.2			Volts	
V_{T-}	Schmitt TTL Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		0.6		Volts	Note 4.
I_{ILPU}	Input Low Current	75	175	350	µA	V_{IL} = GND, Notes 1, 3, 4.
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	All pins except PECL pins typical capacitance = 10 pF. Excludes package. Package Typically 2 pF. Note 4.
C_{OUT}	Output Capacitance		5		pF	All pins. Excludes package. Package Typically 2 pF. Note 4.
C_{IO}	Bidirectional Capacitance		5		pF	All pins. Excludes package. Package Typically 2 pF. Note 4.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DDOP}	Operating Current.			100	mA	V_{DD} = 5.5 V, Outputs Unloaded. TXD+/- = RXD+/- =51.84 Mbit/s,
				145	mA	TXD+/- = RXD+/- =155.52 Mbit/s

Notes on D.C. Characteristics:

1. Digital input pin or digital bidirectional pin with internal pull-up resistor.
2. Digital input pin or digital bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.
5. The values for V_{TXOL} and V_{TXOH} ensure a minimum 550 mV swing at the ECL buffer input when the circuit described in the "Interfacing SPECTRA-155 to ECL or PECL" section is used to attenuate TXD+ and TXD-.
6. ALOS+/- must be DC coupled. When connected as a PECL input, ALOS+/- has characteristics defined by V_{PIL} and V_{PIH}. When connected as a TTL input, ALOS+/- has characteristics as defined by V_{IL} and V_{IH}.

16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 44 - Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tS_{RWB}	RWB to Read Set-up	25		ns
tH_{RWB}	RWB to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 77 - Microprocessor Interface Read Access Timing (Intel Mode)

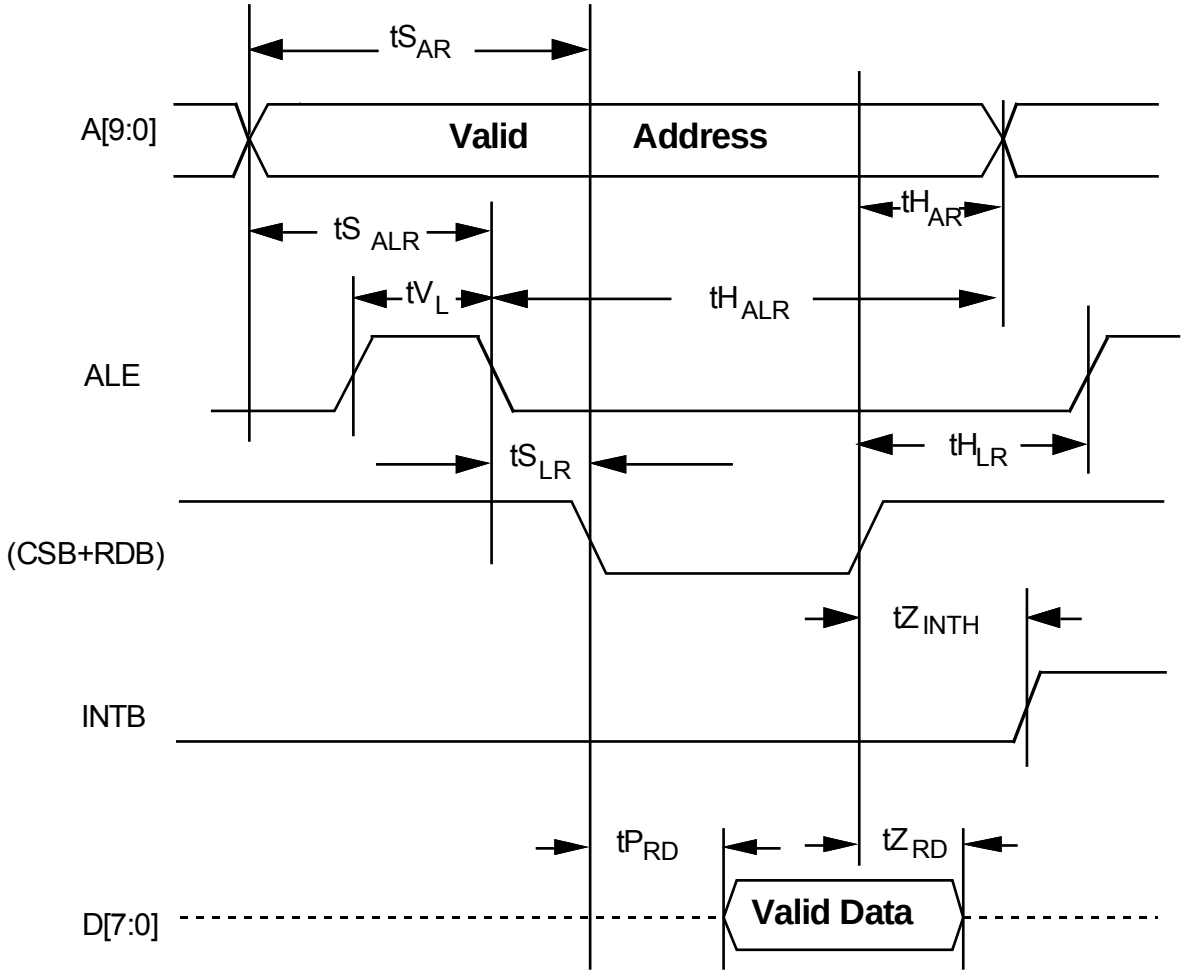
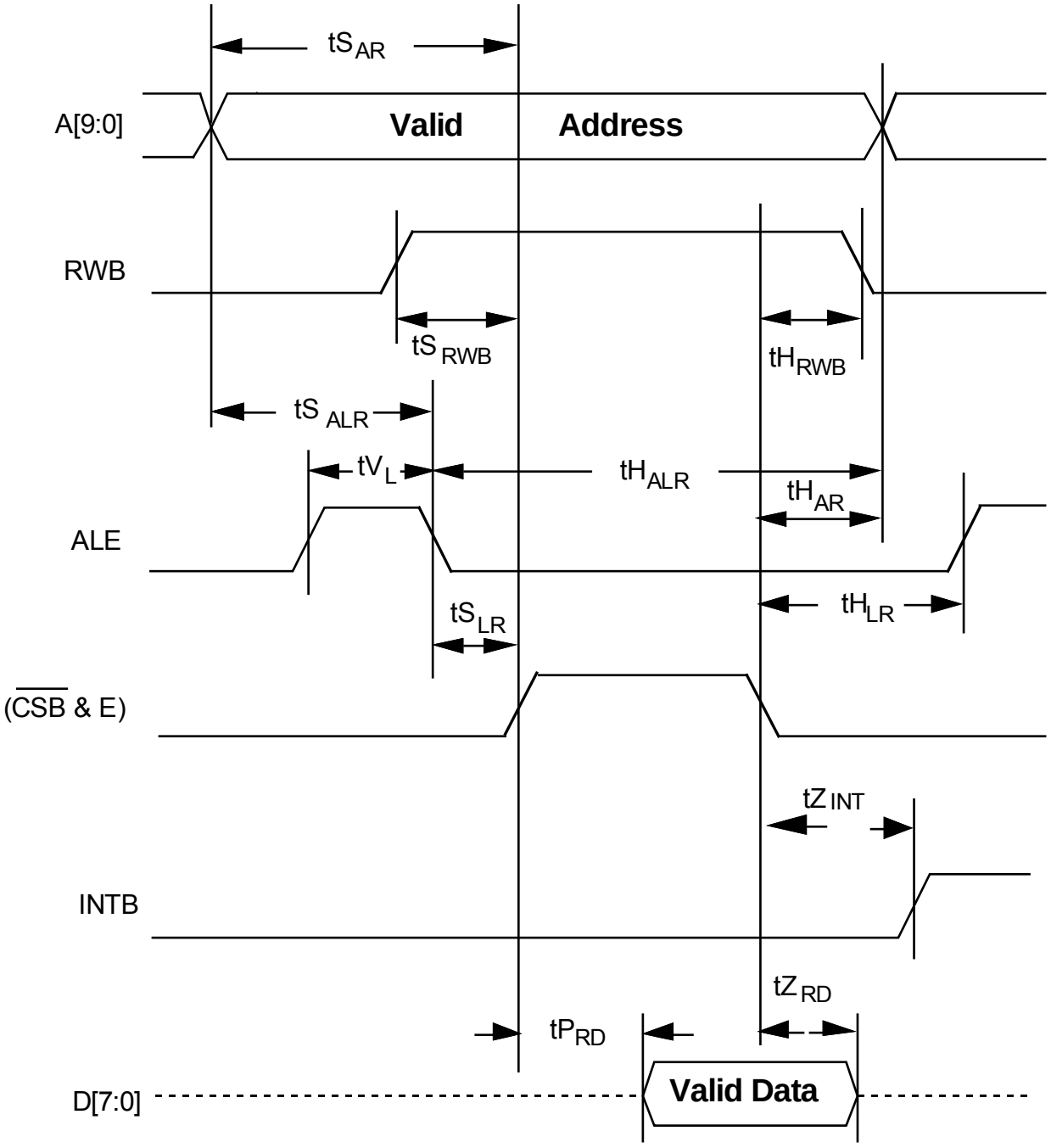


Figure 78 - Microprocessor Interface Read Access Timing (Motorola Mode)



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. In Intel mode, a valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In Motorola mode, a valid read cycle is defined as a logical AND of the E signal, the RWB signal and the inverted CSB signal.

5. Microprocessor Interface timing applies to normal mode register accesses only.

6. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

7. Parameter tH_{AR} and tS_{AR} are not applicable if address latching is used.

8. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

9. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 45 - Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tS_{RWB}	RWB to Write Set-up	25		ns
tH_{RWB}	RWB to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 79 - Microprocessor Interface Write Access Timing (Intel Mode)

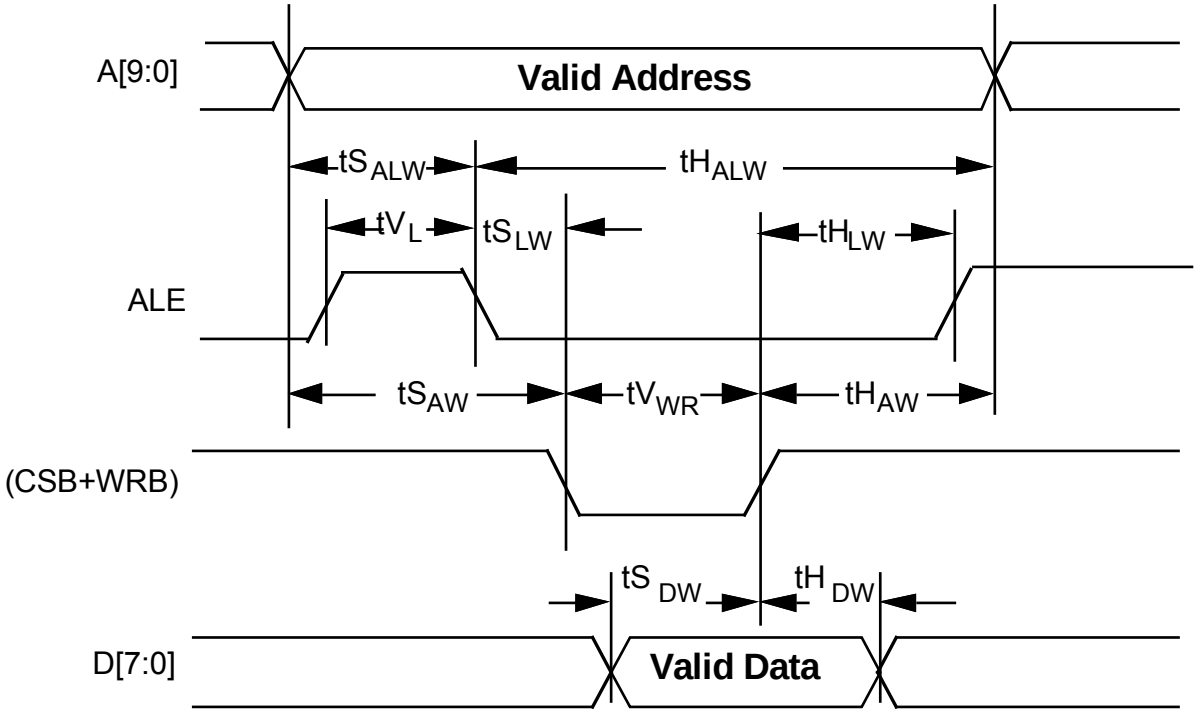
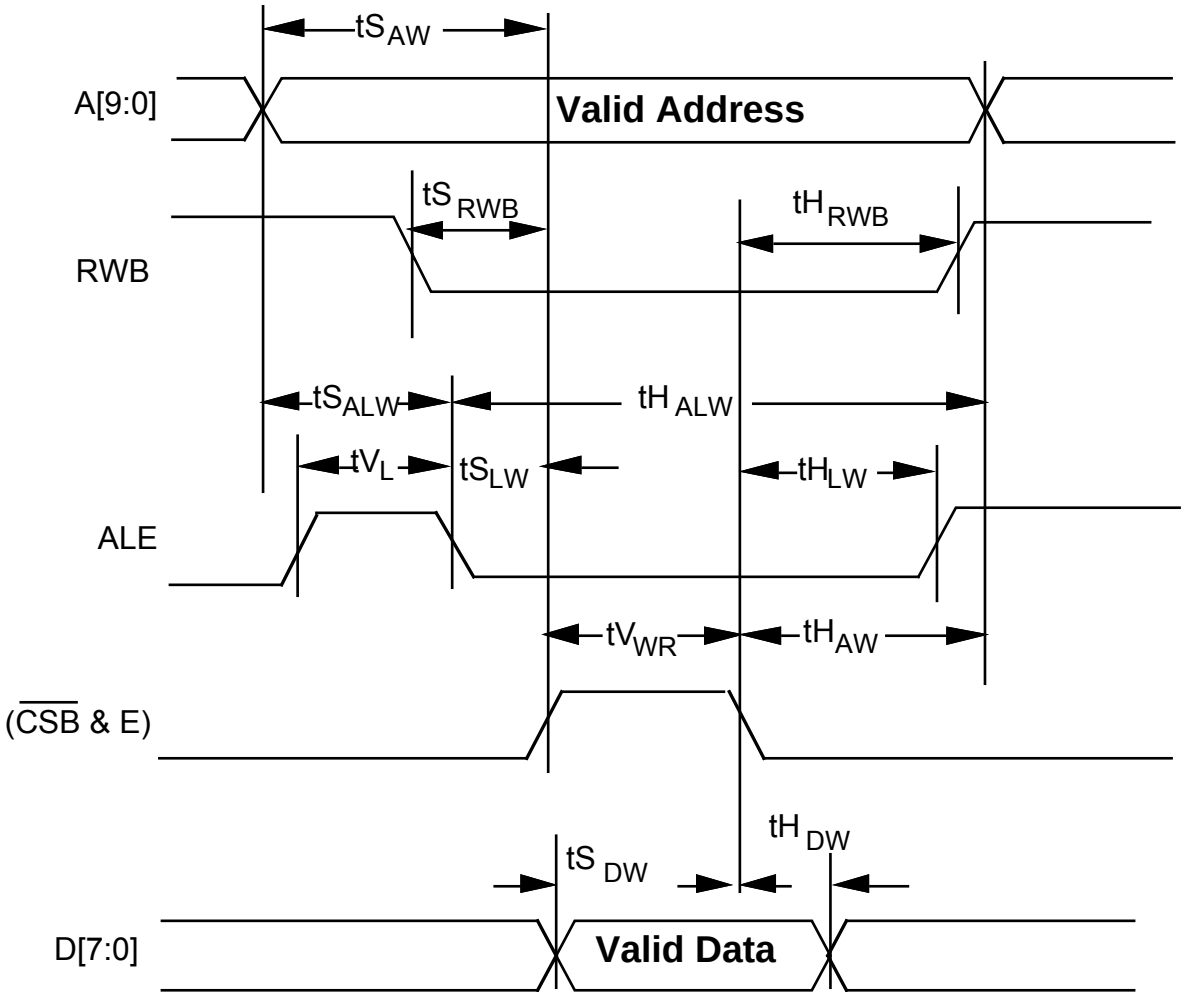


Figure 80 - Microprocessor Interface Write Access Timing (Motorola Mode)



Notes on Microprocessor Interface Write Timing:

1. In Intel mode, a valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In Motorola mode, a valid write cycle is defined as a logical AND of the E signal, the inverted RWB signal and the inverted CSB signal.

3. Microprocessor timing applies to normal mode register accesses only.

4. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

5. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

6. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

17 SPECTRA-155 TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

17.1 Receive Timing

Table 46 - Receive Line Input Interface Timing

Symbol	Description	Min	Max	Units
	RRCLK+/RRCLK- Duty Cycle			
	51.84 or 155.52 MHz (RBYP bit high)	45	55	%
	19.44 or 6.48 MHz (RBYP bit low)	30	70	%
	RRCLK+/RRCLK- Frequency Tolerance†	-20	+20	ppm
	RCLK Duty Cycle (For STS-3/3c (STM-1/AU3/AU4) operation, RCLK is nominally 19.44 MHz. For STS-1 (STM-0/AU3) RCLK is nominally 6.48. RCLK is a divide by eight of the recovered clock or the RRCLK+/- inputs as determined by the RBYP input signal.)	40	60	%
	RXC Duty Cycle (For STS-3/3c (STM-1/AU3/AU4) mode, RXC is the divide by three of the recovered clock or of the RRCLK+/- inputs as determined by the RBYP signal. For STS-1 (STM-0/AU3) mode, RXC is the recovered clock or the RRCLK+/- inputs as determined using the RBYP input signal. RXC is nominally 51.84 MHz.)	45	55	%
tS_{RXD}	RXD+/RXD- Setup time to RRCLK+/RRCLK- (RBYP bit high)	1.5		ns
tH_{RXD}	RXD+/RXD- Hold time to RRCLK+/RRCLK- (RBYP bit high)	2		ns

† The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET/SDH free run accuracy specification.

Figure 81 Receive Line Input Interface Timing

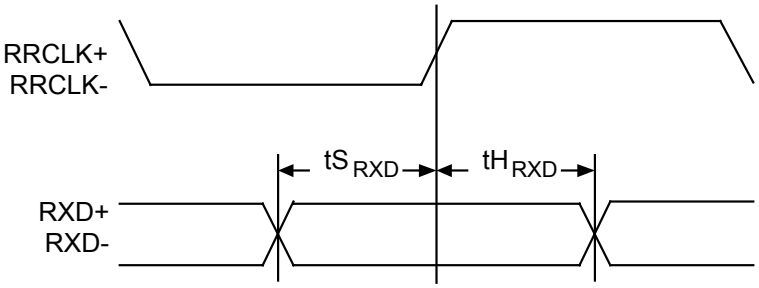


Table 47 - Receive Line Output Timing

Symbol	Description	Min	Max	Units
tP_{RFP}	RCLK High to RFP Valid Prop Delay	-5	15	ns
tP_{RLD}	RLDCLK Low to RLD Valid Prop Delay	-20	20	ns
tP_{RSLD}	RSLDCLK Low to RSLD Valid Prop Delay	-20	20	ns
tP_{ROW}	ROWCLK Low to RSOW, RSUC, RLOW Valid Prop Delay	-250	+250	ns
tP_{ROH}	ROHCLK Low to ROH Valid Prop Delay	-20	20	ns
tP_{RTOH}	RTOHCLK Low to RTOH and RTOHFP Valid Prop Delay	-20	20	ns

Figure 82 - Receive Line Output Timing

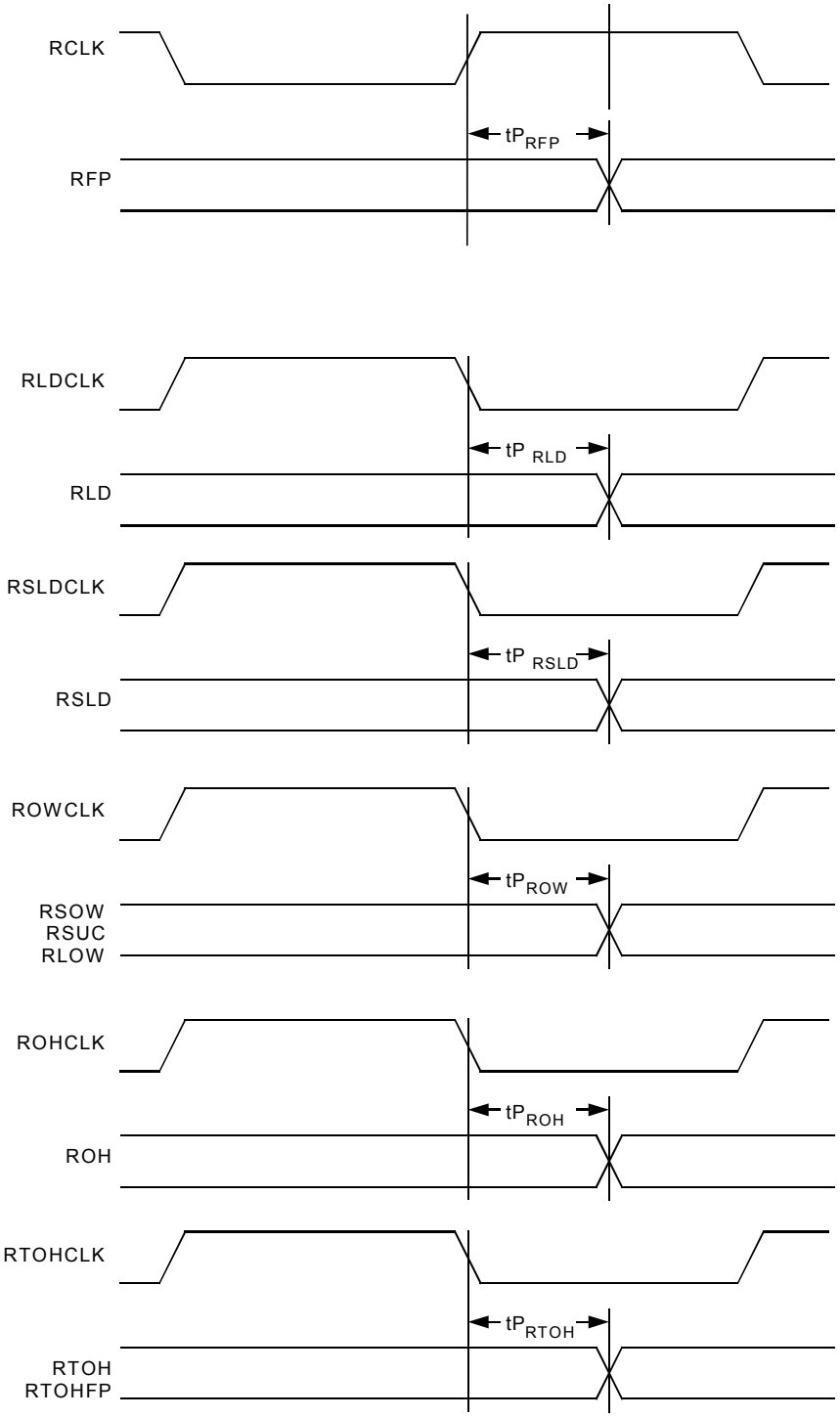


Table 48 - Receive Alarm Signal Output Timing

Symbol	Parameter	Min	Max	Units
tPRALM	RCLK Low to RALM[3:1] Valid	-5	20	ns

Figure 83 - Receive Alarm Signal Output Timing

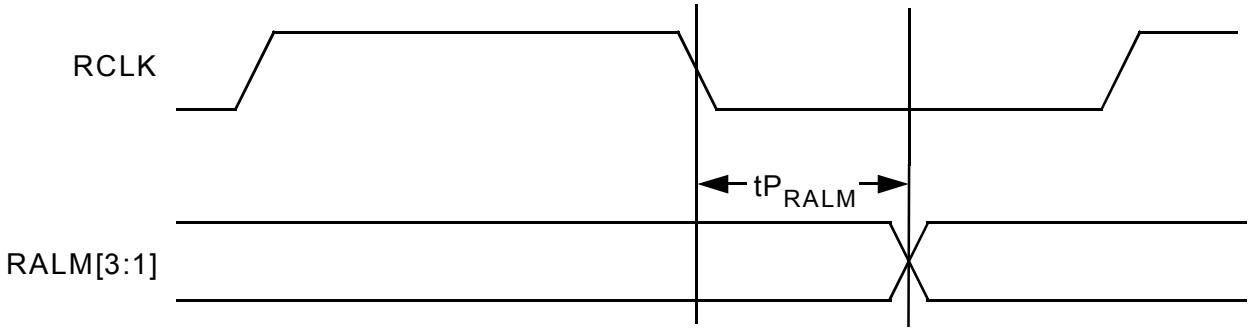


Table 49 - Receive Path Overhead and Alarm Port Output Timing

Symbol	Parameter	Min	Max	Units
tPRPOHFP	RPOHCLK[3:1] Low to RPOHFP[3:1] Valid	-10	40	ns
tPRPOH	RPOHCLK[3:1] Low to RPOH[3:1] Valid	-10	40	ns
tPB3E	RPOHCLK[3:1] Low to B3E[3:1] Valid	-10	40	ns
tPRAD	RPOHCLK[3:1] Low to RAD Valid	-10	40	ns

Figure 84 - Receive Path Overhead and Alarm Port Output Timing

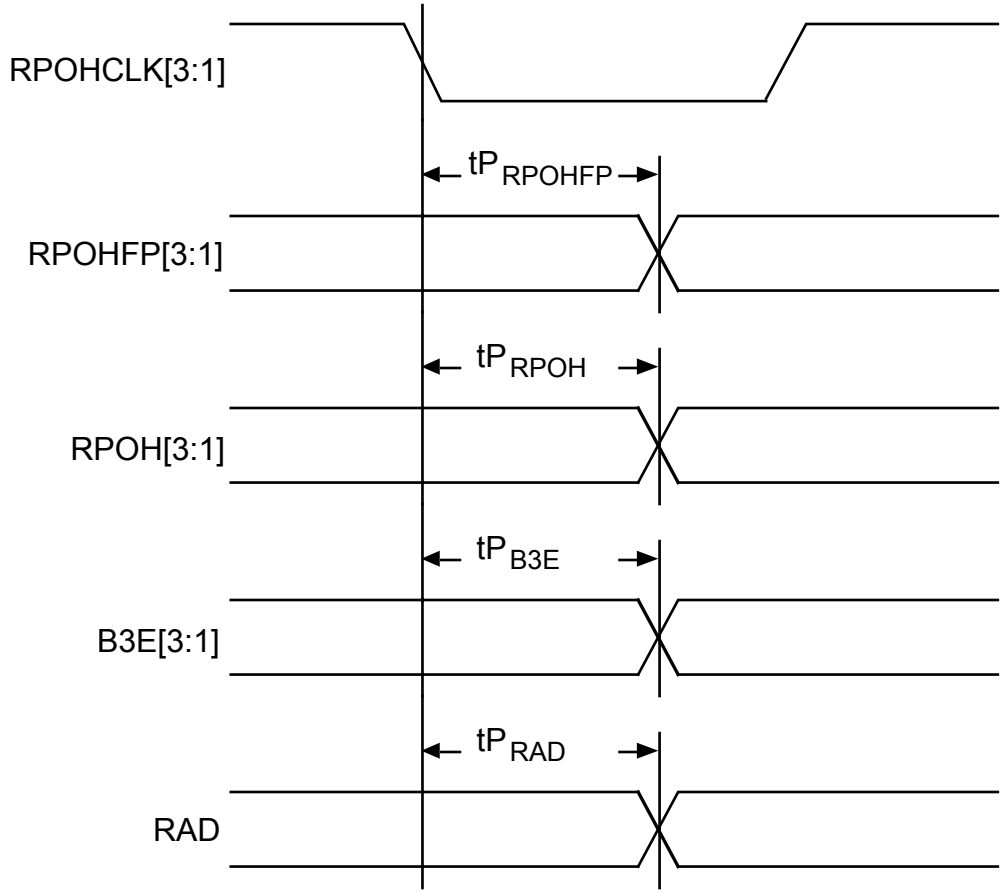


Table 50 - Receive Ring Control Port Output Timing

Symbol	Description	Min	Max	Units
tP_{RRCPFP}	RRCPCLK Low to RRCPFP Valid Prop Delay	-10	10	ns
tP_{RRCPD}	RRCPCLK Low to RRCPDAT Valid Prop Delay	-10	10	ns

Figure 85 - Ring Control Port Output Timing

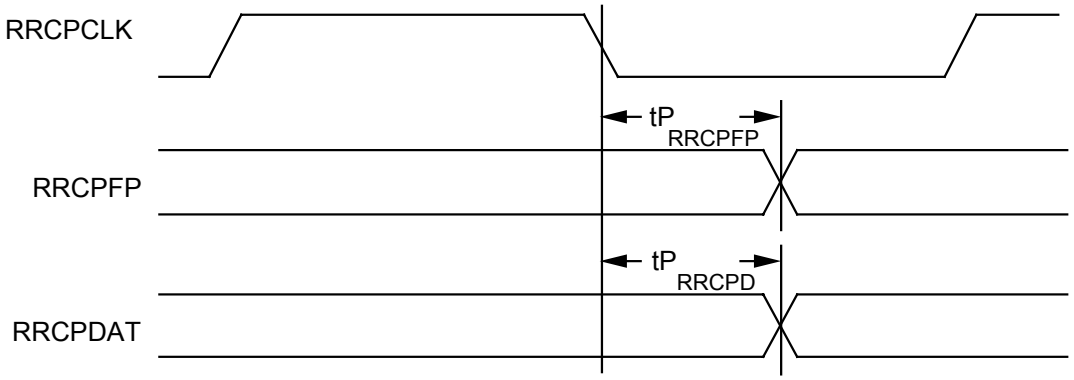


Table 51 - Receive Tandem Connection Input Timing

Symbol	Parameter	Min	Max	Units
tS_{RTCEN}	RTCEN[3:1] Set-up Time	20		ns
tH_{RTCEN}	RTCEN[3:1] Hold Time	20		ns
tS_{RTCOH}	RTCOH[3:1] Set-up Time	20		ns
tH_{RTCOH}	RTCOH[3:1] Hold Time	20		ns

Figure 86 - Receive Tandem Connection Input Timing.

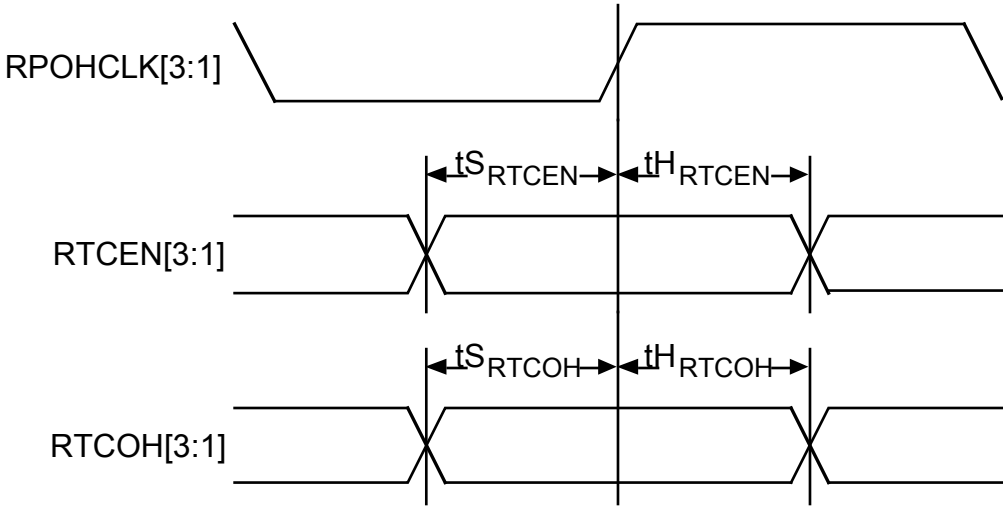


Table 52 - Telecom DROP Bus (Byte and Nibble) Input Timing

Symbol	Parameter	Min	Max	Units
	DCK Freq. (Byte - Nominally 19.44MHz)		20	MHz
	DCK Freq. (Byte - Nominally 6.48MHz)		7	MHz
	DCK Freq. (Nibble - Nominally 38.88 MHz)		40	MHz
	DCK Freq. (Nibble - Nominally 12.96 MHz)		14	MHz
	DCK Duty Cycle	40	60	%
tS_{DFP}	DFP Set-up Time	5		ns
tH_{DFP}	DFP Hold Time	1		ns

Figure 87 - Telecom DROP Bus (Byte and Nibble) Input Timing

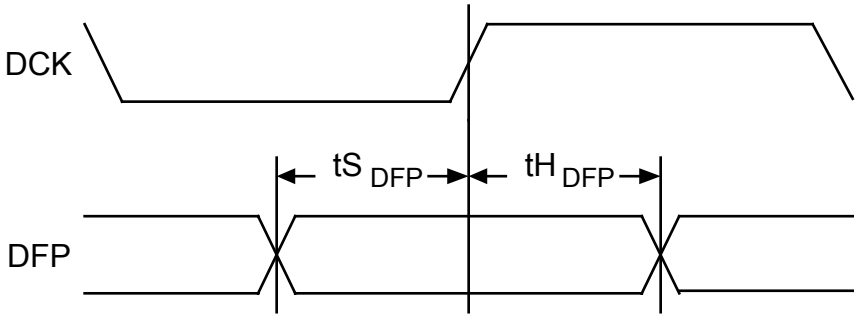


Table 53 - Telecom DROP Bus (Serial) Input Timing

Symbol	Parameter	Min	Max	Units
	SDCK[3:1] Freq. (Nominally 51.84 MHz)		52	MHz
	SDCK[3:1] Duty Cycle	45	55	%
tS_{SDFP}	SDFP[3:1] Set-up Time	5		ns
tH_{SDFP}	SDFP[3:1] Hold Time	1		ns

Figure 88 - Telecom DROP Bus (Serial) Input Timing

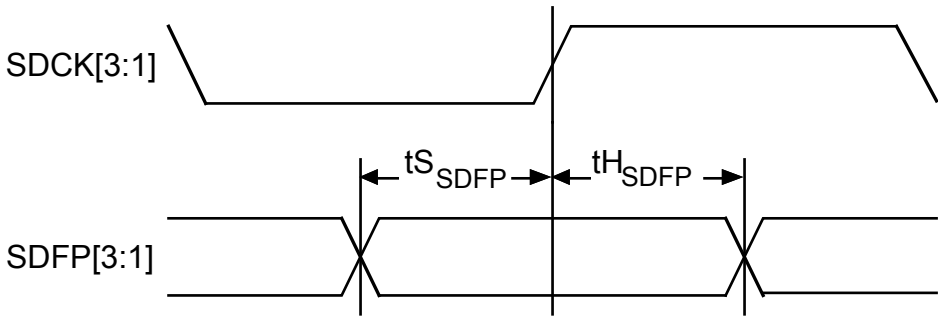


Table 54 - Telecom DROP Bus (Byte and Nibble) Output Timing

Symbol	Parameter	Min	Max	Units
tP_{DD}	DCK High to DD[7:0] Valid	3	20	ns
tP_{DC1}	DCK High to DC1J1V1 Valid	3	20	ns
tP_{DPL}	DCK High to DPL Valid	3	20	ns
tP_{DDP}	DCK High to DDP Valid	3	20	ns

Figure 89 - Telecom DROP Bus (Byte and Nibble) Output Timing

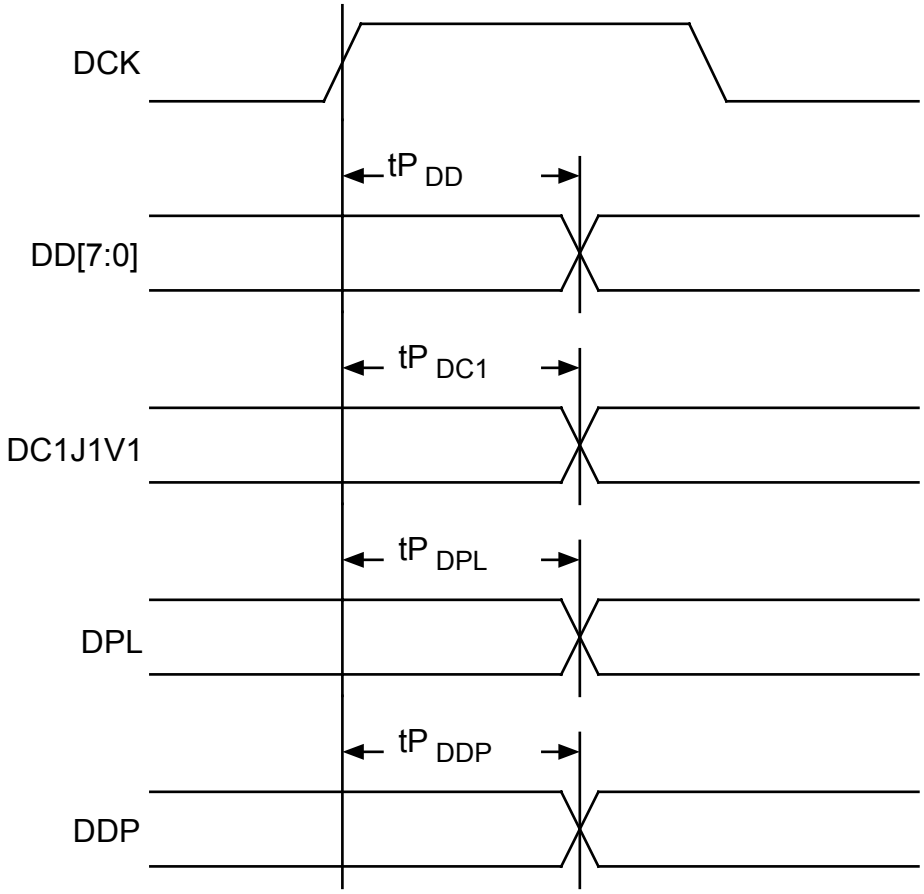


Table 55 - Telecom DROP Bus (Serial) Output Timing

Symbol	Parameter	Min	Max	Units
tP_{SDD}	SDCK[3:1] High to SDD[3:1] Valid (note 5)	1	14	ns
tP_{SDC1}	SDCK[3:1] High to SDC1J1V1[3:1] Valid (note 5)	1	14	ns
tP_{SDPL}	SDCK[3:1] High to SDPL[3:1] Valid (note 5)	1	14	ns

Figure 90 - Telecom DROP Bus (Serial) Output Timing

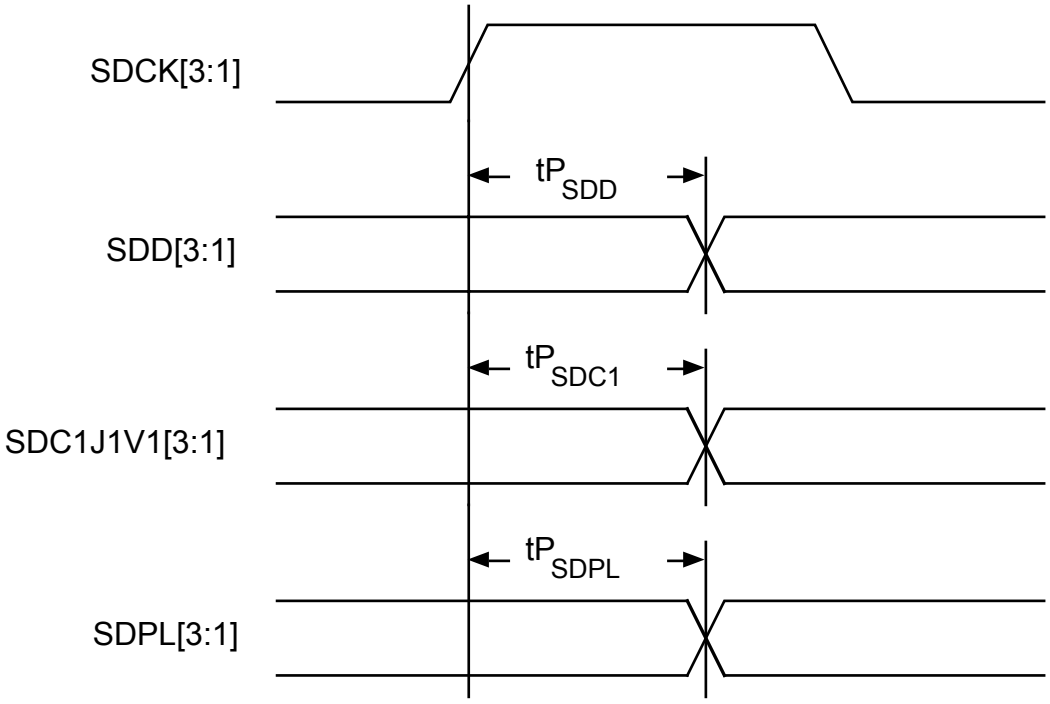


Table 56 - Data Mode Receive Bus (Byte and Nibble) Output Timing

Symbol	Parameter	Min	Max	Units
	DMROCLK Freq. STS-3c (STM-1/AU4) mode, byte data mode (In the absense of pointer movements, DMROCLK is nominally an 18.72 MHz clock generated by gapping a 19.44 MHz clock)			MHz
	DMROCLK Freq. STS-1 (STM-0/AU3) mode, byte data mode (DMROCLK is nominally a 6.192 MHz clock generated by gapping a 6.48 MHz clock when the RDM_FSEN bit in the SPECTRA-155 Data Mode Configuration register is set low. DMROCLK is nomally a 6.048 MHz clock generated by gapping a 6.48 MHz clock when RDM_FSEN is set high)			MHz
	DMROCLK Freq. STS-1 (STM-0/AU3) mode, nibble data mode (In the absense of pointer movements, DMROCLK is nominally an 37.44 MHz clock generated by gapping a 38.88 MHz clock)			MHz
	DMROCLK Freq. STS-1 (STM-0/AU3) mode, byte data mode (DMROCLK is nominally a 12.384 MHz clock generated by gapping a 12.96 MHz clock when the RDM_FSEN bit in the SPECTRA-155 Data Mode Configuration register is set low. DMROCLK is nomally a 12.384 MHz clock generated by gapping a 12.96 MHz clock when RDM_FSEN is set high)			MHz
	DMROCLK Duty Cycle (for consecutive transitions of the gapped clock)	45	55	%
tP_{RDT}	DMROCLK Low to DMRDAT[7:0] Valid	-2	6	ns
tP_{RCK}	DMROCLK High to RCLK Valid (Nibble mode)	-5	3	ns

Figure 91 - Data Mode Receive Bus (Byte and Nibble) Output Timing

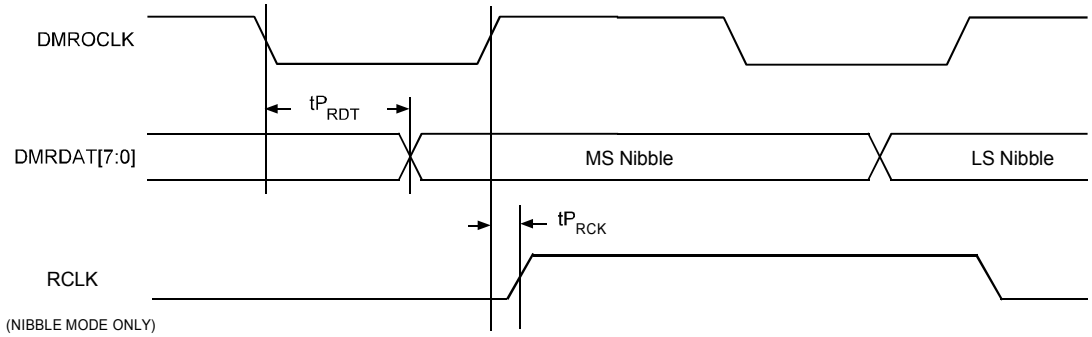


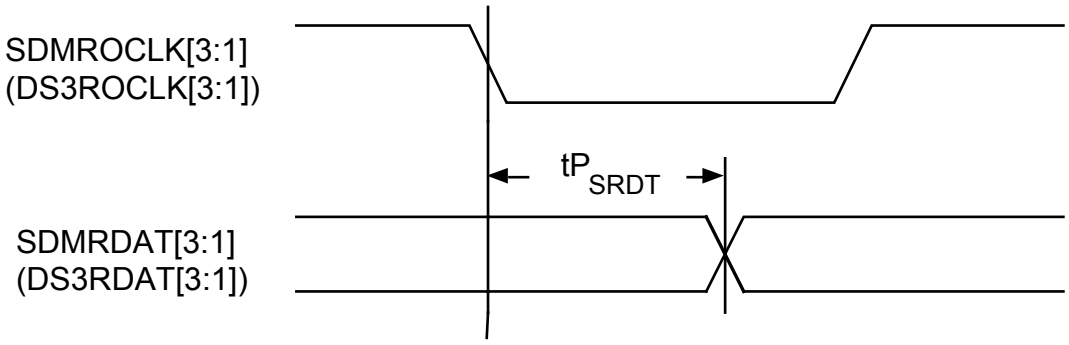
Table 57 - DS3 Receive Bus Input Timing

Symbol	Parameter	Min	Max	Units
	DS3RICLK[3:1] Freq. When used, the DS3RICLK[3:1] inputs must be connected to a clock reference source which has a frequency of 44.928 MHz +/- 100 ppm			
	DS3RICLK[3:1] Duty Cycle	40	60	%

Table 58 - DS3 and Data Mode Receive Bus (Serial) Output Timing

Symbol	Parameter	Min	Max	Units
	DS3ROCLK[3:1] (DS3ROCLK is nominally 44.736 MHz and is generated by gapping DS3RICLK when the DS3_SEL52 bit in the SPECTRA-155 Data Mode Configuration register is set low. DS3ROCLK is generated by gapping an internal 51.84 MHz recovered line clock when the DS3_SEL52 bit is set high)			MHz
	DS3ROCLK[3:1] Duty Cycle (for consecutive transitions of the gapped clock)	40	60	%
tP_{SRDT}	DS3ROCLK[3:1] Low to DS3RDAT[3:1] Valid	-6	2	ns
	SDMROCLK[3:1] (When GAPFS bit in the corresponding D3MD Control register is set low, SDMROCLK is nominally a 49.536 MHz clock generated by gapping a 51.84 MHz clock. When GAPFS is set high, SDMROCLK is nominally a 48.384 MHz clock.)			MHz
	SDMROCLK[3:1] Duty Cycle (for consecutive transitions of the gapped clock)	40	60	%
tP_{SRDT}	SDMROCLK[3:1] Low to SDMRDAT[3:1] Valid	-6	2	ns

Figure 92 - DS3 and Data Mode Receive Bus (Serial) Output Timing



17.2 Transmit Timing

Table 59 - GENERATED BUS Input Timing

Symbol	Parameter	Min	Max	Units
tS_{GFP}	GFP Set-up Time	5		ns
tH_{GFP}	GFP Hold Time	1		ns
tS_{GMFP}	GMFP Set-up Time	5		ns
tH_{GMFP}	GMFP Hold Time	1		ns

Figure 93 - GENERATED Bus Input Timing

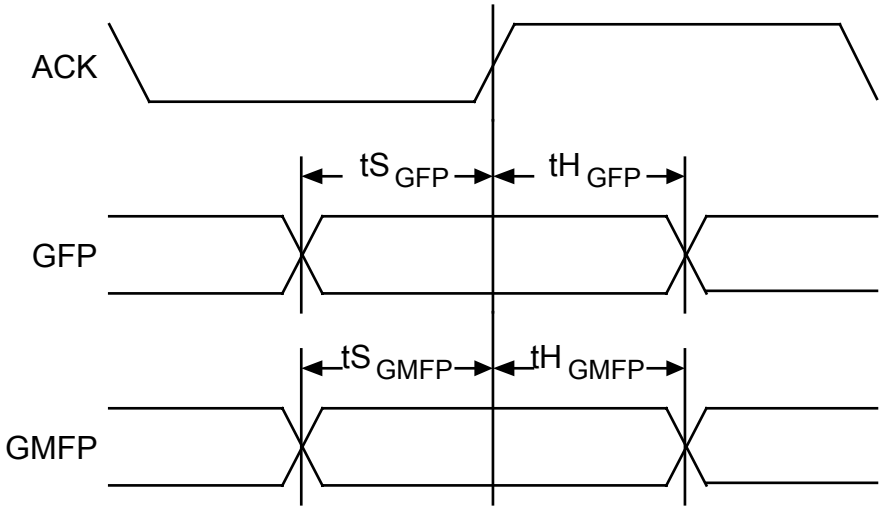


Table 60 - GENERATED Bus (Byte and Nibble) Output Timing

Symbol	Parameter	Min	Max	Units
tP_{GD}	ACK High to GD[1:0] Valid	4	20	ns
tP_{GC1}	ACK High to GC1J1V1 Valid	4	20	ns
tP_{GPL}	ACK High to GPL Valid	4	20	ns
tP_{GDP}	ACK High to GDP Valid	4	20	ns

Figure 94 - GENERATED Bus (Byte and Nibble) Output Timing

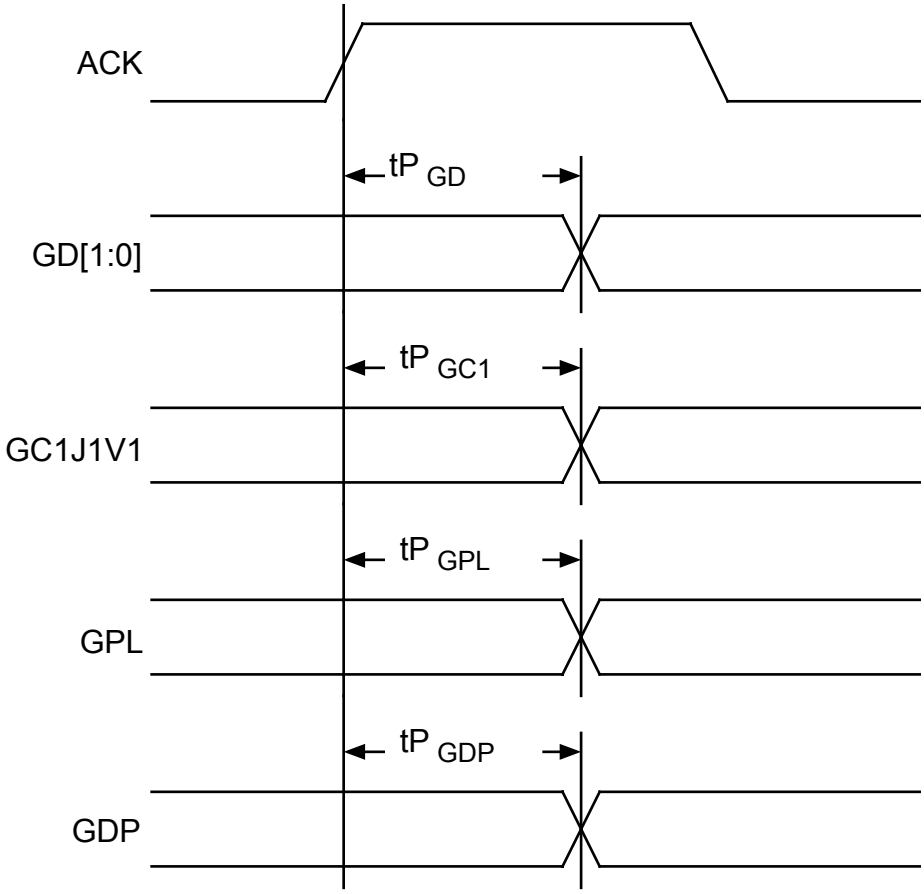


Table 61 - Telecom ADD Bus (Byte and Nibble) Input Timing

Symbol	Parameter	Min	Max	Units
	ACK Freq. STS-3 (STM-1) Mode, Byte Telecom Mode Nominally 19.44 MHz		20	MHz
	ACK Freq. STS-1 (STM-0) Mode, Byte Telecom Mode Nominally 6.48 MHz		7	MHz
	ACK Freq. STS-3 (STM-1) Mode, Nibble Telecom Mode Nominally 38.88 MHz		40	MHz
	ACK Freq. STS-1 (STM-0) Mode, Nibble Telecom Mode Nominally 12.96 MHz		14	MHz
	ACK Duty Cycle	40	60	%
tS_{AD}	AD[7:0] Set-up Time	5		ns
tH_{AD}	AD[7:0] Hold Time	1		ns
tS_{AC1}	AC1J1V1 Set-up Time	5		ns
tH_{AC1}	AC1J1V1 Hold Time	1		ns
tS_{APL}	APL Set-up Time	5		ns
tH_{APL}	APL Hold Time	1		ns
tS_{ADP}	ADP Set-up Time	5		ns
tH_{ADP}	ADP Hold Time	1		ns

Figure 95 - Telecom ADD Bus (Byte and Nibble) Input Timing

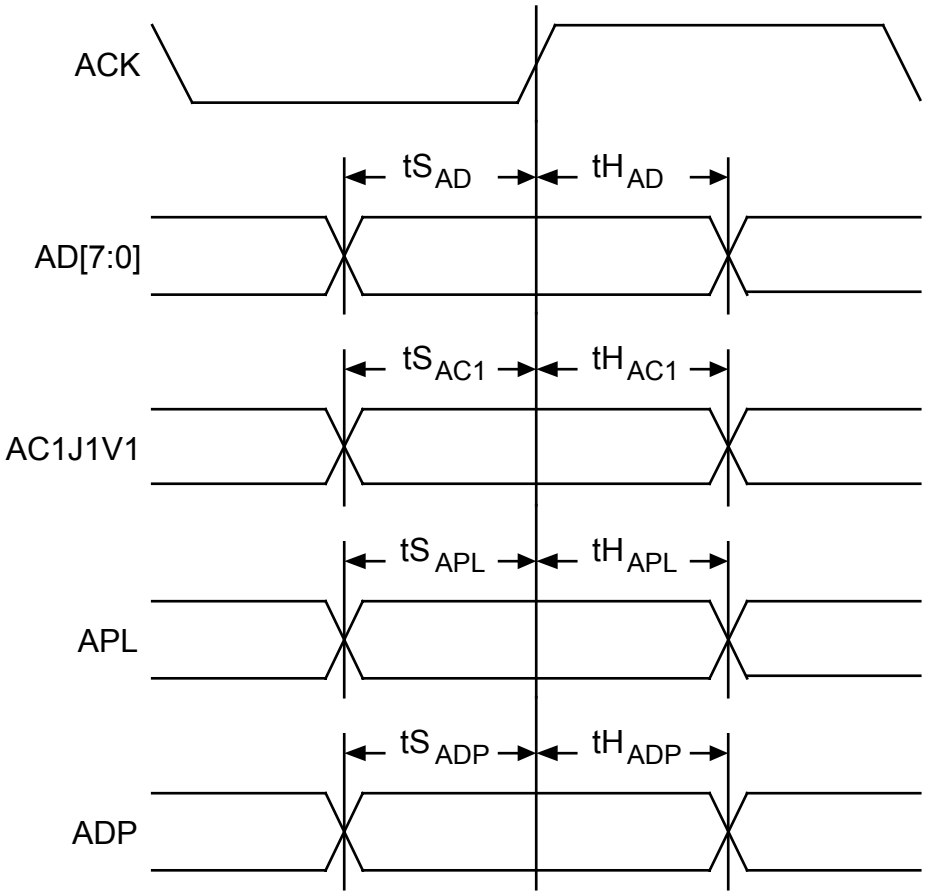


Table 62 - Telecom ADD Bus (Serial) Input Timing

Symbol	Parameter	Min	Max	Units
	SACK[3:1] Freq. (Nominally 51.84 MHz)		52	MHz
	SACK[3:1] Duty Cycle	40	60	%
tS_{SAD}	SAD[3:1] Set-up Time	5		ns
tH_{SAD}	SAD[3:1] Hold Time	1		ns
tS_{SAC1}	SAC1J1V1[3:1] Set-up Time	5		ns
tH_{SAC1}	SAC1J1V1[3:1] Hold Time	1		ns
tS_{SAPL}	SAPL[3:1] Set-up Time	5		ns
tH_{SAPL}	SAPL[3:1] Hold Time	1		ns

Figure 96 - Telecom ADD Bus (Serial) Input Timing

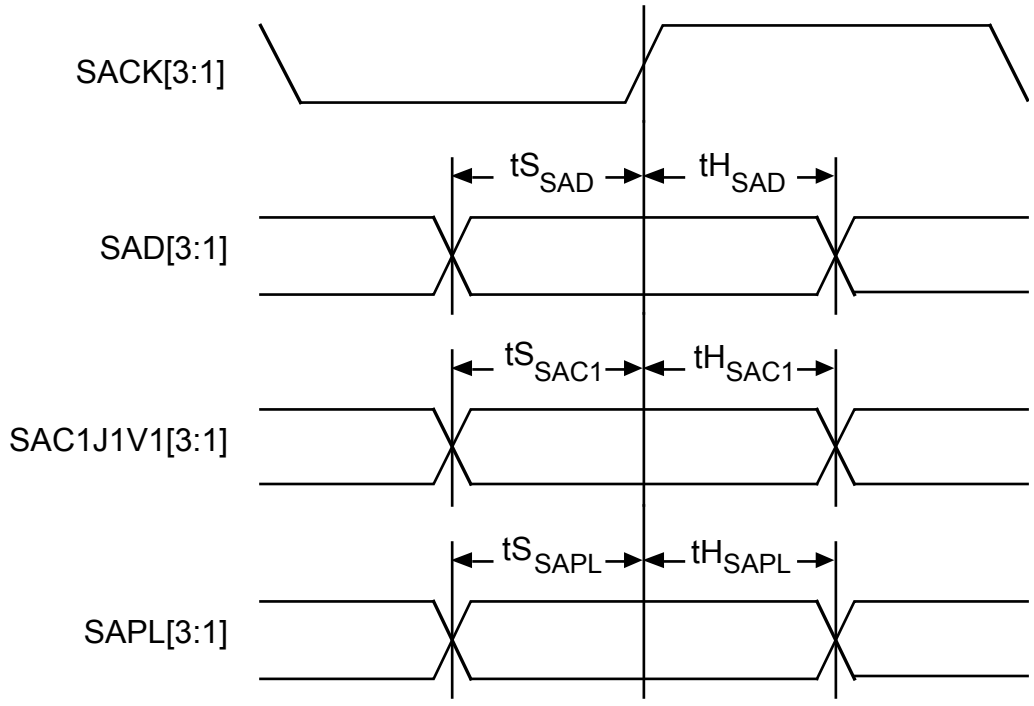


Table 63 - Data Mode Transmit Bus (Byte and Nibble) Input Timing

Symbol	Parameter	Min	Max	Units
	DMTICLK Freq. (must be connected to DMTOCLK)			MHz
	DMTICLK Duty Cycle	40	60	%
tS_{TDT}	DMTDAT[7:0], DMTMSN Set-up Time	5		ns
tH_{TDT}	DMTDAT[7:0], DMTMSN Hold Time	1		ns

Figure 97 - Data Mode Transmit Bus (Byte and Nibble) Input Timing

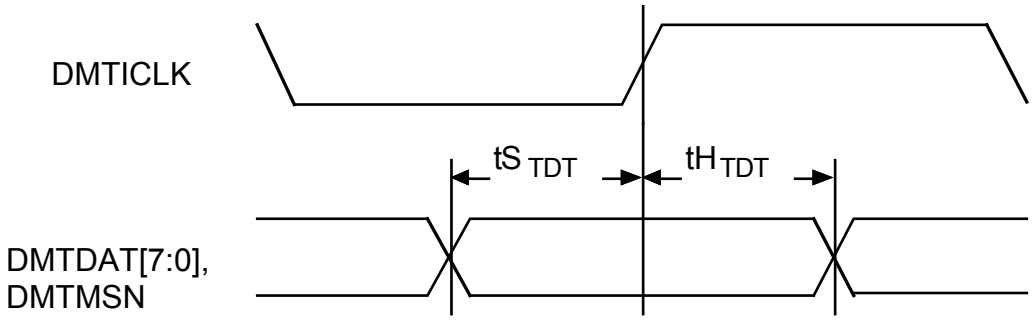


Table 64 - Data Mode Transmit Bus Nibble Output Timing

Symbol	Parameter	Min	Max	Units
tP_{TCLK}	DMTOCLK falling to TCLK valid	-5	5	ns

Figure 98 - Data Mode Transmit Bus Nibble Output Timing

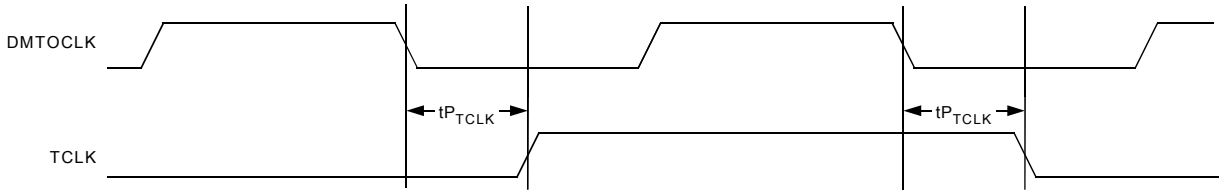


Table 65 - DS3 and Data Mode Transmit Bus (Serial) Input Timing

Symbol	Parameter	Min	Max	Units
	DS3TICLK[3:1] Freq. (Nominally 44.736 MHz)		45	MHz
	DS3TICLK[3:1] Duty Cycle	40	60	%
tS_{STDT}	DS3TDAT[3:1] Set-up Time	2		ns
tH_{STDT}	DS3TDAT[3:1] Hold Time	2		ns
	SDMTICLK[3:1] Freq. (Nominally 49.536 MHz) SDMTICLK[3:1] must be tied to the associated SDMTOCLK[3:1]			MHz
	SDMTICLK[3:1] Duty Cycle	40	60	%
tS_{STDT}	SDMTDAT[3:1] Set-up Time	2		ns
tH_{STDT}	SDMTDAT[3:1] Hold Time	2		ns

Figure 99 - DS3 and Data Mode Transmit Bus (Serial) Input Timing

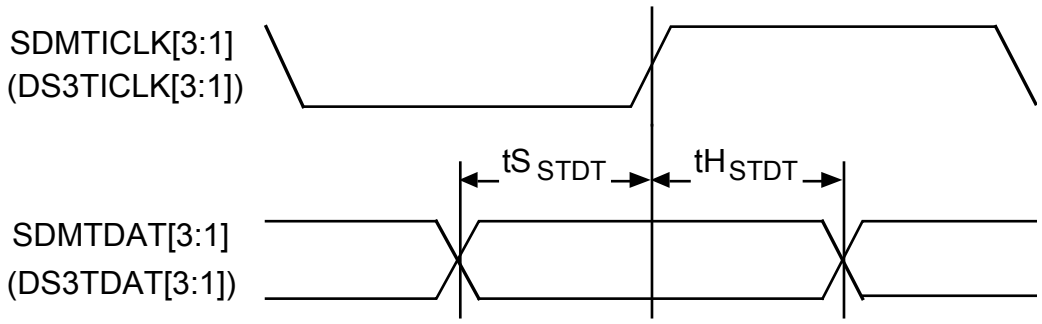


Table 66 - Transmit Path Overhead Input Timing

Symbol	Parameter	Min	Max	Units
tS_{TPOH}	TPOH[3:1] Set-up Time	20		ns
tH_{TPOH}	TPOH[3:1] Hold Time	20		ns
tS_{TPEN}	TPOHEN[3:1] Set-up Time	20		ns
tH_{TPEN}	TPOHEN[3:1] Hold Time	20		ns

Figure 100 - Transmit Path Overhead Input Timing

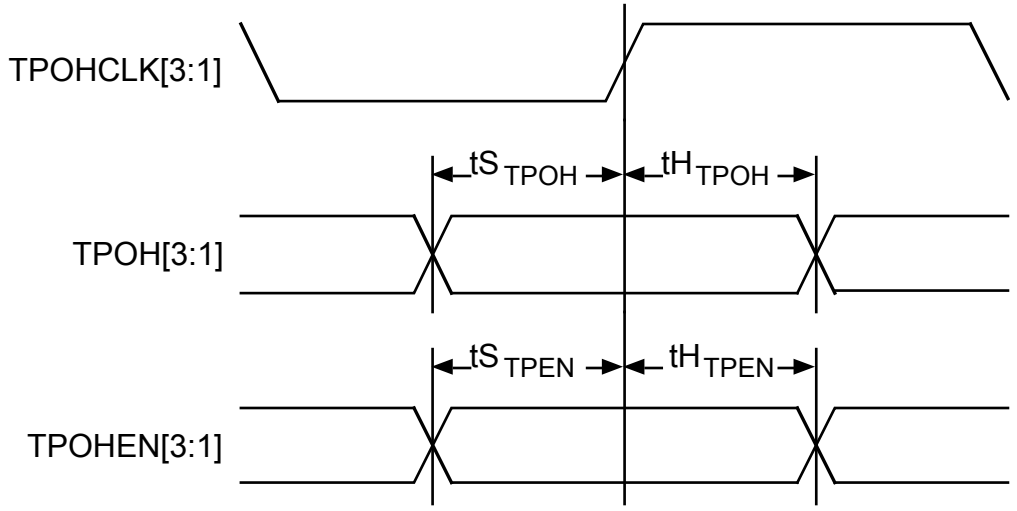


Table 67 - Transmit Alarm Port Input Timing

Symbol	Parameter	Min	Max	Units
tS_{TAD}	TAD Set-up Time	20		ns
tH_{TAD}	TAD Hold Time	20		ns
tS_{TAFP}	TAFP Set-up Time	20		ns
tH_{TAFP}	TAFP Hold Time	20		ns

Figure 101 - Transmit Alarm Port Input Timing

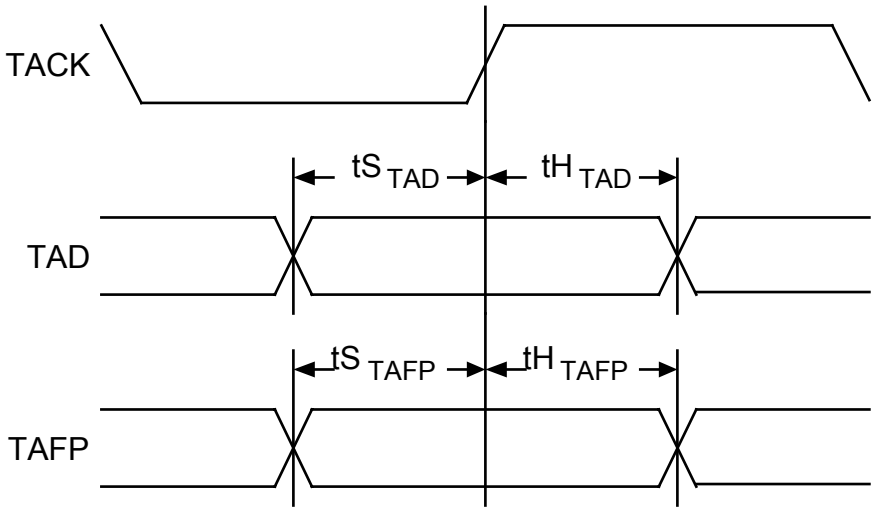


Table 68 - Transmit Transport Overhead Input Timing

Symbol	Description	Min	Max	Units
	TCLK Duty Cycle (For STS-3/3c (STM-1/AU3/AU4) operation, TCLK is nominally 19.44 MHz. For STS-1 (STM-0/AU3) TCLK is nominally 6.48. TCLK is a divide by eight of the synthesized clock or the TRCLK+/- inputs as determined using the TBYP input signal.)	40	60	%
tS_{TLD}	TLD Set-up Time to TLDCLK	30		ns
tH_{TLD}	TLD Hold Time to TLDCLK	0		ns
tS_{TSLD}	TSLD Set-up Time to TSLDCLK	30		ns
tH_{TSLD}	TSLD Hold Time to TSLDCLK	0		ns
tS_{TOW}	TSOW, TLOW, TSUC Set-up Time to TOWCLK	30		ns
tH_{TOW}	TSOW, TLOW, TSUC Hold Time to TOWCLK	0		ns
tS_{TOH}	TOH Set-up Time to TOHCLK	30		ns
tH_{TOH}	TOH Hold Time to TOHCLK	0		ns
tS_{TTOH}	TTOH, TTOHEN Set-up Time to TTOHCLK	30		ns
tH_{TTOH}	TTOH, TTOHEN Hold Time to TTOHCLK	0		ns

Figure 102 - Transmit Transport Overhead Input Timing

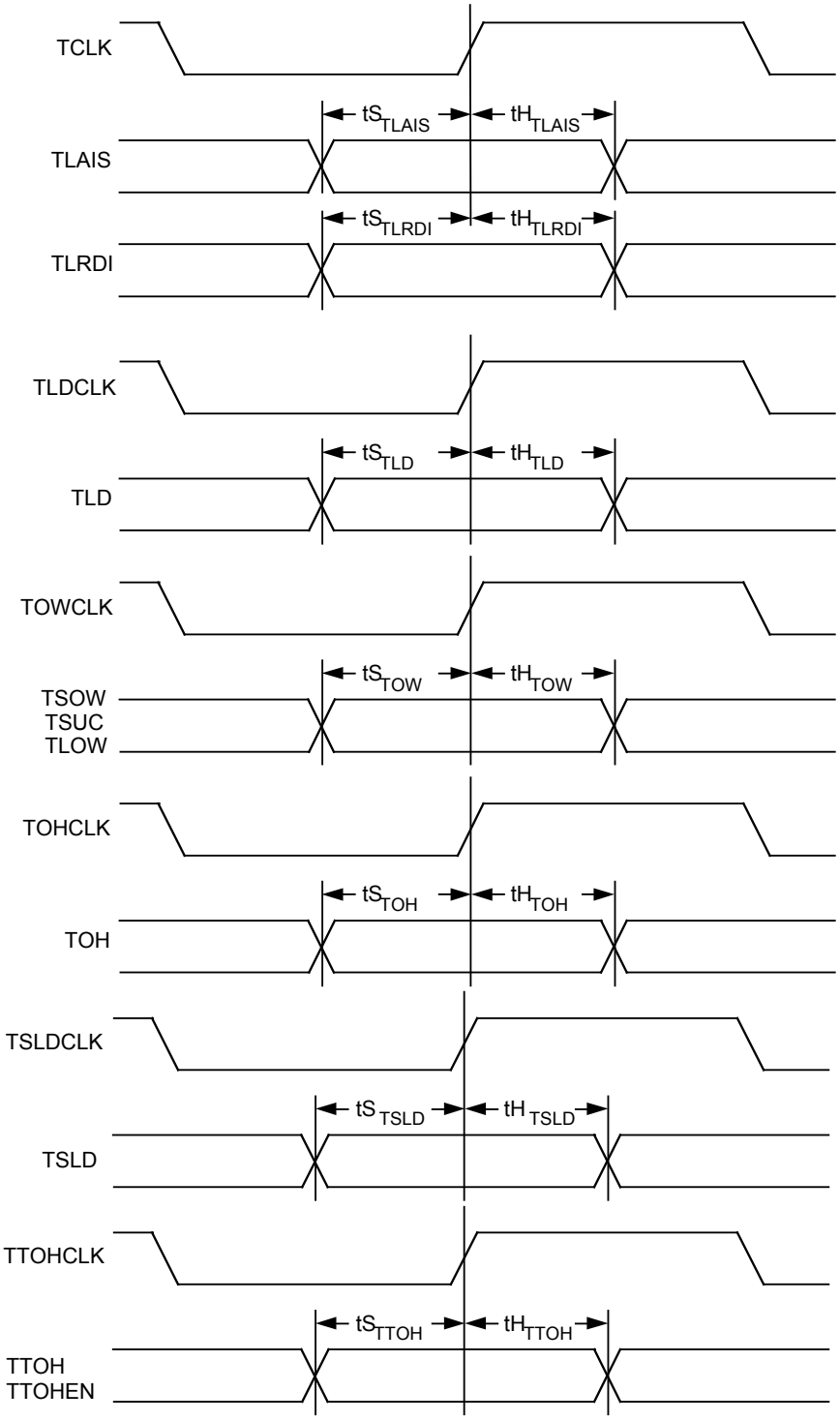


Table 69 - Transmit Ring Control Port Input Timing

Symbol	Description	Min	Max	Units
	TRCPCLK Frequency (nominally 3.24 MHz)		3.4	MHz
	TRCPCLK Duty Cycle	33	67	%
tS_{TRCPFP}	TRCPFP Set-up Time to TRCPCLK	10		ns
tH_{TRCPFP}	TRCPFP Hold Time to TRCPCLK	10		ns
tS_{TRCPD}	TRCPDAT Set-up Time to TRCPCLK	10		ns
tH_{TRCPD}	TRCPDAT Hold Time to TRCPCLK	10		ns

Figure 103 - Transmit Ring Control Port Input Timing

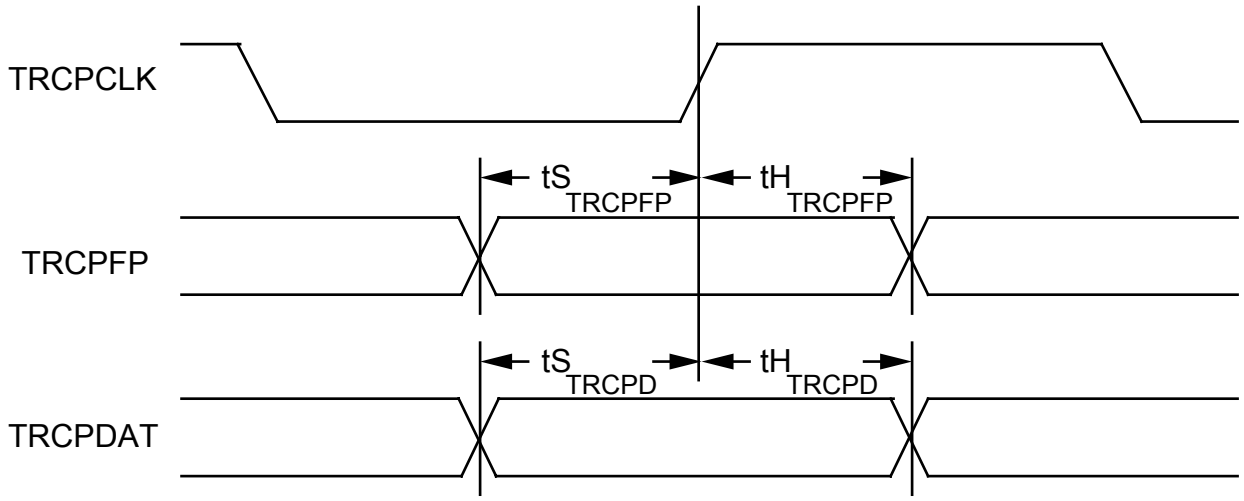


Table 70 - Transmit Overhead Output Timing

Symbol	Description	Min	Max	Units
tP_{TFP}	TCLK High to TFP Valid Prop Delay	0.5	20	ns
tP_{TTOHFP}	TTOHCLK Low to TTOHFP Valid Prop Delay	-20	20	ns
tP_{TPOHFP}	TPOHCLK[3:1] Low to TPOHFP[3:1] Valid	-10	40	ns

Figure 104 - Transmit Overhead Output Timing

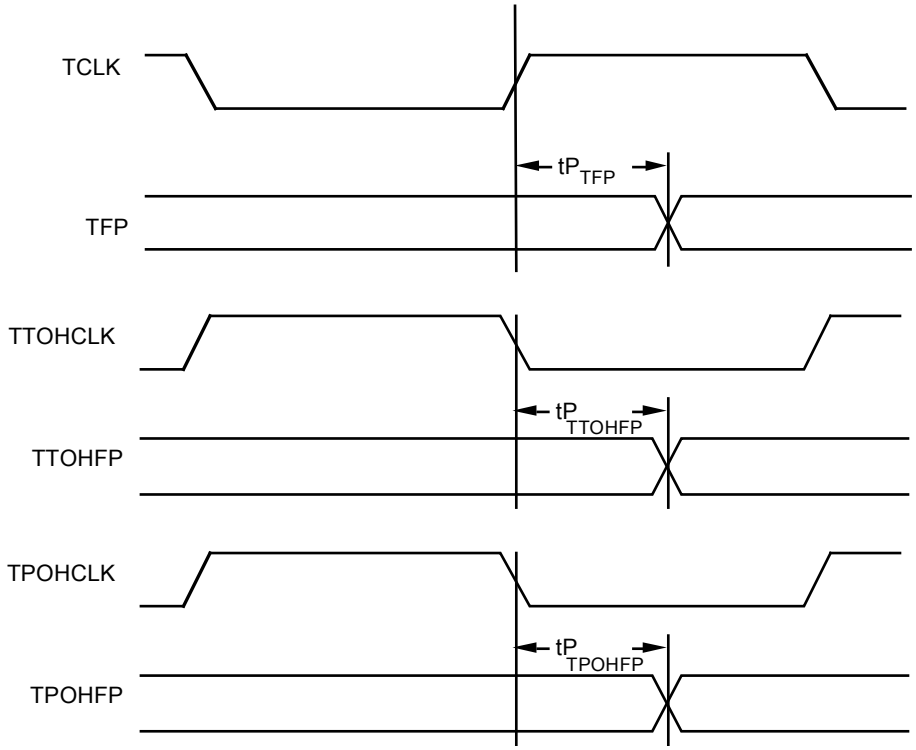


Table 71 - Line Side Transmit Interface Timing

Symbol	Description	Min	Max	Units
	TRCLK+/TRCLK- Duty Cycle			
	51.84 or 155.52 MHz (TBYP high)	45	55	%
	19.44 or 6.48 MHz (TBYP low)	30	70	
	TRCLK+/TRCLK- Frequency Tolerance †	-20	+20	ppm
$tP_{TXDdiff}$	TXC Low to TXD+/TXD- Valid	-3	3	ns

† The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET/SDH free run accuracy specification.

Figure 105 - Line Side Transmit Interface Timing

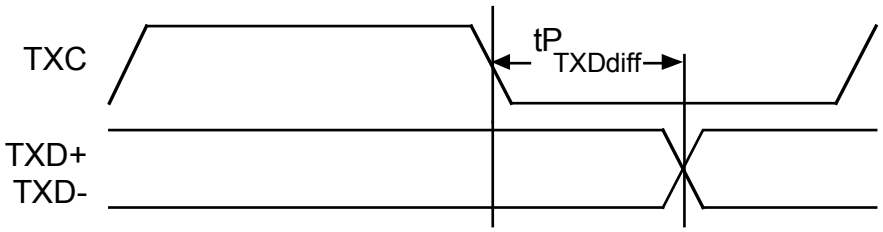
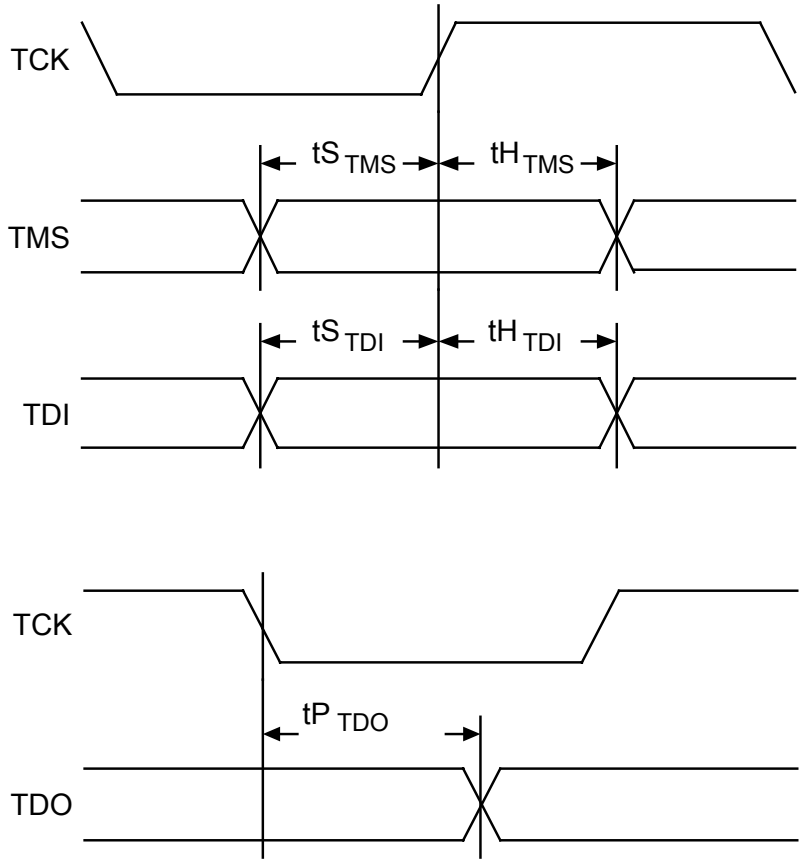


Table 72 - JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Figure 106 - JTAG Port Interface Timing



Notes on Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

4. All output propagation delays are specified with a 50 pF load on the outputs except where indicated.

18 ORDERING AND THERMAL INFORMATION

Table 73 - Ordering information.

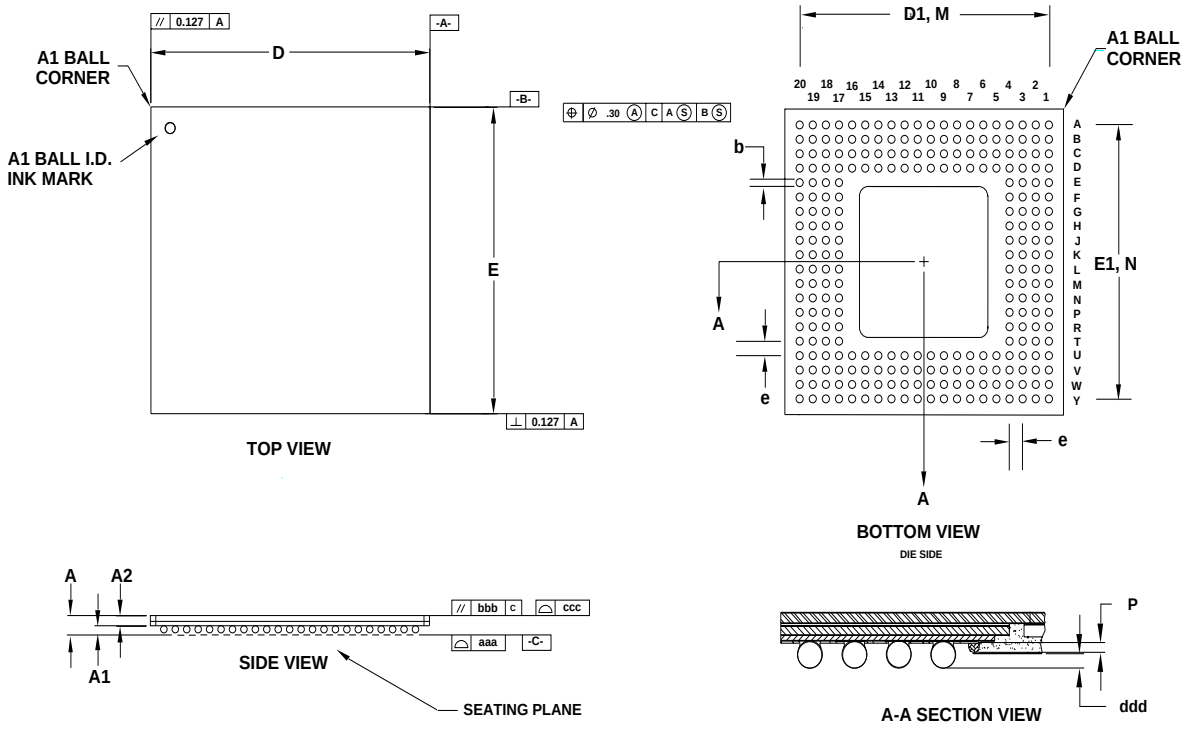
PART NO.	DESCRIPTION
PM5342-BI	256 Super Ball Grid Array (SBGA)

Table 74 - Thermal information.

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5342-BI	-40°C to 85°C	24 °C/W	8 °C/W

19 MECHANICAL INFORMATION

Figure 107 - 256 Pin Super Ball Grid Array (B Suffix):



Notes: 1) ALL DIMENSIONS IN MILLIMETER.

2) DIMENSION aaa DENOTES COPLANARITY

3) DIMENSION bbb DENOTES PARALLEL

4) DIMENSION ccc DENOTES FLATNESS

PACKAGE TYPE: 256 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 27 x 27 x 1.45 MM															
Dim.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	P
Min.	1.32	0.56	0.76	26.90	24.03	26.90	24.03			0.60				0.15	0.20
Nom.	1.45	0.63	0.82	27.00	24.13	27.00	24.13	20x20	1.27	0.75				0.33	0.30
Max.	1.58	0.70	0.88	27.10	24.23	27.10	24.23			0.90	0.15	0.15	0.20	0.50	0.35

NOTES

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