# PM4341A

# T1XC

# SINGLE DSX-1 TRANSCEIVER DEVICE

# DATA SHEET

**ISSUE 7: JUNE 1998**

## PUBLIC REVISION HISTORY

| Issue No. | Issue Date | Details of Change |
|---|---|---|
| 7 | June 1998 | Data Sheet Reformatted — No Change in Technical Content.<br>Generated R7 datasheet from PMC-891007, R11 |
| 6 | July 1996 | Release of Issue 10 of T1XC Eng Doc |
| 5 | | |
| 4 | | |
| 3 | February 1996 | Release of Issue 9 of T1XC Eng Doc |
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| 1 | | |

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# 1 FEATURES

- Integrates a full-featured T1 framer and line interface in a single device with analog circuitry for receiving and transmitting DSX-1 compatible signals and digital circuitry for terminating the duplex DS-1 signal.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power CMOS technology
- Available in either a 68 pin PLCC package, or a high density (14 by 14mm) 80 pin PQFP package.

**The receiver section:**

- Provides analog circuitry for receiving a DSX-1 signal up to 655 feet from the cross-connect. Direct digital inputs are also provided to allow for by-passing the analog front-end.
- Recovers clock and data using a digital phase locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be by-passed.
- Accepts dual rail or single rail digital PCM inputs.
- Supports B8ZS or AMI line code.
- Accepts gapped data streams to support higher rate demultiplexing.
- Frames to SF, ESF, T1DM (DDS), and SLC®96 format DS1 signals.
- Provides loss of signal detection, and red, yellow, and AIS alarm detection. Red, yellow, and AIS alarms are integrated as per industry specifications.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window.
- Provides programmable in-band loopback code detection.
- Supports line and path performance monitoring according to AT&T and ANSI specifications. Accumulators are provided for counting:
    - ESF CRC-6 errors to 333 per second;
    - Framing bit errors to 31 per second;
    - Line code violations to 4095 per second; and
    - Loss of frame or change of frame alignment events to 7 per second.

- Provides ESF bit-oriented code detection, and an HDLC/LAPD interface for terminating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Extracts the data link in ESF, T1DM (DDS) or SLC®96 modes. Extracts the D-channel for Primary Rate interfaces.
- Provides a two-frame elastic store buffer for jitter and wander attenuation that performs controlled slips and indicates slip occurrence and direction.
- Provides robbed bit signalling extraction, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and 2 superframes of signalling debounce on a per-channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signalling conditioning on all channels or on selected channels.
- Optionally provides dual rail digital PCM output signals to allow BPV transparency. Also supports unframed mode.
- Supports transfer of received PCM and signalling data to 1.544 Mbit/s backplane buses or to 2.048 Mbit/s backplane buses.

**The transmitter section:**

- Supports transfer of transmitted PCM and signalling data from 1.544 Mbit/s or 2.048 Mbit/s backplane buses.
- Formats data to SF, ESF, T1DM (DDS), and SLC®96 format DS1 signals.
- Optionally accepts dual rail digital PCM inputs to allow BPV transparency. Also supports unframed mode and framing bit, CRC, or data link by-pass.
- Provides signalling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signalling conditioning on all channels or on selected channels.
- Provides minimum ones density through Bell (bit 7), GTE or DDS zero code suppression on a per channel basis.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window or optionally stuffs ones to maintain minimum ones density.
- Allows insertion of framed or unframed in-band loopback code sequences.

- Allows insertion of a data link in ESF, T1DM (DDS) or SLC®96 modes. Allows insertion of the D- channel for Primary Rate interfaces.
- Supports transmission of the alarm indication signal (AIS) or the yellow alarm signal in all formats.
- Provides ESF bit-oriented code generation and an HDLC/LAPD interface for generating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.
- Supports B8ZS or AMI line code.
- Provides analog circuitry for transmitting a DSX-1 signal. Digitally programmable line build out is provided. Direct digital outputs are also provided.
- Provides dual rail or single rail digital PCM output signals.

## 1.1 APPLICATIONS

- T1 Channel Service Units (CSU) and Data Service Units (DSU)
- T1 Channel Banks (CH BANK) and Multiplexers (CPE MUX)
- Digital Private Branch Exchanges (DPBX)
- Digital Access and Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- T1 Frame Relay Interfaces
- T1 ATM Interfaces
- ISDN Primary Rate Interfaces (PRI)
- SONET Add/Drop Multiplexers (ADM)
- Test Equipment

## 2 REFERENCES

1. American National Standard for Telecommunications, ANSI T1.102-1992 - "Digital Hierarchy - Electrical Interfaces."

2. American National Standard for Telecommunications - Digital Hierarchy - Formats Specification, ANSI T1.107-1991

3. American National Standard for Telecommunications - Carrier to Customer Installation - DS1 Metallic Interface Specification, ANSI T1.403-1989

4. American National Standard for Telecommunications - Integrated Services Digital Network (ISDN) Primary Rate- Customer Installation Metallic Interfaces Layer 1 Specification, ANSI T1.408-1990

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6. Bell Communications Research - DS1 Rate Digital Service Monitoring Unit Functional Specification, TA-TSY-000147, Issue 1, October, 1987.

7. Bell Communications Research - Digital Cross-Connect System Requirements And Objectives, TR-TSY-000170, Issue 1, November 1985.

8. Bell Communications Research - Alarm Indication Signal Requirements and Objectives, TR-TSY-000191 Issue 1, May 1986.

9. Bell Communications Research - The Extended Superframe Format Interface Specification, TR-TSY-000194 Issue 1, December 1987. (Replaced by TR-TSY-000499)

10. Bell Communications Research - Digital Data System (DDS) - T1 Data Multiplexor (T1DM), TA-TSY-000278, Issue 1, November 1985.

11. Bell Communications Research - Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, TR-TSY-000303, Issue 1, September, 1986.

12. Bell Communications Research - Functional Criteria for the DS1 Interface Connector, TR-TSY-000312, Issue 1, March, 1988.

13. Bell Communications Research - Transport Systems Generic Requirements (TSGR): Common Requirement, TR-TSY-000499, Issue 3, December, 1989.

14. AT&T - Digital Channel Bank - Requirements And Objectives, PUB43801, November 1982.

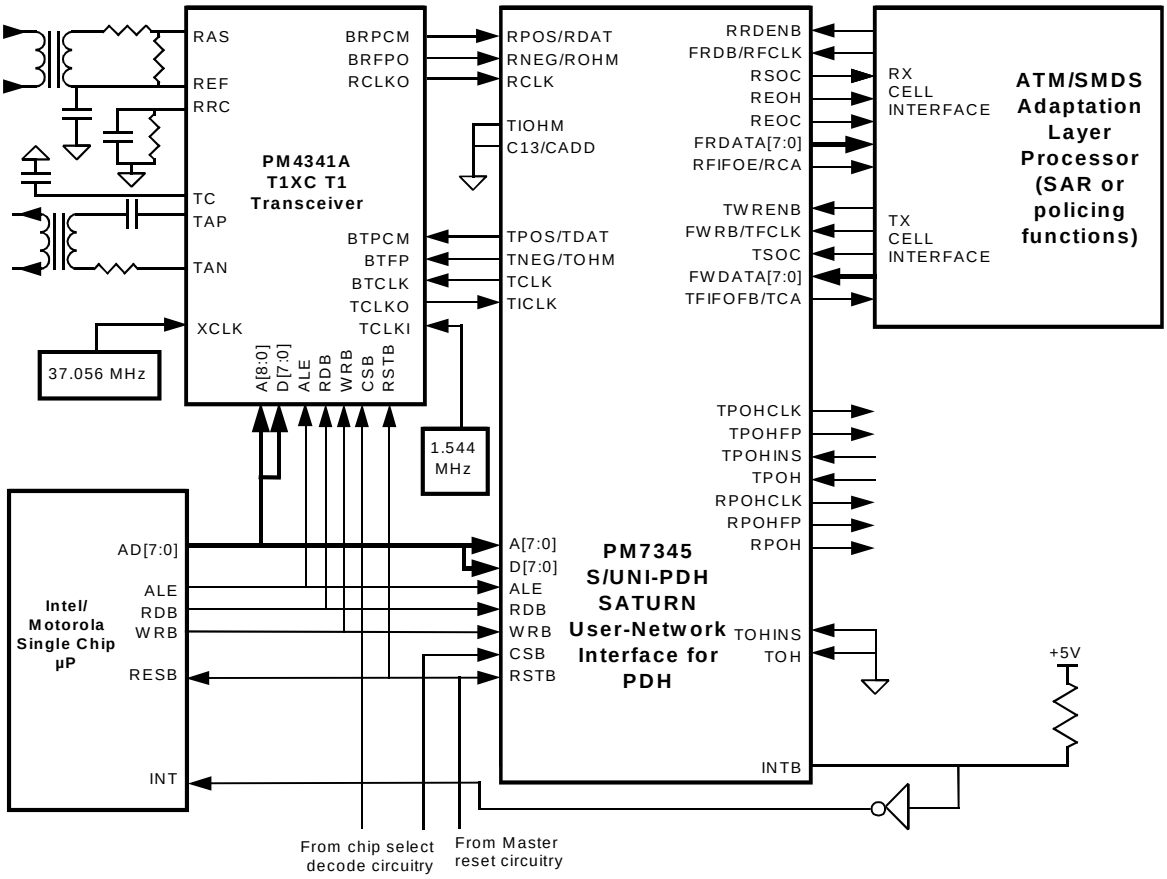
15. AT&T - Digital Channel Bank - Requirements And Objectives - Addendum 1, PUB43801A, January 1985.

16. AT&T - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, PUB54016, October 1984.

17. AT&T, TR 62411 - Accunet T1.5 - "Service Description and Interface Specification" December, 1990.

# 3 APPLICATION EXAMPLES

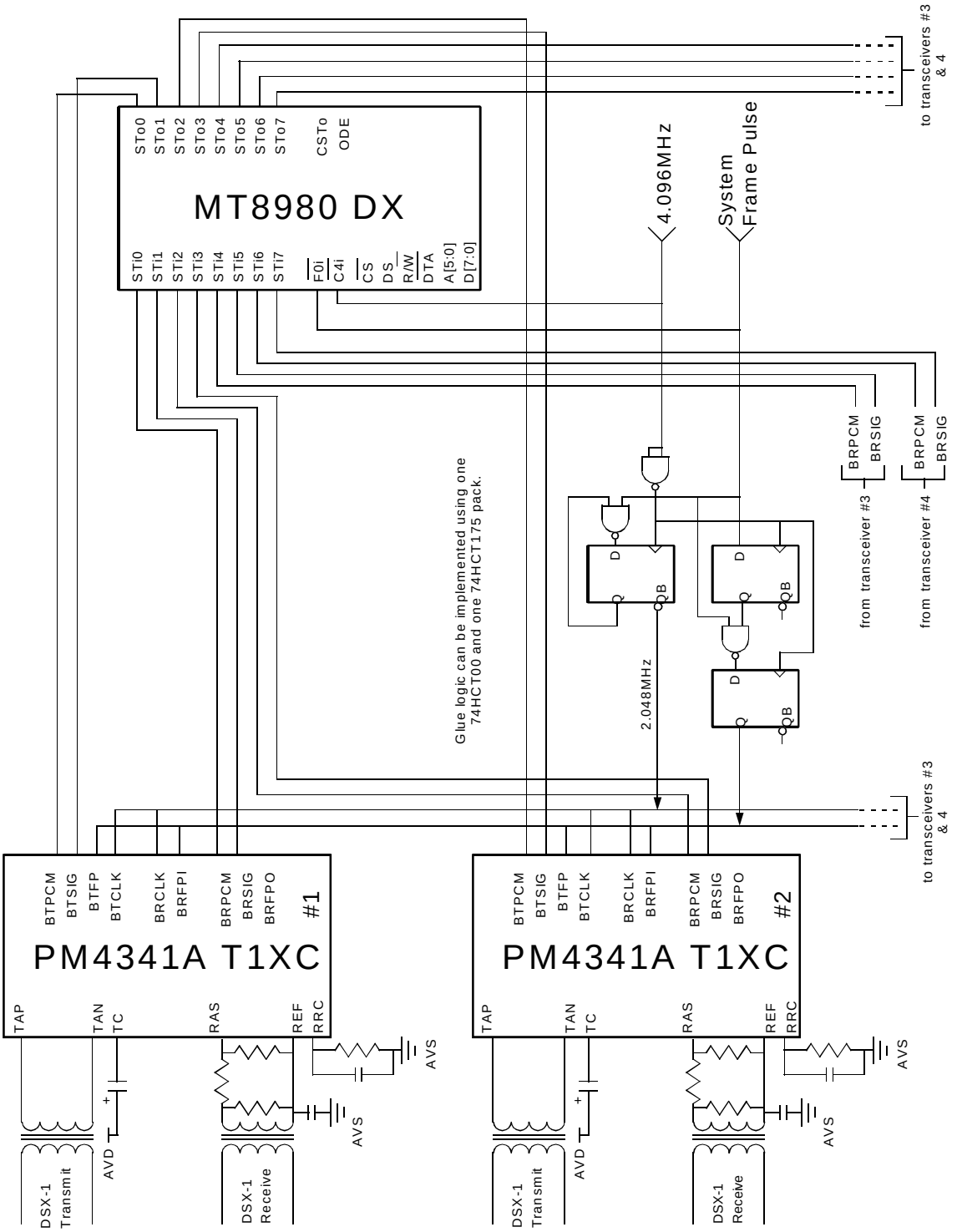
**Figure 1 - Example 1. T1 or E1 ATM Interface Using PM7345**




Example 1 shows the PM4341 T1XC or PM6341 E1XC used with a PM7345 Saturn User Network Interface for PDH (S/UNI-PDH™) to implement ATM wide area user network interfaces (UNI) and network node interfaces (NNI).

In this example, the T1 LIU and framing functions are provided by the PM4341A T1XC. The combination of the T1XC or E1XC devices with the S/UNI-PDH™ allows both PLCP formatted DS1/E1 signals and CCITT G.804 compliant DS1/E1 signals to be processed. The G.804 specification defines ATM cell mappings for a variety of transmission formats, including the 1.544 Mbit/s DS1 and the 2.048 Mbit/s E1 formats.

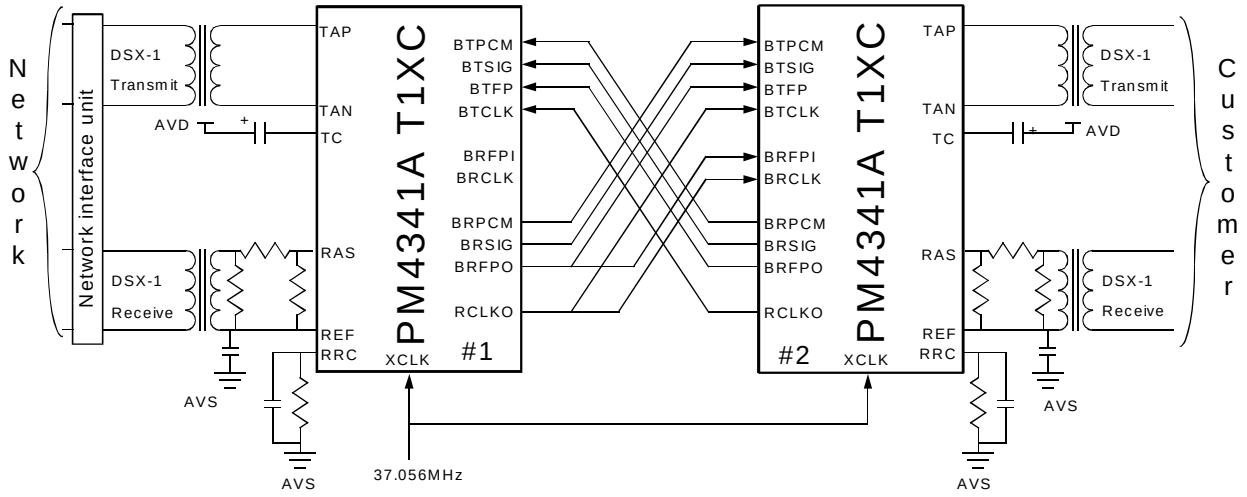
**Figure 2 - Example 2. DSX-1/0 Cross-connect**



Example 2 shows a DSX 1/0 Cross-Connect utilizing four T1XC chips and a Mitel MT8980 Digital Time/Space Switch to implement a simple 1/0 cross-connect. An alternate architecture could use two MT8980s, one as a voice switch and the other as a signalling switch, and 8 T1XCs to cross-connect eight T1s. (Note: a true implementation would require redundancy in the switch core.)

In this example, the T1XC chips are programmed to receive and generate the same framing format, using the 2.048 MHz backplane data rate. The "system frame pulse" signal is stretched through the two D-FF into a pulse of 488ns duration, which is used to frame align the data out of each transceiver through the elastic store and to provide frame alignment indication to the transmitters. The raw system frame pulse signal is used to indicate frame alignment synchronization to the MT8980. Another D-FF is configured as a toggle to generate a 2.048MHz clock from the system 4.096MHz clock source, synchronized to the system frame pulse.

**Figure 3 - Example 3. Multi-featured, jitter attenuating CSU**




Example 3 is an application utilizing 2 T1XC chips to implement a multi-featured Channel Service Unit with jitter attenuation. The T1XCs are programmed to receive and generate the same framing format, using the 1.544 MHz backplane data rate with the Elastic Stores bypassed.

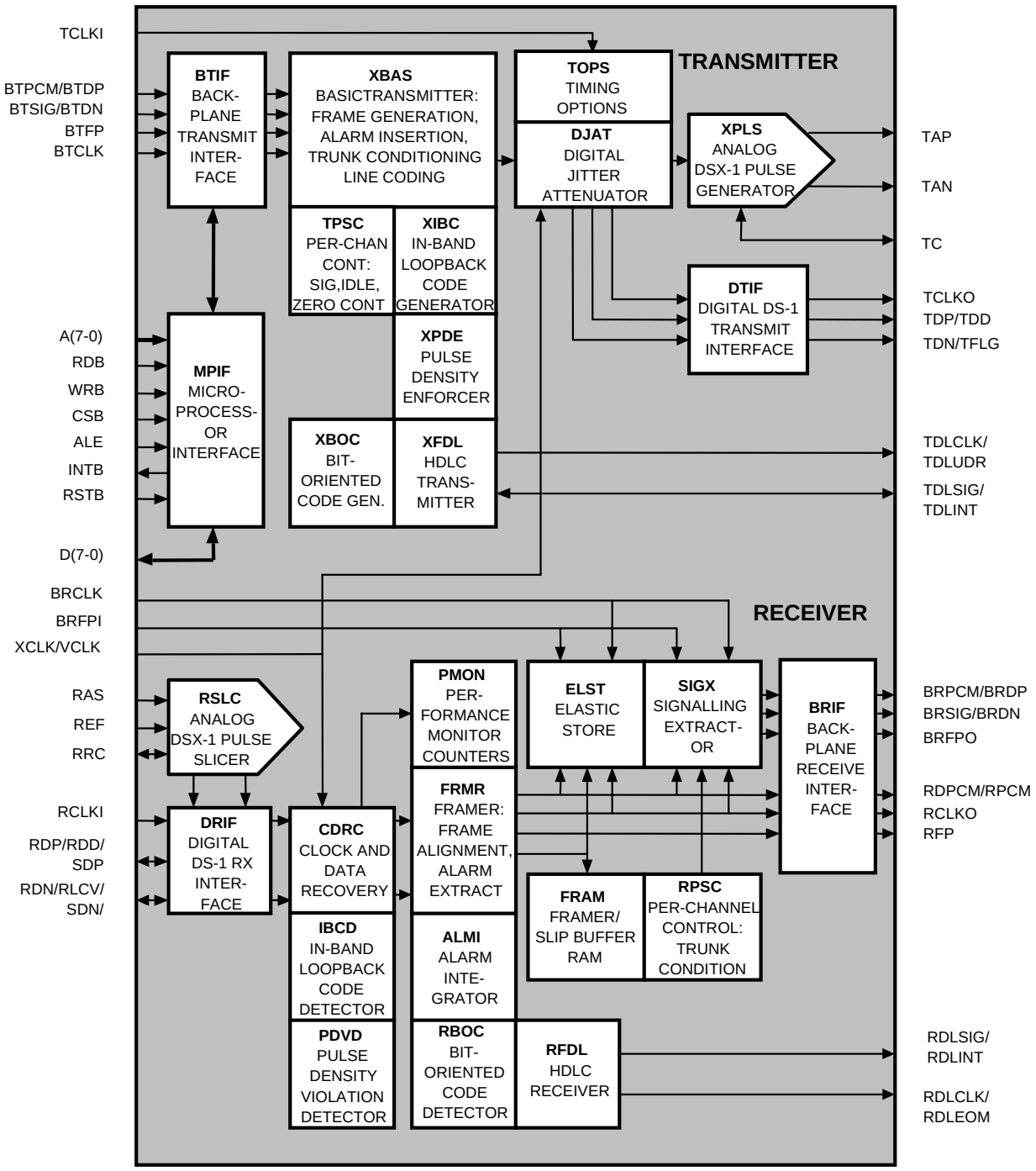
T1XC #1's Timing Options Register is programmed to enable jitter attenuation of the outgoing transmit data to the network, using the backplane transmit clock (BTCLK= recovered clock from customer interface) as the jitter reference. Similarly, T1XC #2 is programmed to attenuate the outgoing transmit data jitter to the customer equipment using its backplane transmit clock (BTCLK= recovered

clock from network interface) as the jitter reference. Also, since T1XC #2's elastic store is bypassed, the TRSLIP bit in the Receive Options register can be set to provide a measure of the frequency difference between the network clock and the customer clock by monitoring the time interval between resulting slip indications.

This application can be readily modified to provide additional features by simply changing the T1XC configurations via software. No external wiring changes are necessary to support framing format conversion or to loop time the network transmit data to the network receive recovered clock.

For example, to provide format conversion of a customer's SF-based equipment to an ESF network, T1XC #1 would be programmed to receive and transmit ESF formatted data, while providing superframe alignment indication on the backplane frame pulse output (BRFPO). T1XC #2 would be programmed to receive and transmit SF formatted data, while providing every second superframe alignment indication on its BRFPO. To provide loop timing of the network transmit to the network receive clock, T1XC #2 would be programmed to use the elastic store, thereby providing the slip buffering to handle the frequency difference between the network and customer equipment clocks. T1XC #1 would be programmed to use its RCLKO for the transmitter clock instead of the input BTCLK.

# 4 BLOCK DIAGRAM



# 5 DESCRIPTION

The PM4341A Single T1 Framer/Transceiver (T1XC) is a feature-rich device suitable for use in many T1 systems with a minimum of external circuitry. The T1XC is software configurable, allowing feature selection without changes to external wiring.

On the receive side, the T1XC recovers clock and data and can be configured to frame to any of the common DS-1 signal formats: SF, ESF, T1DM (DDS), or SLC®96. Analog circuitry is provided to allow direct reception of a DSX-1 compatible signal up to 655 feet from the cross-connect by using only an external transformer and passive components. The T1XC also supports detection of various alarm conditions such as loss of signal, pulse density violation, red alarm, yellow alarm, and AIS alarm. The T1XC detects and indicates the presence of yellow and AIS patterns and also integrates yellow, red, and AIS alarms as per industry specifications.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events is provided. The T1XC also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. An elastic store for slip buffering and adaptation to backplane timing is provided, as is a signalling extractor that supports signalling debounce, signalling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signalling bit fixing on a per-channel basis. Receive side data and signalling trunk conditioning is also provided.

On the transmit side, the T1XC generates framing for SF, ESF, T1DM (DDS), and SLC®96 DS1 formats, or framing can be optionally disabled. Internal analog circuitry allows direct transmission of a DSX-1 compatible signal using only an external transformer. Digitally programmable line build out allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect. The T1XC also supports signalling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. The zero code suppression is selectable to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signalling trunk conditioning is provided.

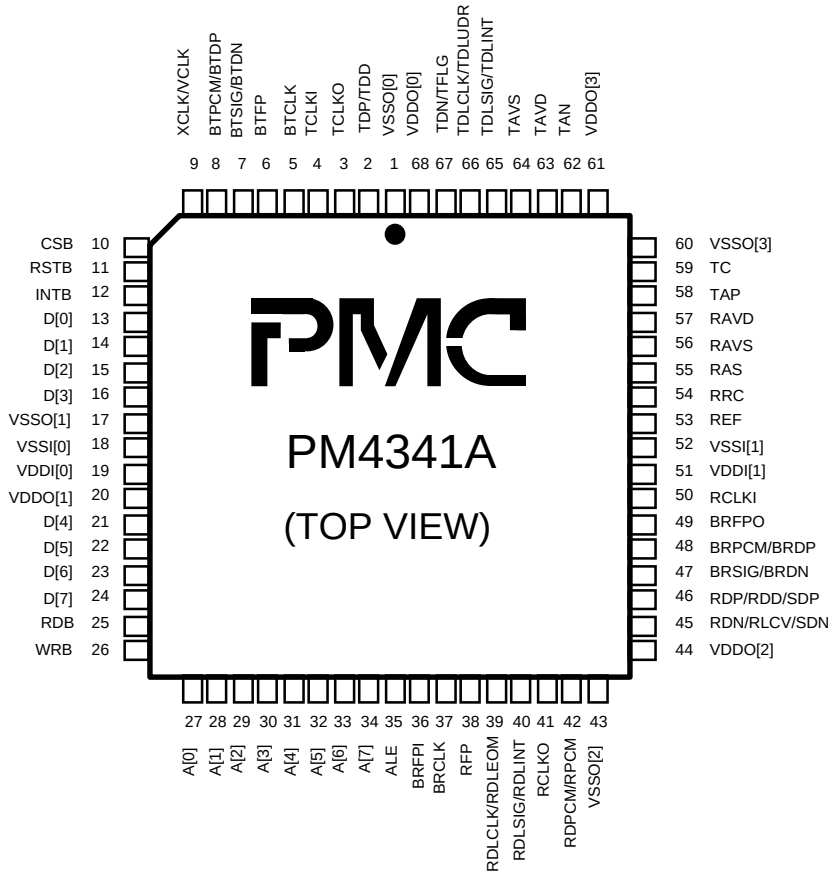
The T1XC can also generate in-band loopback codes, ESF bit oriented codes, and transmit HDLC messages on the ESF data link. The T1XC can generate a low jitter transmit clock and provides a FIFO for transmit jitter attenuation. When not used for jitter attenuation, the full or empty status of this FIFO is made

available to facilitate higher order multiplexing applications by controlling bit-stuffing logic.

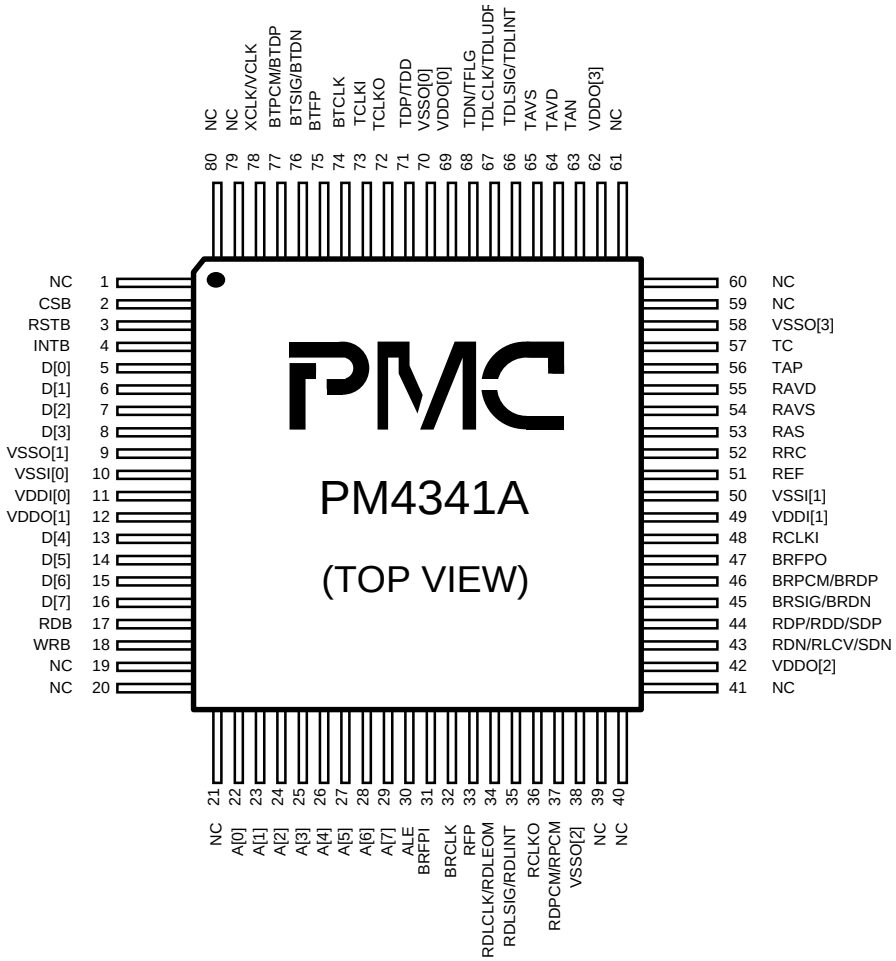
The T1XC provides both a parallel microprocessor interface for controlling the operation of the T1XC device, and serial PCM interfaces that allow 1.544 Mbit/s or 2.048 Mbit/s backplanes to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

# 6 PIN DIAGRAM

## Figure 4 - 68 Pin PLCC



## Figure 5 - 80 Pin PQFP



## 7 PIN DESCRIPTION

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RDP/ | I/O | 44 | 46 | Receive Digital Positive Line Pulse (RDP). This input is available when the T1XC is configured to receive dual-rail formatted data. The RDP input can be enabled for either RZ or NRZ waveforms. When enabled for NRZ, this input may be enabled to be sampled on the rising or falling edge of RCLKI. When enabled for RZ, clock is recovered from the RDP and RDN inputs. |
| RDD/ | | | | Receive Digital DS-1 Signal (RDD). When the T1XC is configured to receive single-rail data, this input may be enabled to be sampled on the rising or falling edge of RCLKI. |
| SDP | | | | Sliced Positive Line Pulse (SDP). This pin becomes an output when the receive analog line interface is powered up. A positive pulse on the SDP output corresponds to the sampled positive pulse excursion on the RAS input. |
| RDN/ | I/O | 43 | 45 | Receive Digital Negative Line Pulse (RDN). This input is available when the T1XC is configured to receive dual-rail formatted data. The RDN input can be enabled for either RZ or NRZ waveforms. When enabled for NRZ, this input may be enabled to be sampled on the rising or falling edge of RCLKI. When enabled for RZ, clock is recovered from the RDP and RDN inputs. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RLCV/<br><br><br><br>SDN | I/O | 43 | 45 | Receive Line Code Violation Indication (RLCV). When the T1XC is configured to receive single-rail data, this input may be enabled to be sampled on the rising or falling edge of RCLKI.<br>Sliced Negative Line Pulse (SDN). This pin becomes an output when the receive analog line interface is powered up. A positive pulse on the SDN output corresponds to the sampled negative pulse excursion on the RAS input. |
| RCLKI | Input | 48 | 50 | Receive Line Clock Input (RCLKI). This input is an externally recovered 1.544 MHz line clock that may be enabled to sample the RDP and RDN inputs on its rising or falling edge when the input format is enabled for dual-rail NRZ; or to sample the RDD and RLCV inputs on its rising or falling edge when the input format is enabled for single-rail. |
| RAS | Input | 53 | 55 | Receive Analog Signal (RAS). This analog input samples the AC signal on an external isolation transformer. It is connected to the positive lead of the transformer secondary through a passive attenuation network. |
| REF | I/O | 51 | 53 | Receive Reference (REF). This analog bidirectional pin provides DC bias to an external isolation transformer. It is connected to the negative lead of the transformer secondary and to a decoupling capacitor to RAVS. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RRC | I/O | 52 | 54 | Receive Peak Hold R-C Network (RRC). This analog bidirectional pin is connected to an external parallel resistor/capacitor network to RAVS. This network is necessary to the operation of the internal peak detector that tracks the incoming signal level. |
| RAVD | Power | 55 | 57 | Receive Analog Power (RAVD). This pin provides the +5V supply to the receive analog line interface. If the receive analog line interface is not used, the power consumption of the T1XC can be reduced by connecting the RAVD pin to the analog ground pin, RAVS. RAVD must be connected to a common, well decoupled +5 VDC supply together with the VDDO[2:0] and VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO and VDDI pins into the RAVD pin. |
| RAVS | Ground | 54 | 56 | Receive Analog Ground (RAVS). This pin provides the ground supply to the receive analog line interface. RAVS must be connected to a common ground together with the VSSO[2:0] and VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO and VSSI pins into the RAVS pin. |
| RCLKO | Output | 36 | 41 | Recovered PCM Clock Output (RCLKO). This output signal is the recovered 1.544 MHz clock, synchronized to the XCLK signal. The RCLKO signal is recovered from the received analog inputs (if the interface is powered up), from the RDP and RDN inputs (if the input format is dual-rail RZ), or from the RCLKI input (if the input format is NRZ). |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RDPCM/ | Output | 37 | 42 | Recovered Decoded PCM (RDPCM). This output is available when the T1XC is configured for decoded data output. This NRZ output signal is the recovered data stream with B8ZS decoding applied, if B8ZS decoding is enabled. It is updated on the falling edge of RCLKO. The RDPCM signal is not meant to be used when the digital receive interface is configured for uni-polar operation since this data should be available at the RDD input. |
| RPCM | | | | Recovered PCM (RPCM). This output is available when the T1XC is configured for raw data output. This NRZ output signal is the recovered data stream without optional B8ZS decoding applied. It is updated on the falling edge of RCLKO. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RFP | Output | 33 | 38 | Receive Frame Pulse (RFP). When the T1XC is configured for receive frame pulse output, RFP pulses high for 1 RCLKO cycle during bit 1 of each 193-bit frame, indicating the frame alignment of the RPCM/RDPCM data stream. RFP does not indicate the frame alignment in RDPCM when the digital receive interface is configured for unipolar operation (i.e. RUNI=1and RDIEN=1 in Register 03h).<br><br>When configured for receive superframe output, RFP pulses high for 1 RCLKO cycle during bit 1 of frame 1 of the 12 or 24 frame superframe, indicating the superframe alignment of the RPCM/RDPCM data stream.<br><br>When configured for receive alternate superframe output, RFP pulses high for 1 RCLKO cycle during bit 1 of frame 1 of every second 12 or 24 frame superframe, indicating the superframe alignment of the RPCM/RDPCM data stream. This alternate superframe indication is useful for performing format conversion from SF to ESF while maintaining the same superframe alignment.<br><br>RFP is updated on the falling edge of RCLKO. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RDLSIG/ | Output | 35 | 40 | Receive Data Link Signal (RDLSIG). The RDLSIG signal is available on this output when the internal HDLC receiver (RFDL) is disabled from use, or, optionally, when the D-channel of the Primary Rate interface is extracted. When the T1XC is configured to receive ESF formatted data, the RDLSIG contains the data stream extracted from the facility data link; when the T1XC is configured to receive SF formatted data, the RDLSIG output is held low; when the T1XC is configured to receive T1DM, RDLSIG reflects the value of the R-bit in the T1DM sync word; when the T1XC is configured for SLC®96, RDLSIG contains the value of the Fs framing bits. When the D-channel is enabled for extraction, RDLSIG contains the contents of channel 24 of each DS-1 frame. RDLSIG is updated on the falling edge of RDLCLK. |
| RDLINT | | | | Receive Data Link Interrupt (RDLINT). The RDLINT signal is available on this output when RFDL is enabled. RDLINT goes high when an event occurs which changes the status of the HDLC receiver. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| RDLCLK/ | Output | 34 | 39 | Receive Data Link Clock (RDLCLK). The RDLCLK signal is available on this output when the internal HDLC receiver (RFDL) is disabled from use, or, optionally, when the D-channel of the Primary Rate interface is extracted. RDLCLK is used to process the data stream contained on the RDLSIG output. When the T1XC is configured to receive SF formatted data, the RDLCLK output is held low. In all other formats the rising edge of RDLCLK can be used to sample the data on RDLSIG. |
| RDLEOM | | | | Receive Data Link End of Message (RDLEOM). The RDLEOM signal is available on this output when RFDL is enabled. RDLEOM goes high when the last byte of a received sequence is read from the RFDL FIFO buffer, or when the FIFO buffer is overrun. |
| BRPCM/ | Output | 46 | 48 | Backplane Receive PCM (BRPCM). The BRPCM signal is available on this output when the backplane is configured for single-rail output. BRPCM contains the recovered data stream passed through ELST, SIGX, and the RPSC. When the ELST is not by-passed, the BRPCM stream is aligned to the backplane timing and is updated on the falling edge of BRCLK. When the ELST is by-passed, BRPCM is aligned to the receive line timing and is updated on the falling edge of RCLKO. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| BRDP | Output | 46 | 48 | Backplane Receive Positive Line Pulse (BRDP). The BRDP signal is available on this output when the backplane is configured for dual-rail output. The BRDP NRZ output represents the RZ receive digital positive pulse signal extracted from the input bipolar signal. BRDP is updated on the falling edge of RCLKO. |
| BRSIG/ | Output | 45 | 47 | Backplane Receive Signalling (BRSIG). The BRSIG signal is available on this output when the backplane is configured for single-rail output. BRSIG contains the extracted signalling bits for each channel in the frame, repeated for the entire superframe. Each channel's signalling bits are valid in bit locations 5,6,7,8 of the channel and are channel-aligned with the BRPCM data stream. When the ELST is not by-passed, the BRSIG stream is aligned to the backplane timing and is updated on the falling edge of BRCLK. When the ELST is by-passed, BRSIG is aligned to the receive line timing and is updated on the falling edge of RCLKO. |
| BRDN | | | | Backplane Receive Negative Line Pulse (BRDN). The BRDN signal is available on this output when the backplane is configured for dual-rail output. The BRDN NRZ output represents the RZ receive digital negative pulse signal extracted from the input bipolar signal. BRDN is updated on the falling edge of RCLKO. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| BRFPO | Output | 47 | 49 | Backplane Frame Pulse Output (BRFPO). When the T1XC is configured for backplane receive frame pulse output, BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of each 193-bit frame, indicating the frame alignment of the BRPCM data stream.<br><br>When configured for backplane receive superframe output, BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of frame 1 of the 12 or 24 frame superframe, indicating the superframe alignment of the BRPCM data stream.<br><br>When configured for backplane alternate receive superframe output, BRFPO pulses high for 1 BRCLK cycle (or 1 RCLKO cycle if ELST is by-passed) during bit 1 of frame 1 of every second 12 or 24 frame superframe, indicating the superframe alignment of the BRPCM data stream. This alternate superframe indication is useful for performing format conversion from SF to ESF while maintaining the same superframe alignment.<br><br>BRFPO is updated on the falling edge of BRCLK or RCLKO. |
| BRCLK | Input | 32 | 37 | Backplane Receive Clock (BRCLK). This clock should be either 1.544MHz or 2.048MHz with optional gapping for adaptation to non-uniform backplane data streams. The T1XC may be configured to ignore the BRCLK input and use the RCLKO signal in its place when the ELST is bypassed. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| BRFPI | Input | 31 | 36 | Backplane Frame Pulse Input (BRFPI). This input is used to frame align the received data to the system backplane. If frame alignment only is required, a pulse at least 1 BRCLK cycle wide must be provided on BRFPI every 193 bit times. If receive signalling alignment is required, receive signalling alignment must be enabled, and a pulse at least 1 BRCLK cycle wide must be provided on BRFPI every 12 or 24 frame times. BRFPI is sampled on the rising edge of BRCLK. |
| BTPCM/ | Input | 77 | 8 | Backplane Transmit PCM (BTPCM). The non-return to zero, digital data stream to be transmitted is input on this pin when the backplane is configured for single-rail input. The BTPCM signal is sampled on the rising edge of BTCLK. |
| BTDP | | | | Backplane Transmit Positive Line Pulse (BTDP). The positive pulse of the dual-rail signal to be transmitted is input on this pin when the backplane is configured for dual-rail input. In dual-rail input mode, the BTDP input by-passes the transmitter and is fed directly into the DJAT. BTDP is sampled on the rising edge of BTCLK. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| BTSIG/ | Input | 76 | 7 | Backplane Transmit Signalling (BTSIG). The BTSIG input signal contains the signalling bits for each channel in the transmit data frame, repeated for the entire superframe. This signal is input on the BTSIG pin when the backplane is configured for single-rail input. Each channel's signalling bits are in bit locations 5,6,7,8 of the channel and are channel-aligned with the BTPCM data stream. BTSIG is sampled on the rising edge of BTCLK. |
| BTDN | | | | Backplane Transmit Negative Line Pulse (BTDN). The negative pulse of dual-rail signal to be transmitted is input on this pin when the backplane is configured for dual-rail input. In dual-rail input mode, the BTDN input by-passes the transmitter and is fed directly into the DJAT. BTDN is sampled on the rising edge of BTCLK. |
| BTFP | Input | 75 | 6 | Backplane Transmit Frame Pulse (BTFP). This input is used to frame align the transmitter to the system backplane. If frame alignment only is required, a pulse at least 1 BTCLK cycle wide must be provided on BTFP every 193 bit times. If superframe alignment is required, transmit superframe alignment must be enabled, and a pulse at least 1 BTCLK cycle wide must be provided on BTFP every 12 or 24 frame times. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| BTCLK | Input | 74 | 5 | Backplane Transmit Clock (BTCLK). This clock should be either 1.544MHz or 2.048MHz with optional gapping for adaptation from non-uniform backplane data streams. The T1XC may be configured to ignore the BTCLK input and use the RCLKO signal in its place. |
| TDLSIG/ | I/O | 66 | 65 | Transmit Data Link Signal (TDLSIG). The TDLSIG signal is input on this pin when the internal HDLC transmitter (XFDL) is disabled from use. TDLSIG is the source for the data stream to be inserted into the ESF data link. When the T1XC is configured to transmit SLC®96 formatted data, the TDLSIG input is the source for the Fs framing bits; when the T1XC is configured to transmit T1DM with R-bit replacement, TDLSIG is the source of the R-bit in the T1DM sync word. TDLSIG is sampled on the rising edge of TDLCLK. |
| TDLINT | | | | Transmit Data Link Interrupt (TDLINT). The TDLINT signal is output on this pin when XFDL is enabled. TDLINT goes high when the last data byte written to the XFDL has been set up for transmission and processor intervention is required to either write control information to end the message, or to provide more data. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| TDLCLK/ | Output | 67 | 66 | Transmit Data Link Clock (TDLCLK). The TDLCLK signal is available on this output when the internal HDLC transmitter (XFDL) is disabled from use. The rising edge of TDLCLK is used to sample the data stream contained on the TDLSIG input. When the T1XC is configured to transmit SF formatted data, the TDLCLK output is held low. |
| TDLUDR | | | | Transmit Data Link Underrun (TDLUDR). The TDLUDR signal is available on this output when XFDL is enabled. TDLUDR goes high when the processor has failed to service the TDLINT interrupt before the transmit buffer is emptied. |
| TCLKO | Output | 72 | 3 | Transmit Clock Output (TCLKO). The TDP, TDN, and TDD outputs may be enabled to be updated on the rising or falling edge of TCLKO. The TAP and TAN outputs are also driven with timing derived from TCLKO. TCLKO is a 1.544 MHz clock that is adequately jitter and wander free in absolute terms to permit an acceptable DSX-1 or DS-1 signal to be generated. Depending on the configuration of the T1XC, TCLKO may be derived from TCLKI, RCLKO, or BTCLK, with or without jitter attenuation. |
| TDP/ | Output | 71 | 2 | Transmit Digital Positive Line Pulse (TDP). This signal is available on the output when the T1XC is configured to transmit dual-rail data. The TDP signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of TCLKO. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| TDD | Output | 71 | 2 | Transmit Digital DS-1 Signal (TDD). This signal is available on the output when configured to transmit single-rail data. The TDD signal may be enabled to be updated on the rising or falling edge of TCLKO. |
| TDN/ | Output | 68 | 67 | Transmit Digital Negative Line Pulse (TDN). This signal is available on the output when the T1XC is configured to transmit dual-rail data. The TDN signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of TCLKO. |
| TFLG | | | | Transmit FIFO Flag (TFLG). This signal is available when configured to transmit single-rail data. The TFLG output indicates when the transmit rate conversion FIFO in DJAT is nearing an empty or a full condition. Either indication may be selected. This output may be enabled to be updated on the rising or falling edge of TCLKO. |
| TAP | Output | 56 | 58 | Transmit Analog Positive Pulse (TAP). This analog output drives an AC signal through an external matching transformer. It is connected to the positive lead of the transformer primary.<br>An analog Transmit Monitor Positive point is internally bonded to this output and is used to monitor the positive pulses on the transmit line. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| TAN | Output | 63 | 62 | Transmit Analog Negative Pulse (TAN). This analog output drives an AC signal through an external matching transformer. It is connected to the negative lead of the transformer primary.<br>An analog Transmit Monitor Negative point is internally bonded to this output and is used to monitor the negative pulses on the transmit line. |
| TC | I/O | 57 | 59 | Transmit Reference Decoupling Capacitor (TC). This analog bidirectional provides decoupling for an internal reference generator. It is connected to a decoupling capacitor to TAVD. |
| TAVD | Power | 64 | 63 | Transmit Analog Power (TAVD). This pin provides the +5 V supply to the transmit analog line interface. Even if the transmit analog line interface is not used, a +5 V supply must be provided. TAVD must be connected to a common, well decoupled +5 VDC supply together with the VDDO[2:0] and VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO and VDDI pins into the TAVD pin. |
| TAVS | Ground | 65 | 64 | Transmit Analog Ground (TAVS). This pin provides the ground supply to the transmit analog line interface. TAVS must be connected to a common ground together with the VSSO[2:0] and VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO and VSSI pins into the TAVS pin. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| TCLKI | Input | 73 | 4 | Transmit Clock Input (TCLKI). This input signal is used to generate the TCLKO clock signal. Depending upon the configuration of the T1XC, TCLKO may be derived directly from TCLKI by dividing TCLKI by 8, or TCLKO may be derived from TCLKI after jitter attenuation. If TCLKI is jitter-free when divided down to 8 kHz, then it is possible to derive TCLKO from TCLKI when TCLKI is a multiple of 8 kHz (i.e. Nx8 kHz, for N equals 1 to 256). The T1XC may be configured to ignore the TCLKI input and utilize BTCLK or RCLKO instead. RCLKO is also substituted for TCLKI if line loopback is enabled. |
| XCLK/<br><br>VCLK | Input | 78 | 9 | Crystal Clock Input (XCLK). This signal provides timing for many portions of the T1XC. Depending on the configuration of the T1XC, XCLK is nominally a 37.056 MHz ± 32ppm or 12.352 MHz ± 50ppm, 50% duty cycle clock.<br>When transmit clock generation or jitter attenuation is not required, XCLK may be driven with a 12.352 MHz clock. When transmit clock generation or jitter attenuation is required, XCLK must be driven with a 37.056 MHz clock. Implementation of Line Loopback is also simplified when a 37.056 MHz clock is used.<br>Vector Clock (VCLK). The VCLK signal is used during T1XC production test to verify internal functionality. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| INTB | Output | 4 | 12 | Active low open-drain Interrupt signal (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources, including the internal HDLC transceiver. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source. |
| CSB | Input | 2 | 10 | Active low chip select (CSB). This signal must be low to enable T1XC register accesses. CSB must go high at least once after a powerup to clear internal test modes. If CSB is not used, then it should be tied to an inverted version of RSTB, in which case RDB and WRB determine register access. |
| D[0]<br>D[1]<br>D[2]<br>D[3]<br>D[4]<br>D[5]<br>D[6]<br>D[7] | I/O | 5<br>6<br>7<br>8<br>13<br>14<br>15<br>16 | 13<br>14<br>15<br>16<br>21<br>22<br>23<br>24 | Bidirectional data bus (D[7:0]). This bus is used during T1XC read and write accesses. |
| RDB | Input | 17 | 25 | Active low read enable (RDB). This signal is pulsed low to enable a T1XC register read access. The T1XC drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low. |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| WRB | Input | 18 | 26 | Active low write strobe (WRB). This signal is pulsed low to enable a T1XC register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB + CSB, where '+' indicates a logical or. |
| ALE | Input | 30 | 35 | Address latch enable (ALE). This signal latches the address bus contents, A[7:0], when low, allowing the T1XC to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. |
| RSTB | Input | 3 | 11 | Active low reset (RSTB). This signal is set low to asynchronously reset the T1XC. RSTB is a Schmitt-trigger input with integral pull-up. |
| A[0] | Input | 22 | 27 | Address bus (A[7:0]). This bus selects specific registers during T1XC register accesses. |
| A[1] | | 23 | 28 | |
| A[2] | | 24 | 29 | |
| A[3] | | 25 | 30 | |
| A[4] | | 26 | 31 | |
| A[5] | | 27 | 32 | |
| A[6] | | 28 | 33 | |
| A[7] | | 29 | 34 | |
| VDDO[0] | Power | 69 | 68 | Pad ring power pins (VDDO[3:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO pins into the VDDI pins. |
| VDDO[1] | | 12 | 20 | |
| VDDO[2] | | 42 | 44 | |
| VDDO[3] | | 62 | 61 | |

| Pin Name | Type | Pin No. PQFP | Pin No. PLCC | Function |
|---|---|---|---|---|
| VDDI[0]<br>VDDI[1] | Power | 11<br>49 | 19<br>51 | Core power pins (VDDI[1:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDO[2:0] pins. |
| VSSO[0]<br>VSSO[1]<br>VSSO[2]<br>VSSO[3] | Ground | 70<br>9<br>38<br>58 | 1<br>17<br>43<br>60 | Pad ring ground pins (VSSO[3:0]). These pins must be connected to a common ground together with the VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO pins into the VSSI pins. |
| VSSI[0]<br>VSSI[1] | Ground | 10<br>50 | 18<br>52 | Core ground pins (VSSI[1:0]). These pins must be connected to a common ground together with the VSSO[2:0] pins. |

**Notes on Pin Description:**

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSO are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. TAVD and TAVS are the +5V and ground connections, respectively, for the transmit analog circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM4341A between the core, pad ring, and transmit analog supply rails. Failure to properly make these connections may result in improper operation or damage to the device. Care must be taken to avoid coupling of noise into the transmit analog supply rails.

2. RAVD and RAVS are the +5 V and ground connections, respectively, for the receive analog circuitry of the device. These power supply connections need only be used if the receive analog function is desired and should then connect to a common +5 V or ground rail, as appropriate, with the core, pad ring, and transmit analog supply rails. There is no low impedance connection within the PM4341A between the receive analog supply rail and other supply rails. When the receive analog function is not desired, RAVD should be connected to RAVS. Care must be taken to avoid coupling of noise into the receive analog supply rails.

3. Inputs RSTB and ALE have integral pull-up resistors.

4. Pins 1,19,20,21,39,40,41,59,60,61,79, and 80 on the 80-pin PQFP are not connected. These pins should be left unconnected in any application.

5. The TDLSIG/TDLINT pin has an integral pull-up resistor and defaults to being an input after a reset.

6. When the internal RFDL is enabled, the RDLINT output goes high:

    - when the number of bytes specified in the RFDL Interrupt Status/Control Register have been received on the data link,
    - immediately on detection of RFDL FIFO buffer overrun,
    - immediately on detection of end of message,
    - immediately on detection of an abort condition, or,
    - immediately on detection of the transition from receiving all ones to flags.

    The interrupt is cleared at the start of the next RFDL Data Register read that results in an empty FIFO buffer. This is independent of the FIFO buffer fill level for which the interrupt is programmed. If there is still data remaining in the buffer, RDLINT will remain high. An interrupt due to a RFDL FIFO buffer overrun condition is not cleared on a RFDL Data Register read but on a RFDL Status Register read. The RDLINT output can always be forced low by disabling the RFDL (setting the EN bit in the RFDL Configuration Register to logic 0, or by disabling the internal HDLC receiver in the T1XC Receive Data Link Configuration Register), or by forcing the RFDL to terminate reception (setting the TR bit in the RFDL Configuration Register to logic 1).

    The RDLINT output may be forced low by disabling the interrupts with the RFDL Interrupt Status/Control Register. However, the internal interrupt latch is not cleared, and the state of this latch can still be read through the RFDL Interrupt Status/Control Register.

7. The RDLEOM output goes high:

    - immediately on detection of RFDL FIFO buffer overrun,
    - when the data byte written into the RFDL FIFO buffer due to an end of message condition is read,
    - when the data byte written into the RFDL FIFO buffer due to an abort condition is read, or,

- when the data byte written into the RFDL FIFO buffer due to the transition from receiving all ones to flags is read.

RDLEOM is set low by reading the RFDL Status Register or by disabling the RFDL.

8. The TDLUDR output goes high when the processor is unable to service the TDLINT request for more data within a specific time-out period. This period is dependent upon the frequency of TDLCLK:
    - for a TDLCLK frequency of 4 kHz (ESF FDL at the full 4 kHz rate), the time-out is 1.0 ms;
    - for a TDLCLK frequency of 2 kHz (half the ESF FDL), the time-out is 2.0ms;
    - for a TDLCLK frequency of 8 kHz (T1DM R-bit insertion), the time-out is 500µs.

# 8 FUNCTIONAL DESCRIPTION

## 8.1 Digital DS-1 Receive Interface (DRIF)

The Digital DS-1 Receive Interface provides control over the various input options available on the multifunctional digital receive pins RDP/RDD/SDP and RDN/RLCV/SDN. When configured for dual-rail input, the multifunctional pins become the RDP and RDN inputs. These inputs can be enabled to receive either return-to-zero (RZ) or non-return-to-zero (NRZ) signals; the NRZ input signals can be sampled on either the rising or falling edge of RCLKI. When the interface is configured for single-rail input, the multifunctional pins become the RDD and RLCV inputs, which can be sampled on either the rising or falling RCLKI edge. Finally, when the analog interface is used, the multifunction pins become the SDP and SDN outputs, indicating the sliced pulses corresponding to the received positive and negative analog line pulses.

## 8.2 Analog DSX-1 Pulse Slicer (RSLC)

The Analog DSX-1 Pulse Slicer function is provided by the RSLC block. The Receive Data Slicer (RSLC) block provides the first stage of signal conditioning for a G.703 1544kbit/s serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ output pulse is generated by the RSLC block, bipolar input signals must rise to 67% of their peak amplitude. This level is referred to as the slicing level. The threshold criteria insures accurate pulse or mark recognition in the presence of noise.

The RSLC block can be disabled by strapping the receive analog power pin, RAVD to ground. When RLSC is disabled, the T1XC accepts RZ DS1 input pulses on the RDP/RDD and RDN/RLCV pins.

The RSLC block relies on an external network for compliance to the DSX-1 input port specifications. The RSLC block is configured via an off-chip attenuator pad to operate in one of two modes: terminating mode or bridging mode.

According to G.703, the amplitude of a DSX-1 terminating mode received pulse at the 1:2 line-coupling transformer's primary should be in the range from 3.6V to 1.2V (depending on the length of the cable from the signal source). In this mode, the T1XC can receive signal levels down to a squelching level of 227mV±20%. Assuming a worst-case squelching level of 272mV, there is 12.9dB margin between the minimum expected signal level and the minimum receivable signal level.

In bridging mode, the T1XC is connected to a monitor jack which bridges across the line and attenuates the signal levels by 20 dB, so the expected pulse amplitude at the 1:2 line-coupling transformer's primary should be in the range from 360mV to 120mV (depending on the length of the cable from the signal source). In this mode, the T1XC can receive signal levels down to a squelching level of 50mV±20% which means that there is 6.0dB margin between the minimum expected signal level and the minimum receivable signal level, in the worst case.

The RSLC block provides a squelching circuit, which indicates an alarm when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. The SQ status bit in the RSLC Interrupt Enable/Status register (5DH) goes high whenever the RSLC block is squelching the input signal. The RSLC can be configured to generate an interrupt whenever the SQ status bit changes state.

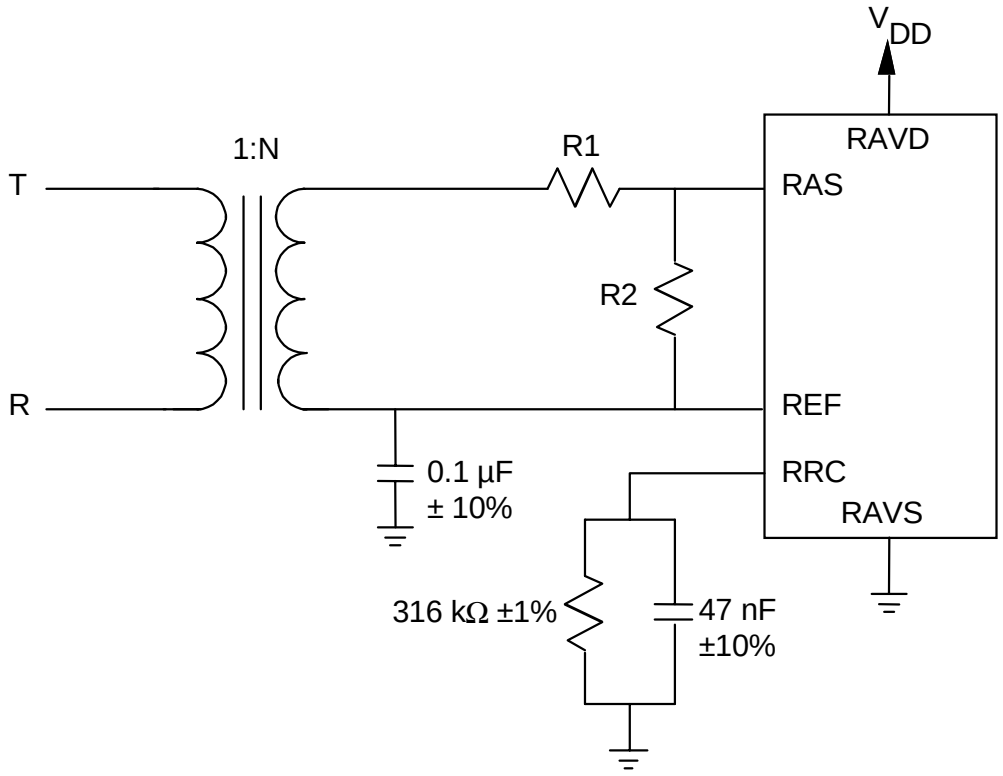
The off-chip attenuator pad network is shown in Figure 6 and the network values below are recommended for the specified applications:

**Table 1 - Recommended Receive Network Values**

| Mode | Turns Ratio (N ± 5%) | R1 (Ω ± 1%) | R2 (Ω ± 1%) | Squelch Level at Primary (mV ± 20%) |
|---|---|---|---|---|
| Terminating | 2 | 309 | 93 | 227 |
| Bridging | 2 | 0 | 402 | 50 |

Tight tolerances are required on the resistors and turns ratio to meet the return loss specification.

**Figure 6 - External Analog Receive Interface Circuit**




**Notes:**

1. All capacitors ceramic
2. Some transformer manufacturers produce a dual part containing both the 1:2 & 1:1.36 transformers required for the receive and transmit interfaces, respectively.

The transformer used should be designed for use in T1 applications. Many manufacturers have standard products for these applications. Typical characteristics of a suitable transformer are given in the following table.

**Table 2 - Typical Characteristics of Receive Transformer**

| Turns Ratio (PRI:SEC) | OCL (mH min.) | $C_{w/w}$ (pF max.) | $L_L$ (µH max.) | DCR pri. (Ω max.) | DCR sec. (Ω max.) |
|---|---|---|---|---|---|
| 1:2 | 1.20 | 35 | 0.80 | 0.80 | 1.2 |

where OCL is the open-circuit inductance,

$C_{w/w}$ is the inter-winding capacitance,

$L_L$ is the leakage inductance, and

DCR is the DC resistance.

PMC-Sierra has verified the operation of the RSLC functional block with the following transformers:

- Pulse Engineering PE64931 (1:1:1) and PE64952 (1:2CT)
- BH Electronics 500-1775 (1:1:1) and 500-1777 (1:2CT)

Many manufacturers produce dual transformers containing the 1:2 CT and 1:1.36 transformers necessary for the receiver and transmitter circuits. PMC-Sierra has verified the operation of XPLS and RSLC with the following dual parts:

- Pulse Engineering PE64952
- Pulse Engineering PE65774 (for extended temperature range)

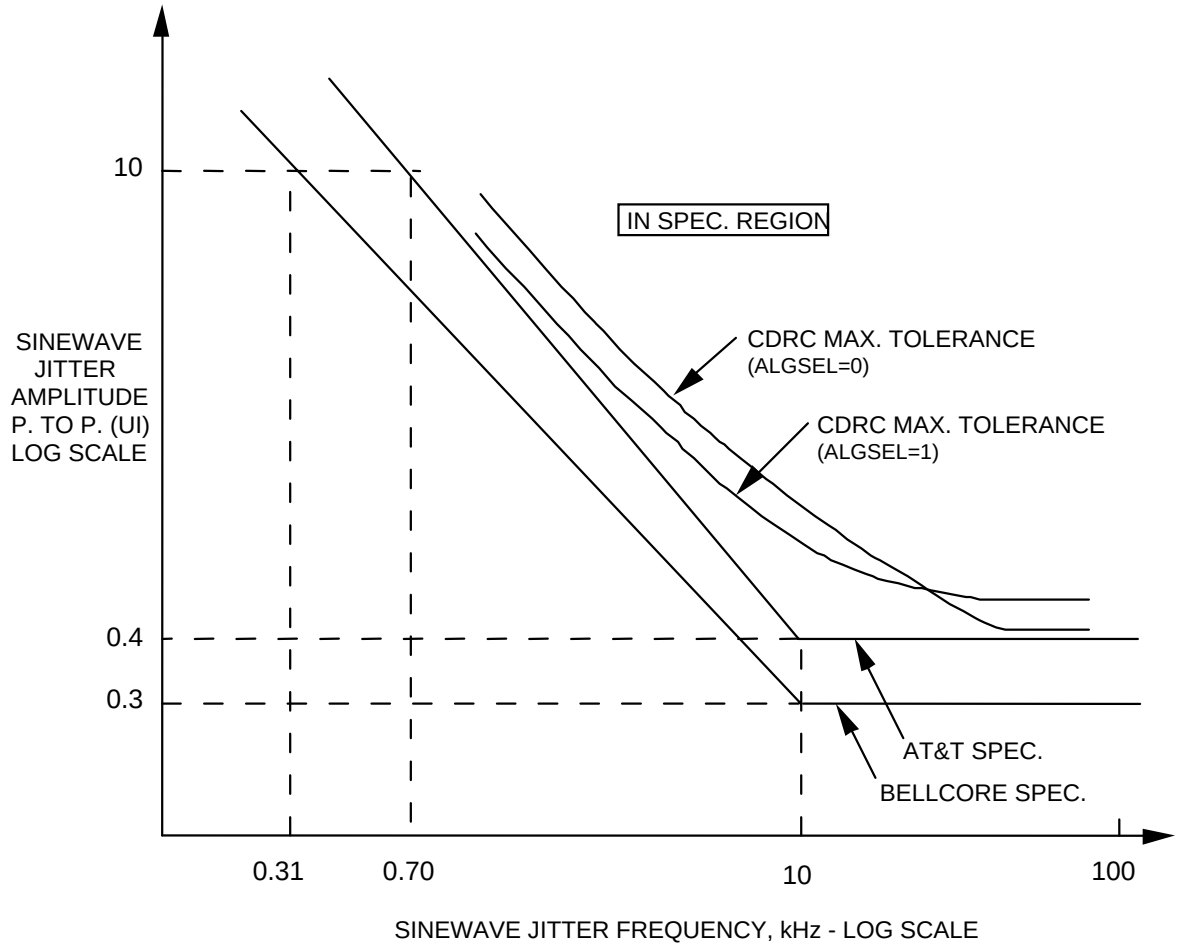
BH Electronics 500-1777

## 8.3 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by a Data and Clock Recovery (CDRC) block. The CDRC provides clock and PCM data recovery, B8ZS decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and recovers the NRZ data. Loss of signal is indicated after 176 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals and is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals.

The input jitter tolerance of CDRC complies with the Bell Core Document TA-TSY-000170 and with the AT&T specification TR62411. The tolerance is measured with a QRSS sequence ($2^{20}$-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance (approaching 0.5UIpp) at the expense of the low frequency tolerance; the low frequency tolerance of the second algorithm is approximately 80% of that of the first algorithm.

**Figure 7 - CDRC Jitter Tolerance**




## 8.4 Framer (FRMR)

The framing function is provided by the FRMR block. This block searches for the framing bit position in the incoming recovered PCM stream. It works in conjunction with the FRAM block and the DATA RECOVERY (DREC) block to search for the framing bit pattern in SF, ESF, T1DM, or SLC®96 framing formats. When searching for frame, the FRMR examines each of the 193 (SF, T1DM, SLC®96), or each of 4*193 (ESF) framing bit candidates. The FRAM block is addressed and controlled by the FRMR while frame synchronization is acquired.

The time required to find frame alignment to an error-free PCM stream containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0) is dependent upon the framing format. For

standard superframe format (SF; also known as D4 format), the FRMR block will determine frame alignment within 4.4ms 99 times out of 100. For SLC®96 format, the FRMR will determine frame alignment within 9.9ms 99 times out of 100. For extended superframe format (ESF), the FRMR will determine frame alignment within 15ms 99 times out of 100. For T1DM format, the FRMR will determine frame alignment within 1.125ms 99 times out of 100.

Once the FRMR has found frame, the internal INFRAME indication is set high and the incoming PCM data is continuously monitored for framing bit errors, bit error events ( a framing bit error in SF or SLC®96, a framing bit error or sync bit error in T1DM, or a CRC-6 error in ESF), and severe errored framing events. The FRMR also detects loss of frame, based on a selectable ratio of framing bit errors.

The FRMR extracts the yellow alarm signal bits from the incoming PCM data stream in SF and SLC®96 framing formats, and extracts the Y-bit from the T1DM sync word in T1DM framing format. The FRMR also extracts the SLC®96 data link in SLC®96 framing format, extracts the facility data link bits in ESF framing format, and extracts the R-bit from the T1DM sync word in T1DM framing format.

The FRMR can also be disabled to allow reception of unframed data. While the FRMR is disabled, control of the FRAM block is relinquished for use as the elastic store.

## 8.5 Framer/Slip Buffer RAM (FRAM)

The Framer/Slip Buffer RAM function is provided by the FRAMER RAM (FRAM) block. The FRAM is used to store up to 4 frames of PCM data while the FRMR is finding frame and up to 2 frames of PCM data during normal operation (i.e. when accessed by Elastic Store). The FRAM is shared between the Elastic Store (ELST) and the FRMR: when frame synchronization is lost, the FRMR takes control of the FRAM and uses it to find frame; when frame synchronization is determined, the FRMR relinquishes control of FRAM to ELST which buffers the incoming PCM data.

## 8.6 Inband Loopback Code Detector (IBCD)

The Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in either framed or unframed data streams. The inband code sequences are expected to be overwritten by the framing bit in framed data streams. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code

in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403-1989, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

## 8.7 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The TSB detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

## 8.8 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the PMON block. The TSB accumulates CRC error events, Frame Synchronization bit error events, Line Code Violation events, and Loss Of Frame events, or optionally, Change of Frame Alignment (COFA) events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

Generation of the transfer clock within the T1XC chip is performed by writing to any counter register location. The holding register addresses are contiguous to facilitate polling operations.

## 8.9 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1989 and in TR-TSY-000194. The 64$^{th}$ code (111111) is similar to the DL FLAG sequence and is used by the RBOC to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the control register.

Valid BOC are indicated through an internal status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

## 8.10 HDLC Receiver (RFDL)

The HDLC Receiver function is provided by the RFDL block. The RFDL is a microprocessor peripheral used to receive LAPD/HDLC frames on the ESF facility data link (FDL).

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-level FIFO buffer. The Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three bytes (programmable via the RFDL configuration register) are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

When the internal HDLC receiver is disabled, the serial data extracted by the FRMR block is output on the RDLSIG pin updated on the falling clock edge output on the RDLCLK pin. Optionally, when the internal HDLC receiver is used, the D-channel of the Primary Rate interface can be output on the RDLSIG pin updated on the falling clock edge of RDLCLK.

## 8.11 Alarm Integrator (ALMI)

The Alarm Integration function is provided by the ALMI block. This block detects the presence of YELLOW, RED, and AIS Carrier Fail Alarms (CFA) in SF, T1DM, SLC®96, or ESF formats. The alarm detection and integration is compatible with the specifications defined in Bell Pub 43801, TA-TSY-000278, TR-TSY-000008,

ANSI T1.403-1989, and TR-TSY-000191. Alarm detection and validation for SLC®96 is handled the same as SF framing format.

The ALMI block declares the presence of YELLOW alarm when the YELLOW pattern has been received for 425 ms (± 50 ms); the YELLOW alarm is removed when the YELLOW pattern has been absent for 425 ms (± 50 ms). The presence of RED alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the RED alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). In T1DM framing format the RED alarm declaration criteria can be selected to be either 400 ms (± 100 ms) or 2.55 sec (±40 ms); removal of the RED alarm in T1DM can be selected to be either 100 ms (±50 ms) or 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 1.5 sec (±100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a random $10^{-3}$ bit error rate.

The ALMI also indicates the presence or absence of the YELLOW, RED, and AIS alarm signal conditions over 40 ms, 40ms, and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

## 8.12 Elastic Store (ELST)

The Elastic Store function is provided by the ELST block.

The ELST synchronizes incoming PCM frames to the local backplane clock, BRCLK. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the backplane timing is derived from the receive line data (i.e. the RCLKO output is used), the elastic store can be bypassed to eliminate the 2 frame delay. In this configuration the elastic store can be used to measure frequency differences between the recovered line clock and another 1.544 MHz clock applied to the BRCLK input. A typical example might be to measure the difference in frequency between two received T1 streams (i.e. East-West frequency difference) by monitoring the number of SLIP occurrences of one direction with respect to the other.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The last frame which was read will be repeated.

A slip operation is always performed on a frame boundary.

To allow for the extraction of signalling information in the PCM data channels, superframe identification is also passed through the ELST.

For payload conditioning, the ELST inserts a programmable idle code into all channels when the FRMR is out of frame synchronization. This code is set to all 1's when the ELST is reset.

## 8.13 Signalling Extractor (SIGX)

The Signalling Extraction function is provided by the SIGX block. This block provides signalling bit extraction from a PCM stream for ESF, SF, and SLC®96 framing formats, and serializes the bits into a 1.544 Mbit/s serial stream channel-aligned to the outgoing PCM data stream. The signalling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5,6,7,8) in ESF framing format; in SF and SLC®96 formats the A and B bits are repeated in locations C and D (i.e. the signalling stream contains the bits ABAB for each channel). This signalling data stream is compatible with the Basic Transmitter XBAS block. The SIGX also provides user control over signalling freezing and provides control over channel data inversion, signalling bit fixing and signalling debounce on a per-channel basis. The block contains three superframes worth of signal buffering to ensure that there is a greater than 95% probability that the signalling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signalling debounce enabled, the per-channel signalling state must be in the same state for 2 superframes before appearing on the serial output stream.

The SIGX provides one superframe of signal freezing on the occurrence of slips. When a slip event occurs, the SIGX freezes the output signalling for the entire superframe in which the slip occurred; the signaling is unfrozen when the next slip-free superframe occurs.

## 8.14 Receive Per-channel Serial Controller (RPSC)

The Receive Per-channel Serial Controller (RPSC) function is provided by a second PCSC block.

The RPSC allows data and signalling trunk conditioning to be applied on the receive DS-1 stream on a per-channel basis. It also allows per-channel control of data inversion, idle code substitution, and digital milliwatt code substitution. The definition of the serial streams for the RPSC is analogous to those for TPSC.

## 8.15 Signalling Aligner (SIGA)

The Signalling Aligner can be positioned either after the signalling extractor or before the basic transmitter to provide superframe alignment between the backplane and either the received DS-1 stream or the transmit DS-1 stream. The purpose of the signalling alignment block is to maintain signalling bit integrity across superframe boundaries.

## 8.16 Backplane Receive Interface (BRIF)

The Backplane Receive Interface allows data to be presented to a backplane in either a 1.544Mbit/s or a 2.048Mbit/s serial stream, allows BPV transparency by outputting dual-rail data at 1.544Mbit/s, and allows access to the recovered PCM stream (either the B8ZS decoded stream, or the undecoded stream) at 1.544Mbit/s.

When configured to provide a 1.544Mbit/s data rate, the block generates the output data stream on the BRPCM pin containing 24 channel bytes of data followed by a single bit containing the framing bit. The BRSIG output pin contains 24 bytes of signalling nibble data located in the least significant nibble of each byte followed by a single bit position representing the "place holder" for the framing bit. The framing alignment indication on the BRFPO pin indicates the first bit of the 193-bit frame (or, optionally, the first bit of the first frame of the superframe, or every second superframe).

When configured to provide a 2.048Mbit/s data rate, the block internally gaps the 2.048MHz rate backplane clock to provide a serial PCM data on the BRPCM pin containing three channel bytes of data followed by one byte of "filler" (can be logic "0" or logic "1"). The data stream on the BRSIG pin is similar, containing three bytes of valid signalling nibbles (i.e. three channels' signalling contained in the least significant nibble of each of the three byte locations) followed by one byte of "filler". The frame alignment indication is provided on the BRFPO pin, going to logic "1" for one BRCLK cycle during the first bit of the "filler" byte,

indicating the next data byte is the first channel of the frame, or the first channel of the first frame of the superframe.

## 8.17 Basic Transmitter (XBAS)

The Basic Transmitter function is provided by an XBAS.

The BASIC TRANSMITTER (XBAS) block generates the 1.544 Mbit/s T1 data stream according to SF, ESF, T1DM, or SLC®96 formats.

A serial PCM control stream provides per channel control of idle code substitution, data inversion (either all 8 bits, sign bit only, or magnitude only), digital milliwatt substitution, and zero code suppression. Three types of zero code suppression (GTE, Bell and DDS) are supported and selected on a per channel basis to provide minimum ones density control. A serial signalling control stream provides per channel control of robbed bit signalling and selection of the signalling source. All channels can be forced into a trunk conditioning state (idle code substitution and signalling conditioning) by use of the Master Trunk Conditioning bit in the Configuration Register.

A data link is provided for ESF, T1DM and SLC®96 modes. Serial data input and clock output allow a variety of data link sources including bit oriented codes and LAPD messages. Support is provided for the transmission of framed or unframed Inband Code sequences and transmission of AIS or Yellow alarm signals for all formats.

PCM output signals may be selected to conform to B8ZS or AMI line coding.

The transmitter can be disabled for framing via the disable bit in the Transmit Functions Enable register. When transmitting ESF formatted data, the framing bit, datalink bit, or the CRC-6 bit from the input PCM stream can be by-passed to the output PCM stream. Finally, the transmitter can be by-passed completely to provide BPV transparency.

## 8.18 Transmit Per-Channel Serial Controller (TPSC)

The Transmit Per-channel Serial Controller allows data and signalling trunk conditioning or idle code to be applied on the transmit DS-1 stream on a per-channel basis. It also allows per-channel control of zero code suppression, data inversion, and application of digital milliwatt.

The Transmit Per-channel Serial Controller function is provided by a PER-CHANNEL SERIAL CONTROLLER (PCSC) block. The PCSC is a general

purpose triple serializer. Data is sourced from 3 banks of 24 8-bit registers, each bank supporting a single serial output.

The TPSC interfaces directly to the XBAS TSB and provides serial streams for signalling control, idle code data and PCM data control.

The registers are accessible from the µP interface in an indirect address mode. The BUSY indication signal can be polled from an internal status register to check for completion of the current operation.

## 8.19 Inband Loopback Code Generator (XIBC)

The Inband Loopback Code Generator function is provided by the XIBC block. This block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code and can be either framed or unframed. When the XIBC is enabled to generate framed IBC, the framing bit overwrites the inband code pattern. The contents of the code and its length are programmable from 3 to 8 bits. The XIBC interfaces directly to the XBAS Basic Transmitter block.

## 8.20 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1989. The 64$^{th}$ code (111111) is similar to the HDLC Flag sequence and is used in the XBOC to disable transmission of any bit oriented codes.

Bit oriented codes are transmitted on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The transmitted bit oriented codes have priority over any data transmitted on the FDL except for ESF YELLOW Alarm. The code to be transmitted is programmed by writing the code register.

## 8.21 HDLC Transmitter (XFDL)

The HDLC Transmitter function is provided by the XFDL block. This block is designed to provide a serial data link for the XBAS Basic Transmitter block. The XFDL is used under microprocessor or DMA control to transmit HDLC data frames in the ESF Facility Data Link when the T1XC is enabled to use the internal HDLC transmitter. The XFDL performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion.

Data to be transmitted is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. Upon completion of the frames, a CRC-CCITT frame check sequence is transmitted, followed by idle flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled for use (via the EN bit in the XFDL Configuration register), the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted are written into the Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. After the last data frame byte is transmitted, the CRC word (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag characters.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the TDLUDR signal. Optionally, the interrupt and underrun signals can be independently enabled to also generate an interrupt on the INTB output, providing a means to notify the controlling processor of changes in the XFDL operating status.

When the internal HDLC transmitter is disabled, the serial data to be transmitted on the Facility Data Link can be input on the TDLSIG pin timed to the clock rate output on the TDLCLK pin.

## 8.22 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the digital output of the transmitter, detecting when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the TSB can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

## 8.23 Digital Jitter Attenuator (DJAT)

The Digital Jitter Attenuation function is provided by the DJAT block. This block receives jittery, dual-rail T1 data in NRZ format from XBAS on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock (either BTCLK or RCLKO). The respective input data emerges from the FIFO timed to the jitter attenuated clock (TCLKO) referenced to either TCLKI, BTCLK, or RCLKO.

The jitter attenuator generates the jitter-free 1.544 MHz TCLKO output transmit clock by adaptively dividing the 37.056 MHz XCLK signal according to the phase difference between the generated TCLKO and input data clock to DJAT (either BTCLK or RCLKO). Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within DJAT so that the frequency of TCLKO is equal to the average frequency of the input data clock. To best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 6.6 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 6.6 Hz are tracked by the generated TCLKO. To provide a smooth flow of data out of DJAT, TCLKO is used to read data out of the FIFO.

If the FIFO read pointer (timed to TCLKO) comes within one bit of the write pointer (timed to the input data clock, BTCLK or RCLKO), DJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

### 8.23.1 Jitter Characteristics

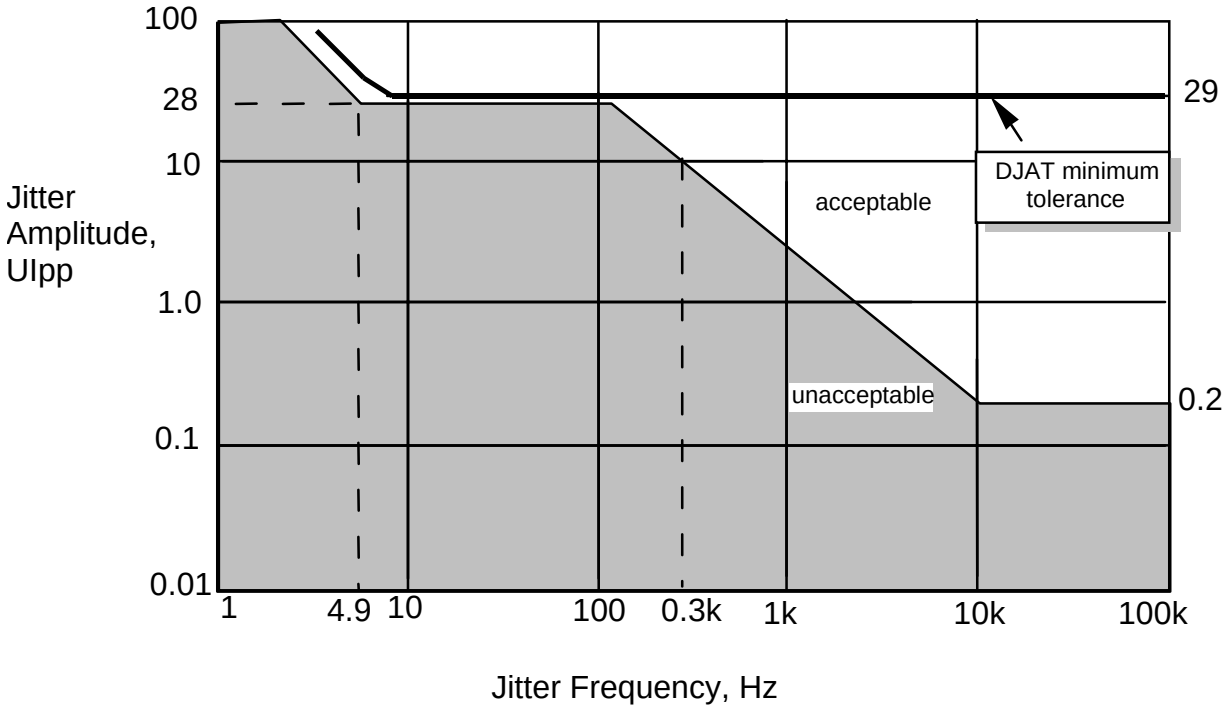
The DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 28 UIpp of input jitter at jitter frequencies above 6 Hz. For jitter frequencies below 6 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

DJAT exhibits negligible jitter gain for jitter frequencies below 6.6 Hz, and attenuates jitter at frequencies above 6.6 Hz by 20 dB per decade. In most applications the DJAT Block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (37.056 MHz) digital phase locked loop for transmit clock generation. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

### 8.23.2 Jitter Tolerance

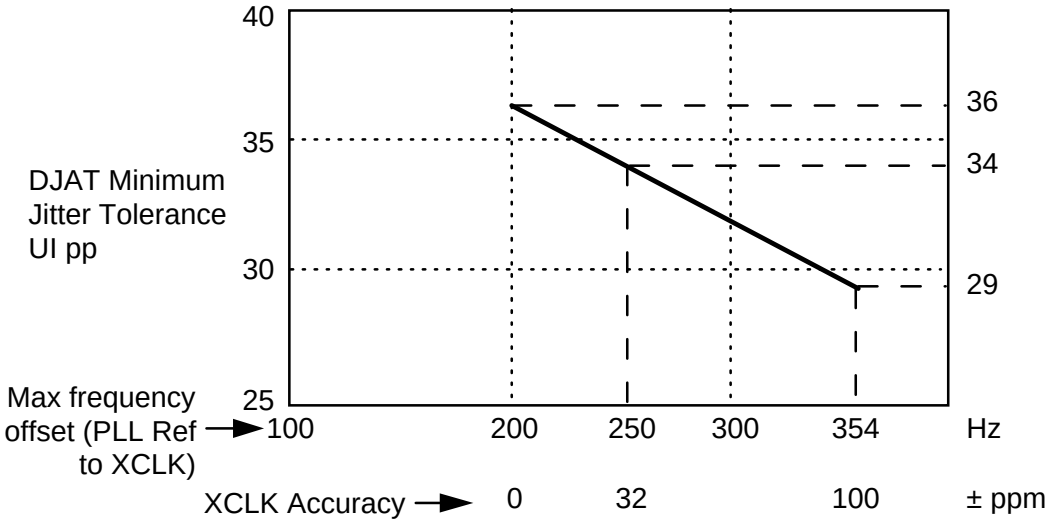
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

**Figure 8 - DJAT Jitter Tolerance**




The accuracy of the XCLK frequency and that of the DJAT PLL reference input clock used to generate the jitter-free TCLKO have an effect on the minimum jitter tolerance. Given that the DJAT PLL reference clock accuracy can be ±200 Hz from 1.544 MHz, and that the XCLK input accuracy can be ±100 ppm from 37.056 MHz, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK/24 are shown in Figure 9.

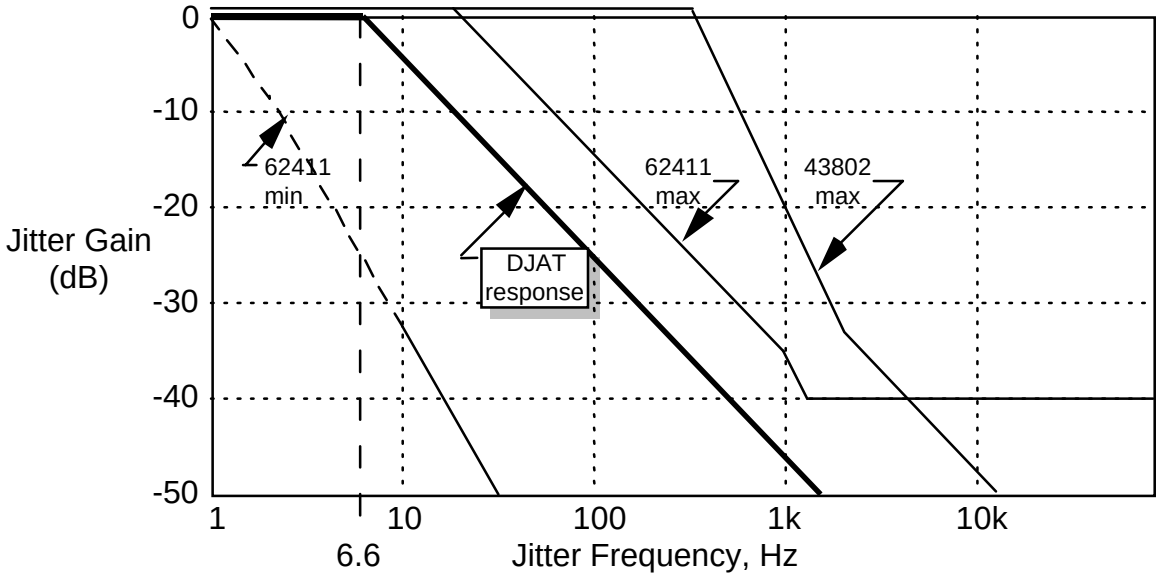
**Figure 9 - DJAT Minimum Jitter Tolerance vs XCLK Accuracy**




### 8.23.3 Jitter Transfer

The output jitter for jitter frequencies from 0 to 6.6 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 6.6 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 10 below:

**Figure 10 - DJAT Jitter Transfer**



### 8.23.4 Frequency Range

In the non-attenuating mode, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 to 1.608 MHz. The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (29 UIpp) and maximum XCLK frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or XCLK frequency offset.

## 8.24 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the DJAT TSB, the reference signal for the digital PLL, and the clock source used to derive the output TCLKO signal.

## 8.25 Digital DS-1 Transmit Interface (DTIF)

The Digital DS-1 Transmit Interface provides control over the various output options available on the multifunctional digital transmit pins TDP/TDD and TDN/TFLG. When configured for dual-rail output, the multifunctional pins become the TDP and TDN outputs. These outputs can be formatted as either return-to-zero (RZ) or non-return-to-zero (NRZ) signals and can be updated on either the rising or falling edge of TCLKO. When the interface is configured for single-rail output, the multifunctional pins become the TDD and TFLG outputs, which can be enabled to be updated on either the rising or falling TCLKO edge. Further, the TFLG output can be enabled to indicate FIFO empty or FIFO full status.

The DTIF block also provides Alarm Indication Signalling (AIS) generation capability by generating alternating mark signals on the TDP/TDN outputs, or all-ones on the TDD output, when the TAISEN bit is set in the Transmit DS1 Interface Configuration register. This is useful when the internal loopback modes are used.

## 8.26 Analog DSX-1 Pulse Generator (XPLS)

The Analog DSX-1 Pulse Generator function is provided by the XPLS block. This block converts Non Return to Zero (NRZ) pulses into Alternate Mark Inversion (AMI) line signals suitable for use in the DSX-1 intra-office environment. The dual-rail NRZ pulses are supplied by the DJAT block. A logical "1" on the TDP output from DJAT causes a positive pulse to be transmitted; a similar signal on the TDN output from DJAT causes a negative pulse to be transmitted. If both TDP and TDN are logical "0" or "1," no output pulse is transmitted.

The output pulse shape is synthesized digitally with an internal Digital to Analog (D/A) converter. The converter is updated at eight times the T1 rate with words stored in a ROM. These words define the output pulse shape.

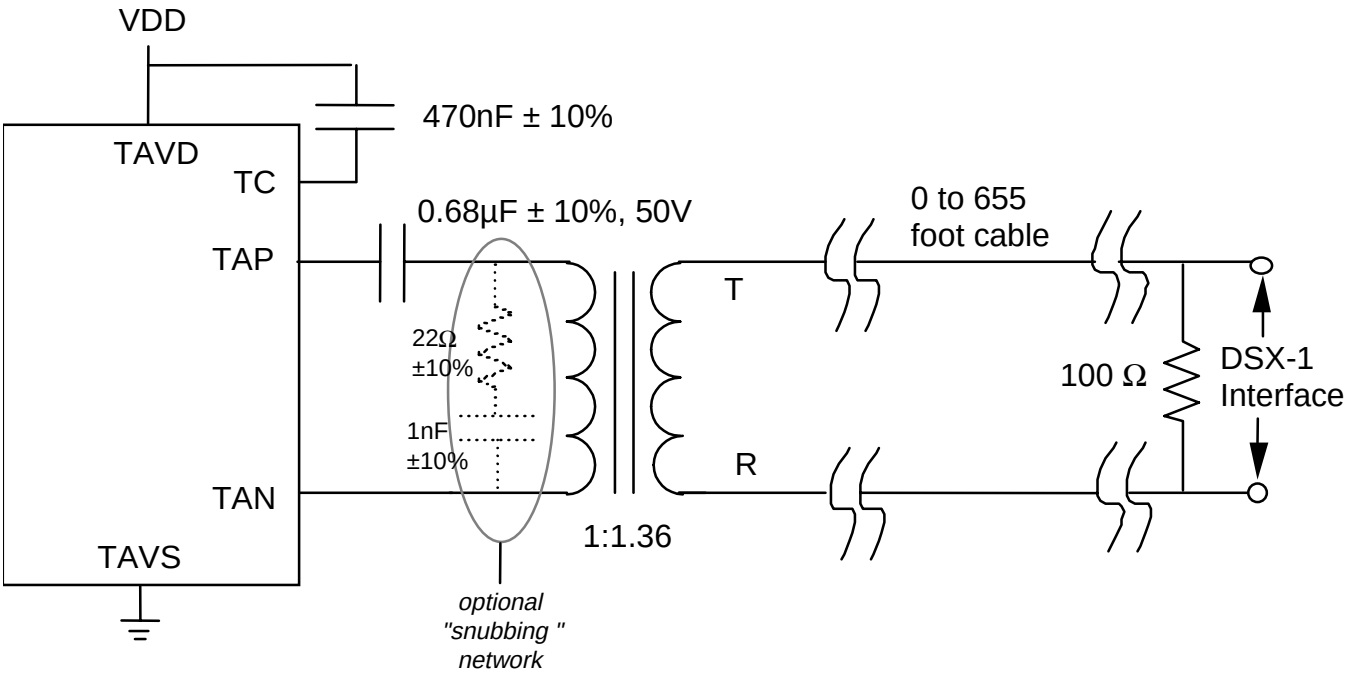
AMI signalling is created by exciting either the internal TIP or RING DRIVERS that drive a line-coupling transformer differentially via the TAP and TAN outputs. This differential driving scheme insures a small positive to negative pulse imbalance. The drivers, with the step-up transformer, amplify the output pulses to their final levels. The TIP and RING drivers also supply the high current capability required to drive the low impedance output load.

The cable length used in the link between the XPLS and the DSX-1 cross-connect greatly affects the resulting pulse shapes. This is compensated for by selecting from one of eight different pulse output shapes built into XPLS. For short line length settings, a small, negative-going spike may be observed on the falling edge of the DSX-1 pulse. This spike can be filtered out by using the optional "snubbing" network shown in Figure 11. This snubber network should not be required when driving longer lines.

The XPLS includes a driver performance monitor to detect nonfunctional links. Two monitor inputs, PM_TIP and PM_RING, are internally bonded to the XPLS's own TAP and TAN outputs. If no pulses are detected alternately across the PM_TIP or PM_RING monitor points for 62 or 63 consecutive TCLKO periods, the monitored link is declared failed. The exact threshold (62 or 63 pulses) depends on the line build-out and the pattern of bipolar violations. The XPLS can be programmed to produce an interrupt whenever the link monitor state changes.

The XPLS block provides Alarm Indication Signalling (AIS) generation capability by generating alternating mark signals on the link when the TAIS bit is programmed high. This is useful when the internal loopback modes are used.

**Figure 11 - External Analog Transmit Interface Circuit**




The transformer used should be designed for use in T1/CEPT/ISDN-PRI applications. Many manufacturers have standard products for these applications. Typical characteristics of a suitable transformer are given in the following table.

**Table 3 - Typical Characteristics of Transmit Transformer**

| Turns Ratio (PRI:SEC) | OCL (mH min.) | $C_{w/w}$ (pF max.) | $L_L$ (µH max.) | DCR pri. (Ω max.) | DCR sec. (Ω max.) |
|---|---|---|---|---|---|
| 1:1.36 | 1.20 | 35 | 0.80 | 0.80 | 1.2 |

Where OCL is the open-circuit inductance,

$C_{w/w}$ is the inter-winding capacitance,

$L_L$ is the leakage inductance, and

DCR is the DC resistance.

PMC-Sierra has verified the operation of the XPLS functional block with the following 1:1.36 transformers:

- Pulse Engineering PE64937 (1:1.36)
- Pulse Engineering PE65340 (1:1.36) (for extended temperature range)
- BH Electronics 500-1776 (1:1.36)

Many manufacturers produce dual transformers containing the1:2 CT and 1:1.36 transformers necessary for the receiver and transmitter circuits. PMC-Sierra has verified the operation of XPLS and RSLC with the following dual parts:

- Pulse Engineering PE64952
- Pulse Engineering PE65774 (for extended temperature range)
- BH Electronics 500-1777

## 8.27 Backplane Transmit Interface (BTIF)

The Backplane Transmit Interface allows data to be taken from a backplane in either a 1.544Mbit/s or a 2.048Mbit/s serial stream and allows BPV transparency by accepting dual-rail data input at 1.544Mbit/s.

When configured to receive a 1.544Mbit/s data rate stream, the block expects the input data stream on the BTPCM pin to contain 24 channel bytes of data followed by a single bit location for the framing bit. The BTSIG input pin must contain 24 bytes of signalling nibble data located in the least significant nibble of each byte followed by a single bit position for the framing bit. The framing alignment indication on the BTFP pin indicates the framing bit position of the 193-bit frame (or, optionally, the framing bit position of the first frame of the superframe, or every second superframe).

When configured to receive a 2.048Mbit/s data rate stream, the block internally gaps the 2.048MHz rate backplane clock to convert the serial PCM data on the BTPCM pin containing three channel bytes of data followed by one byte of "filler" (which can be logic "0" or logic "1") into an internal 1.544Mbit/s serial stream for transmission. The data stream on the BTSIG pin, containing three bytes of valid signalling nibbles (i.e. three channels' signalling contained in the least significant nibble of each of the three byte locations) followed by one byte of "filler", is similarly converted to an internal 1.544Mbit/s rate. The frame alignment indication provided on the BTFP pin must go to logic "1" for one BTCLK cycle during the first bit of the "filler" byte, indicating the next data byte is the first channel of the frame, or the first channel of the first frame of the superframe.

## 8.28 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the T1XC to be configured, controlled and monitored via internal registers.

# 9 REGISTER DESCRIPTION

## 9.1 Normal Mode Register Memory Map

| Address | Register |
|---|---|
| 00H | T1XC Receive Options |
| 01H | T1XC Receive Backplane Options |
| 02H | T1XC Datalink Options |
| 03H | T1XC Receive DS1 Interface Configuration |
| 04H | T1XC Transmit DS1 Interface Configuration |
| 05H | T1XC Transmit Backplane Options |
| 06H | T1XC Transmit Framing and Bypass Options |
| 07H | T1XC Transmit Timing Options |
| 08H | T1XC Master Interrupt Source #1 |
| 09H | T1XC Master Interrupt Source #2 |
| 0AH | T1XC Master Diagnostics |
| 0BH | T1XC Master Test |
| 0CH | T1XC Revision/Chip ID |
| 0DH | T1XC Master Reset |
| 0EH | T1XC Phase Status Word (LSB) |
| 0FH | T1XC Phase Status Word (MSB) |
| 10H | CDRC Configuration |
| 11H | CDRC Interrupt Enable |
| 12H | CDRC Interrupt Status |
| 13H | CDRC Reserved |
| 14H | XPLS Line Length Configuration |
| 15H | XPLS Control/Status |
| 16H | XPLS CODE Indirect Address |
| 17H | XPLS CODE Indirect Data |
| 18H | DJAT Interrupt Status |

| Address | Register |
|---|---|
| 19H | DJAT Reference Clock Divisor (N1) Control |
| 1AH | DJAT Output Clock Divisor (N2) Control |
| 1BH | DJAT Configuration |
| 1CH | ELST Configuration |
| 1DH | ELST Interrupt Enable/Status |
| 1EH | ELST Trouble Code |
| 1FH | ELST Reserved |
| 20H | FRMR Configuration |
| 21H | FRMR Interrupt Enable |
| 22H | FRMR Interrupt Status |
| 23H | FRMR Reserved |
| 24H | Reserved |
| 25H | Reserved |
| 26H | Reserved |
| 27H | Reserved |
| 28H | Reserved |
| 29H | Reserved |
| 2AH | RBOC Enable |
| 2BH | RBOC Code Status |
| 2CH | ALMI Configuration |
| 2DH | ALMI Interrupt Enable |
| 2EH | ALMI Interrupt Status |
| 2FH | ALMI Alarm Detection Status |
| 30H | TPSC Configuration |
| 31H | TPSC µP Access Status |
| 32H | TPSC Channel Indirect Address/Control |
| 33H | TPSC Channel Indirect Data Buffer |
| 34H | XFDL Configuration |

| Address | Register |
|---|---|
| 35H | XFDL Interrupt Status |
| 36H | XFDL Transmit Data |
| 37H | XFDL Reserved |
| 38H | RFDL Configuration |
| 39H | RFDL Interrupt Control/Status |
| 3AH | RFDL Status |
| 3BH | RFDL Receive Data |
| 3CH | IBCD Configuration |
| 3DH | IBCD Interrupt Enable/Status |
| 3EH | IBCD Activate Code |
| 3FH | IBCD Deactivate Code |
| 40H | SIGX Configuration |
| 41H | SIGX µP Access Status |
| 42H | SIGX Channel Indirect Address/Control |
| 43H | SIGX Channel Indirect Data Buffer |
| 44H | XBAS Configuration |
| 45H | XBAS Alarm Transmit |
| 46H | XIBC Control |
| 47H | XIBC Loopback Code |
| 48H | PMON Reserved |
| 49H | PMON Status |
| 4AH | PMON LCV Count (LSB) |
| 4BH | PMON LCV Count (MSB) |
| 4CH | PMON BEE Count (LSB) |
| 4DH | PMON BEE Count (MSB) |
| 4EH | PMON FER Count |
| 4FH | PMON OOF/COFA Count |
| 50H | RPSC Configuration |

| Address | Register |
|---|---|
| 51H | RPSC µP Access Status |
| 52H | RPSC TSC Channel Indirect Address/Control |
| 53H | RPSC Channel Indirect Data Buffer |
| 54H | PDVD Reserved |
| 55H | PDVD Interrupt Enable/Status |
| 56H | XBOC Reserved |
| 57H | XBOC Code |
| 58H | XPDE Reserved |
| 59H | XPDE Interrupt Enable/Status |
| 5AH-5BH | Reserved |
| 5CH | RSLC Reserved |
| 5DH | RSLC Interrupt Enable/Status |
| 5EH-7FH | Reserved |
| 80H-FFH | Reserved for Test |

# 10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the T1XC. Normal mode registers (as opposed to test mode registers) are selected when A[7] is low.

**Notes on Normal Mode Register Bits:**

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the T1XC to determine the programming state of the chip.

3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect T1XC operation unless otherwise noted.

## 10.1 Internal Registers

### Register 00H: T1XC Receive Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | UNF | 0 |
| Bit 5 | R/W | ELSTBYP | 0 |
| Bit 4 | R/W | TRSLIP | 0 |
| Bit 3 | R/W | SRPCM | 0 |
| Bit 2 | R/W | SRSFP | 0 |
| Bit 1 | R/W | ALTRFP | 0 |
| Bit 0 | R/W | CCOFA | 0 |

This register allows software to configure the receive functions of the T1XC.

UNF:

The UNF bit allows the T1XC to operate with unframed DS-1 data. When UNF is set to logic 1, the FRMR is disabled and the recovered data passes through the receiver section of the T1XC without frame or channel alignment. While UNF is held at logic 1, the Alarm Integrator continues to operate and detects and integrates RED and AIS alarm. When UNF is set to logic 0, the T1XC operates normally, searching for frame alignment on the incoming data.

ELSTBYP:

The ELSTBYP bit allows the Elastic Store (ELST) to be bypassed, eliminating the one frame delay incurred through the ELST. When set to logic 1, the received data and clock inputs to ELST are internally routed directly to the ELST outputs.

TRSLIP:

The TRSLIP bit allows the ELST to be used to measure, through SLIP indications, the frequency difference between the recovered receive line clock and the transmit clock driving the XBAS when the ELST is bypassed. When TRSLIP is set to logic 1, the transmit clock input to XBAS is internally substituted for the BRCLK input to the system side of the ELST. When TRSLIP is set to logic 0, the BRCLK input is routed to the system side of the ELST. The TRSLIP bit is valid only when ELSTBYP is set to logic 1.

SRPCM:

The SRPCM bit selects the output signal seen on the multifunction output RPCM/ RDPCM. When set to logic 1, the multifunction output becomes RPCM, the undecoded PCM output from the Clock and Data Recovery (CDRC) . When SRPCM is set to logic 0, the multifunction output becomes RDPCM, the B8ZS-decoded PCM output from the CDRC .

SRSFP:

The SRSFP bit selects the output signal seen on the multifunction output RFP. When set to logic 1, the multifunction output becomes RSFP, the receive superframe pulse indication, which pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the FRMR ). When SRSFP is set to logic 0, the multifunction output becomes RFP, which pulses high during each framing bit (i.e. every 193 bits).

ALTRFP:

The ALTRFP bit suppresses every second output pulse on the multifunction output RFP. When ALTRFP is set to logic 1, the output signal on RFP pulses every 386 bits, indicating every second framing bit (if the SRSFP bit is logic 0); or the output signal on RFP pulses every 24 or 48 frames (if the SRSFP bit is logic 1). When ALTRFP is set to logic 0, the output signal on RFP pulses in accordance to the SRSFP bit setting.

CCOFA:

The CCOFA bit determines whether the PMON counts Change-Of-Frame Alignment (COFA) events or out-of-frame (OOF ) events. When CCOFA is set to logic 1, COFA events are counted by PMON. When CCOFA is set to logic 0, OOF events are counted by PMON.

Upon reset of the T1XC, these bits are cleared to zero.

### Register 01H: T1XC Receive Backplane Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | ALTFDL | 0 |
| Bit 5 | R/W | RXDMAGAT | 0 |
| Bit 4 | R/W | BRX2M | 0 |
| Bit 3 | R/W | BRX2RAIL | 0 |
| Bit 2 | R/W | BRXSFP | 0 |
| Bit 1 | R/W | ALTBRFP | 0 |
| Bit 0 | R/W | RXMTKC | 0 |

This register allows software to configure the Receive backplane interface format of the T1XC.

ALTFDL:

The ALTFDL bit enables the framing bit position on the backplane PCM output to contain a copy of the FDL bit. When ALTFDL is set to logic 1, each M-bit value in the ESF-formatted stream is duplicated and replaces the subsequent CRC bit or F-bit in the output signal stream on BRPCM. When ALTFDL is set to logic 0, the output BRPCM stream contains the received M, CRC, or F bits in the framing bit position. Note that this function is only valid for ESF-formatted streams, ALTFDL should be set to logic 0 when other framing formats are being received.

RXDMAGAT:

The RXDMAGAT bit selects the gating of the RDLINT output with the RDLEOM output when the internal HDLC receiver is used with DMA. When RXDMAGAT is set to logic 1, the RDLINT DMA output is gated with the RDLEOM output so that RDLINT is forced to logic 0 when RDLEOM is logic 1. When RXDMAGAT is set to logic 0, the RDLINT and RDLEOM outputs operate independently.

BRX2M:

The BRX2M bit selects the 2.048 MHz data rate and format of the backplane data and frame alignment signals. When BRX2M is set to logic 1, the clock rate on the BRCLK input is expected to be 2.048MHz, and the data stream on BRPCM is output as 1 byte of "filler" followed by 3 bytes of channel data, repeated 8 times. When BRX2M is set to logic 0, the backplane data rate and

format is identical to T1 (i.e. 1.544MHz rate with 24 contiguous channel bytes followed by 1 framing bit).

BRX2RAIL:

The BRX2RAIL bit selects whether the backplane receive data signal on the multifunction outputs BRPCM/BRDP and BRSIG/BRDN are in either dual rail or single rail format. When BRX2RAIL is set to logic 1, the multifunction pins become the BRDP and BRDN dual rail outputs, which contain the received positive and negative line pulses timed to the 1.544MHz receive line rate, RCLKO. When BRX2RAIL is set to logic 0, the multifunction pins become the BRPCM and BRSIG digital outputs.

BRXSFP:

The BRXSFP bit selects the output signal seen on the backplane output BRFPO. When set to logic 1, the BRFPO output pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the FRMR ). When BRXSFP is set to logic 0, the BRFPO output pulses high during each framing bit (i.e. every 193 bits).

ALTBRFP:

The ALTBRFP bit suppresses every second output pulse on the backplane output BRFPO. When ALTBRFP is set to logic 1, the output signal on BRFPO pulses every 386 bits, indicating every second framing bit (if the BRXSFP bit is logic 0); or the output signal on BRFPO pulses every 24 or 48 frames (if the BRXSFP bit is logic 1). This latter setting (i.e. both ALTBRFP and BRXSFP set to logic 1) is useful for converting SF formatted data to ESF formatted data between two T1XC devices. When ALTBRFP is set to logic 0, the output signal on BRFPO pulses in accordance to the BRXSFP bit setting.

RXMTKC:

The RXMTKC bit allows global trunk conditioning to be applied to the received data and signalling streams, BRPCM and BRSIG. When RXMKTC is set to logic 1, the data on BRPCM for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC; similarly, the signalling data on BRSIG for each channel is replaced with the data contained in the signalling trunk conditioning registers. When RXMKTC is set to logic 0, the data and signalling signals are modified on a per-channel basis in accordance with the control bits contained in the per-channel control registers within the RPSC.

Upon reset of the T1XC, these bits are cleared to zero.

### Register 02H: T1XC Datalink Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RXDMASIG | 0 |
| Bit 6 | R/W | RXDCHAN | 0 |
| Bit 5 | R/W | TXDMASIG | 0 |
| Bit 4 | R/W | TXDCHAN | 0 |
| Bit 3 | R/W | RDLINTE | 0 |
| Bit 2 | R/W | RDLEOME | 0 |
| Bit 1 | R/W | TDLINTE | 0 |
| Bit 0 | R/W | TDLUDRE | 0 |

This register allows software to configure the datalink options of the T1XC.

RXDMASIG:

The RXDMASIG bit selects the internal HDLC receiver (RFDL) data-received interrupt (INT) and end-of-message (EOM) signals to be output on the RDLINT and RDLEOM pins when the RXDCHAN bit is logic 0. When RXDMASIG is set to logic 1, the RDLINT and RDLEOM output pins can be used by a DMA controller to process the datalink. When RXDMASIG is set to logic 0, the RFDL INT and EOM signals are no longer available to a DMA controller; the signals on RDLINT and RDLEOM become the extracted datalink data and clock, RDLSIG and RDLCLK. In this mode, the data stream available on the RDLSIG output corresponds to the extracted facility datalink in ESF, the extracted R-bit value of the sync word in T1DM, or the extracted Fs framing bits in SLC®96. When RXDCHAN is set to logic 1, the RXDMASIG bit has no effect.

RXDCHAN:

The RXDCHAN bit selects whether the Primary Rate D-Channel is extracted and made available on the RDLSIG output, or whether the RDLINT/RDLSIG and RDLEOM/RDLCLK pins operate as defined by the RXDMASIG bit. When RXDCHAN is set to logic 1, the D-Channel data (channel 24 of every frame) is output on RDLSIG and a burst clock is output on RDLCLK. When RXDCHAN is set to logic 0, the RDLINT/RDLSIG and RDLEOM/RDLCLK pins contain the signals selected by the RXDMASIG bit.

TXDMASIG:

The TXDMASIG bit selects the internal HDLC transmitter (XFDL) request for service interrupt (INT) and data underrun (UDR) signals to be output on the TDLINT and TDLUDR pins when the TXDCHAN bit is logic 0. When TXDMASIG is set to logic 1, the TDLINT and TDLUDR output pins can be used by a DMA controller to service the datalink. When TXDMASIG is set to logic 0, the XFDL INT and UDR signals are no longer available to a DMA controller; the signals on TDLINT and TDLUDR become the serial datalink data input and clock, TDLSIG and TDLCLK. In this mode an external controller is responsible for formatting the data stream presented on the TDLSIG input to correspond to the facility datalink in ESF, the R-bit value of the sync word in T1DM, or the Fs framing bits in SLC®96. When TXDCHAN is set to logic 1, the TXDMASIG bit has no effect.

TXDCHAN:

The TXDCHAN bit selects whether the Primary Rate D-Channel is inserted into channel 24 of each frame via the TDLSIG input, or whether the TDLINT/TDLSIG and TDLUDR/TDLCLK pins operate as defined by the TXDMASIG bit. When TXDCHAN is set to logic 1, the D-Channel data is expected on TDLSIG, sampled on the rising edge of a burst clock provided on TDLCLK. When TXDCHAN is set to logic 0, the TDLINT/TDLSIG and TDLUDR/TDLCLK pins contain the signals selected by the TXDMASIG bit.

RDLINTE:

The RDLINTE bit enables the RFDL received-data interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLINTE is set to logic 1, an event causing an interrupt in the RFDL (which is visible on the RDLINT output pin when RXDMASIG is logic 1 and RXDCHAN is logic 0) also causes an interrupt to be generated on the INTB output. When RDLINTE is set to logic 0, an interrupt event in the RFDL does not cause an interrupt on INTB.

RDLEOME:

The RDLEOME bit enables the RFDL end-of-message interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLEOME is set to logic 1, an end-of-message event causing an EOM interrupt in the RFDL (which is visible on the RDLEOM output pin when RXDMASIG is logic 1 and RXDCHAN is logic 0) also causes an interrupt to be generated on the INTB output. When RDLEOME is set to logic 0, an EOM interrupt event in the RFDL does not cause an interrupt on INTB. NOTE: within the RFDL, an end-of-message

event causes an interrupt on both the EOM and INT RFDL interrupt outputs. See the Operation section for further details on using the RFDL.

TDLINTE:

The TDLINTE bit enables the XFDL request for service interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLINTE is set to logic 1, an request for service interrupt event in the XFDL (which is visible on the TDLINT output pin when TXDMASIG is logic 1 and TXDCHAN is logic 0) also causes and interrupt to be generated on the INTB output. When TDLINTE is set to logic 0, an interrupt event in the XFDL does not cause an interrupt on INTB.

TDLUDRE:

The TDLUDRE bit enables the XFDL transmit data underrun interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLUDRE is set to logic 1, an underrun event causing an interrupt in the XFDL (which is visible on the TDLUDR output pin when TXDMASIG is logic 1 and TXDCHAN is logic 0) also causes and interrupt to be generated on the INTB output. When TDLUDRE is set to logic 0, an underrun event in the XFDL does not cause an interrupt on INTB.

Upon reset of the T1XC, these bits are cleared to zero.

### Register 03H: T1XC Receive DS1 Interface Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | SDOEN | 0 |
| Bit 5 | R/W | RDIEN | 0 |
| Bit 4 | R/W | RDNINV | 0 |
| Bit 3 | R/W | RDPINV | 0 |
| Bit 2 | R/W | RUNI | 0 |
| Bit 1 | R/W | RFALL | 0 |
| Bit 0 | R/W | RRZ | 0 |

This register enables the Receive DS1 Interface to handle the various input waveform formats.

SDOEN:

The SDOEN bit enables the sliced positive and negative pulses from the analog receive slicer to be visible on the SDP and SDN pins when the Analog DSX-1 Receive Slicer is active. When SDOEN is set to logic 1, the multifunction pins SDP/RDP/RDD and SDN/RDN/RLCV become the sliced positive and negative pulse outputs, SDP and SDN. Pulses will be seen on the SDP and SDN outputs if RSLC is powered up. When SDOEN is set to logic 0, the multifunction pins SDP/RDP/RDD and SDN/RDN/RLCV become the digital inputs, RDP/RDD and RDN/RLCV. The function of the digital inputs is determined by the RUNI bit.

RDIEN:

The RDIEN bit enables data received on the digital inputs, RDP/RDD and RDN/RLCV, to be used internally instead of the outputs from the Analog DSX-1 Receive Slicer. When RDIEN is set to logic 1 and SDOEN is set to logic 0, digital data input on the multifunction pins RDP/RDD and RDN/RLCV are handled in accordance with the remaining bit setting in this register and the resulting signals are used internally to drive the clock and data recovery block. When RDIEN is set to logic 0, the output signals from the analog RSLC are used internally to drive the CDRC block.

RDPINV,RDNINV:

The RDPINV and RDNINV bits enable the DS-1 Receive Interface to logically invert the signals received on multifunction pins SDP/RDP/RDD and

SDN/RDN/RLCV, respectively. When RDPINV is set to logic 1, the interface inverts the signal on the RDP/RDD input. When RDPINV is set to logic 0, the interface passes the RDP/RDD signal unaltered. When RDNINV is set to logic 1, the interface inverts the signal on the RDN/RLCV input. When RDNINV is set to logic 0, the interface passes the RDN/RLCV signal unaltered.

RUNI:

The RUNI bit enables the interface to receive uni-polar digital data and line code violation indications on the multifunction pins SDP/RDP/RDD and SDN/RDN/RLCV. When RUNI is set to logic 1, the SDP/RDP/RDD and SDN/RDN/RLCV multifunction pins become the data and line code violation inputs, RDD and RLCV, sampled on the selected RCLKI edge. When RUNI is set to logic 0, the SDP/RDP/RDD and SDN/RDN/RLCV multifunction pins become the positive and negative pulse inputs, RDP and RDN, sampled on the selected RCLKI edge.

RFALL:

The RFALL bit enables the DS-1 Receive Interface to sample the multifunction pins on the falling RCLKI edge. When RFALL is set to logic 1, the interface is enabled to sample either the RDD and RLCV inputs, or the RDP and RDN inputs, on the falling RCLKI edge. When RFALL is set to logic 0, the interface is enabled to sample the inputs on the rising RCLKI edge.

RRZ:

The RRZ bit configures the interface to receive return-to-zero formatted waveforms. When RRZ is set to logic 1, the interface is configured to pass the signals on the RDP and RDN inputs unaltered directly into the CDRC . The RCLKI input is ignored. When RRZ is set to logic 0, the interface is configured to sample either the RDD input or the RDP and RDN inputs on the RCLKI edge specified by the RFALL bit and generate an internal RZ representation of these inputs with duration equal to half the RCLKI period. The internally-generated RZ signals are then passed on to CDRC. The RRZ bit is only valid when RUNI is set to logic 0.

When the system is reset, the contents of the register are set to logic 0, enabling the analog Receive Slicer Interface to handle the incoming DSX-1 signal.

### Register 04H: T1XC Transmit DS1 Interface Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | FIFOBYP | 0 |
| Bit 6 | R/W | TAISEN | 0 |
| Bit 5 | R/W | TDNINV | 0 |
| Bit 4 | R/W | TDPINV | 0 |
| Bit 3 | R/W | TUNI | 0 |
| Bit 2 | R/W | FIFOFULL | 0 |
| Bit 1 | R/W | TRISE | 0 |
| Bit 0 | R/W | TRZ | 0 |

This register enables the Transmit DS1 Interface to generate the required digital output waveform format.

FIFOBYP:

The FIFOBYP bit enables the transmit bi-polar input signals to DJAT to be bypassed around the FIFO to the bi-polar outputs. When jitter attenuation is not being used, and the XPLS pulse driver is being driven with a "jitter-free" 12.352MHz clock on TCLKI, the DJAT FIFO can be bypassed to reduce the delay through the transmitter section by typically 24 bits. NOTE: under this condition, the BTCLK signal must be synchronous to the TCLKI. When FIFOBYP is set to logic 1, the bi-polar inputs to DJAT are routed around the FIFO and directly into XPLS. When FIFOBYP is set to logic 0, the bi-polar transmit data passes through the DJAT FIFO.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TDP/TDD and TDN/TFLG multifunction pins. When TAISEN is set to logic 1 and TUNI is set to logic 0, the bi-polar TDP and TDN outputs are forced to pulse alternately, creating an all-ones signal; when TAISEN and TUNI are both set to logic 1, the uni-polar TDD output is forced to all-ones. When TAISEN is set to logic 0, the TDP/TDD and TDN/TFLG multifunction outputs operate normally. The transition to transmitting AIS on the TDP and TDN outputs is done in such a way as to not introduce any bi-polar violations.

TDPINV,TDNINV:

The TDPINV and TDNINV bits enable the DS-1 Transmit Interface to logically invert the signals output on the TDP/TDD and TDN/TFLG multifunction pins,

respectively. When TDPINV is set to logic 1, the TDP/TDD output is inverted. When TDPINV is set to logic 0, the TDP/TDD output is not inverted. When TDNINV is set to logic 1, the TDN/TFLG output is inverted. When TDNINV is set to logic 0, the TDN/TFLG output is not inverted.

TUNI:

The TUNI bit enables the transmit interface to generate uni-polar digital outputs on the TDP/TDD and TDN/TFLG multifunction pins. When TUNI is set to logic 1, the TDP/TDD and TDN/TFLG multifunction pins become the unipolar outputs TDD and TFLG, updated on the selected TCLKO edge. When TUNI is set to logic 0, the TDP/TDD and TDN/TFLG multifunction pins become the bipolar outputs TDP and TDN, also updated on the selected TCLKO edge. When the TUNI bit is set to logic 1 (unipolar mode), the analog transmit data outputs, TAP and TAN, from the XPLS block cannot be used.

FIFOFULL:

The FIFOFULL bit determines the indication given on the TFLG output pin. When FIFOFULL is set to logic 1, the TFLG output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming full. When FIFOFULL is set to logic 0, the TFLG output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming empty.

TRISE:

The TRISE bit configures the interface to update the multifunction outputs on the rising edge of TCLKO. When TRISE is set to logic 1, the interface is enabled to update the TDP/TDD and TDN/TFLG output pins on the rising TCLKO edge. When TRISE is set to logic 0, the interface is enabled to update the outputs on the falling TCLKO edge.

TRZ:

The TRZ bit configures the interface to transmit bipolar return-to-zero formatted waveforms. When TRZ is set to logic 1, the interface is enabled to generate the TDP and TDN output signals as RZ waveforms with duration equal to half the TCLKO period. When TRZ is set to logic 0, the interface is enabled to generate the TDP and TDN output signals as NRZ waveforms with duration equal to the TCLKO period, updated on the selected edge of TCLKO. The TRZ bit can only be used when TUNI and TRISE are set to logic 0.

When the system is reset, the contents of the register are set to logic 0, enabling the Transmit Interface to output NRZ formatted positive and negative pulse data on the TDP and TDN outputs, updated on the falling TCLKO edge.

### Register 05H: T1XC Transmit Backplane Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | ABXXEN | 0 |
| Bit 3 | R/W | BTXCLK | 0 |
| Bit 2 | R/W | BTX2M | 0 |
| Bit 1 | R/W | BTX2RAIL | 0 |
| Bit 0 | R/W | BTXSFP | 0 |

This register allows software to configure the Transmit backplane interface format of the T1XC.

ABXXEN:

The ABXXEN bit selects the format of the BTSIG transmit signalling input signal. When ABXXEN is set to logic 1, BTSIG is expected to contain only the A and B signalling bits in the upper two bit positions of the lower nibble of each channel (i.e. ABXX), with the lower two bit positions being "Don't Cares". When ABXXEN is set to logic 0, BTSIG is expected to contain all four signalling bit in the lower nibble of each channel (i.e. ABCD), or it is expected to contain the A and B bits duplicated in the lower nibble (i.e. ABAB).

BTXCLK:

The BTXCLK bit selects the source of the XBAS transmit clock input signal. When BTXCLK is set to logic 1, the XBAS transmit clock is driven with the 1.544MHz recovered PCM output clock (RCLKO) from the receiver section. When BTXCLK is set to logic 0, the XBAS transmit clock is driven with the 1.544MHz backplane transmit clock (BTCLK), or the internal "gapped" clock derived from the 2.048MHz BTCLK. Note that this bit must be set to logic 1 when Line Loopback is enabled.

BTX2M:

The BTX2M bit selects the 2.048 MHz data rate and format of the backplane transmit data and frame alignment signals. When BTX2M is set to logic 1, the clock rate on the BTCLK input is expected to be 2.048 MHz, and the data stream on BTPCM and BTSIG is expected to be formatted as 1 byte of "filler" followed by 3 bytes of channel data, repeated 8 times. When BTX2M is set to

logic 0, the backplane transmit data rate and format is identical to T1 (i.e. 1.544MHz rate with 24 contiguous channel bytes followed by 1 framing bit).

BTX2RAIL:

The BTX2RAIL bit selects whether the backplane transmit data signal presented to the transmitter on the multifunction inputs BTPCM/BTDP and BTSIG/BTDN are in either dual-rail or single-rail format. When BTX2RAIL is set to logic 1, the multifunction pins become the BTDP and BTDN dual-rail inputs, which bypass the XBAS and input directly into the jitter attenuator. It is expected that the framing bits be already inserted into the dual-rail streams before they are input on BTDP and BTDN. When BTX2RAIL is set to logic 0, the multifunction pins become the BTPCM and BTSIG digital inputs. The dual-rail mode works correctly only when the backplane data rate is set to 1.544 MHz.

BTXSFP:

The BTXSFP bit selects the type of backplane frame alignment signal presented to the transmitter BTFP input. When BTXSFP is set to logic 1, a pulse on the BTFP indicates the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the XBAS ). When BTXSFP is set to logic 0, a pulse on the BTFP indicates each framing bit. If the signalling aligner is used to ensure signalling bit integrity while XBAS generates an arbitrary superframe alignment between the backplane and the transmit DS-1 stream (i.e. SIGAEN is logic 1 and TXSIGA is logic 1 in register 06H), then BTXSFP must be set to logic 0. If the superframe alignment of the backplane is to be enforced on the transmit DS-1 stream, the BTXSFP bit must be set to logic 1. In this case the signalling aligner is unnecessary.

Upon reset of the T1XC, these bits are cleared to zero.

### Register 06H: T1XC Transmit Framing and Bypass Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | SIGAEN | 0 |
| Bit 4 | R/W | TXSIGA | 0 |
| Bit 3 | R/W | FDIS | 0 |
| Bit 2 | R/W | FBITBYP | 0 |
| Bit 1 | R/W | CRCBYP | 0 |
| Bit 0 | R/W | FDLBYP | 0 |

This register allows software to configure the bypass options of the transmitter, the use and location of the Signalling Alignment block, and controls the global transmit framing disable.

SIGAEN:

The SIGAEN bit enables the operation of the signalling aligner (SIGA) to ensure superframe alignment between the backplane and either the receive or transmit DS-1 streams. When set to logic 1, the SIGA is inserted into the signalling bit data path either after the SIGX or before the XBAS , as selected by the TXSIGA register bit. When the signalling aligner is used, the backplane frame alignment indication must also be changed to indicate superframe alignment for either the receive or transmit backplane, based on the value of TXSIGA. When SIGAEN is set to logic 0, the SIGA is removed from the circuit and the TXSIGA bit is ignored.

TXSIGA:

The TXSIGA bit selects the location of the signalling aligner. When set to logic 1, the SIGA is inserted into the signalling bit data path before the XBAS. When set to logic 0, the SIGA is inserted into the data path after the SIGX.

FDIS:

The FDIS bit allows the framing generation through the XBAS to be disabled and the transmit data to pass through the XBAS unchanged. When FDIS is set to logic 1, XBAS is disabled from generating framing. When FDIS is set to logic 0, XBAS is enabled to generate and insert the framing into the transmit data.

FBITBYP:

The FBITBYP bit allows the frame synchronization bit in the input data stream, BTPCM, to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FBITBYP is set to logic 1, the input frame synchronization bit is re-inserted into the output data stream. When FBITBYP is set to logic 0, the XBAS is allowed to generate the output frame synchronization bits.

CRCBYP:

The CRCBYP bit allows the framing bit corresponding to the CRC-6 bit position in the input data stream, BTPCM, to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When CRCBYP is set to logic 1, the input CRC-6 bit is re-inserted into the output data stream. When CRCBYP is set to logic 0, the XBAS is allowed to generate the output CRC-6 bits.

FDLBYP:

The FDLBYP bit allows the framing bit corresponding to the facility data link bit position in the input data stream, BTPCM, to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FDLBYP is set to logic 1, the input FDL bit is re-inserted into the output data stream. When FDLBYP is set to logic 0, the XBAS is allowed to generate the output FDL bit.

Upon reset of the T1XC, these bits are cleared to zero.

### Register 07H: T1XC Transmit Timing Options

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | HSBPSEL | 0 |
| Bit 6 | R/W | XCLKSEL | 0 |
| Bit 5 | R/W | OCLKSEL1 | 0 |
| Bit 4 | R/W | OCLKSEL0 | 0 |
| Bit 3 | R/W | PLLREF1 | 0 |
| Bit 2 | R/W | PLLREF0 | 0 |
| Bit 1 | R/W | TCLKISEL | 0 |
| Bit 0 | R/W | SMCLKO | 0 |

This register allows software to configure the options of the transmit timing section.

HSBPSEL:

The HSBPSEL bit selects the source of the high-speed clock used in the ELST, SIGX, TPSC, and RPSC blocks. This allows the T1XC to interface to higher rate backplanes (>2.048MHz, externally gapped, or 2.048MHz, internally gapped). Note, however, that the externally gapped instantaneous backplane clock frequency must not exceed 3.0MHz. When HSBPSEL is set to logic 1, the XCLK input signal is divided by 2 and used as the high-speed clock to these blocks. XCLK must be driven with 37.056MHz. When HSBPSEL is set to logic 0, the high-speed clock is driven with the internal 12.352MHz clock source selected by the XCLKSEL bit.

XCLKSEL:

The XCLKSEL bit selects the source of the high-speed clock used in the CDRC, FRMR, and PMON blocks. When XCLKSEL is set to logic 1, the XCLK input signal is used as the high-speed clock to these blocks. XCLK must be driven with 12.352MHz. When XCLKSEL is set to logic 0, the high-speed clock is driven with the internal DJAT generated smooth 12.352MHz clock source. XCLK must be driven with 37.056MHz.

OCLKSEL1, OCLKSEL0:

The OCLKSEL[1:0] bits select the source of the Digital Jitter Attenuator FIFO output clock signal. When OCLKSEL1 is set to logic 1, the DJAT FIFO output clock is driven with the input data clock driving the DJAT ICLK input. In this mode the jitter attenuation is disabled and the input clock must be jitter-free.

When OCLKSEL1 is set to logic 0, the DJAT FIFO output clock is driven with either the TCLKI input clock or an internal smooth 1.544MHz clock, as selected by the OCLKSEL0 bit. When OCLKSEL0 is set to logic 1, the DJAT FIFO output clock is driven with the TCLKI input clock. When OCLKSEL0 is set to logic 0, the DJAT FIFO output clock is driven with the internal smooth 1.544MHz clock selected by the TCLKISEL and SMCLKO bits.

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Digital Jitter Attenuator phase locked loop reference signal as follows:

**Table 4 - PLLREF[1:0] Options**

| PLLREF1 | PLLREF0 | Source of PLL Reference |
|---|---|---|
| 0 | 0 | Transmit clock used by XBAS ( either the 1.544MHz BTCLK, the gapped clock derived from the 2.048MHz BTCLK, or the 1.544MHz RCLKO, as selected by BTXCLK and BTX2M) |
| 0 | 1 | BTCLK input |
| 1 | 0 | RCLKO output |
| 1 | 1 | TCLKI input |

TCLKISEL,SMCLKO:

The TCLKISEL and SMCLKO bits select the source of the internal smooth 1.544MHz and 12.352MHz output clock signals. When TCLKISEL and SMCLKO are set to logic 0, the internal 1.544MHz and 12.352MHz clock signals are driven by the smooth 1.544MHz and 12.352MHz clock sources generated by DJAT. When TCLKISEL is set to logic 0 and SMCLKO is set to logic 1, the internal 1.544MHz clock signal is driven by the TCLKI input signal divided by 8, and the internal 12.352MHz clock signal is driven by the TCLKI input signal. When TCLKISEL and SMCLKO are set to logic 1, the internal 1.544MHz clock signal is driven by the XCLK input signal divided by 8, and the internal 12.352MHz clock signal is driven by the XCLK input signal. The combination of TCLKISEL set to logic 1 and SMCLKO set to logic 0 should not be used.

The following table illustrates the required bit settings for these various clock sources to affect the transmitted data:

**Table 5 - Transmit Clock Options**

| Input Transmit Data | Bit Settings | XCLK Freq | Affect on Output Transmit Data |
|---|---|---|---|
| Backplane transmit data timed to 1.544 MHz BTCLK. | HSBPSEL =0<br>XCLKSEL =0<br>OCLKSEL1 =0<br>OCLKSEL0 =0<br>PLLREF1 =0<br>PLLREF0 =X<br>TCLKISEL =0<br>SMCLKO =0<br>PLLREF1 =1<br>PLLREF0 =0<br>PLLREF1 =1<br>PLLREF0 =1 | 37.056MHz | Jitter attenuated. TCLKO is a smooth 1.544MHz.<br>TCLKO referenced to BTCLK.<br>TCLKO referenced to RCLKO.<br>TCLKO referenced to TCLKI. |
| Backplane transmit data timed to 2.048MHz BTCLK. Internal transmit clock is "gapped". | HSBPSEL =1<br>XCLKSEL =0<br>OCLKSEL1 =0<br>OCLKSEL0 =0<br>PLLREF1 =0<br>PLLREF0 =0<br>TCLKISEL =0<br>SMCLKO =0<br>PLLREF1 =0<br>PLLREF0 =1<br>PLLREF1 =1<br>PLLREF0 =0<br>PLLREF1 =1<br>PLLREF0 =1 | 37.056MHz | Jitter attenuated. TCLKO is a smooth 1.544MHz.<br>TCLKO referenced to internal "gapped" transmit clock.<br>TCLKO referenced to 2.048MHz BTCLK.<br>TCLKO referenced to RCLKO.<br>TCLKO referenced to TCLKI. |

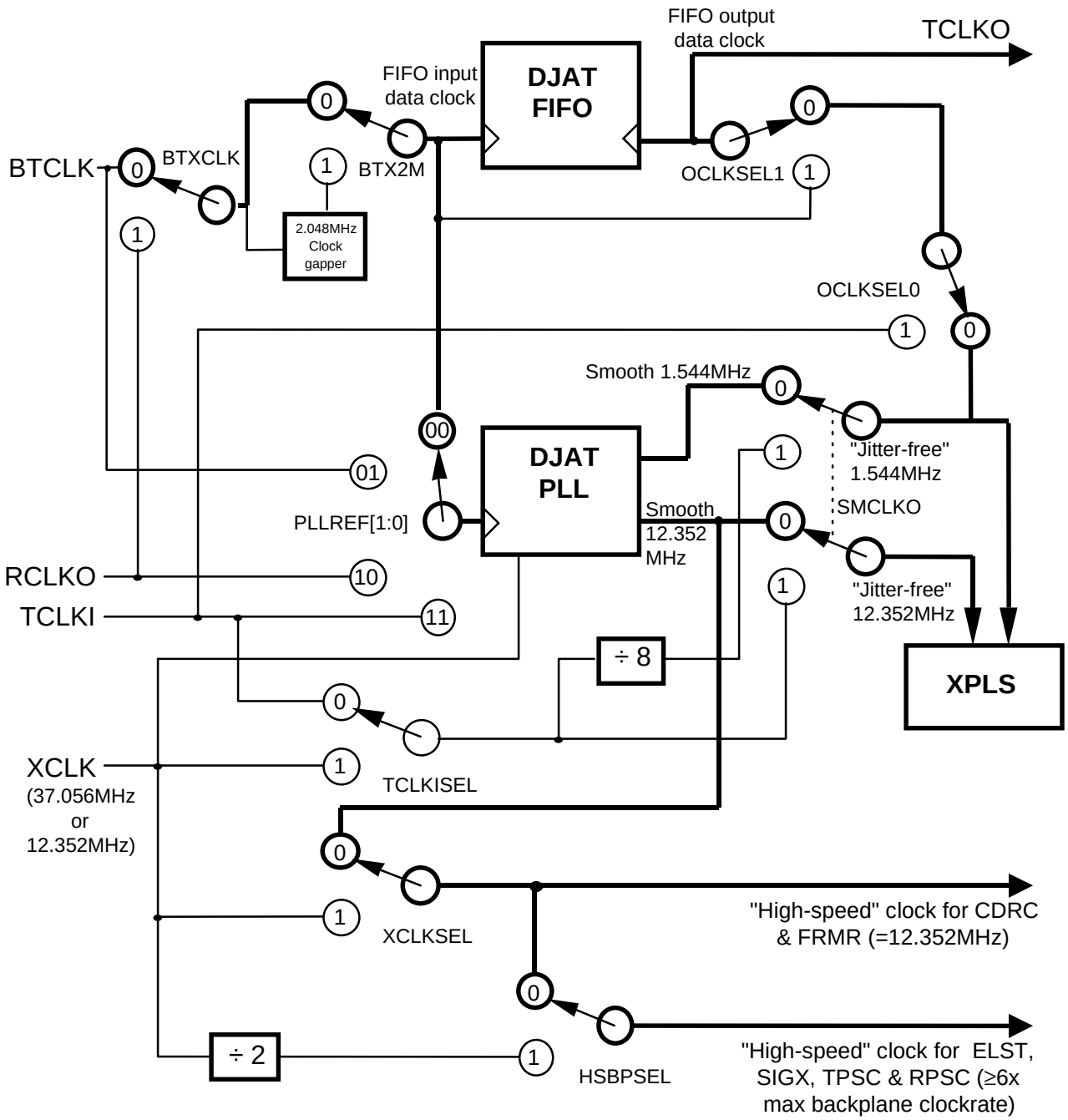
| Input Transmit Data | Bit Settings | XCLK Freq | Affect on Output Transmit Data |
|---|---|---|---|
| Backplane transmit data timed to >2.048MHz backplane clock. BTCLK is externally "gapped". | HSBPSEL =1<br>XCLKSEL =0<br>OCLKSEL1 =0<br>OCLKSEL0 =0<br>PLLREF1 =0<br>PLLREF0 =X<br>TCLKISEL =0<br>SMCLKO =0<br>PLLREF1 =1<br>PLLREF0 =0<br>PLLREF1 =1<br>PLLREF0 =1 | 37.056MHz | Jitter attenuated. TCLKO is a smooth 1.544MHz.<br>TCLKO referenced to externally "gapped" transmit clock.<br>TCLKO referenced to RCLKO.<br>TCLKO referenced to TCLKI. |
| Backplane transmit data timed to BTCLK. | HSBPSEL =0<br>XCLKSEL =0<br>OCLKSEL1 =1<br>OCLKSEL0 =X<br>PLLREF1 =X<br>PLLREF0 =X<br>TCLKISEL =0<br>SMCLKO =0<br>XCLKSEL =1<br>TCLKISEL =1<br>SMCLKO =1 | 37.056MHz<br><br>12.352MHz | No jitter attenuation. TCLKO is equal to internal transmit clock, either BTCLK, gapped BTCLK, or RCLKO.<br>Same as above. |

| Input Transmit Data | Bit Settings | XCLK Freq | Affect on Output Transmit Data |
|---|---|---|---|
| Backplane transmit data timed to BTCLK. | HSBPSEL =0<br>XCLKSEL =0<br>OCLKSEL1 =0<br>OCLKSEL0 =1<br>PLLREF1 =X<br>PLLREF0 =X | 37.056MHz | No jitter attenuation. TCLKO is equal to TCLKI (useful for higher rate MUX applications). |
| | TCLKISEL =0<br>SMCLKO =0<br>XCLKSEL =1<br>TCLKISEL =1<br>SMCLKO =1 | 12.352MHz | Same as above. |
| Backplane transmit data timed to BTCLK. | HSBPSEL =0<br>XCLKSEL =0<br>OCLKSEL1 =0<br>OCLKSEL0 =0<br>PLLREF1 =X | 37.056MHz | TCLKI is a jitter-free 12.352MHz clock. TCLKO is equal to TCLKI÷8. |
| | PLLREF0 =X<br>TCLKISEL =0<br>SMCLKO =1<br>XCLKSEL =1 | 12.352MHz | Same as above. |
| Backplane transmit data timed to BTCLK. | HSBPSEL =0<br>XCLKSEL =1<br>OCLKSEL1 =0<br>OCLKSEL0 =0<br>PLLREF1 =X<br>PLLREF0 =X<br>TCLKISEL =1<br>SMCLKO =1 | jitter-free 12.352MHz | XCLK is a jitter-free 12.352MHz clock. TCLKO is equal to XCLK÷8. |

Note that where a gapped backplane transmit clock is used, the DJAT SYNC bit must be disabled. Where DJAT is unused, the DJAT SYNC, CENT and LIMIT bits must be disabled.

Upon reset of the T1XC, the Transmit Timing Options bits are cleared to zero, selecting digital jitter attenuation with TCLKO referenced to the backplane transmit clock, BTCLK. The following Figure 12 illustrates the various bit setting options, with the reset condition highlighted.

**Figure 12 - Transmit Timing Options**



### Register 08H: T1XC Master Interrupt Source #1

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R | IBCD | 0 |
| Bit 5 | R | FRMR | 0 |
| Bit 4 | R | PDVD | 0 |
| Bit 3 | R | ELST | 0 |
| Bit 2 | R | RFDL | 0 |
| Bit 1 | R | RBOC | 0 |
| Bit 0 | R | ALMI | 0 |

This register allows software to determine the block which produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

### Register 09H: T1XC Master Interrupt Source #2

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R | DJAT | 0 |
| Bit 4 | R | XPDE | 0 |
| Bit 3 | R | RSLC | 0 |
| Bit 2 | R | XPLS | 0 |
| Bit 1 | R | XFDL | 0 |
| Bit 0 | R | CDRC | 0 |

This register allows software to determine the block which produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

### Register 0AH: T1XC Master Diagnostics

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | PAYLB | 0 |
| Bit 4 | R/W | LINELB | 0 |
| Bit 3 | R/W | DMLB | 0 |
| Bit 2 | R/W | DDLB | 0 |
| Bit 1 | R/W | TXMFP | 0 |
| Bit 0 | R/W | TXDIS | 0 |

This register allows software to enable the diagnostic mode of the T1XC.

PAYLB:

The PAYLB bit selects the payload loopback mode, where the received data output from the ELST is internally connected to the transmit data input of the XBAS. The data read out of ELST is timed to the transmitter clock, and the transmit frame alignment is used to synchronize the output frame alignment of ELST. During payload loopback, the data output on BRPCM is forced to logic 1. When PAYLB is set to logic 1, the payload loopback mode is enabled. When PAYLD is set to logic 0, the loopback mode is disabled. Payload loopback will only function if the input signals BTSIG, BTCLK and BTFP are active.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered positive and negative pulse outputs from the CDRC block are internally connected to the digital inputs of the DJAT. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, the contents of the DJAT Reference Clock Divisor and Output Clock Divisor registers must be reprogrammed to decimal 47 to correctly attenuate the jitter on the 1.544 MHz receive clock, the BTXCLK bit in register 05H must be set to logic 1 to select the RCLKO clock as the transmit clock source, and the Timing Options Register settings should be reviewed to ensure the options are such that data will pass error-free and "jitter"-free through DJAT (typically, the default setting, 00H, for register 7 will be appropriate for line loopback).

Note that when DJAT is not being used (e.g. where a 12.352 or 16.384 MHz XCLK is used), TCLKI must be synchronized with RCLKO for error free operation of Line Loopback.

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the digital positive and negative RZ pulse outputs from DJAT are internally connected to the receive positive and negative pulse inputs of CDRC. When DDLB is set to logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled. If diagnostic digital loopback is to be used, the TUNI bit must be set to logic 0 in the Transmit DS1 Interface Configuration register, and the RUNI bit must be set to logic 0 in the Receive DS1 Interface Configuration register.

DMLB:

The DMLB bit enables the diagnostic metallic loopback mode, where the digital, RZ positive and negative sliced versions of the analog signals output on the TAP and TAN pins from XPLS are internally connected to the receive positive and negative pulse inputs of CDRC. Some line build-outs require large negative pulses in order to satisfy the template at the far end of the line. However, as DMLB is essentially a zero-line-length loopback, the 0-110' line length template should be selected if DMLB is to be used. When DMLB is set to logic 1, the diagnostic metallic loopback mode is enabled. When DMLB is set to logic 0, the diagnostic metallic loopback mode is disabled. If diagnostic metallic loopback is to be used, the TUNI bit must be set to logic 0 in the Transmit DS1 Interface Configuration register, and the RUNI bit must be set to logic 0 in the Receive DS1 Interface Configuration register.

TXMFP:

The TXMFP bit introduces a mimic framing pattern in the digital output of the basic transmitter by forcing a copy of the current framing bit into bit location 1 of the frame, thereby creating a mimic pattern in the bit position immediately following the correct framing bit. When TXMFP is set to logic 1, the mimic framing pattern is generated. When TXMFP is set to logic 0, no mimic pattern is generated.

TXDIS:

The TXDIS bit provides a method of suppressing the output of the basic transmitter. When TXDIS is set to logic 1, the digital output of XBAS is disabled by forcing it to logic 0. When TXDIS is set to logic 0, the digital output of XBAS is not suppressed.

Upon reset of the T1XC, these register bits are cleared to zero.

### Register 0BH: T1XC Master Test

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | W | PMCTST | X |
| Bit 3 | W | DBCTRL | 0 |
| Bit 2 | R/W | IOTST | 0 |
| Bit 1 | W | HIZDATA | 0 |
| Bit 0 | R/W | HIZIO | 0 |

This register is used to select T1XC test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the T1XC ; a software reset of the T1XC does not affect the state of the bits in this register.

PMCTST:

The PMCTST bit is used to configure the T1XC for PMC's manufacturing tests. When PMCTST is set to logic 1, the T1XC microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the T1XC to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the T1XC for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the T1XC . While the HIZIO bit is a logic 1, all output pins of the T1XC except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

### Register 0CH: T1XC Revision/Chip ID

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | TYPE | 0 |
| Bit 6 | R | ID[6] | 0 |
| Bit 5 | R | ID[5] | 0 |
| Bit 4 | R | ID[4] | 0 |
| Bit 3 | R | ID[3] | 0 |
| Bit 2 | R | ID[2] | 0 |
| Bit 1 | R | ID[1] | 1 |
| Bit 0 | R | ID[0] | 0 |

The version identification bits, ID[6:0], are set to a fixed value representing the version number of the T1XC.

The chip identification bit, TYPE, is set to logic 0 representing the T1XC.

### Register 0DH: T1XC Master Reset

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R/W | RESET | 0 |

The RESET bit implements a software reset. If the RESET bit is a logic 1, the entire T1XC is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the T1XC out of reset. Holding the T1XC in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

### Register 0EH: T1XC Phase Status Word (LSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | PSB[7] | X |
| Bit 6 | R | PSB[6] | X |
| Bit 5 | R | PSB[5] | X |
| Bit 4 | R | PSB[4] | X |
| Bit 3 | R | PSB[3] | X |
| Bit 2 | R | PSB[2] | X |
| Bit 1 | R | PSB[1] | X |
| Bit 0 | R | PSB[0] | X |

This register contains the least significant byte, PSB[7:0], of the 9-bit phase status word. The 9-bit phase status word indicates the relative phase difference between the received DS-1 line timing (available on RCLKO) and a system timing which uses either a 2.048MHz backplane (input on BRCLK, with BRX2M=1 in Reg. 00H) or a 1.544MHz backplane (input on BRCLK, with BRX2M=0). By utilizing the value of the phase status word, the system timing can be locked to the receive line timing via an external software controlled phase-locked-loop.

The least significant 8 bits contained in this register indicate a count value (either 0-255 for BRX2M=1 or 0-192 for BRX2M=0) of the number of system backplane clock cycles between successive 125µs frame pulses. The most significant 5 bits (PSB[7:3]) represent a channel number (0-31 for BRX2M=1 or 0-23 for BRX2M=0) and the least significant 3 bits (PSB[2:0]) represent the bit number within the channel (0-7). The count value corresponds to the location within the system frame where the receive line-timed frame pulse occurred. If the received line clock frequency is higher on average than the system clock frequency, the phase status word value will be seen to decrease during successive register reads. If the received line clock frequency is lower on average than the system clock frequency, the phase status word value will be seen to increase during successive register reads.

The 9th bit of the Phase Status Word indicates the "frame count" and will toggle when two successive 8-bit counter values straddle a frame boundary. The PSB[8] bit will toggle when the bit and channel count indicated by PSB[7:0] exceeds channel 31, bit 7 (when BRX2M=1; or channel 23, bit 7 when BRX2M=0) or the count goes below channel 0, bit 0. This is determined by comparing the PSB[7:5] bits of the current phase status word value to those of

the previous word value; PSB[8] is toggled only under the following conditions (all other bit value transitions leave PSB[8] unchanged):

**Table 6 - Phase Status Word Operation**

| Previous PSB[7:5] | Current PSB[7:5] | Affect on PSB[8] |
|---|---|---|
| 000 | 11X | toggle |
| 000 | 1X1 | toggle |
| 11X | 000 | toggle |
| 1X1 | 000 | toggle |

The contents of the Phase Status Word registers (address 0EH and 0FH) are internally updated on each receive line data frame pulse; a write to either T1XC register address 0EH or 0FH must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. write to register address 0EH or 0FH

2. read register address 0FH (read Phase Status Word MSB)

3. read register address 0EH (read Phase Status Word LSB)

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

### Register 0FH: T1XC Phase Status Word (MSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R | PSB[8] | X |

This register contains the most significant bit of the 9-bit phase status word.

The PSB[8] bit toggles when the bit and channel count (from the Phase Status Word LSB register) exceeds channel 31, bit 7 (channel 23, bit 7 when BRX2M=0) or goes below channel 0, bit 0.

The contents of the Phase Status Word registers (address 0EH and 0FH) are internally updated on each receive line data frame pulse; a write to either T1XC register address 0EH or 0FH must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. write to register address 0EH or 0FH

2. read register address 0FH (read Phase Status Word MSB)

3. read register address 0EH (read Phase Status Word LSB)

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

### Register 10H: CDRC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | AMI | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | ALGSEL | 0 |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

AMI:

The alternate mark inversion (AMI) bit specifies the line code of the incoming DS1 signal. A logic 1 selects AMI line code; a logic 0 selects B8ZS line code.

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5UIpp for jitter frequencies above 20KHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20KHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4UIpp at the higher frequencies.

Note that in Line Loopback mode (Register 0AH, LINELB bit =1) AGSEL should be set to logic 0 for optimal performance.

### Register 11H: CDRC Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | LCVE | 0 |
| Bit 6 | R/W | LOSE | 0 |
| Bit 5 | R/W | B8ZSE | 0 |
| Bit 4 | R/W | Z8DE | 0 |
| Bit 3 | R/W | Z16DE | 0 |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The bit positions LCVE,LOSE,B8ZSE, Z8DE and Z16DE (bits 7 to 3) of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, B8ZS Pattern, 8 Zeros, or 16 Zeros), either singly or in combination, are enabled to generate an interrupt on the microprocessor INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

When the T1XC is reset, LCVE,LOSE,B8ZSE, Z8DE, and Z16DE are set to logic 0, disabling these events from generating an interrupt.

### Register 12H: CDRC Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | LCVI | X |
| Bit 6 | R | LOSI | X |
| Bit 5 | R | B8ZSI | X |
| Bit 4 | R | Z8DI | X |
| Bit 3 | R | Z16DI | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R | LOS | X |

The bit positions LCVI,LOSI,B8ZSI, Z8DI, and Z16DI (bits 7 to 3) of this register indicate which of the status events generated an interrupt. A logic 1 in these bit positions indicate that the corresponding event was detected and generated an interrupt; a logic 0 in these bit positions indicate that no corresponding event has been detected. The bit positions LCVI, B8ZSI, Z8DI, and Z16DI are set on the assertion of the corresponding event. LOSI is set on any change of state of the LOS alarm. Bits LCVI, LOSI, B8ZSI, Z8DI, and Z16DI are cleared by reading this register. The current state of the LOS alarm can be determined by reading bit 0 of this register.

### Register 14H: XPLS Line Length Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | RPT | 0 |
| Bit 6 | R/W | SM | 0 |
| Bit 5 | R | 0 | 0 |
| Bit 4 | R | 1 | 1 |
| Bit 3 | R | 0 | 0 |
| Bit 2 | R/W | ILS[2] | 0 |
| Bit 1 | R/W | ILS[1] | 0 |
| Bit 0 | R/W | ILS[0] | 0 |

This register allows software to select the length of cable that XPLS is required to drive and to enable generation of user-programmable output templates.

RPT:

The RPT bit enables the 4-bit DAC codes contained in the Register Programmable Template CODE registers to generate the output waveform. When RPT is set to a logic 1, the internal user-programmable XPLS CODE registers supply the DAC codes used to generate the waveform. When RPT is set to logic 0, the DAC codes contained in the internal ROM generate the output waveform in accordance with the line length selected.

SM:

The SM bit allows software to select one of eight waveform templates by enabling the ILS[2:0] select bits. When SM is set to logic 1, the ILS[2:0] bit positions select one of eight waveform templates. When SM is set to logic 0, the ILS[2:0] bits are ignored and the default 330-440 ft. waveform template is selected.

The eight available templates are selected via the following values of ILS[2:0]:

**Table 7 - Transmit Line Length Options**

| ILS[2:0] | Length (ft.) |
|---|---|
| 000 | 0-110 |
| 001 | 110-220 |
| 011 | 220-330 |
| 010 | 330-440 |
| 110 | 440-550 |
| 111 | 550-660 |
| 101 | >660 |
| 100 | square |

The >660 setting is used when driving very long lines. The square pulse template allows the use of external line buildout networks with the T1XC.

### Register 15H: XPLS Control/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | TAIS | 0 |
| Bit 2 | R | DPMV | X |
| Bit 1 | R | DPMI | X |
| Bit 0 | R/W | DPME | 0 |

TAIS:

The TAIS bit enables the XPLS to generate an unframed all-ones AIS alarm on the TAP and TAN output pins. When TAIS is set to logic 1, the outputs are forced to pulse alternately, creating an all-ones signal. When TAIS is set to logic 0, the outputs operate normally. The transition to transmitting AIS is done in such a way as to not introduce any bi-polar violations.

DPMV:

The DPMV bit reflects the current state of the DPM alarm signal.

DPMI:

The DPMI bit is set to logic 1 when any change of state occurs on the Driver Performance Monitor (DPM) alarm signal. This bit is cleared when the register is read.

DPME:

The DPME bit controls the generation of an interrupt on the microprocessor INTB pin by the driver performance monitor portion of XPLS. When DPME is set to logic 1, an interrupt is generated on INTB whenever an alarm condition occurs on the driver performance monitor points. A driver performance monitor alarm is declared whenever a period of 62 or 63 consecutive bit periods with no pulses on either the TAP or TAN output pins occurs. The exact threshold (62 or 63 bit periods) depends on the line build-out and the pattern of bipolar violations. When DPME is set to logic 0, detection of a driver performance monitor alarm condition is disabled from generating an interrupt.

### Register 16H: XPLS CODE Indirect Address

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | CRA2 | 0 |
| Bit 1 | R/W | CRA1 | 0 |
| Bit 0 | R/W | CRA0 | 0 |

This register allows software to select any one of the eight internal waveform CODE registers, addressed by the CRA[2:0] bits, for subsequent access through the CODE Indirect Data register. When accessing the internal CODE registers, the address of the desired register must first be written to this register. Then, by reading or writing the Indirect Data register (Register 17H), the microprocessor can either read from or write to the internal register identified by the CRA[2:0] bits.

The CRA[2:0] bits address the internal registers as follows:

**Table 8 - XPLS Internal Code Register Map**

| CRA2 | CRA1 | CRA0 | Internal Code Register |
|---|---|---|---|
| 0 | 0 | 0 | CODE register #0 - first code applied |
| 0 | 0 | 1 | CODE register #1 |
| 0 | 1 | 0 | CODE register #2 |
| 0 | 1 | 1 | CODE register #3 |
| 1 | 0 | 0 | CODE register #4 |
| 1 | 0 | 1 | CODE register #5 |
| 1 | 1 | 0 | CODE register #6 |
| 1 | 1 | 1 | CODE register #7 - last code applied |

See the Operation section for more details on setting up custom waveform templates.

### Register 17H: XPLS CODE Indirect Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | CRD3 | 0 |
| Bit 2 | R/W | CRD2 | 0 |
| Bit 1 | R/W | CRD1 | 0 |
| Bit 0 | R/W | CRD0 | 0 |

This register allows software to access the contents of any one of the eight internal waveform CODE registers, addressed by the CRA[2:0] bits in the CODE Indirect Address register. When accessing the internal CODE registers, the address of the desired register must first be written to the Indirect Address register (Register 16H). Then, by reading or writing the Indirect Data register, the microprocessor can either read from or write to the internal register identified by the CRA[2:0] bits.

The value read from or written to the internal CODE registers is contained in the CRD[3:0] bits. CRD3 is the most significant bit.

See the Operation section for more details on setting up custom waveform templates.

### Register 18H: DJAT Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R | OVRI | X |
| Bit 0 | R | UNDI | X |

This register contains the indication of the DJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When UNDI is a logic 1, an overrun event has occurred. OVRI is cleared by a read to this register.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. UNDI is cleared by a read to this register.

### Register 19H: DJAT Reference Clock Divisor (N1) Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | N1[7] | 0 |
| Bit 6 | R/W | N1[6] | 0 |
| Bit 5 | R/W | N1[5] | 1 |
| Bit 4 | R/W | N1[4] | 0 |
| Bit 3 | R/W | N1[3] | 1 |
| Bit 2 | R/W | N1[2] | 1 |
| Bit 1 | R/W | N1[1] | 1 |
| Bit 0 | R/W | N1[0] | 1 |

This register defines an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the DJAT PLL reference clock input (DJAT REF). The DJAT REF divisor magnitude, (N1+1), is the ratio between the frequency of the DJAT REF input and the frequency applied to the phase discriminator input. If the SYNC bit is set to logic 1 in Register 1Bh, the Clock Divisors N1 and N2 (Registers19h and 1Ah) must be set such that N1+1 and N2+1 are both multiples of 48.

Writing to this register will reset the PLL and, if the SYNC bit in the DJAT Configuration register is high, will also reset the FIFO.

Upon reset of the T1XC, the default value of N1 is set to decimal 47 (2FH).

### Register 1AH: DJAT Output Clock Divisor (N2) Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | N2[7] | 0 |
| Bit 6 | R/W | N2[6] | 0 |
| Bit 5 | R/W | N2[5] | 1 |
| Bit 4 | R/W | N2[4] | 0 |
| Bit 3 | R/W | N2[3] | 1 |
| Bit 2 | R/W | N2[2] | 1 |
| Bit 1 | R/W | N2[1] | 1 |
| Bit 0 | R/W | N2[0] | 1 |

This register defines an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the DJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input. If the SYNC bit is set to logic 1 in Register 1Bh, the Clock Divisors N1 and N2 (Registers19h and 1Ah) must be set such that N1+1 and N2+1 are both multiples of 48.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Upon reset of the T1XC, the default value of N2 is set to decimal 47 (2FH).

### Register 1BH: DJAT Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | WIDEN | 1 |
| Bit 4 | R/W | CENT | 0 |
| Bit 3 | R/W | UNDE | 0 |
| Bit 2 | R/W | OVRE | 0 |
| Bit 1 | R/W | SYNC | 1 |
| Bit 0 | R/W | LIMIT | 1 |

This register controls the operation of the DJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

WIDEN:

The WIDEN bit controls the width of the generated DSX-1 pulse from the XPLS block. When WIDEN is set to logic 1, the high phase of one cycle of the smooth, 12.352 MHz clock generated by the DJAT PLL is modified to be nominally 27ns wider. This results in the XPLS producing an enhanced DSX-1 pulse width. When WIDEN is set to logic 0, the smooth, 12.352MHz clock from DJAT is not modified, resulting in DSX-1 pulses of minimum allowable width. These narrow pulses reduce the amount of energy sourced by T1XC into the line. The WIDEN bit has no effect when the DJAT PLL is not used (i.e. the SMCLKO bit in register 7 is set to logic 1); if an enhanced width DSX-1 pulse is desired under this condition, the externally applied 12.352MHz clock phase must be explicitly modified before it is applied to the T1XC.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. When using the 2Mbit/s transmit backplane option, the SYNC bit must be set to logic 0. If the SYNC bit is set to logic 1, the Clock Divisors N1 and N2 (Registers19h and 1Ah) must be set such that N1+1 and N2+1 are both multiples of 48.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Upon reset of the T1XC, the LIMIT and SYNC bits are set to logic 1, and the OVRE, UNDE, and CENT bits are set to logic 0.

### Register 1CH: ELST Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | ACCEL | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | IR | 0 |
| Bit 0 | R/W | OR | 0 |

This register controls the format of the expected input frame to the ELST and the format of the generated output frame from the ELST.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

IR:

The IR bit selects the input frame format. The IR bit must be cleared to logic 0 to properly handle the T1 frame format being input into the ELST. SETTING IR TO LOGIC 1 IS A RESERVED SETTING AND SHOULD NOT BE USED.

OR:

The OR bit selects the output frame format. The OR bit must be cleared to properly generate the T1 frame format output from the ELST. SETTING OR TO LOGIC 1 IS A RESERVED SETTING AND SHOULD NOT BE USED.

Upon reset of the T1XC, these bits are set to logic 0.

### Register 1DH: ELST Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | SLIPE | 0 |
| Bit 1 | R | SLIPD | X |
| Bit 0 | R | SLIPI | X |

SLIPE:

The SLIPE bit position enables generation of an interrupt on the microprocessor INTB pin when a slip event occurs.

SLIPI:

The SLIPI bit indicates whether a slip event has occurred since the last read of the Enable/Status register. SLIPI is a logic 1 if a slip has occurred; SLIPI is a logic 0 is no slip has occurred. The SLIPI bit is cleared after the register is read.

SLIPD:

The SLIPD bit indicates the direction of the last slip when SLIPI is a logic 1. If a slip has occurred and the SLIPD bit is a logic 1 then the slip was due to the frame buffer becoming full. If a slip has occurred and the SLIPD bit is a logic 0 then the slip was due to the frame buffer becoming empty.

Upon reset of the T1XC, SLIPE is set to logic 0, disabling generation of an interrupt.

### Register 1EH: ELST Trouble Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D7 | 1 |
| Bit 6 | R/W | D6 | 1 |
| Bit 5 | R/W | D5 | 1 |
| Bit 4 | R/W | D4 | 1 |
| Bit 3 | R/W | D3 | 1 |
| Bit 2 | R/W | D2 | 1 |
| Bit 1 | R/W | D1 | 1 |
| Bit 0 | R/W | D0 | 1 |

This register allows the Trouble Code, transmitted in place of channel data when the framer is out of frame, to be programmed to any 8-bit value. A common requirement during a out of frame condition is to insert all ones in the channel data, therefore, the Trouble Code register is set to all ones when the T1XC is reset. The code is transmitted from MSB (D7) to LSB (D0).

The writing of the trouble code pattern into the register is asynchronous with respect to the clocks within the T1XC. One channel of trouble code data will always be corrupted if the register is written while the receiver is out of frame.

### Register 20H: FRMR Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | M2O[1] | 0 |
| Bit 6 | R/W | M2O[0] | 0 |
| Bit 5 | R/W | ESFFA | 0 |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

This register selects the framing format and the frame loss criteria used by the FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF, SLC®96, and ESF framing formats. A logic 00 selects 2 of 4 framing bits in error; a logic 01 selects 2 of 5 bits in error; a logic 10 selects 2 of 6 bits in error. In T1DM framing format, the ratio of errored to total framing bits before declaring out of frame is always 4 out of 12. A logic 11 in the M2O[1:0] bits is reserved and should not be used.

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR does not declare inframe while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF:

The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either standard superframe, T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 or 11 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format.

When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the facility data link data. A logic 00 in these bits enable the FRMR to receive FDL data at the full 4 kHz rate from every odd frame. A logic 01 in these bits enable the FRMR to receive FDL data at a 2 kHz rate from frames 3,7,11,15,19,23. A logic 10 in these bits enable the FRMR to receive FDL data at a 2 kHz rate from frames 1,5,9,13,17,21. Logic value 11 is reserved and should not be used.

The valid combinations of the ESFFA, ESF, FMS1, and FMS0 bits are summarized in the table below:

**Table 9 - FRMR Frame Format Options**

| ESF | FMS1 | FMS0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Select SF framing format |
| 0 | 0 | 1 | Select T1DM framing format |
| 0 | 1 | 0 | Select SLC96 framing format |
| 0 | 1 | 1 | Select T1DM framing format |
| 1 | 0 | 0 | Select ESF framing format & 4 kHz FDL Data Rate |
| 1 | 0 | 1 | Select ESF framing format & 2 kHz FDL Data Rate using frames 3,7,11,15,19,23. |
| 1 | 1 | 0 | Select ESF framing format & 2 kHz FDL Data Rate using frames 1,5,9,13,17,21 |
| 1 | 1 | 1 | RESERVED |

### Register 21H: FRMR Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | R/W | ACCEL | 0 |
| Bit 5 | R/W | COFAE | 0 |
| Bit 4 | R/W | FERE | 0 |
| Bit 3 | R/W | BEEE | 0 |
| Bit 2 | R/W | SFEE | 0 |
| Bit 1 | R/W | MFPE | 0 |
| Bit 0 | R/W | INFRE | 0 |

This register selects which of the MFP, COFA, FER, BEE, SFE, or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as framing bit errors for SF formatted data, CRC-6 mismatch errors for ESF formatted data, Ft bit errors for SLC®96 formatted data, and either framing bit errors or sync word errors

for T1DM formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt. When BEEE is set to logic 0, bit error events are disabled from generating an interrupt.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF, ESF, or SLC®96 formatted data, and 2 or more framing bit errors or sync word errors during the current superframe for T1DM formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the framer is now "inframe". When INFRE is set to logic 1, the assertion or deassertion of the "inframe" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "inframe" state is disabled from generating an interrupt.

Upon reset of the T1XC, these bits are set to logic 0, disabling the generation of interrupts.

### Register 22H: FRMR Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | COFAI | X |
| Bit 6 | R | FERI | X |
| Bit 5 | R | BEEI | X |
| Bit 4 | R | SFEI | X |
| Bit 3 | R | MFPI | X |
| Bit 2 | R | INFRI | X |
| Bit 1 | R | MFP | X |
| Bit 0 | R | INFR | X |

This register indicates whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. This register also indicates whether a mimic framing pattern was detected or whether there was a change in the "inframe" state of the frame circuitry.

COFAI,FERI,BEEI,SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the "inframe" state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP,INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

### Register 2AH: RBOC Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | IDLE | 0 |
| Bit 1 | R/W | AVC | 0 |
| Bit 0 | R/W | BOCE | 0 |

This register selects the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt on the microprocessor INTB pin when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

### Register 2BH: RBOC Code Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | IDLEI | X |
| Bit 6 | R | BOCI | X |
| Bit 5 | R | BOC[5] | X |
| Bit 4 | R | BOC[4] | X |
| Bit 3 | R | BOC[3] | X |
| Bit 2 | R | BOC[2] | X |
| Bit 1 | R | BOC[1] | X |
| Bit 0 | R | BOC[0] | X |

This register indicates the current state value of the BOC[5:0] bits and indicates whether an interrupt was generated by a change in the code value.

IDLEI:

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates whether an interrupt was generated by the detection of a valid BOC. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

When the T1XC is reset, the BOC[5:0] bits are set to logic 1, and the BOCI and IDLEI bits are set to logic 0.

### Register 2CH: ALMI Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

This register allows selection of the framing format and the data rate of the Facility Data Link in ESF to allow operation of the CFA detection algorithms.

ESF:

The ESF bit selects either extended superframe format or enables the frame mode select bits to select either regular superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, "alternate" T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format; and a logic 11 in these bit positions enable the "alternate" T1DM framing format. The "alternate" T1DM framing format configures the ALMI to process the RED ALARM as if the SF, SLC®96, or ESF framing format were selected; the YELLOW ALARM is still processed as T1DM.

When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the Facility Data Link (FDL) data. A logic 00 in these bits enables the ALMI to receive FDL data and validate the YELLOW alarm at the full 4 kbit rate. A logic 01 or 10 in these bits enables the ALMI to receive FDL data and validate the YELLOW alarm at a 2 kbit rate.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

**Table 10 - ALMI Frame Format Options**

| ESF | FMS1 | FMS0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Select Superframe framing format |
| 0 | 0 | 1 | Select T1DM framing format |
| 0 | 1 | 0 | Select SLC-96 framing format |
| 0 | 1 | 1 | Select "alternate" T1DM mode |
| 1 | 0 | 0 | Select ESF framing format & 4 kbit FDL Data Rate |
| 1 | 0 | 1 | Select ESF framing format & 2 kbit FDL Data Rate |
| 1 | 1 | 0 | Select ESF framing format & 2 kbit FDL Data Rate. |
| 1 | 1 | 1 | RESERVED |

### Register 2DH: ALMI Interrupt Enable

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | FASTD | 0 |
| Bit 3 | R/W | ACCEL | 0 |
| Bit 2 | R/W | YELE | 0 |
| Bit 1 | R/W | REDE | 0 |
| Bit 0 | R/W | AISE | 0 |

This register selects which of the three CFA's can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of RED and AIS alarms. When FASTD is set to a logic 1, deassertion of RED alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, RED and AIS alarm deassertion times remain as defined in the ALMI description.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

YELE,REDE,AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of YELLOW, RED, and AIS CFA's can be enabled to generate an interrupt.

Upon reset of the T1XC, these bits are cleared to logic 0.

### Register 2EH: ALMI Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R | YELI | X |
| Bit 4 | R | REDI | X |
| Bit 3 | R | AISI | X |
| Bit 2 | R | YEL | X |
| Bit 1 | R | RED | X |
| Bit 0 | R | AIS | X |

This register indicates which of the three CFA's generated an interrupt when their logic state changed in bit positions 5 through 3; and indicates the current state of each CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change has occurred. Both the status bit positions (bits 5 through 3) and the interrupt generated because of the change in CFA state are cleared to logic 0 when this register is read.

### Register 2FH: ALMI Alarm Detection Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R | REDD | X |
| Bit 1 | R | YELD | X |
| Bit 0 | R | AISD | X |

This register indicates the presence or absence of one or more OOF occurrences within the last 40ms; the presence or absence of the YELLOW ALARM signal over the last 40ms; and indicates the presence or absence of the AIS ALARM signal over the last 60ms.

REDD:

When REDD is a logic 1, one or more out of frame events have occurred during the last 40ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40ms interval.

YELD:

When YELD is logic 1, a valid YELLOW signal was present during the last 40ms interval. When YELD is logic 0, the YELLOW signal was absent during the last 40ms interval. For each framing format, a valid YELLOW signal is deemed to be present if:

- bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for SF and SLC®96 framing formats;
- the Y-bit is not logic 0 for 4 or fewer times during the 40 ms interval for T1DM framing format;
- the 16-bit YELLOW bit oriented code is received error-free 8 or more times during the interval for ESF framing format with a 4 kHz data link;
- the 16-bit YELLOW bit oriented code is received error-free 4 or more times during the interval for ESF framing format with a 2 kHz data link.

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60ms interval. When AISD is logic 0, the AIS signal was absent during the last 60ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received PCM data stream is not logic 0 for 126 or fewer times.

### Register 30H: TPSC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | IND | 0 |
| Bit 0 | R/W | PCCE | 0 |

This register allows selection of the microprocessor read access type and output enable control for the Transmit Per-channel Serial Controller.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the T1XC is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, each channel's PCM Control byte, IDLE Code byte, and SIGNALLING Control byte are passed on to the XBAS. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

### Register 31H: TPSC µP Access Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BUSY | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

### Register 32H: TPSC Channel Indirect Address/Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | R/WB | 0 |
| Bit 6 | R/W | A6 | 0 |
| Bit 5 | R/W | A5 | 0 |
| Bit 4 | R/W | A4 | 0 |
| Bit 3 | R/W | A3 | 0 |
| Bit 2 | R/W | A2 | 0 |
| Bit 1 | R/W | A1 | 0 |
| Bit 0 | R/W | A0 | 0 |

This register allows the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, an write to the internal TPSC register is requested.

### Register 33H: TPSC Channel Indirect Data Buffer

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D7 | 0 |
| Bit 6 | R/W | D6 | 0 |
| Bit 5 | R/W | D5 | 0 |
| Bit 4 | R/W | D4 | 0 |
| Bit 3 | R/W | D3 | 0 |
| Bit 2 | R/W | D2 | 0 |
| Bit 1 | R/W | D1 | 0 |
| Bit 0 | R/W | D0 | 0 |

This register contains either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-channel functions on the Transmit PCM data, provide the per-channel Transmit IDLE Code, and provide the per-channel Transmit signalling control and the alternate signalling bits. The functions are allocated within the registers as follows:

**Table 11 - TPSC Indirect Register Map**

| | |
|---|---|
| 01H | PCM Data Control byte for Channel 1 |
| 02H | PCM Data Control byte for Channel 2 |
| • | • |
| • | • |
| • | • |
| 17H | PCM Data Control byte for Channel 23 |
| 18H | PCM Data Control byte for Channel 24 |
| 19H | IDLE Code byte for Channel 1 |
| 1AH | IDLE Code byte for Channel 2 |
| • | • |
| • | • |
| • | • |
| 2FH | IDLE Code byte for Channel 23 |
| 30H | IDLE Code byte for Channel 24 |
| 31H | SIGNALLING Control byte for Channel 1 |
| 32H | SIGNALLING Control byte for Channel 2 |
| • | • |
| • | • |
| • | • |
| 47H | SIGNALLING Control byte for Channel 23 |
| 48H | SIGNALLING Control byte for Channel 24 |

The bits within each control byte are allocated as follows:

### TPSC Internal Registers 01-18H: PCM Data Control byte

| Bit | Type | Function |
|---|---|---|
| Bit 7 | R/W | INVERT |
| Bit 6 | R/W | IDLC |
| Bit 5 | R/W | DMW |
| Bit 4 | R/W | SIGNINV |
| Bit 3 | | Unused |
| Bit 2 | | Unused |
| Bit 1 | R/W | ZCS0 |
| Bit 0 | R/W | ZCS1 |

INVERT:

When the INVERT bit is set to a logic 1, data from the BTPCM input is inverted for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit from the BTPCM input is inverted for that channel.

The INVERT and SIGNINV can be used to produce the following types of inversions:

**Table 12 - TPSC INVERT and SIGNINV Functions**

| INVERT | SIGNINV | Effect on PCM Channel Data |
|---|---|---|
| 0 | 0 | PCM Channel data is unchanged |
| 1 | 0 | All 8 bits of the PCM channel data are inverted |
| 0 | 1 | Only the MSB of the PCM channel data is inverted (SIGN bit inversion) |
| 1 | 1 | All bits EXCEPT the MSB of the PCM channel data is inverted (Magnitude inversion) |

IDLC:

When the IDLC bit is set to a logic 1, data from the IDLE Code Byte replaces the BTPCM input data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the BTPCM input data for the duration of that channel.

Data inversion, idle and digital milliwatt insertion are performed independent of the transmit framing format selected. Digital milliwatt insertion takes precedence over idle code insertion which, in turn, takes precedence over the various data inversions.

ZCS0, ZCS1:

The ZCS[1:0] bits select the zero code suppression used as follows:

**Table 13 - TPSC Zero Code Suppression Options**

| ZCS1 | ZCS0 | Description |
|---|---|---|
| 0 | 0 | No Zero Code Suppression |
| 0 | 1 | GTE Zero Code Suppression ("jammed bit 8", except in signalling frames when "jammed bit 7" is used if the signalling bit is 0) |
| 1 | 0 | DDS Zero Code Suppression (data byte replaced with "10011000") |
| 1 | 1 | Bell Zero Code Suppression ("jammed bit 7") |

### TPSC Internal Registers 19-30H: IDLE Code byte

| Bit | Type | Function |
|---|---|---|
| Bit 7 | R/W | IDLE7 |
| Bit 6 | R/W | IDLE6 |
| Bit 5 | R/W | IDLE5 |
| Bit 4 | R/W | IDLE4 |
| Bit 3 | R/W | IDLE3 |
| Bit 2 | R/W | IDLE2 |
| Bit 1 | R/W | IDLE1 |
| Bit 0 | R/W | IDLE0 |

The contents of the IDLE Code byte register is substituted for the channel data on BTPCM when the IDLC bit in the PCM Control Byte is set to a logic 1. The IDLE Code is transmitted from MSB (bit 7) to LSB (bit 0).

### TPSC Internal Registers 31-48H: SIGNALLING Control byte

| Bit | Type | Function |
|---|---|---|
| Bit 7 | R/W | SIGC0 |
| Bit 6 | R/W | SIGC1 |
| Bit 5 | | Unused |
| Bit 4 | | Unused |
| Bit 3 | R/W | A' |
| Bit 2 | R/W | B' |
| Bit 1 | R/W | C' |
| Bit 0 | R/W | D' |

Signalling insertion is controlled by the SIGC[1:0] bits. The source of the signalling bits is determined by SIGC0: when SIGC0 is set to a logic 1, signalling data is taken from the A', B', C', and D' bits; when SIGC0 is set to logic 0, signalling data is taken from the A,B,C, and D bit locations on the BTSIG input. Signalling insertion is controlled by SIGC1: when SIGC1 is set to a logic 1 and ESF, SF, or SLC®96 transmit format is selected, insertion of signalling bits is

enabled; when SIGC1 is set to logic 0, the insertion of signalling bits is disabled. For SF and SLC®96 formats, the C' and D' or C and D bits from Signalling Control byte or BTSIG, respectively, are inserted into the A and B signalling bit positions of every second superframe that is transmitted. It is assumed that C=A and D=B.

### Register 34H: XFDL Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | EOM | 0 |
| Bit 3 | R/W | INTE | 0 |
| Bit 2 | R/W | ABT | 0 |
| Bit 1 | R/W | CRC | 0 |
| Bit 0 | R/W | EN | 0 |

EN:

The enable bit (EN) controls the overall operation of the XFDL. When the EN bit is set to a logic 1, the XDFL is enabled and flag sequences are sent until data is written into the Transmit Data register. When the EN bit is set to logic 0, the XFDL is disabled.

CRC:

The CRC enable bit controls the generation of the CCITT-CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial = $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the Transmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

INTE:

The INTE bit enables the generation of an interrupt via the TDLINT output. Setting the INTE bit to logic 1 enables the generation of an interrupt; setting INTE to logic 0 disables the generation of an interrupt. If the TDLINTE bit is also set to logic 1 in the Datalink Options register, the interrupt generated on the TDLINT output is also generated on the microprocessor INTB pin.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins.

### Register 35H: XFDL Interrupt Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R | INT | 1 |
| Bit 0 | R/W | UDR | 0 |

INT:

The INT bit indicates when the XFDL is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register. The INT bit is set to logic 1 when the T1XC is reset.

UDR:

The UDR bit indicates when the XFDL has underrun the data in the Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the Transmit Data register has completed before the new byte was written into the Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in this register.

### Register 36H: XFDL Transmit Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | TD7 | X |
| Bit 6 | R/W | TD6 | X |
| Bit 5 | R/W | TD5 | X |
| Bit 4 | R/W | TD4 | X |
| Bit 3 | R/W | TD3 | X |
| Bit 2 | R/W | TD2 | X |
| Bit 1 | R/W | TD1 | X |
| Bit 0 | R/W | TD0 | X |

Data written to this register is serialized and transmitted on the facility data link least significant bit first. The XFDL signals when the next data byte is required by setting the TDLINT output high (if enabled) and by setting the INT bit in the Status register high. When INT and/or TDLINT is set, the Transmit Data register must be written with the new data within 4 data bit periods to prevent the occurrence of an underrun. At a 4 kbit/sec FDL data rate this period corresponds to 1.00 ms.

### Register 38H: RFDL Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | TR | 0 |
| Bit 0 | R/W | EN | 0 |

EN:

The enable bit (EN) controls the overall operation of the RFDL. When set, the RDFL is enabled; when reset the RFDL is disabled. When the block is disabled, the FIFO and interrupts are all cleared, however, the programming of the Enable/Status Register is not affected. When the block is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception bit (TR) forces the RFDL to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration register will reset itself after a rising and falling edge have occurred on the CLK input to the RFDL once the write to this register has completed and WEB goes inactive. If the Configuration register is read after this time, the TR bit value returned will be zero.

The RFDL handles the TR input in the same manner as clearing and setting the EN bit, therefore, the RFDL state machine will begin searching for flags and an interrupt will be generated when the first flag is detected.

### Register 39H: RFDL Interrupt Control/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | INTC1 | 0 |
| Bit 1 | R/W | INTC0 | 0 |
| Bit 0 | R | INT | 0 |

INTC1,INTC0:

The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:

**Table 14 - RFDL Fill Level Interrupt Options**

| INTC1 | INTC0 | Description |
|---|---|---|
| 0 | 0 | Disable interrupts (All sources) |
| 0 | 1 | Enable interrupt when FIFO receives data |
| 1 | 0 | Enable interrupt when FIFO has 2 bytes of data |
| 1 | 1 | Enable interrupt when FIFO has 3 bytes of data |

INT:

The INT bit reflects the status of the external RDLINT interrupt unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the RDLINT output is forced to 0 and the INT bit of the Enable/Status register will reflect the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a

FIFO overrun is cleared on a Status register read, by disabling the block, or by setting TR high.

The contents of the Enable/Status register should only be changed when the RFDL is disabled to prevent any erroneous interrupt generation.

### Register 3AH: RFDL Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | FE | X |
| Bit 6 | R | OVR | X |
| Bit 5 | R | FLG | X |
| Bit 4 | R | EOM | X |
| Bit 3 | R | CRC | X |
| Bit 2 | R | NVB2 | X |
| Bit 1 | R | NVB1 | X |
| Bit 0 | R | NVB0 | X |

NVB[2:0]:

The NVB[2:0] bit positions indicate the number of valid bits in the Receive Data Register byte. It is possible that not all of the bits in the Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. A NVB[2:0] value of 000 binary indicates that only the MSB in the register is valid. NVB[2:0] is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0. NVB[2:0] are set to 111 binary on reset of the T1XC.

CRC:

The CRC bit is set if a CRC error was detected in the last received LAPD frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

On an interrupt generated from the detection of first flag, reading the Status register will return invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

EOM:

The End of Message bit (EOM) follows the RDLEOM output. It is set when:

- The last byte in the LAPD frame (EOM) is being read from the Receive Data Register,

- An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO,
- The first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO,
- Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO.

FLG:

The flag bit (FLG) is set if the RFDL has detected the presence of the LAPD flag sequence (01111110) in the data. FLG is reset only when the LAPD abort sequence (01111111) is detected in the data or when the RFDL is disabled. This bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO. The reception of bit-oriented codes over the data link will also force an abort due to its eight ones pattern.

OVR:

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

FE:

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data. The FE bit is set to logic 1 on reset of the T1XC.

If the Receive Data register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status register by forcing all bits to logic zero on the first Status register read immediately following the Received Data register read which caused the underrun condition.

### Register 3BH: RFDL Receive Data

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | RD7 | X |
| Bit 6 | R | RD6 | X |
| Bit 5 | R | RD5 | X |
| Bit 4 | R | RD4 | X |
| Bit 3 | R | RD3 | X |
| Bit 2 | R | RD2 | X |
| Bit 1 | R | RD1 | X |
| Bit 0 | R | RD0 | X |

RD0 corresponds to the first bit of the serial byte received by the RFDL.

This register is actually a 4 level FIFO. If data is available, the FE bit in the Status register is low. If INTC[1:0] (in the Enable/Status register) is set to 01, the Receive Data register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to 11 the Receiver Data register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status register is read. When the LAPD abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial to parallel converter is written into the FIFO.

A read of the Receive Data register increments the FIFO pointer at the end of the read. If the Receive Data register read causes an FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signalled in the next Status read by returning all zeros.

### Register 3CH: IBCD Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | ACCEL | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | DSEL1 | 0 |
| Bit 2 | R/W | DSEL0 | 0 |
| Bit 1 | R/W | ASEL1 | 0 |
| Bit 0 | R/W | ASEL0 | 0 |

This register provides the selection of the Activate and De-activate loopback code lengths (from 3 bits to 8 bits) as follows:

**Table 15 - IBCD Code Length Options**

| DEACTIVATE Code | | ACTIVATE Code | | |
|---|---|---|---|---|
| DSEL1 | DSEL0 | ASEL1 | ASEL0 | CODE LENGTH |
| 0 | 0 | 0 | 0 | 5 bits |
| 0 | 1 | 0 | 1 | 6 (or 3*) bits |
| 1 | 0 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 1 | 8 (or 4*) bits |

*Note: 3 and 4 bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

### Register 3DH: IBCD Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | LBACP | X |
| Bit 6 | R | LBDCP | X |
| Bit 5 | R/W | LBAE | 0 |
| Bit 4 | R/W | LBDE | 0 |
| Bit 3 | R | LBAI | X |
| Bit 2 | R | LBDI | X |
| Bit 1 | R | LBA | X |
| Bit 0 | R | LBD | X |

LBACP,LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the microprocessor INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the microprocessor INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI,LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes generated the interrupt when their state changed. A logic 1 in these bit positions indicate that a state change in that code has generated an interrupt; a logic 0 in these bit positions indicate that no state change has occurred.

LBA,LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the

presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

### Register 3EH: IBCD Activate Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | ACT7 | 0 |
| Bit 6 | R/W | ACT6 | 0 |
| Bit 5 | R/W | ACT5 | 0 |
| Bit 4 | R/W | ACT4 | 0 |
| Bit 3 | R/W | ACT3 | 0 |
| Bit 2 | R/W | ACT2 | 0 |
| Bit 1 | R/W | ACT1 | 0 |
| Bit 0 | R/W | ACT0 | 0 |

This 8 bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 00001, then the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Upon reset of the T1XC, the register contents are set to logic 0.

### Register 3FH: IBCD Deactivate Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | DACT7 | 0 |
| Bit 6 | R/W | DACT6 | 0 |
| Bit 5 | R/W | DACT5 | 0 |
| Bit 4 | R/W | DACT4 | 0 |
| Bit 3 | R/W | DACT3 | 0 |
| Bit 2 | R/W | DACT2 | 0 |
| Bit 1 | R/W | DACT1 | 0 |
| Bit 0 | R/W | DACT0 | 0 |

This 8 bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 001, then the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Upon reset of the T1XC, the register contents are set to logic 0.

### Register 40H: SIGX Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | R/W | IND | 0 |
| Bit 0 | R/W | PCCE | 0 |

This register allows selection of the framing format, the microprocessor access type, and allows enabling of the per-channel configuration registers.

ESF:

The framing format is controlled by the ESF, FMS1, and FMS0 bits. The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either regular superframe or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF or SLC®96.

FMS1,FMS0:

The FMS1 bit selects standard Superframe or SLC®96 framing formats. A logic 0 in the FMS1 bit enables the SF framing format; a logic 1 in the FMS1 bit position enables the SLC®96 framing format. The FMS0 bit disables the signalling extraction and bit fixing. A logic 0 in the FMS0 bit position enables the SIGX to provide an extracted signalling bit stream and to provide bit fixing on the processed PCM stream; a logic 1 in the FMS0 bit position disables the signalling extraction, forcing the signalling output stream to logic 0 and disables bit fixing on the PCM stream.

When ESF is selected (ESF bit set to logic 1), the extended superframe format is selected and the FMS1 and FMS0 bits are ignored.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

**Table 16 - SIGX Frame Format Options**

| ESF | FMS1 | FMS0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Select Superframe framing format |
| 0 | 1 | 0 | Select SLC®96 framing format |
| 0 | X | 1 | Disable signalling extraction |
| 1 | X | X | Select ESF framing format |

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the T1XC is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, data inversion, bit fixing, and signalling debouncing are performed on a per-channel basis. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

Upon reset of the T1XC, the ESF, FMS[1:0], IND, and PCCE bits are all set to logic 0, selecting the Superframe framing format, disabling µP indirect access, and disabling per-channel functions.

### Register 41H: SIGX µP Access Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BUSY | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

### Register 42H: SIGX Channel Indirect Address/Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | R/WB | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | A5 | 0 |
| Bit 4 | R/W | A4 | 0 |
| Bit 3 | R/W | A3 | 0 |
| Bit 2 | R/W | A2 | 0 |
| Bit 1 | R/W | A1 | 0 |
| Bit 0 | R/W | A0 | 0 |

This register allows the µP to access to internal SIGX registers addressed by the A[5:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal SIGX register is requested, when R/WB is set to a logic 0, an write to the internal SIGX register is requested.

### Register 43H: SIGX Channel Indirect Data Buffer

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R/W | D3 | 0 |
| Bit 2 | R/W | D2 | 0 |
| Bit 1 | R/W | D1 | 0 |
| Bit 0 | R/W | D0 | 0 |

This register contains either the data to be written into the internal SIGX registers when a write request is initiated or the data read from the internal SIGX registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the nibble to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data bits.

The internal registers of the SIGX control the per-channel functions on the Receive PCM data and allow the µP to read the channel's current signalling data. The address bit A5 selects whether a channel's configuration data register is to be accessed (A5=1) or whether a channel's signalling data register is to be accessed. The channel registers are allocated within the SIGX as follows:

**Table 17 - SIGX Indirect Register Map**

| | |
|---|---|
| 01H | Channel 1 Signalling Data |
| 02H | Channel 2 Signalling Data |
| • | • |
| • | • |
| • | • |
| 17H | Channel 23 Signalling Data |
| 18H | Channel 24 Signalling Data |
| 19-1FH | Ignored |
| 20H | SIGX Configuration |
| 21H | Channel 1 Per-channel Configuration Data |
| 22H | Channel 2 Per-channel Configuration Data |
| • | • |
| • | • |
| • | • |
| 37H | Channel 23 Per-channel Configuration Data |
| 38H | Channel 24 Per-channel Configuration Data |
| 39-3FH | Ignored |

The bits within each channel register byte are allocated as follows:

### SIGX Internal Registers 01-18H: SIGNALLING Data

| Bit | Type | Function |
|---|---|---|
| Bit 7 | | Unused |
| Bit 6 | | Unused |
| Bit 5 | | Unused |
| Bit 4 | | Unused |
| Bit 3 | R | A |
| Bit 2 | R | B |
| Bit 1 | R | C |
| Bit 0 | R | D |

When the SIGNALLING Data registers are read, the byte returned contains the 4 signalling bits in the 4 least significant bit positions. If SF or SLC®96 framing format is selected then C=A and D=B. The bits read correspond to the signalling state extracted from the third to last superframe received.

When reading the extracted signalling data for a channel with signalling state debounce enabled, the signalling data returned is the debounced version, meaning that the signalling state value for that channel must have been the same for two consecutive superframes before it was allowed to propagate through the signalling buffers and be visible in the signalling data registers. If the state was not the same, the current state (accessible via these registers) is not changed.

### SIGX Internal Registers 21-38H: PER-CHANNEL Configuration Data

| Bit | Type | Function |
|---|---|---|
| Bit 7 | | Unused |
| Bit 6 | | Unused |
| Bit 5 | | Unused |
| Bit 4 | | Unused |
| Bit 3 | R/W | INV |
| Bit 2 | R/W | FIX |
| Bit 1 | R/W | POL |
| Bit 0 | R/W | DEB |

INV:

The INV bit controls data inversion for the selected channel: a logic 1 in the INV bit position enables data inversion; a logic 0 disables data inversion. Inversion only affects the channel data, F-bits are passed unchanged.

FIX:

The FIX bit controls whether the signalling bit ( the least significant bit of the channel byte) is fixed to the polarity specified by the POL bit. A logic 1 in the FIX position enables bit fixing; a logic 0 in the FIX position disables bit fixing.

POL:

The POL bit selects the logic level the signalling bit is fixed to when bit fixing is enabled. NOTE: when data inversion is selected for the channel and bit fixing is enabled, then the sense of POL is also inverted (i.e. if inversion is enabled and POL=1, then the bit will be fixed to logic 0).

DEB:

The DEB bit controls whether a channel's signalling bits are to be debounced. Debouncing requires that the signalling bits be in the same state for two successive superframes before the signalling bits are changed to that state.

### Register 44H: XBAS Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | MTRK | 0 |
| Bit 6 | R/W | Reserved | 0 |
| Bit 5 | R/W | B8ZS | 0 |
| Bit 4 | R/W | ESF | 0 |
| Bit 3 | R/W | FMS1 | 0 |
| Bit 2 | R/W | FMS0 | 0 |
| Bit 1 | R/W | ZCS1 | 0 |
| Bit 0 | R/W | ZCS0 | 0 |

Bit 6 of the configuration register is reserved and must be set to logic 0 for proper operation.

ZCS[1:0]:

The ZCS[1:0] bits select the Zero Code Suppression format to be used. These bits are logically ORed with the ZCS[1:0] bits in the TPSC per-channel PCM Control byte. The bits are encoded as follows:

**Table 18 - XBAS Zero Code Suppression Options**

| ZCS1 | ZCS0 | Zero Code Suppression Format |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | GTE Zero Code Suppression ("jammed bit 8", except in signalling frames when "jammed bit 7" is used if the signalling bit is 0) |
| 1 | 0 | DDS Zero Code Suppression (data byte replaced with "10011000") |
| 1 | 1 | Bell Zero Code Suppression ("jammed bit 7") |

B8ZS:

The B8ZS bit enables B8ZS line coding when it is a logic 1.

ESF, FMS1, FMS0:

The ESF bit selects either Extended Superframe format or enables the Frame Mode Select bits (FMS) to select either regular superframe, T1DM or SLC®96 framing formats. The mode is encoded as follows:

**Table 19 - XBAS Frame Format Options**

| ESF | FMS1 | FMS0 | MODE |
|---|---|---|---|
| 0 | 0 | 0 | SF framing format |
| 0 | 0 | 1 | T1DM framing format (R bit unaffected) |
| 0 | 1 | 0 | SLC®96 |
| 0 | 1 | 1 | T1DM framing format (FDL data replaces R bit) |
| 1 | 0 | 0 | ESF framing format - 4 kbit/s data link |
| 1 | 0 | 1 | ESF framing format - 2 kbit/s data link (frames 3,7,11,15,19,23) |
| 1 | 1 | 0 | ESF framing format - 2 kbit/s data link (frames 1,5,9,13,17,21) |
| 1 | 1 | 1 | ESF framing format - 4 kbit/s data link |

MTRK:

The MTRK bit forces trunk conditioning, idle code substitution and signalling conditioning, on all channels when MTRK is a logic 1. This has the same effect as setting the IDLC bit in the PCM Control byte and the SIG0 bit in the SIGNALLING Control byte for all channels.

Reserved:

The Reserved bit should be set to logic 0 for proper operation.

### Register 45H: XBAS Alarm Transmit

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | XYEL | 0 |
| Bit 0 | R/W | XAIS | 0 |

This register controls the transmission of YELLOW or AIS alarm.

XYEL:

The XYEL bit enables the XBAS to generate a YELLOW alarm in the appropriate framing format. When XYEL is set to logic 1, XBAS is enabled to set bit 2 of each channel to logic 0 for SF and SLC®96 formats, the Y-bit to logic 0 for T1DM format, and XBAS is enabled to transmit repetitions of 1111111100000000 (the YELLOW Alarm BOC) on the FDL for ESF format. When XYEL is set to logic 0, XBAS is disabled from generating the YELLOW alarm.

XAIS:

The XAIS bit enables the XBAS to generate an unframed all-ones AIS alarm. When XAIS is set to logic 1, the XBAS bi-polar outputs are forced to pulse alternately, creating an all-ones signal. When XAIS is set to logic 0, the XBAS bi-polar outputs operate normally.

### Register 46H: XIBC Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | EN | 0 |
| Bit 6 | R/W | UF | 0 |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | CL1 | 0 |
| Bit 0 | R/W | CL0 | 0 |

EN:

The EN bit controls whether the Inband Code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

UF:

The UF bit controls whether the code is transmitted framed or unframed. A logic 1 in the UF bit position selects unframed inband code transmission; a logic 0 in the UF bit position selects framed inband code transmission. Note: the UF register bit controls the XBAS directly and is not qualified by the EN bit. When UF is set to logic 1, the XBAS is disabled and no framing is inserted regardless of the setting of EN. The UF bit should only be written to logic 1 when the EN bit is set, and should be cleared to logic 0 when the EN bit is cleared.

CL1, CL0:

The bit positions CL[1:0] (bits 1 & 0) of this register indicate the length of the inband loopback code sequence, as follows:

**Table 20 - XIBC Code Length Options**

| CL1 | CL0 | Code Length |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e. a 3-bit code would use the 6-bit code length setting).

### Register 47H: XIBC Loopback Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | IBC7 | X |
| Bit 6 | R/W | IBC6 | X |
| Bit 5 | R/W | IBC5 | X |
| Bit 4 | R/W | IBC4 | X |
| Bit 3 | R/W | IBC3 | X |
| Bit 2 | R/W | IBC2 | X |
| Bit 1 | R/W | IBC1 | X |
| Bit 0 | R/W | IBC0 | X |

This register contains the inband loopback code pattern to be transmitted. The code is transmitted most significant bit ( IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code '011' would be written as the 6-bit code '011011').

When the T1XC is reset, the contents of this register are not affected.

**Register 49H: PMON Interrupt Status**

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R/W | Reserved | 0 |
| Bit 1 | R | XFER | 0 |
| Bit 0 | R | OVR | 0 |

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

Reserved:

This bit must be programmed to logic 0 for proper operation.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

### 10.1.1 Registers 4A-4FH: Latching Performance Data

All the Performance Data registers are updated as a group by writing to any of the PMON count registers (addresses 4AH-4FH). A write to any of these locations loads performance data located in the PMON into the internal holding

registers. The data contained in the holding registers can then be subsequently read by µP accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed. NOTE: it is necessary to write to one, and only one, count register address to latch all the count data register values into the holding registers and to reset all the counters for each polling cycle.

The PMON is loaded with new performance data within 3.5 recovered clock periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the PMON count register write.

When the T1XC is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

### Register 4AH: PMON LCV Count (LSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | LCV7 | X |
| Bit 6 | R | LCV6 | X |
| Bit 5 | R | LCV5 | X |
| Bit 4 | R | LCV4 | X |
| Bit 3 | R | LCV3 | X |
| Bit 2 | R | LCV2 | X |
| Bit 1 | R | LCV1 | X |
| Bit 0 | R | LCV0 | X |

This register contains the lower eight bits of the 12 bit Line Code Violation event counter. A Line Code Violation event is defined as the occurrence of a Bipolar Violation.

### Register 4BH: PMON LCV Count (MSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | R | LCV11 | X |
| Bit 2 | R | LCV10 | X |
| Bit 1 | R | LCV9 | X |
| Bit 0 | R | LCV8 | X |

This register contains the upper four bits of the 12 bit Line Code Violation event counter.

### Register 4CH: PMON BEE Count (LSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BEE7 | X |
| Bit 6 | R | BEE6 | X |
| Bit 5 | R | BEE5 | X |
| Bit 4 | R | BEE4 | X |
| Bit 3 | R | BEE3 | X |
| Bit 2 | R | BEE2 | X |
| Bit 1 | R | BEE1 | X |
| Bit 0 | R | BEE0 | X |

This register contains the lower eight bits of the 9-bit Bit Error event counter. A Bit Error event is defined as a CRC-6 error in ESF, a framing bit error in SF, an $F_T$-bit error in SLC®96, and an F-bit or sync bit error (there can be up to 7 bits in error per frame) in T1DM.

### Register 4DH: PMON BEE Count (MSB)

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | R | BEE8 | X |

This register contains the upper bit of the 9-bit Bit Error event counter.

### Register 4EH: PMON FER Count

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | FER4 | X |
| Bit 3 | R | FER3 | X |
| Bit 2 | R | FER2 | X |
| Bit 1 | R | FER1 | X |
| Bit 0 | R | FER0 | X |

This register contains the value of the 5 bit Framing Bit Error event counter.

### Register 4FH: PMON OOF/COFA Count

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R | OOF2/COFA2 | X |
| Bit 1 | R | OOF1/COFA1 | X |
| Bit 0 | R | OOF0/COFA0 | X |

This register contains the value of the 3 bit counter accumulating Out Of Frame or Change Of Frame Alignment events. The COFA bit in register 00H controls whether Change of Frame Alignment or Out Of Frame events are counted.

### Register 50H: RPSC Configuration

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | R/W | IND | 0 |
| Bit 0 | R/W | PCCE | 0 |

This register allows selection of the microprocessor read access type and output enable control for the Receive Per-channel Serial Controller.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the T1XC is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, the Data Trunk Conditioning Code byte and Signalling Trunk Conditioning Code byte are enabled to modify the received data and extracted signalling data streams (visible on BRPCM and BRSIG, if selected) under direction of each channel's PCM Control byte. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

### Register 51H: RPSC µP Access Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R | BUSY | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | | Unused | X |
| Bit 1 | | Unused | X |
| Bit 0 | | Unused | X |

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

### Register 52H: RPSC Channel Indirect Address/Control

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | R/WB | 0 |
| Bit 6 | R/W | A6 | 0 |
| Bit 5 | R/W | A5 | 0 |
| Bit 4 | R/W | A4 | 0 |
| Bit 3 | R/W | A3 | 0 |
| Bit 2 | R/W | A2 | 0 |
| Bit 1 | R/W | A1 | 0 |
| Bit 0 | R/W | A0 | 0 |

This register allows the µP to access the internal RPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal RPSC register is requested; when R/WB is set to a logic 0, an write to the internal RPSC register is requested.

### Register 53H: RPSC Channel Indirect Data Buffer

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | D7 | 0 |
| Bit 6 | R/W | D6 | 0 |
| Bit 5 | R/W | D5 | 0 |
| Bit 4 | R/W | D4 | 0 |
| Bit 3 | R/W | D3 | 0 |
| Bit 2 | R/W | D2 | 0 |
| Bit 1 | R/W | D1 | 0 |
| Bit 0 | R/W | D0 | 0 |

This register contains either the data to be written into the internal RPSC registers when a write request is initiated or the data read from the internal RPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal RPSC registers control the per-channel functions on the Receive PCM data, provide the per-channel Data Trunk Conditioning Code, and provide the per-channel Signalling Trunk Conditioning Code. The functions are allocated within the registers as follows:

**Table 21 - RPSC Indirect Register Map**

| | |
|---|---|
| 01H | PCM Data Control byte for Channel 1 |
| 02H | PCM Data Control byte for Channel 2 |
| • | • |
| • | • |
| • | • |
| 17H | PCM Data Control byte for Channel 23 |
| 18H | PCM Data Control byte for Channel 24 |
| 19H | Data Trunk Conditioning byte for Channel 1 |
| 1AH | Data Trunk Conditioning byte for Channel 2 |
| • | • |
| • | • |
| • | • |
| 2FH | Data Trunk Conditioning byte for Channel 23 |
| 30H | Data Trunk Conditioning byte for Channel 24 |
| 31H | Signalling Trunk Conditioning byte for Channel 1 |
| 32H | Signalling Trunk Conditioning byte for Channel 2 |
| • | • |
| • | • |
| • | • |
| 47H | Signalling Trunk Conditioning byte for Channel 23 |
| 48H | Signalling Trunk Conditioning byte for Channel 24 |

The bits within each control byte are allocated as follows:

### RPSC Internal Registers 01-18H: PCM Data Control byte

| Bit | Type | Function |
|---|---|---|
| Bit 7 | R/W | INVERT |
| Bit 6 | R/W | DTRKC |
| Bit 5 | R/W | DMW |
| Bit 4 | R/W | SIGNINV |
| Bit 3 | | Unused |
| Bit 2 | | Unused |
| Bit 1 | | Unused |
| Bit 0 | | Unused |

INVERT:

When the INVERT bit is set to a logic 1, data output on the BRPCM pin is the bit inverse of the received data for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit of the data output on the BRPCM pin is inverse of the received data most significant bit for that channel.

The INVERT and SIGNINV can be used to produce the following types of inversions:

**Table 22 - RPSC Inversion Options**

| INVERT | SIGNINV | Effect on PCM Channel Data |
|---|---|---|
| 0 | 0 | PCM Channel data is unchanged |
| 1 | 0 | All 8 bits of the received PCM channel data are inverted |
| 0 | 1 | Only the MSB of the received PCM channel data is inverted (SIGN bit inversion) |
| 1 | 1 | All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion) |

DTRKC:

When the DTRKC bit is set to a logic 1, data from the Data Trunk Conditioning Code Byte replaces the BRPCM output data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the BRPCM output data for the duration of that channel.

Data inversion, data trunk conditioning, and digital milliwatt insertion are performed independent of the received framing format. Digital milliwatt insertion takes precedence over data trunk conditioning which, in turn, takes precedence over the various data inversions.

### RPSC Internal Registers 19-30H: Data Trunk Conditioning Code byte

| Bit | Type | Function |
|---|---|---|
| Bit 7 | R/W | DTRK7 |
| Bit 6 | R/W | DTRK6 |
| Bit 5 | R/W | DTRK5 |
| Bit 4 | R/W | DTRK4 |
| Bit 3 | R/W | DTRK3 |
| Bit 2 | R/W | DTRK2 |
| Bit 1 | R/W | DTRK1 |
| Bit 0 | R/W | DTRK0 |

The contents of the Data Trunk Conditioning Code byte register is substituted for the channel data on BRPCM when the DTRKC bit in the PCM Control Byte is set to a logic 1. The Data Trunk Conditioning Code is transmitted from MSB (bit 7) to LSB (bit 0).

### RPSC Internal Registers 31-48H: Signalling Trunk Conditioning byte

| Bit | Type | Function |
|---|---|---|
| Bit 7 | R/W | STRKC |
| Bit 6 | | Unused |
| Bit 5 | | Unused |
| Bit 4 | | Unused |
| Bit 3 | R/W | A' |
| Bit 2 | R/W | B' |
| Bit 1 | R/W | C' |
| Bit 0 | R/W | D' |

The contents of the Signalling Trunk Conditioning Code byte register is substituted for the channel signalling data on BRSIG when the STRKC bit is set to a logic 1. The Signalling Trunk Conditioning Code is placed in least significant nibble of the channel byte.

### Register 55H: PDVD Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R | PDV | X |
| Bit 3 | R | Z16DI | X |
| Bit 2 | R | PDVI | X |
| Bit 1 | R/W | Z16DE | 0 |
| Bit 0 | R/W | PDVE | 0 |

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist. When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether interrupts are enabled or disabled.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit

may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

### Register 57H: XBOC Code

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | R/W | BC[5] | 1 |
| Bit 4 | R/W | BC[4] | 1 |
| Bit 3 | R/W | BC[3] | 1 |
| Bit 2 | R/W | BC[2] | 1 |
| Bit 1 | R/W | BC[1] | 1 |
| Bit 0 | R/W | BC[0] | 1 |

This register enables the XBOC to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the ESF Facility Data Link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, overwriting any HDLC packets currently being transmitted. When the register is written with 111111, the XBOC is disabled.

### Register 59H: XPDE Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | R/W | STUFE | 0 |
| Bit 6 | R/W | STUFF | 0 |
| Bit 5 | R | STUFI | X |
| Bit 4 | R | PDV | X |
| Bit 3 | R | Z16DI | X |
| Bit 2 | R | PDVI | X |
| Bit 1 | R/W | Z16DE | 0 |
| Bit 0 | R/W | PDVE | 0 |

STUFE:

The STUFE bit enables the occurrence of pulse stuffing to generate an interrupt on INTB. When STUFE is set to logic 1, an interrupt is generated on the occurrence of a bit stuff. When STUFE is a logic 0, bit stuffing occurrences do not generate an interrupt on INTB.

STUFF:

The STUFF bit enables pulse stuffing to occur upon detection of a violation of the pulse density rule. Bit stuffing is performed in such a way that the resulting data stream no longer violates the pulse density rule. When STUFF is set to logic 1, bit stuffing is enabled and the STUFI bit indicates the occurrence of bit stuffs. When STUFF is a logic 0, bit stuffing is disabled and the PDVI bit indicates occurrences of pulse density violation. Also, when STUFF is a logic 0, PCM data passes through XPDE unaltered.

STUFI:

The STUFI bit is valid when pulse stuffing is active. This bit indicates when a bit stuff occurred to eliminate a pulse density violation and that an interrupt was generated due to the bit stuff (if STUFE is logic 1). When pulse stuffing is active, PDVI remains logic 0, indicating that the stuffing has removed the density violation. The STUFI bit is reset to logic 0 once this register is read. If the STUFE bit is also logic 1, the interrupt is also cleared once this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists.

When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether the corresponding interrupt enables are enabled or disabled. When STUFF is set to logic 1, the PDVI and Z16DI bits are forced to logic 0.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist (if STUFE is logic 0). When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

### Register 5DH: RSLC Interrupt Enable/Status

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | | Unused | X |
| Bit 3 | | Unused | X |
| Bit 2 | R | SQ | X |
| Bit 1 | R | SQI | X |
| Bit 0 | R/W | SQE | 0 |

SQ:

The SQ bit reflects the current state of the squelch alarm.

SQI:

The SQI bit is set to logic 1 when the squelch alarm is either asserted or deasserted. The bit is cleared to logic 0 when the register is read.

SQE:

The SQE bit enables the generation of an interrupt when the squelch alarm changes state. When SQE is set to logic 1, the squelch alarm event is enabled to generate an interrupt on the microprocessor INTB pin.

When the T1XC is reset, the SQE bit is set to logic 0, disabling a squelch event from generating an interrupt.

# 11 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the T1XC. Test mode registers (as opposed to normal mode registers) are mapped into addresses 80H-FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the T1XC are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

**Notes on Test Mode Register Bits:**

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

## 11.1 Test Mode Register Memory Map

| Address | Register |
|---|---|
| 80H-8FH | T1XC Reserved |
| 90H | CDRC TREG 0 |
| 91H | CDRC TREG 1 |
| 92H | CDRC Reserved |
| 93H | CDRC Reserved |
| 94H | XPLS TREG 0 |
| 95H | XPLS TREG 1 |
| 96H | XPLS TREG 2 |
| 97H | XPLS TREG 3 |
| 98H | DJAT TREG 0 |

| Address | Register |
|---|---|
| 99H | DJAT TREG 1 |
| 9AH | DJAT TREG 2 |
| 9BH | DJAT Reserved |
| 9CH | ELST TREG 0 |
| 9DH | ELST TREG 1 |
| 9EH | ELST TREG 2 |
| 9FH | ELST Reserved |
| A0H | FRMR TREG 0 |
| A1H | FRMR TREG 1 |
| A2H | FRMR TREG 2 |
| A3H | FRMR Reserved |
| A4H | T1XC Reserved |
| A5H | T1XC Reserved |
| A6H | T1XC Reserved |
| A7H | T1XC Reserved |
| A8H | T1XC Reserved |
| A9H | T1XC Reserved |
| AAH | RBOC TREG 0 |
| ABH | RBOC TREG 1 |
| ACH | ALMI TREG 0 |
| ADH | ALMI TREG 1 |
| AEH | ALMI Reserved |
| AFH | ALMI Reserved |
| B0H | TPSC TREG 0 |
| B1H | TPSC TREG 1 |
| B2H | TPSC Reserved |
| B3H | TPSC Reserved |
| B4H | XFDL TREG 0 |

| Address | Register |
|---|---|
| B5H | XFDL TREG 1 |
| B6H | XFDL Reserved |
| B7H | XFDL Reserved |
| B8H | RFDL TREG 0 |
| B9H | RFDL TREG 1 |
| BAH | RFDL Reserved |
| BBH | RFDL Reserved |
| BCH | IBCD TREG 0 |
| BDH | IBCD TREG 1 |
| BEH | IBCD Reserved |
| BFH | IBCD Reserved |
| C0H | SIGX TREG 0 |
| C1H | SIGX TREG 1 |
| C2H | SIGX TREG 2 |
| C3H | SIGX Reserved |
| C4H | XBAS TREG 0 |
| C5H | XBAS TREG 1 |
| C6H | XIBC TREG 0 |
| C7H | XIBC TREG 1 |
| C8H | PMON TREG 0 |
| C9H | PMON TREG 1 |
| CAH-CFH | PMON Reserved |
| D0H | RPSC TREG 0 |
| D1H | RPSC TREG 1 |
| D2H | RPSC Reserved |
| D3H | RPSC Reserved |
| D4H | PDVD TREG 0 |
| D5H | PDVD TREG 1 |

| Address | Register |
|---|---|
| D6H | XBOC TREG 0 |
| D7H | XBOC TREG 1 |
| D8H | XPDE TREG 0 |
| D9H | XPDE TREG 1 |
| DAH | FRAM TREG 0 |
| DBH | FRAM TREG 1 |
| DCH | RSLC TREG 0 |
| DDH | RSLC TREG 1 |
| DEH-FFH | Reserved |

## 11.2 Internal Registers

### Register 0BH: T1XC Master Test

| Bit | Type | Function | Default |
|---|---|---|---|
| Bit 7 | | Unused | X |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | W | PMCTST | X |
| Bit 3 | W | DBCTRL | 0 |
| Bit 2 | R/W | IOTST | 0 |
| Bit 1 | W | HIZDATA | 0 |
| Bit 0 | R/W | HIZIO | 0 |

This register is used to select T1XC test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the T1XC ; a software reset of the T1XC does not affect the state of the bits in this register.

PMCTST:

The PMCTST bit is used to configure the T1XC for PMC's manufacturing tests. When PMCTST is set to logic 1, the T1XC microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the T1XC to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the T1XC for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the

microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in this section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the T1XC . While the HIZIO bit is a logic 1, all output pins of the T1XC except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

## 11.3 Test Mode 0

In test mode 0, the T1XC allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Test Mode Select Register is set to logic 1 and the following addresses must be written with 00H: 91H, 99H, 9DH, A1H, B5H, B9H, C1H, C5H. Also, to enable input and output signals to propagate through the Interface blocks, the values 00H, 01H, 00H , and 0CH must be written to addresses 01H, 03H, 04H, and 07H, respectively.

Reading the following address locations returns the values for the indicated inputs :

**Table 23 - Test Mode 0 Primary Input Reading Map**

| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 90H | | | | | | RCLKI | RDN | RDP |
| 98H | | | | | XCLKI | TCLKI | | |
| 9CH | BRFPI | BRCLK | | | | | | |
| B4H | | | | | | | TDLSIG | |
| C4H | BTCLK | | BTFP | | BTSIG | | | BTPCM |

Writing the following address locations forces the outputs to the value in the corresponding bit position:

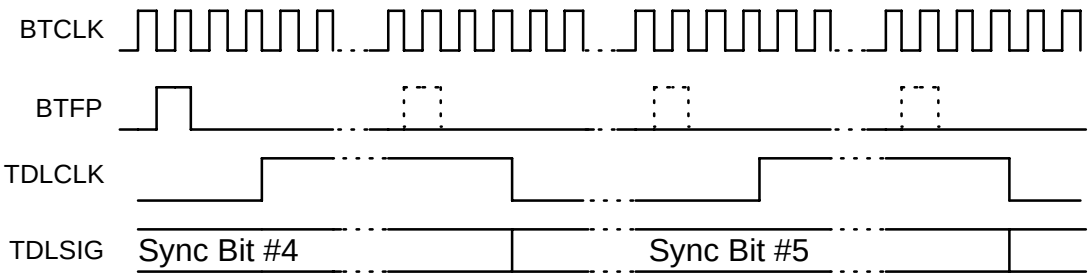
## Table 24 - Test Mode 0 Primary Output Writing Map

| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 90H | | INTB† | | | | | RDPCM | RCLKO |
| 98H | | | | | | TCLKO | TDN | TDP |
| 9CH | | INTB† | | | | | BRFPO | |
| A0H | | | | | RFP | | | |
| A2H | | INTB† | RDLSIG | RDLCLK | | | | |
| C0H | | | | | | BRPCM | BRSIG | |
| C4H | TDLCLK | | | | | | | |

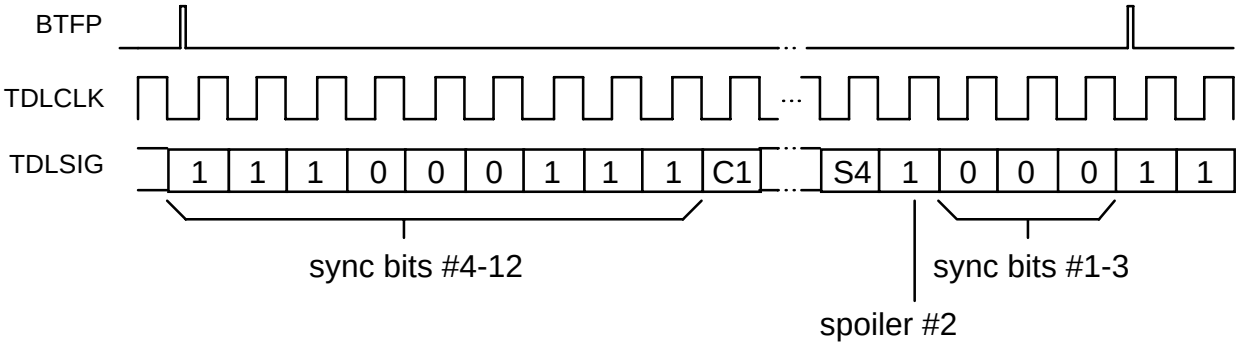
Notes: † Writing a logic 1 to any of the block interrupt signals asserts the INTB output low.

## 12 TIMING DIAGRAMS

**Figure 13 - SLC®96 Transmit Datalink Interface**

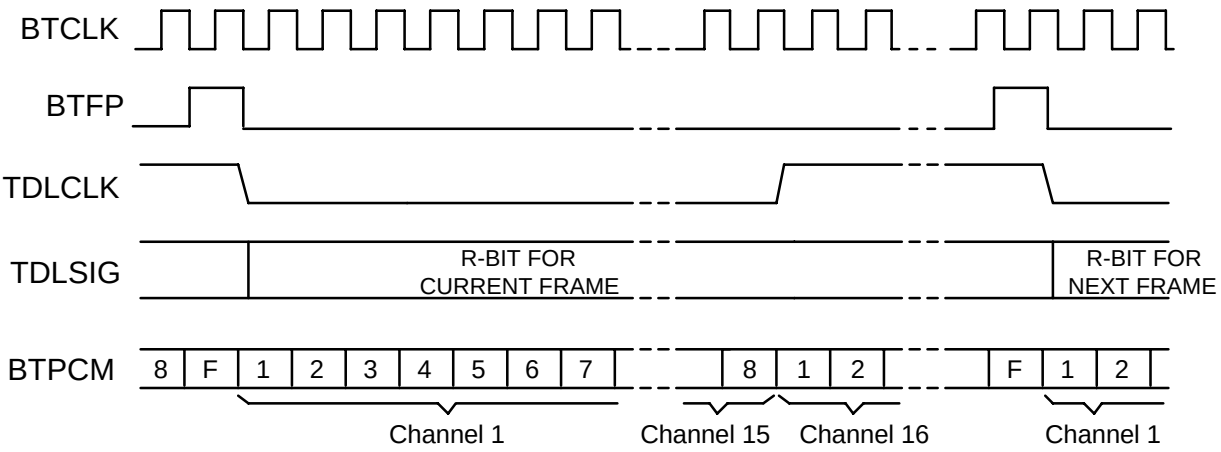



BTFP is the SLC®96 superframe pulse, occurring once every 9 ms. It indicates the presence of the fourth Synchronization pattern bit on the TDLSIG input. The TDLSIG pattern should be aligned to the BTFP superframe pulse as follows so that robbed bit signalling can be inserted in the correct signalling frames:



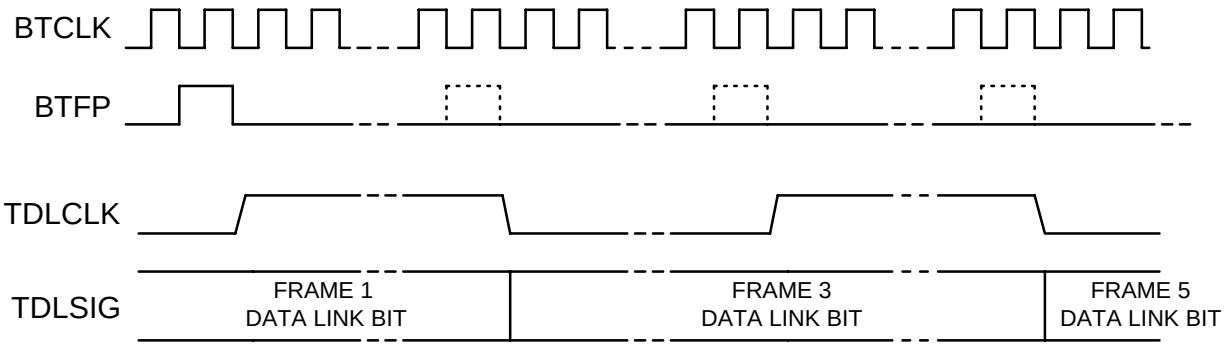

The XBAS is configured to generate SLC®96 formatted data. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the superframe alignment (BTXSFP=1). The dotted frame pulses are shown for reference, indicating the subsequent frame boundaries of the superframe.

**Figure 14 - T1DM Transmit Datalink Interface**



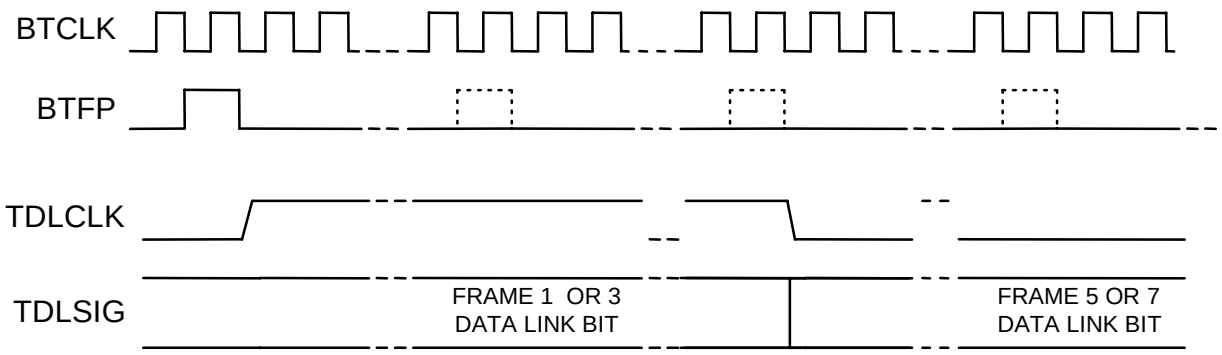

The XBAS is configured to generate T1DM formatted data. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the frame alignment (BTXSFP=0).

**Figure 15 - ESF 4Kbit/s Transmit Datalink Interface**



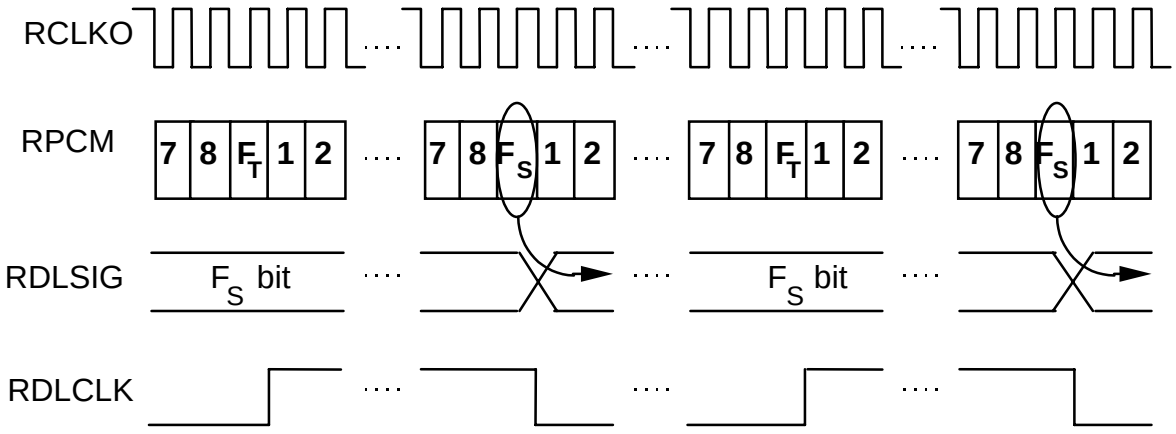

The XBAS is configured to generate ESF formatted data with a 4 kbit/s data link. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the superframe alignment (BTXSFP=1). The dotted frame pulses are shown for reference, indicating the subsequent frame boundaries of the superframe.

**Figure 16 - ESF 2Kbit/s Transmit Datalink Interface**



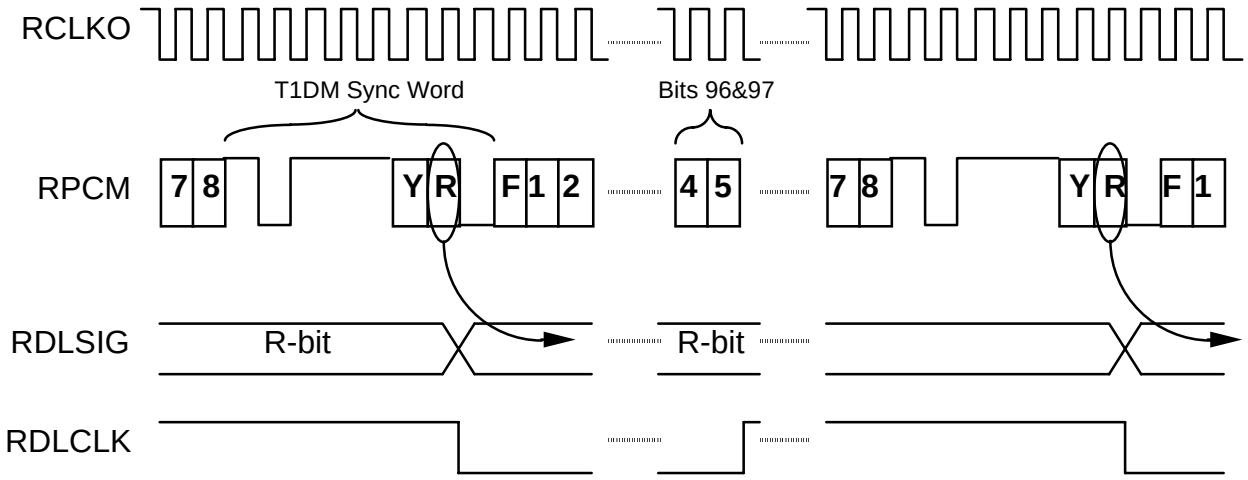

The XBAS is configured to generate ESF formatted data with a 2 kbit/s data link. The data sampled on the TDLSIG input is inserted into the framing bit position of frames 1,5,9,13,17,21 when the "lower" 2 kbit/s channel is selected; the data is inserted into frames 3,7,11,15,19,23 when the "upper" 2 kbit/s channel is selected. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the superframe alignment (BTXSFP=1). The dotted frame pulses are shown for reference, indicating the subsequent frame boundaries of the superframe.

**Figure 17 - SLC®96 Receive Datalink Interface**



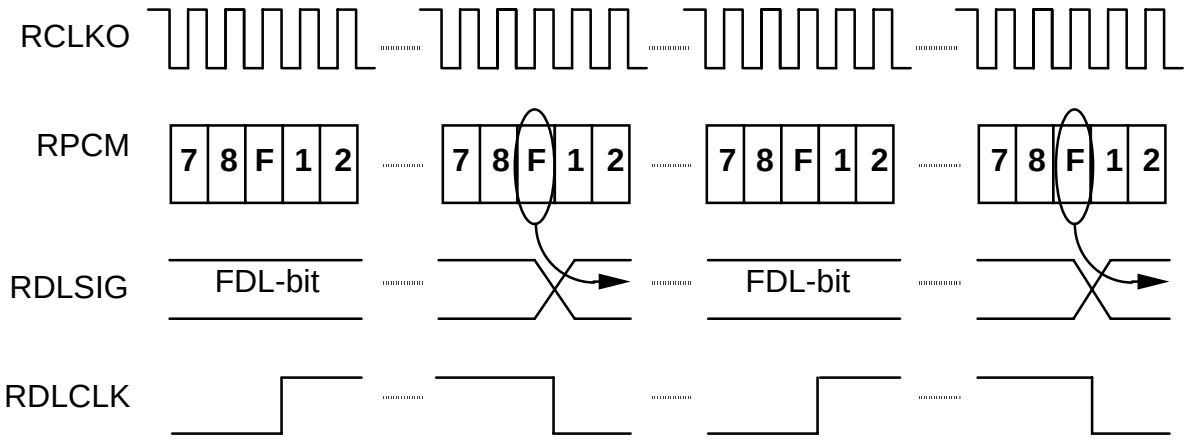

The FRMR is configured to receive SLC®96 formatted data. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

**Figure 18 - T1DM Receive Datalink Interface**



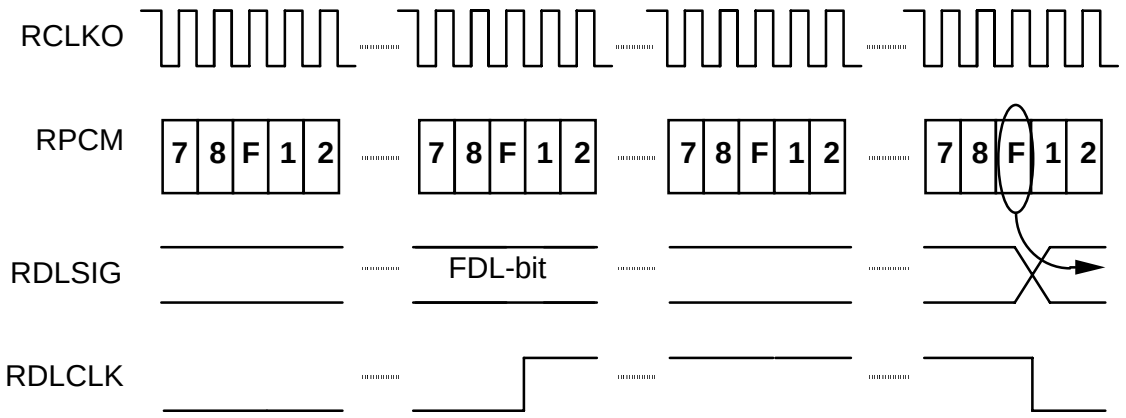

The FRMR is configured to receive T1DM formatted data. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

**Figure 19 - ESF 4Kbit/s Receive Datalink Interface**



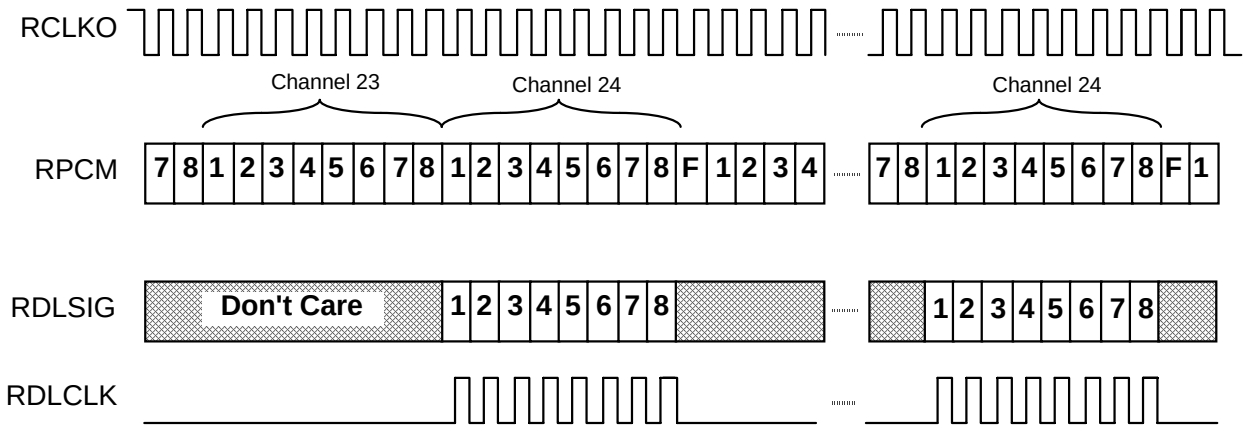

The FRMR is configured to receive ESF formatted data with a 4 kbit/s data link. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

**Figure 20 - ESF 2Kbit/s Receive Datalink Interface**



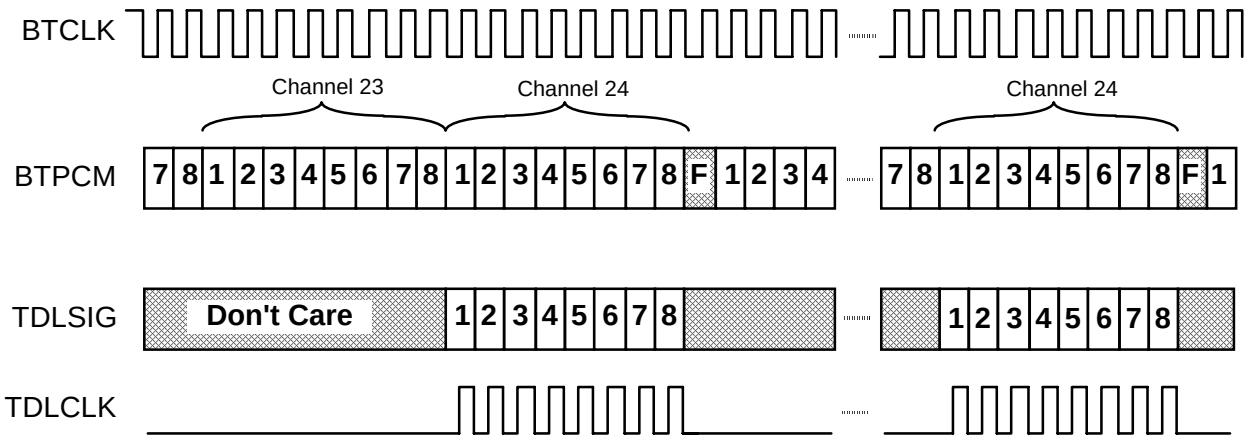

The FRMR is configured to receive ESF formatted data with a 2 kbit/s data link. The data output on the RDLSIG pin is extracted from the framing bit position of frames 1,5,9,13,17,21 when the "lower" 2 kbit/s channel is selected; the data is extracted from frames 3,7,11,15,19,23 when the "upper" 2 kbit/s channel is selected. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

**Figure 21 - D-Channel Receive Datalink Interface**



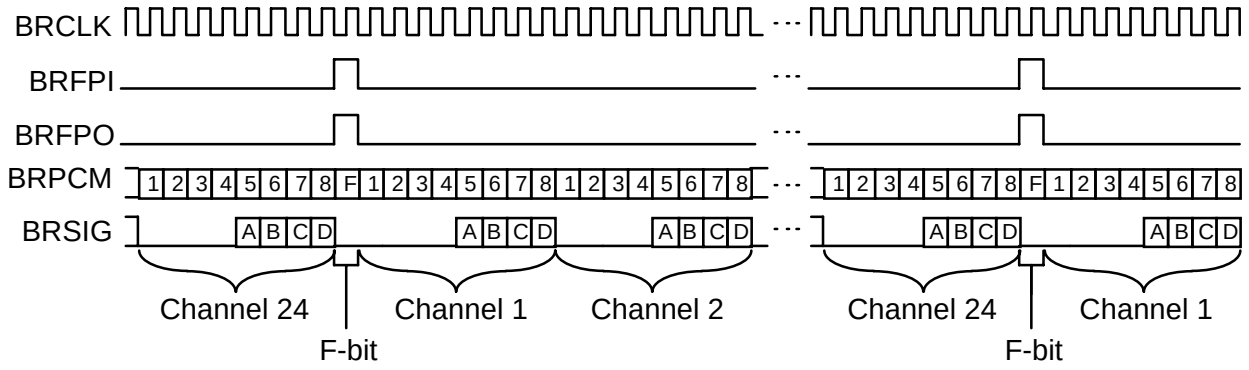

The FRMR is configured to receive SF or ESF formatted data. The Data Link Options register is programmed to provide access to the D-Channel data link (RXDMASIG=X, RXDCHAN=1).

**Figure 22 - D-Channel Transmit Datalink Interface**



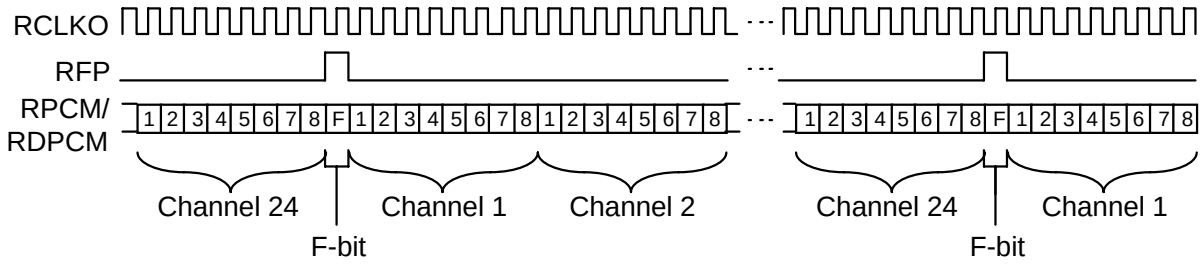

The XBAS is configured to transmit SF or ESF formatted data. The Data Link Options register is programmed to provide access to the D-Channel transmit data link (TXDMASIG=X, TXDCHAN=1).

**Figure 23 - 1.544MHz Receive Backplane Interface**



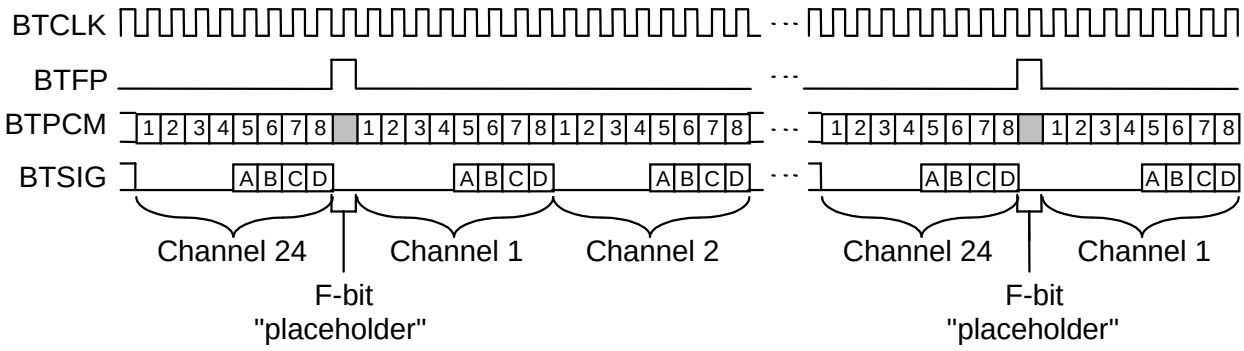

The Receive Backplane is configured to generate 1.544MHz, single-rail formatted data with frame alignment indication. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=0. (If BRXSFP=1, the BRFPO output only pulses on the frame boundary indication the start of the superframe alignment; if ALTBRFP=1, the BRFPO output pulses on every second indication of either the frame or the superframe boundary).

**Figure 24 - 1.544MHz Receive Line Data Interface**



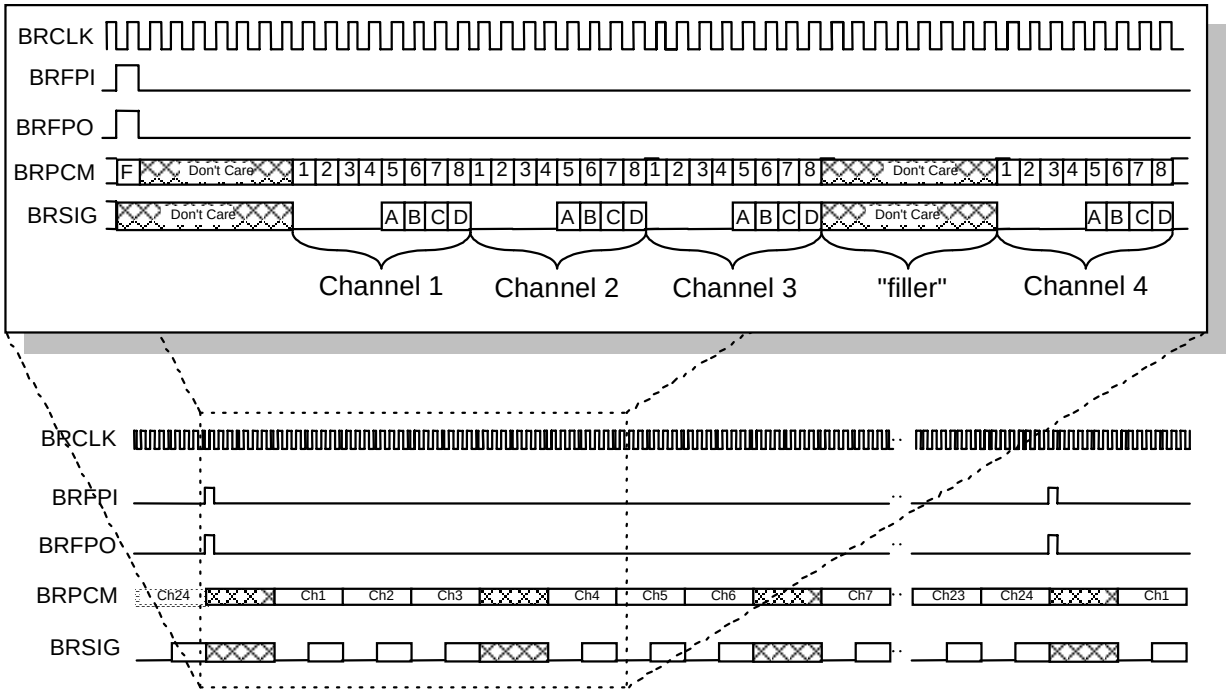

The Receive Options register is programmed to SRSFP=0, ALTRFP=0, SRPCM=X. (If SRSFP=1, the RFP output only pulses on the frame boundary indication the start of the superframe alignment; if ALTRFP=1, the RFP output pulses on every second indication of either the frame or the superframe boundary). This diagram does not apply when the digital receive interface is configured for uni-polar operation.

**Figure 25 - 1.544MHz Transmit Backplane Interface**



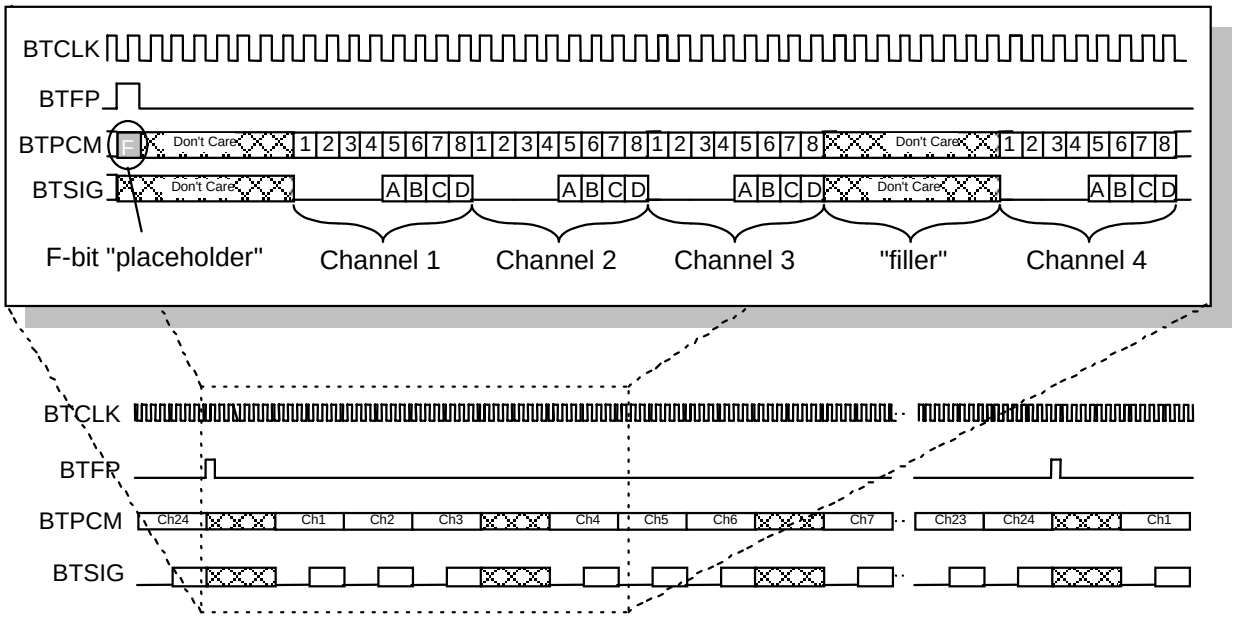

The Transmit Backplane is configured to receive 1.544MHz, single-rail formatted data with frame alignment indication. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=0. (If BTXSFP=1, the BTFP input should only pulse on the frame boundary indicating the start of the superframe alignment.

**Figure 26 - 2.048MHz Receive Backplane Interface**



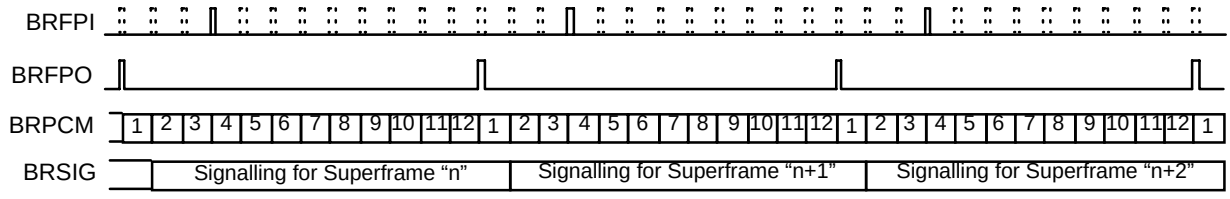

The Receive Backplane is configured to generate 2.048MHz, single-rail formatted data with frame alignment indication. The Receive Backplane Options register is programmed to BRX2M=1, BRX2RAIL=0, BRXSFP=0. (If BRXSFP=1, the BRFPO output only pulses on the frame boundary indication the start of the superframe alignment; if ALTBRFP=1, the BRFPO output pulses on every second indication of either the frame or the superframe boundary).

**Figure 27 - 2.048MHz Transmit Backplane Interface**




The Transmit Backplane is configured to receive 2.048MHz, single-rail formatted data with frame alignment indication. The Transmit Backplane Options register is programmed to BTX2M=1, BTX2RAIL=0, BTXSFP=0. (If BTXSFP=1, the BTFP input should only pulse on the frame boundary indicating the start of the superframe alignment.) If desired, the contents of the F-bit placeholder bit positions can be bypassed around the XBAS and be inserted into the outgoing stream via the FBITBYP, CRCBYP, or FDLBYP bits of register 6, the Transmit Framing and Bypass Options register.

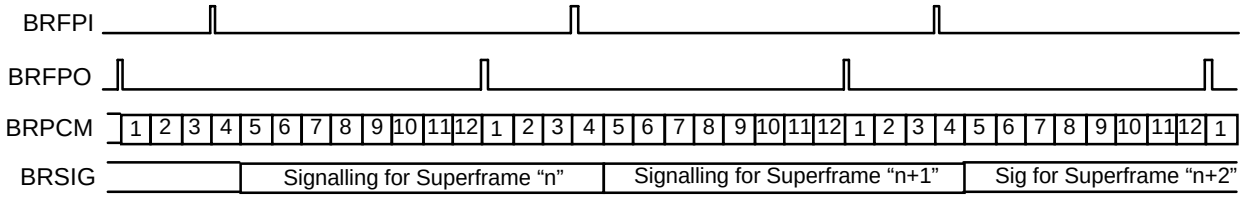
**Figure 28 - 1.544MHz Receive Backplane Interface - without signalling alignment**




The FRMR is configured to receive SF formatted data and the Receive Backplane is configured to output 1.544MHz, single-rail formatted data with superframe alignment indication, and no signalling alignment. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0,

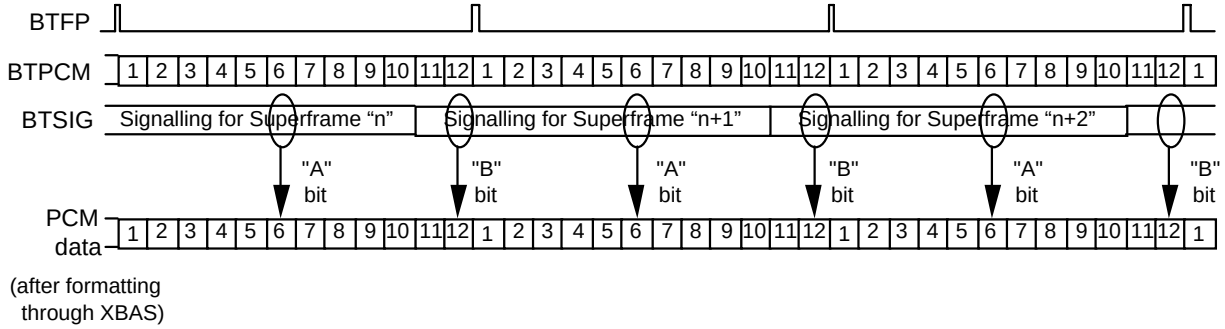
BRXSFP=1; the T1XC Receive Options register is programmed to SIGAEN=0, TXSIGA=X, or SIGAEN=1 and TXSIGA=1. The pulse applied on BRFPI can repeat every frame (dotted pulses) or every superframe, and forces only frame alignment of the PCM data and extracted signalling to the location of the input BRFPI. The superframe boundary of the signalling data lags the output superframe pulse on BRFPO by one frame.

**Figure 29 - 1.544MHz Receive Backplane Interface - with signalling alignment**




The FRMR is configured to receive SF formatted data and the Receive Backplane is configured to output 1.544MHz, single-rail formatted data with superframe alignment indication, and signalling alignment. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=1; the T1XC Receive Options register is programmed to SIGAEN=1 and TXSIGA=0. The pulse applied on BRFPI is expected to repeat every superframe, and forces both frame alignment of the PCM data and superframe alignment of the extracted signalling to the location of the input BRFPI. The superframe boundary of the PCM data is indicated by the output superframe pulse on BRFPO, which is separated by an integral number of frames from the BRFPI pulse. The superframe boundary of the signalling data lags the input superframe pulse on BRFPI by one frame.

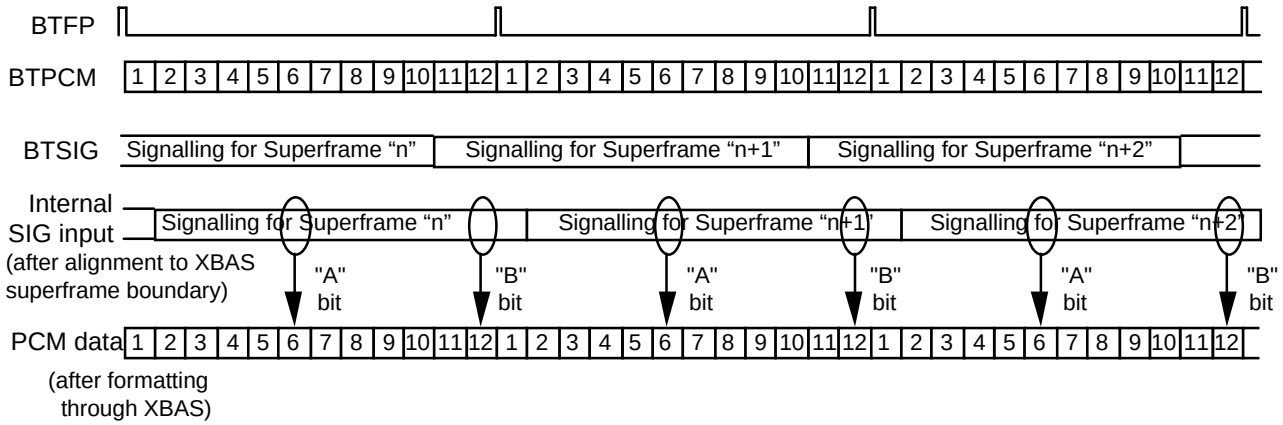
**Figure 30 - 1.544MHz Transmit Backplane Interface - without signalling alignment**




(after formatting through XBAS)

The XBAS is configured to transmit SF formatted data and the Transmit Backplane is configured to accept 1.544MHz, single-rail formatted data with superframe alignment indication, and no signalling alignment. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=1; the T1XC Receive Options register is programmed to SIGAEN=0, TXSIGA=X, or SIGAEN=1 and TXSIGA=0. The pulse applied on BTFP is expected to repeat every superframe, and forces superframe alignment of the transmitted PCM data. A potential problem arises when the signalling data on BTSIG is allowed to change midway through a transmit superframe boundary defined by the BTFP pulse. Under this condition the transmitted signalling bits are taken from two separate sets of signalling bits (i.e. the "A" bit is taken from superframe "n" and the "B" bit is taken from superframe "n+1"), which can generate non-existent signalling states. This same situation can exist if XBAS is allowed to generate its own superframe alignment and BTFP pulses every frame (i.e. BTXSFP=0). Under this condition the signalling bits may also be taken from two separate superframes.

**Figure 31 - 1.544MHz Transmit Backplane Interface - with signalling alignment**

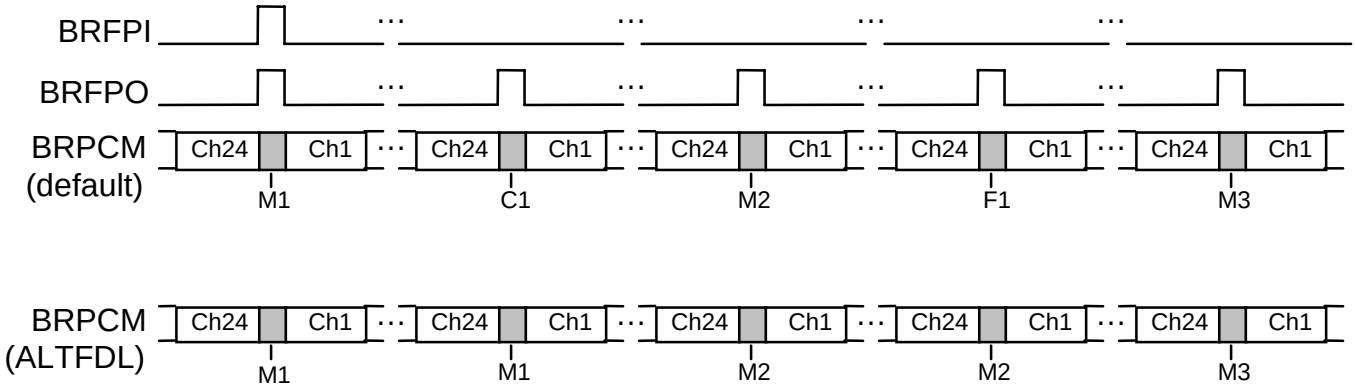



The XBAS is configured to transmit SF formatted data and the Transmit Backplane is configured to accept 1.544MHz, single-rail formatted data with superframe alignment indication, and signalling alignment. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=1; the T1XC Receive Options register is programmed to SIGAEN=1 and TXSIGA=1. The pulse applied on BTFP is expected to repeat every superframe, and forces superframe alignment of the transmitted PCM data. Internally, the signalling data on BTSIG is aligned to the internal superframe pulse generated by XBAS, thereby ensuring the signalling data does not change midway through the superframe. This internally-aligned stream is passed on to the XBAS for insertion into the transmit PCM. The "A" and "B" signalling bits now

are taken from the same superframe set of bits, eliminating the potential transmission of non-existent signalling states.

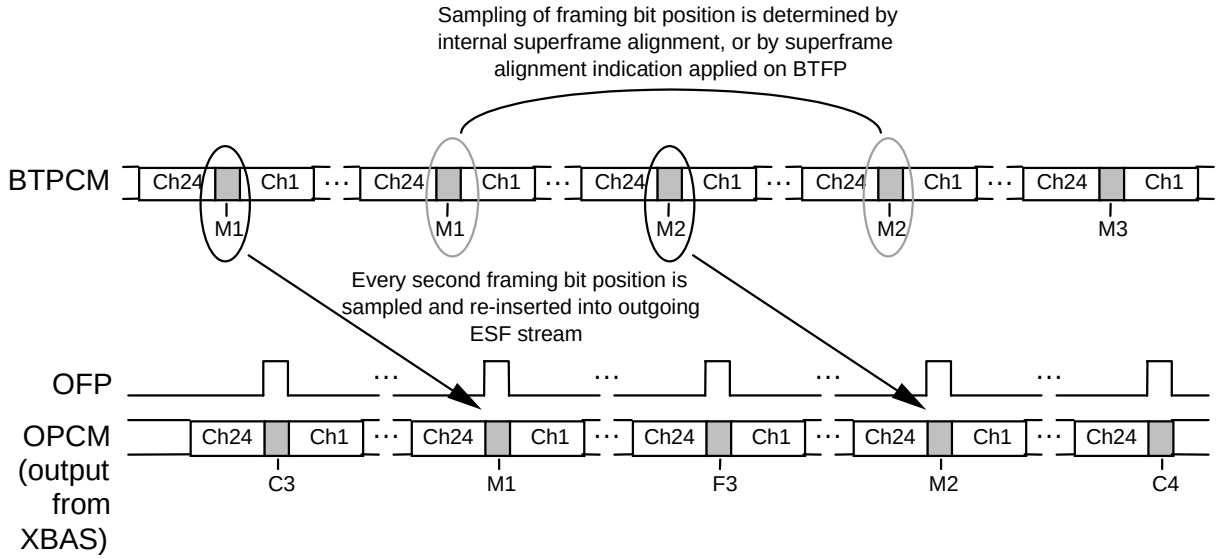
In a system that ensures that the transmit signalling changes only on the indicated superframe boundary on BTFP, the signalling aligner in the transmit direction is unnecessary.

**Figure 32 - 1.544MHz Receive Backplane Interface - with ALTFDL**




The FRMR is configured to receive ESF formatted data and the Receive Backplane is configured to output 1.544MHz, single-rail formatted data with frame alignment indication, and signalling alignment. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=0; the T1XC Receive Options register is programmed to SIGAEN=1 and TXSIGA=0. When ALTFDL=0 is programmed in the Receive Backplane Options register, the PCM data on BRPCM contains all the overhead bits (M-bits, CRC6 bits, and F-bits) in the framing bit positions. When ALTFDL=1 is programmed in the Receive Backplane Options register, the PCM data on BRPCM contains only the data link bits in the framing bit position, with each M-bit duplicated and occupying the subsequent framing bit location (overwriting the CRC-6 or F-bit).

**Figure 33 - 1.544MHz Transmit Backplane Interface - with ALTFDL**




The XBAS is configured to transmit ESF formatted data and the Transmit Backplane is configured to accept 1.544MHz, single-rail formatted data. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=0; the T1XC Receive Options register is programmed to SIGAEN=0 and TXSIGA=X. The data link, with each bit duplicated, is carried in the framing bit position on the BTPCM stream. To transmit this data link in the correct position in the ESF-formatted stream, the FDL bypass function must be used by programming the FDLBYP=1 in the Transmit Framing and Bypass Options register.

# 13 OPERATION

## 13.1 Configuring the T1XC from Reset

After a system reset (either via the RSTB pin or via the RESET register bit), the T1XC will default to the following settings:

**Table 25 - Default Settings**

| Setting | Receiver Section | Transmitter Section |
|---|---|---|
| Framing Format | SF | SF |
| Line Code | B8ZS | AMI |
| DS1 interface | • RSLC active, outputs from RSLC used internally for clock and data recovery<br>• Pins SDP/RDP/RDD and SDN/RDN/RLCV active as digital inputs RDP and RDN, but ignored | • XPLS active, default line buildout for 330-440 ft. line length<br>• Digital interface active<br>• TDP, TDN outputs NRZ data updated on falling TCLKO edge |
| System Backplane | • 1.544MHz data rate<br>• BRPCM, BRSIG active<br>• BRFPO indicates frame pulses | • 1.544MHz data rate<br>• BTPCM active<br>• BTFP indicates frame alignment<br>• BTSIG inactive |
| Data Link | • internal RFDL disabled<br>• RDLSIG and RDLCLK outputs held low | • internal XFDL disabled<br>• TDLCLK output held low, TDLSIG input ignored |
| Options | • ELST not bypassed<br>• RPCM outputs B8ZS-decoded PCM<br>• RFP indicates frame pulses<br>• PMON accumulates OOFs (not COFAs) | • Signalling alignment disabled<br>• F, CRC, FDL bit bypass disabled |

| Setting | Receiver Section | Transmitter Section |
|---|---|---|
| Timing Options | Not applicable | • Digital jitter attenuation enabled, with TCLKO referenced to BTCLK |
| Diagnostics | • All diagnostic modes disabled | • All diagnostic modes disabled |

To configure the T1XC for ESF framing format, after a reset, the following registers should be written with the indicated values:

**Table 26 - ESF Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 00H | Select B8ZS line code for receiver |
| Write XBAS Configuration Register | 44H | 3XH | Select B8ZS, enable for ESF in transmitter (bits defined by 'X' determine the FDL data rate & Zero Code suppression algorithm used) |
| Write FRMR Configuration Register | 20H | 1XH<br>or<br>5XH<br>or<br>9XH | Select ESF, 2 of 4 OOF threshold<br><br>Select ESF, 2 of 5 OOF threshold<br><br>Select ESF, 2 of 6 OOF threshold<br>(bits defined by 'X' determine the FDL data rate, should be same as those written to XBAS) |
| Write RBOC Enable Register | 2AH | 00H<br>or<br>02H | Enable 8 out of 10 validation<br><br>Enable 4 out of 5 validation |
| Write ALMI Configuration Register | 2CH | 1XH | Select ESF (bits defined by 'X' determine the ESF YELLOW data rate, should be same as those written to FRMR) |

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write IBCD Configuration Register | 3CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 3EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 3FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 40H | 1XH | Select ESF (bits defined by 'X' should be same as those written to FRMR) |

To configure the T1XC for SLC®96 framing format, after a reset, the following registers should be written with the indicated values:

**Table 27 - SLC®96 Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 80H | Select AMI line code for receiver |
| Write XBAS Configuration Register | 44H | 08H | Select AMI, enable for SLC®96 in transmitter |
| Write FRMR Configuration Register | 20H | 08H<br>or<br>48H<br>or<br>88H | Select SLC®96, 2 of 4 OOF threshold<br>Select SLC®96, 2 of 5 OOF threshold<br>Select SLC®96, 2 of 6 OOF threshold |
| Write ALMI Configuration Register | 2CH | 08H | Select SLC®96 |
| Write IBCD Configuration Register | 3CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 3EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 3FH | 44H | Program Loopback Deactivate Code pattern |

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write SIGX Configuration Register | 40H | 08H | Select SLC®96 |

To configure the T1XC for SF framing format, after a reset, the following registers should be written with the indicated values:

**Table 28 - SF Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 80H | Select AMI line code for receiver |
| Write XBAS Configuration Register | 44H | 00H | Select AMI, enable for SF in transmitter |
| Write FRMR Configuration Register | 20H | 00H<br>or<br>40H<br>or<br>80H | Select SF, 2 of 4 OOF threshold<br><br>Select SF, 2 of 5 OOF threshold<br><br>Select SF, 2 of 6 OOF threshold |
| Write ALMI Configuration Register | 2CH | 00H | Select SF |
| Write IBCD Configuration Register | 3CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 3EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 3FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 40H | 00H | Select SF |

To configure the T1XC for T1DM framing format, after a reset, the following registers should be written with the indicated values:

**Table 29 - T1DM Frame Format**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 80H | Select AMI line code for receiver |
| Write XBAS Configuration Register | 44H | 04H<br>or<br>0CH | Select AMI, enable for T1DM in transmitter |
| Write FRMR Configuration Register | 20H | 04H<br>or<br>44H<br>or<br>84H | Select T1DM, 2 of 4 OOF threshold<br><br>Select T1DM, 2 of 5 OOF threshold<br><br>Select T1DM, 2 of 6 OOF threshold |
| Write ALMI Configuration Register | 2CH | 04H<br>or<br>0CH | Select T1DM with standard RED integration<br>Select T1DM with alternate RED integration |
| Write IBCD Configuration Register | 3CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register | 3EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register | 3FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 40H | 04H | Disable robbed bit signalling extraction |

To access the Performance Monitor Registers, the following polling sequence should be used:

**Table 30 - PMON Polling Sequence**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write PMON LCV Count (LSB) Register | 4AH | 00H | Latch performance data into all PMON registers |

| Action | Addr | Data | Effect |
|---|---|---|---|
| Read LCV Count (LSB) Register | 4AH | | Read least significant byte of line code violation count |
| Read LCV Count (MSB) Register | 4BH | | Read most significant byte of line code violation count |
| Read BEE Count (LSB) Register | 4CH | | Read least significant byte of bit error event count |
| Read BEE Count (MSB) Register | 4DH | | Read most significant byte of bit error event count |
| Read FER Count Register | 4EH | | Read Framing bit error count |
| Read OOF/COFA Count Register | 4FH | | Read out-of-frame event count (or change of frame alignment event count if COFA bit in T1XC Receive Options Register is set) |

To configure the T1XC to utilize the internal HDLC transmitter and receiver, the following registers should be written with the indicated values:

**Table 31 - ESF FDL Processing**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write T1XC Datalink Options Register | 02H | A0H | Enable RFDL & XFDL to process the ESF Facility Datalink (XBAS and FRMR must be configured for ESF framing format). The DMA signals are available on RDLINT, RDLEOM, TDLINT, TDLUDR outputs. |

## 13.2 Using the Internal FDL Transmitter

If the XFDL is to be used, then during initialization of T1XC, XFDL should be enabled by setting the EN bit in the XFDL Configuration Register to logic 1. If the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. The XFDL will transmit idle codes until valid data is presented to it.

The XFDL can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the TDLINT and TDLUDR outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the XFDL Status Register to determine when to write to the XFDL Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses either the TDLINT output, or the main processor INTB output and the interrupt source registers, to determine when to write to the XFDL Transmit Data Register. In the DMA controlled mode, the TDLINT output of the XFDL is used as a DMA request input to the DMA controller, and the TDLUDR output is used as an interrupt to the processor to allow handling of exceptions. The TDLUDR output can also be enabled to generate a processor interrupt through the common INTB output via the TDLUDRE bit in the Datalink Options register.

### 13.2.1 Polled Mode

If the XFDL data transfer is operating in the polled mode (TXDMASIG, TDLINTE, and TDLUDRE bits in the Datalink Options Register are set to logic 0), then a timer periodically starts up a service routine, which should process data as follows:

1. Read the XFDL Interrupt Status Register and poll the UDR and INT bits.

2. If UDR=1, then clear the UDR bit in the XFDL Interrupt Status Register to logic 0, and restart the current frame. Go to step 1.

3. If INT=1, then:

   a) If there is still data to send, then write the next data byte to the XFDL Transmit Data Register;

   b) If all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1.

4. If EOM bit was set to logic 1 in step 3b, then:

   a) Read the XFDL Interrupt Status Register and check the UDR bit.

   b) If UDR =1 then reset the UDR bit in the XFDL Interrupt Status Register

   and the EOM bit in the XFDL Configuration Register to logic 0, and retransmit the last frame.

5. Go to step 1.

### 13.2.2 Interrupt Mode

In the case of interrupt driven data transfer, the TDLINT output is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode. The INTE bit in the XFDL Configuration Register must be set to logic 1. Alternately, the INTB output can be connected to the interrupt input of the processor if the TDLINTE bit of the Datalink Options Register is set to logic 1. If this mode is used, additional polling of the Master Interrupt Source register must be performed to identify the cause of the interrupt before the initiating the interrupt service routine.

### 13.2.3 DMA-Controlled Mode

The XFDL can also be used with a DMA controller to process the frame data. In this case, the TDLUDR output is connected to the processor interrupt input. The TDLINT output of the XFDL is connected to the DMA request input of the DMA controller. The INTE bit in the XFDL Configuration Register must be set to logic 1 before enabling the XFDL. The DMA controller writes a data byte to the XFDL whenever the TDLINT output is high. If there is a problem during transmission and an underrun condition occurs, then the TDLUDR output goes high and the processor is interrupted. The processor can then halt the DMA controller, reset the UDR bit in the XFDL Interrupt Status Register, reset the frame data pointers, and restart the DMA controller to resend the data frame. After the message transmission is completed, the DMA controller must initiate a write to set the EOM bit in the XFDL Configuration Register and then verify that TDLUDR is not set prior to setting EOM.

## 13.3 Using the Internal FDL Receiver

On power up of the T1XC, the RFDL should be disabled by setting the EN bit in the Configuration Register to logic 0. The Interrupt Control/Status Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated.

After the Interrupt Control/Status Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOMR bits are passed through the buffer, this dummy write allows the Status Register to accurately reflect the current state of the data link. A Status Register read after a Data Register read of the dummy byte will return EOMR as logic 1 and FLG as

logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data.

### 13.3.1 Polled Mode

In the polled mode, the RDLINT and RDLEOM outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the RFDL Interrupt Control/Status to determine when to read the RFDL Receive Data Register. If the RFDL data transfer is operating in the polled mode, entry to the service routine is from a timer. The processor service routine should process the data in the following order:

1. Poll the INT bit in the RFDL Interrupt Control/Status Register (reg. 39H) until it is set to logic 1. Once INT is set to logic 1, then proceed to step 2.

2. Read the RFDL Receive Data Register (reg. 3BH).

3. Read the RFDL Status Register (reg 3AH) to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

   c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

   ELSE

   d) Save the last data byte read.

   e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register (reg 3AH) to process the frame properly.

   f) If FE=0, then go to step 2, else go to step 1.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

### 13.3.2 Interrupt Mode

In the interrupt driven mode, the processor controlling the RFDL uses either the RDLINT output, or the main processor INTB output (RDLINTE bit of the T1XC Datalink Options Register (reg 02H) is set to logic 1) and the Interrupt Source Registers (reg. 08H and 09H), to determine when to read the RFDL Receive Data Register. The RXDMASIG bit in the T1XC Datalink Options Register should be set to logic 1. RDLINTE of the same register should be set to logic 1 if the INTB output is used as the interrupt source. The processor interrupt service routine should process the data in the following order:

1. Wait for an interrupt originating from the RFDL. Once the interrupt is set, then proceed to step 2.

2. Read the RFDL Receive Data Register (reg. 3BH).

3. Read the RFDL Status Register (reg 3AH) to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

   c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

   ELSE

   d) Save the last data byte read.

   e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register (reg 3AH) to process the frame properly.

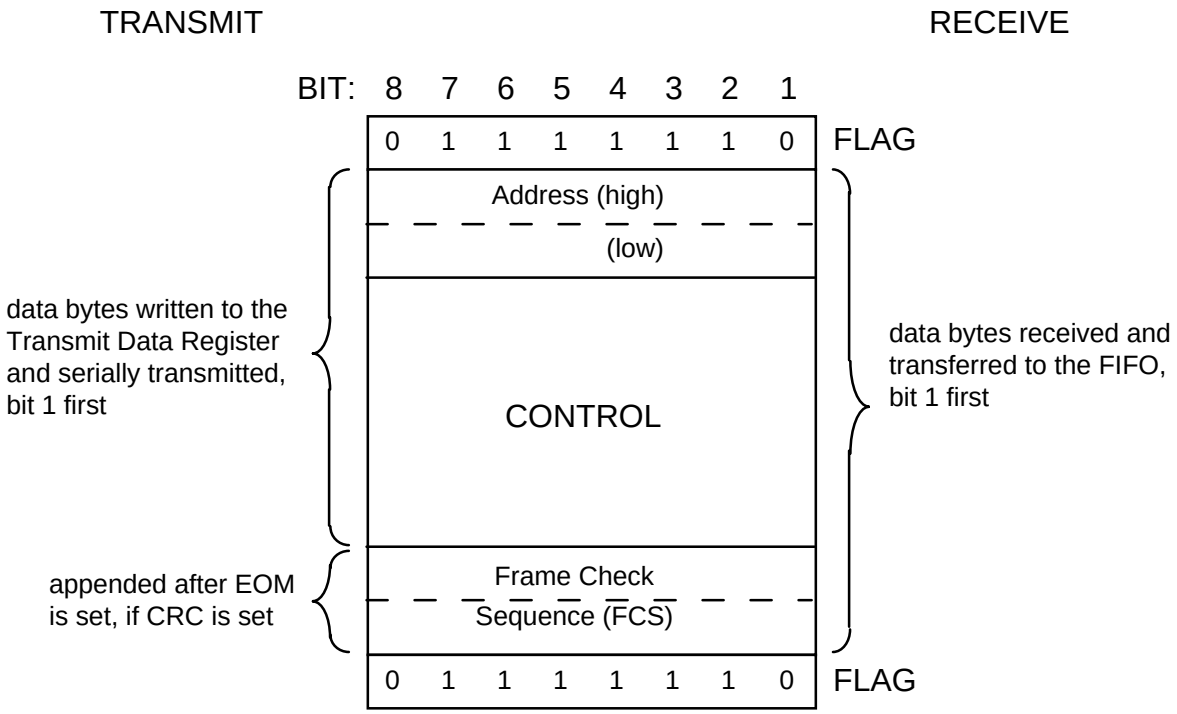
   f)If FE= EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register (reg 3AH 2, else go to step 1.

### 13.3.3 DMA- Controlled Mode

The RFDL can also be used with a DMA controller to process the frame data. In the DMA controlled mode, the RDLINT output of the RFDL is used as a DMA request input to the DMA controller, and the RDLEOM output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame. The RXDMASIG bit of the T1XC Datalink Options Register (reg 02H) should be set to logic 1.

The RDLINT output of the RFDL is connected through a gate to the DMA request input of the DMA controller to optionally inhibit the DMA request if the RDLEOM output is high. The DMA controller reads the data bytes from the RFDL whenever the RDLINT output is high. When the current byte read from the RFDL Data Register is the last byte in a frame (due to an end-of-message or an abort), or an overrun condition occurs, then the RDLEOM output goes high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame. The RDLEOM output can optionally be enabled to generate a processor interrupt through the common INTB output via the RDLEOME bit in the Datalink Options register, rather than tying the RDLEOM output directly to the microprocessor. This allows a central microprocessor controlling the T1XC operation to also respond to conditions affecting the DMA servicing of RFDL. When using the INTB output, the central processor must poll the T1XC Master Interrupt Source Registers (reg. 08H and 09H) to identify the source of the interrupt before beginning any interrupt service routine.

**Figure 34 - Typical Data Frame**



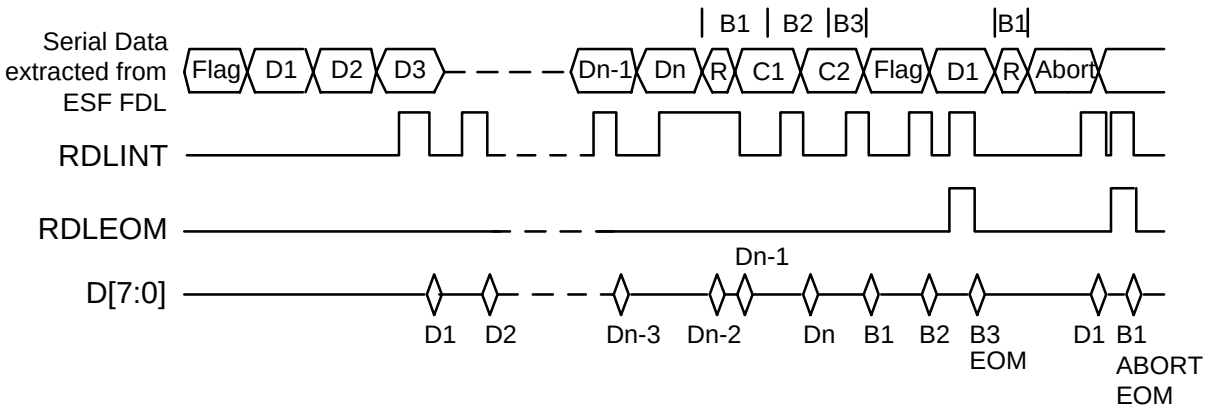

Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

### 13.3.4 Key used on subsequent diagrams:

| | |
|---|---|
| Flag | - flag sequence (01111110) |
| Abort | - abort sequence (01111111) |
| D1 - Dn | - n frame data bytes |
| R | - remainder bits (less than 8) |
| C1, C2 | - CRC-CCITT information |
| B1, B2, B3 | - groupings of 8 bits |

**Figure 35 - RFDL Normal Data and Abort Sequence**



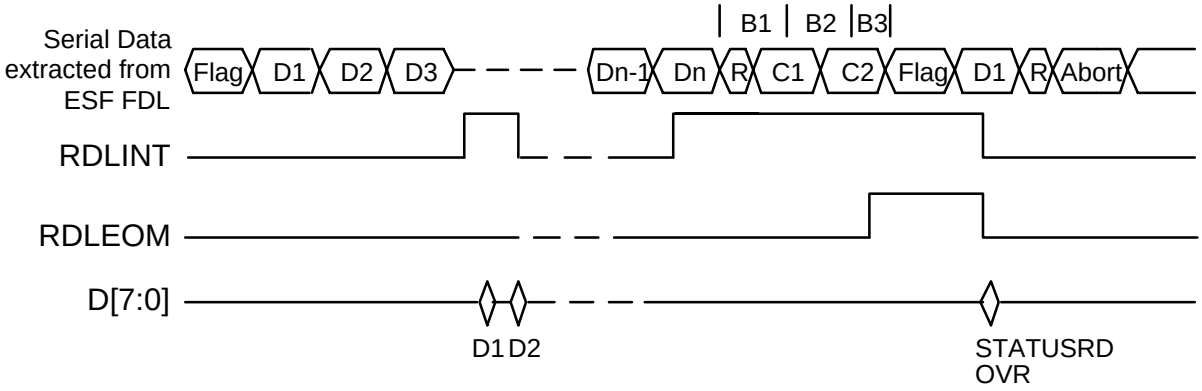

This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the Data Register, followed by a read of the Status Register. A read of the Data Register sets the RDLINT output to low if no more data exists in the FIFO buffer. The status of the FE bit returned in the Status Register read will indicate the FIFO buffer fill status as well. The Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RDLINT output does not go low after the first Data Register read because a data byte still remains to be read. The RDLINT output goes low after Data Register read Dn-1. The FE bit will be logic 0 in Status Register read Dn-2 and logic 1 in Status Register read Dn-1.

The RDLEOM output goes high as soon as the last byte in the frame is read from the Data Register. The RDLINT output will go low if the FIFO buffer is empty. The next Status Register read will return a value of logic 1 for the EOMR and FLG bits, and cause the RDLEOM output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the Data Register and the RDLEOM output is set high. The processor then reads the Status Register which will return a value of logic 1 for the EOMR and FLG bits, and set the RDLEOM output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

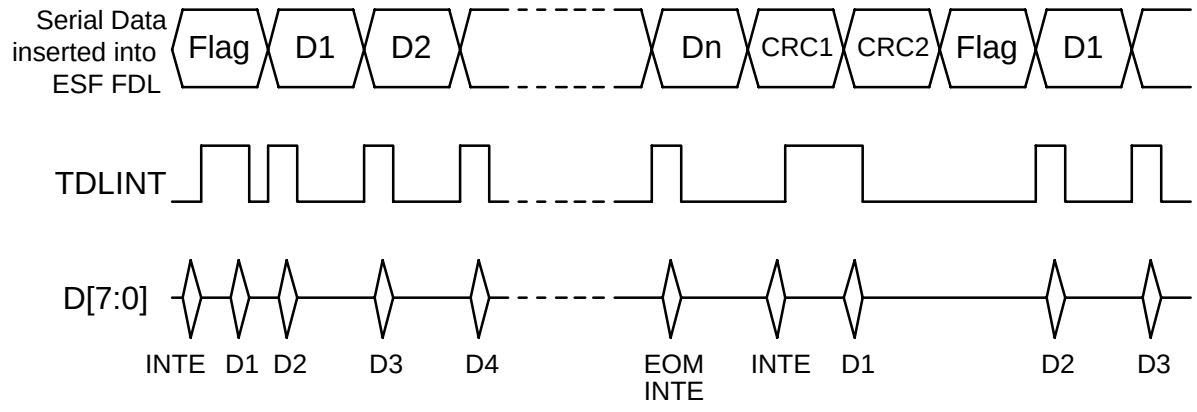
After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

**Figure 36 - RFDL FIFO Overrun**



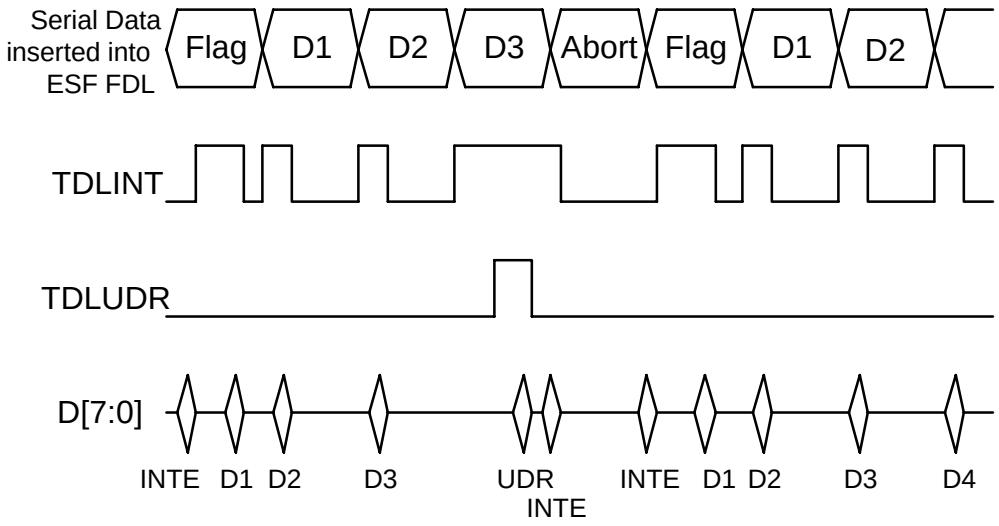

This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the RDLEOM output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

**Figure 37 - XFDL Normal Data Sequence**



This diagram shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the Configuration Register to logic 1, thus enabling the TDLINT signal. When TDLINT goes high, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the Transmit Data Register. When this byte begins to be shifted out on the data link, TDLINT goes high. This restarts the interrupt service routine, and the next data byte (D2) is written to the Transmit Data Register. When D2 begins to be shifted out on the data link, TDLINT goes high again. This cycle continues until the last data byte (Dn) of the frame is written to the Transmit Data Register. When Dn begins to be shifted out on the data link, TDLINT again goes high. Since all the data has been sent, the interrupt service routine sets the EOM bit in the Configuration Register to logic 1. The TDLINT interrupt should also be disabled at this time by setting the INTE bit to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TDLINT signal can be re-enabled by setting the INTE bit in the Configuration Register to logic 1, and the cycle starts again.

**Figure 38 - XFDL Underrun Sequence**




This diagram shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within five rising clock edges after TDLINT goes high at the beginning of the transmission of byte D3. The TDLUDR interrupt becomes active at this point, and an abort, followed

by a flag, is sent out on the data link. Meanwhile, the processor must clear the TDLUDR interrupt by setting the UDR bit in the Status Register to logic 0. The TDLINT interrupt should also be disabled at this time by setting the INTE bit in the Configuration Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

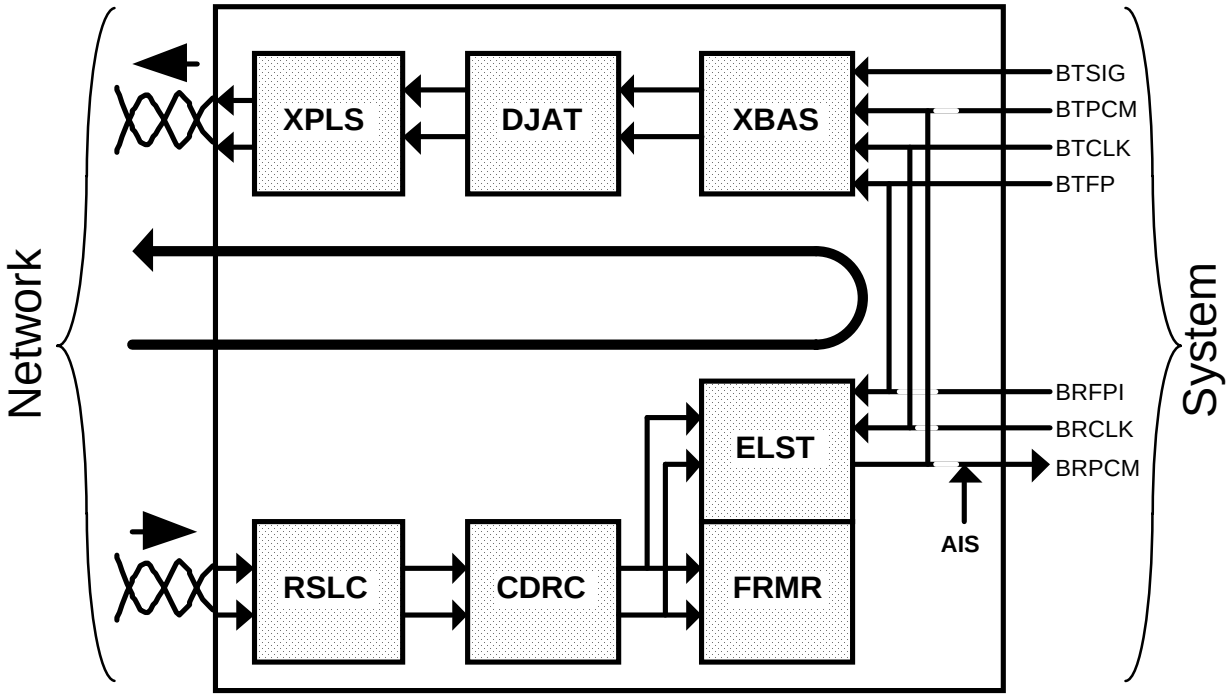
## 13.4 Using the Loopback Modes

The T1XC provides four loopback modes to aid in network and system diagnostics. The network loopbacks (PAYLOAD and LINE) can be initiated at any time via the µP interface, but are usually initiated once an inband loopback activate code is detected. The system loopbacks (Diagnostic DIGITAL and METALLIC) can be initiated at any time by the system via the µP interface to check the path of system data through the transceiver.

### 13.4.1 Payload Loopback

When PAYLOAD loopback (PAYLB) is initiated by writing 20H to the Master Diagnostics Register (0AH), the T1XC is configured to internally connect the output of the ELST to the PCM input of XBAS. The data is read out of ELST timed to the transmitter clock, and the transmit frame alignment indication is used to synchronize the output frame alignment of ELST. Conceptually, the data flow through T1XC in this loopback condition can be shown as follows:

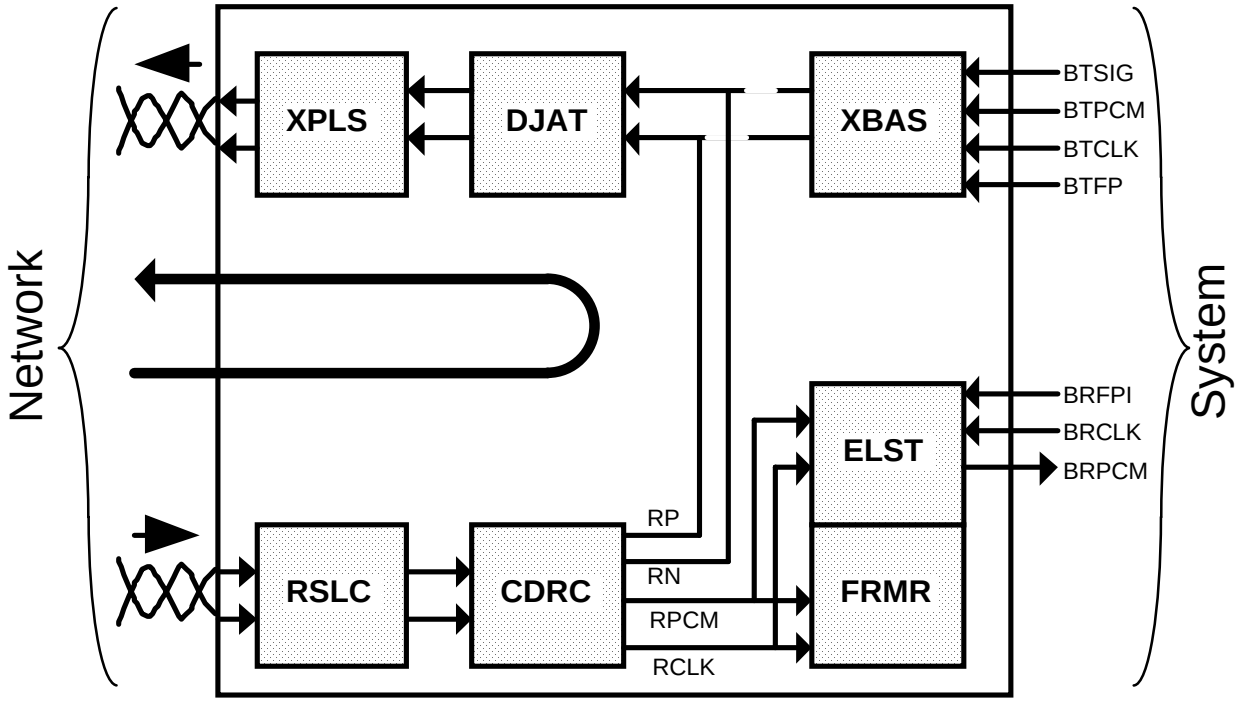
**Figure 39 - Payload Loopback**




### 13.4.2 Line Loopback

When LINE loopback (LINELB) is initiated by writing 10H to the Master Diagnostics Register (0AH), the T1XC is configured to internally connect the dual-rail positive and negative line data pulses output from CDRC to the dual-rail inputs of DJAT. The jitter in line data is attenuated through DJAT, therefore the DJAT Divisor registers (19H and 1AH) must be programmed to the value 2FH. Also, the transmit clock source must be changed from BTCLK to the recovered clock RCLKO by writing 08H to the Transmit Backplane Options register (05H). Conceptually, the data flow through T1XC in this loopback condition can be shown as follows:

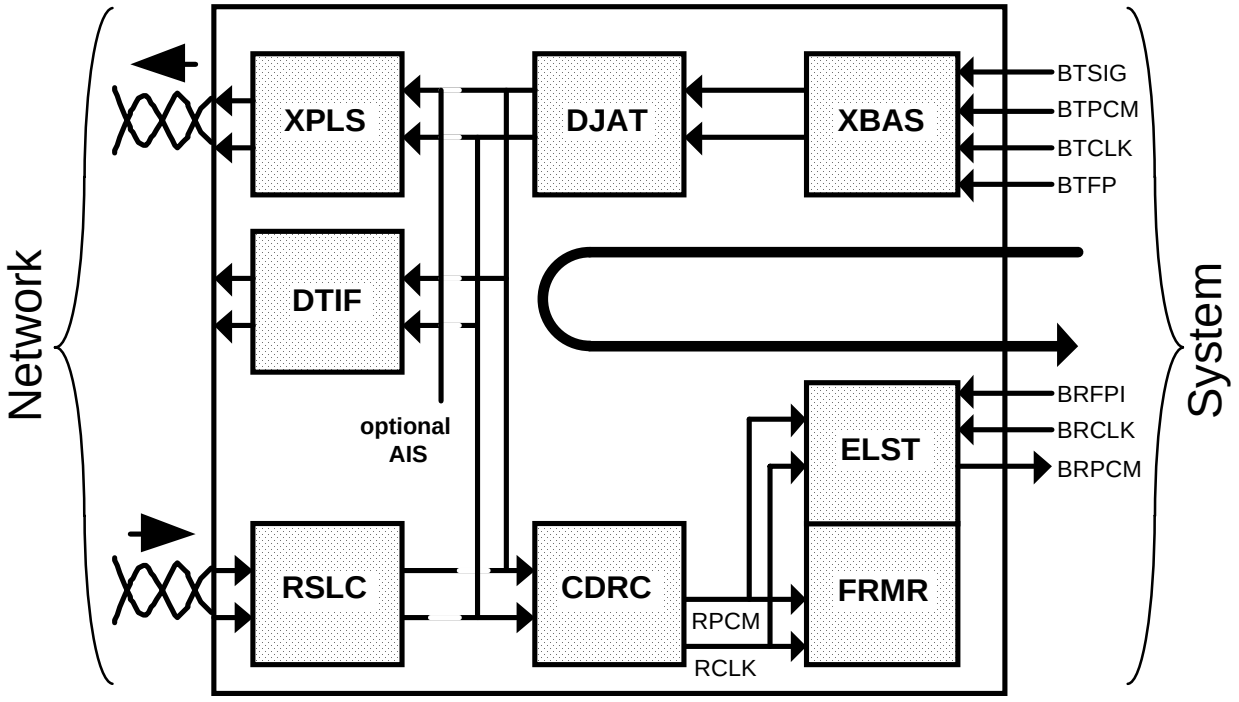
**Figure 40 - Line Loopback**




### 13.4.3 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) is initiated by writing 04H to the Master Diagnostics Register (0AH), the T1XC is configured to internally connect the dual-rail positive and negative data pulses output from DJAT to the dual-rail inputs of CDRC. As a result, if DDLB is to be used, TUNI must be set to logic 0 in the Transmit Interface Configuration register (04H) and RUNI must be set to logic 0 in the Receive Interface Configuration register (03H). Conceptually, the data flow through T1XC in this loopback condition can be shown as follows:

**Figure 41 - Diagnostic Digital Loopback**



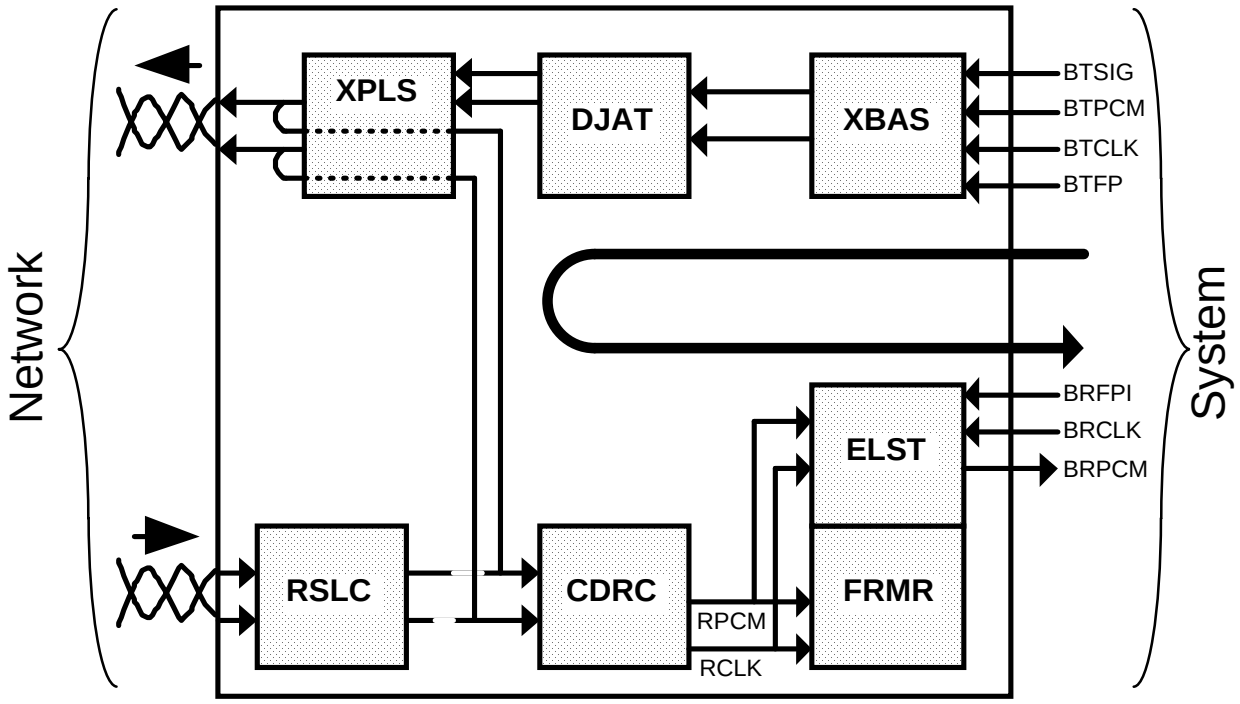

### 13.4.4 Diagnostic Metallic Loopback

When Diagnostic Metallic loopback (DMLB) is initiated by writing 08H to the Master Diagnostics Register (0AH), the T1XC is configured to internally connect the RZ dual-rail positive and negative data pulses from XPLS Performance Monitor, representing the sliced versions of the analog output signals on the TAP and TAN pins, to the dual-rail inputs of CDRC. The Performance Monitor inputs internal to XPLS have a fixed slicing threshold and their monitoring position is located at the driver outputs. With this configuration waveform templates for very long line lengths can cause erroneous data to be looped back when the "negative" excursion of the transmit pulse exceeds the slicing threshold. Therefore, when using DMLB, an XPLS template for short line lengths (0-110 ft.) must be selected by writing 40H to the XPLS Line Length Configuration register (14H).

Because the XPLS feeds back bipolar data when in metallic loopback, RUNI must be set to logic zero in the Receive Interface Configuration register (03H) to configure the receive side for bipolar data. Similarly, since XPLS cannot be used when the transmit side is set to unipolar mode, TUNI must be logic 0 in the Transmit Interface Configuration register (04H).

Conceptually, the data flow through T1XC in this loopback condition can be shown as follows:

**Figure 42 - Diagnostic Metallic Loopback**




## 13.5 Using the Per-Channel Serial Controllers

### 13.5.1 Initialization

Before the TPSC (RPSC) block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 0. Then, all 72 locations of the TPSC (RPSC) must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 1.

### 13.5.2 Direct Access Mode

Direct access mode to the TPSC or RPSC is not used in the T1XC. However, direct access mode is selected by default whenever the T1XC is reset. The IND

bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

### 13.5.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC or RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC or RPSC is processing an access request; when the BUSY bit is logic 0, the TPSC or RPSC has completed the request.

The indirect write programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write the channel data to the TPSC (RPSC) Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.

4. Read the requested channel data from the TPSC (RPSC) Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

## 13.6 Programming the XPLS Waveform Template

The internal XPLS CODE registers, at address 17H, can be used to create a custom waveform across the analog transmit outputs, TAP and TAN. These eight CODE registers are accessed indirectly through register 16H and contain 4-bit binary values corresponding to one of 16 quantized levels for the amplitude of the output pulse during each of eight synchronous, "high-speed" clock periods within a TCLKO cycle. The full swing of the amplifier outputs TAP and TAN ranges from 0 to 3.89 Volts. The codes select the voltage level into 50Ω as follows:

**Table 32 - Typical Output Voltages for XPLS Codes**

| CODE (Reg 17H) | Typical Output Voltage | CODE (Reg 17H) | Typical Output Voltage |
|---|---|---|---|
| 0000 | 0.00 V | 1000 | 2.09 V |
| 0001 | 0.28 V | 1001 | 2.35 V |
| 0010 | 0.54 V | 1010 | 2.60 V |
| 0011 | 0.80 V | 1011 | 2.86 V |
| 0100 | 1.06 V | 1100 | 3.12 V |
| 0101 | 1.32 V | 1101 | 3.38 V |
| 0110 | 1.57 V | 1110 | 3.63 V |
| 0111 | 1.83 V | 1111 | 3.89 V |

The contents of the CODE registers are used by XPLS and internally applied to the output D/A converter in sequence, beginning with CODE reg #0, on the first falling edge of the internal, synchronous high-speed clock once TCLKO has gone low. The first four codes determine the shape of the bulk of the pulse, whereas the last four codes determine the shape of the tail end of the pulse. Depending on the polarity of the input pulse (either on the positive pulse input or the negative pulse input to XPLS), the bulk of the pulse is generated on either TAP or TAN, with the tail generated on TAN or TAP, respectively. The pulse is produced differentially across the transformer primary so that, for example, while the first four codes are generating the pulse on TAP, TAN is grounded through the output amplifier. To generate the negative portion of the pulse, the last four codes generate the tail of the pulse on TAN while TAP is grounded through the other output amplifier. The ON-resistance of either TAP or TAN output amplifier is nominally 2.6Ω when acting as a ground for the transformer. The output

impedance of the amplifier when driving the pulse is typically <0.5Ω at half the bit rate.

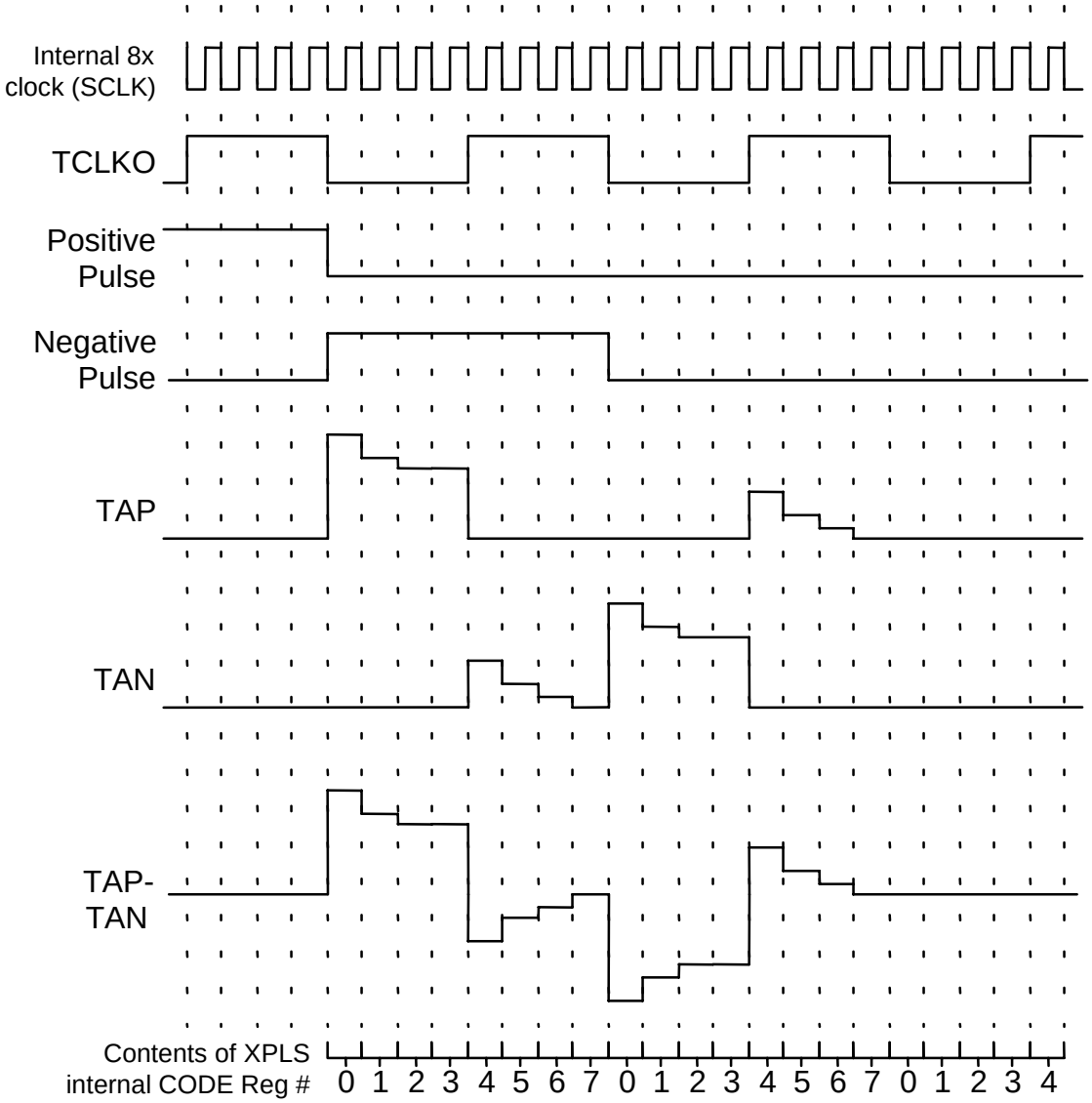
The default preprogrammed XPLS code sequence values are as follows:

**Table 33 - Preprogrammed XPLS Code Sequences**

| Length Setting (ft.) | Code Register Values | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Register #** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| 0-110 | B | A | A | A | 3 | 3 | 2 | 1 |
| 110-220 | C | B | A | A | 4 | 3 | 2 | 1 |
| 220-330 | E | C | B | B | 5 | 4 | 2 | 1 |
| 330-440 | E | D | B | B | 6 | 5 | 3 | 1 |
| 440-550 | F | E | B | B | 8 | 5 | 3 | 1 |
| 550-660 | F | C | B | A | 8 | 5 | 3 | 1 |
| >660 | F | C | A | A | A | 5 | 3 | 1 |

Figure 43 shows the relationship between the TCLKO, the internal synchronous, high-speed clock SCLK timing, and the application of the CODE register contents for a positive pulse immediately followed by a negative pulse. The resultant waveform across TAP and TAN is also shown.

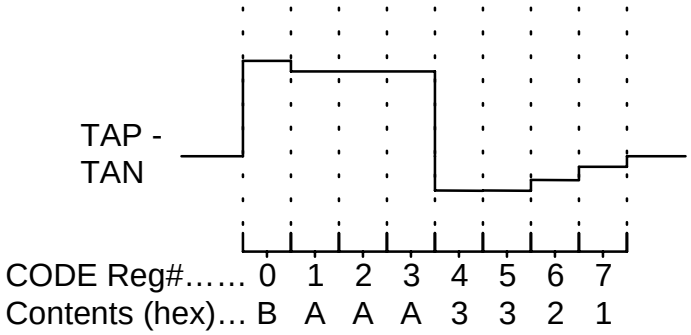
**Figure 43 - CODE Register Sequence During Pulse Generation**




The actual waveform produced at the transformer secondary depends upon the turns ratio of the transformer used, the series resistance on the primary side used to match the line, the output impedance of the amplifier, the on-resistance of the amplifier while providing the transformer ground, and the transformer winding resistance. To ensure that the amplifiers can drive the reflected load, it is recommended that a transformer have a turns ratio of no more than 1:2. It is also recommended that the codes presented here be used as a guideline and that the actual code values be verified (and modified) on the bench with the device driving the actual transformer and termination expected in the application.

The example in Figure 44 shows the D/A codes necessary for XPLS to drive a DSX-1 pulse using a Pulse Engineering 1:1.36 ± 5% turns ratio step-up transformer (PE # 64952, or PE 65774) and 0-110ft of 22 AWG twisted pair cable. (These code values are the same as those contained in the internal XPLS ROM for the 0-110 ft. waveform template, i.e. SM=1, ILS[2:0]=000.)

**Figure 44 - CODE Register Sequence For 0-110 feet Build-out**




To program the XPLS CODE registers for a custom waveform template, the following sequence should be used:

1. Set the RPT bit in the XPLS Configuration Register to logic 0.
2. Write the CODE register address (0-7) in the XPLS CODE Indirect Address register.
3. Write the desired code value to the XPLS CODE Indirect Data Register (register 17H).
4. Repeat steps 2 and 3 until all the CODE registers are written.
5. Enable XPLS to generate the new waveform by setting RPT to logic 1.

The contents of the XPLS CODE registers can be reviewed at any time by using the following sequence:

1. Write the CODE register address (0-7) in the XPLS CODE Indirect Address register.
2. Read the XPLS CODE Indirect Data Register (register 17H). This returns the code contents of the desired code register.

## 13.7 Using the Digital Jitter Attenuator

The key to using DJAT lies in selecting the appropriate divisors for the phase comparison between the selected reference clock and the generated smooth TCLKO. These divisors, N1 and N2, are programmed by writing to registers 19h and 1Ah, respectively. whenever the SYNC bit is set to logic 1, N1+1 and N2+1 must each be divisible by 48.

### 13.7.1 Default Application

Upon reset, the T1XC default condition provides jitter attenuation with TCLKO referenced to the transmit clock, BTCLK. The DJAT SYNC bit is also logic 1 by default. DJAT is configured to divide its input clock rate, BTCLK, and its output clock rate, TCLKO, both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the DJAT DPLL. The phase delay between BTCLK and TCLKO is synchronized to the physical data delay through the FIFO. For example, if the phase delay between BTCLK and TCLKO is 12UI, the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with the transmit backplane running at 1.544MHz.

### 13.7.2 Data Burst Application

In applications where the 2.048MHz transmit backplane rate (or a higher backplane rate with external gapping) is used, a few factors must be considered to adequately filter the resultant TCLKO into a smooth 1.544MHz clock. The magnitude of the phase shifts in the incoming bursty data are too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

When using the 2.048MHz transmit backplane rate, the input clock to DJAT is a gapped version of the 2.048MHz BTCLK. The phase shifts of the input clock with respect to the generated TCLKO in this case are large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to C0H (i.e. divisors of 193). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The DJAT SYNC option must be disabled, since the divisor magnitude of 193 is not an integer multiple of the FIFO length, 48.

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

With SYNC disabled, CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth TCLKO is 40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

### 13.7.3 Elastic Store Application

In multiplex applications where the jitter attenuation is not required, the DJAT FIFO can be used to provide an elastic store function. For example, in a M12 application, the data is written into the FIFO at 1.544MHz and the data is read out of the FIFO with a gapped DS2 rate clock applied on TCLKI. In this configuration, the Timing Options OCLKSEL[1:0] bits should be programmed to 01, the TCLKISEL bit should be programmed to 1, and the SMCLKO bit should be programmed to 1. Also, the DJAT SYNC and LIMIT bits should be disabled and the CENT bit enabled. This provides the maximum phase difference between the input clock and the gapped output clock of 40UI. The maximum jitter and wander between the two clocks is 8UIp-p.

### 13.7.4 Alternate TCLKO Reference Application

In applications where TCLKO is referenced to an Nx8 kHz clock source applied on TCLKI, DJAT can be configured by programming the output clock divisor, N2, to C0H and the input clock divisor, N1, to the value (N-1). The resultant input clocks to the phase comparator are both 8kHz. The DJAT SYNC and LIMIT bits should be disabled in this configuration.

## 13.8 Using the Performance Monitor Counter Values

All PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval at a $10^{-3}$ BER is less than 0.001%. The odds of any one of the counters saturating during a one second sampling interval go up as the BER increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown below for various counters:

**Table 34 - PMON Counter Saturation Characteristics**

| Counter | Format | BER |
|---|---|---|
| LCV | all | $2.75 \times 10^{-3}$ |
| FER | SF | $4.0 \times 10^{-3}$ |
| | T1DM | $4.0 \times 10^{-3}$ |
| | SLC®96 | $8.0 \times 10^{-3}$ |
| | ESF | $1.58 \times 10^{-2}$ |
| BEE | SF | $6.4 \times 10^{-2}$ |
| | T1DM | $9.2 \times 10^{-3}$ |
| | SLC®96 | $1.35 \times 10^{-1}$ |
| | ESF | cannot saturate |

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. Figure 45-Figure 52 show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above $10^{-3}$, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

**Figure 45 - LCV Count vs. BER**

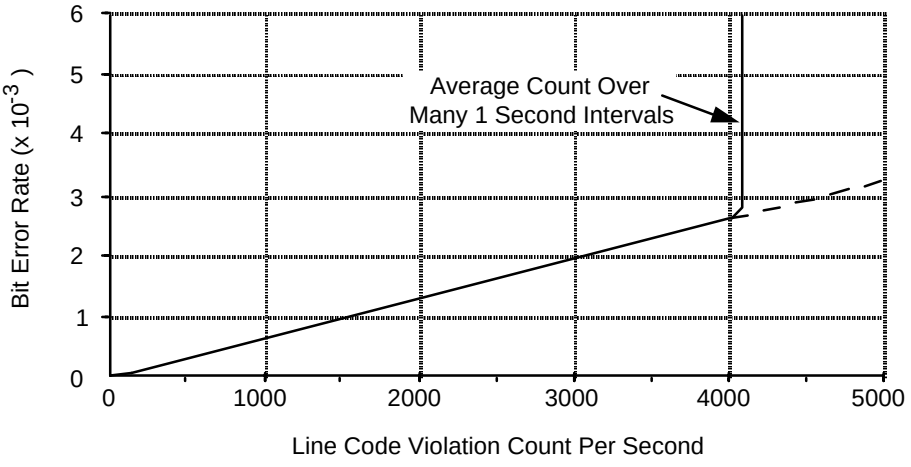


**Figure 46 - FER Count vs. BER for SF and T1DM Framing Formats**

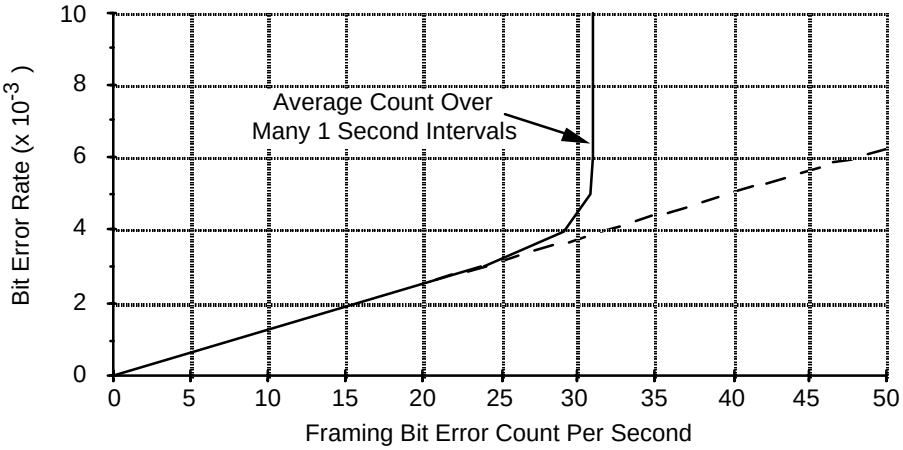



**Figure 47 - FER Count vs. BER for SLC®96 Framing Format**

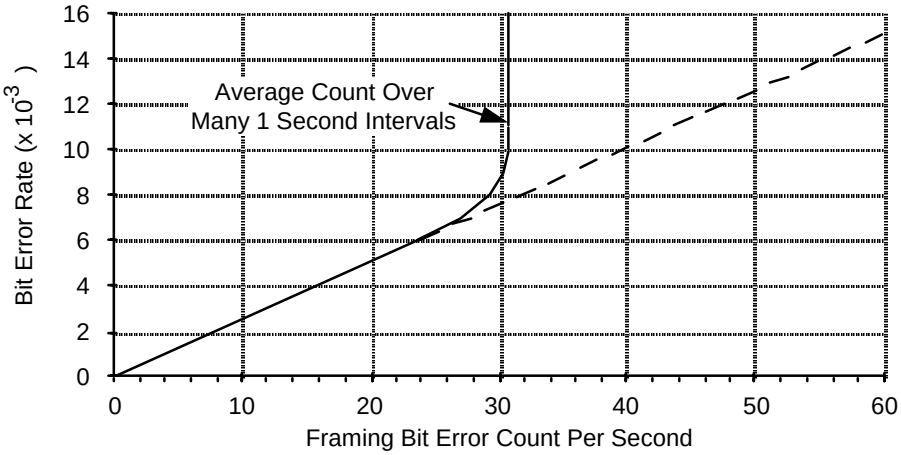


**Figure 48 - FER Count vs. BER for ESF Framing Format**

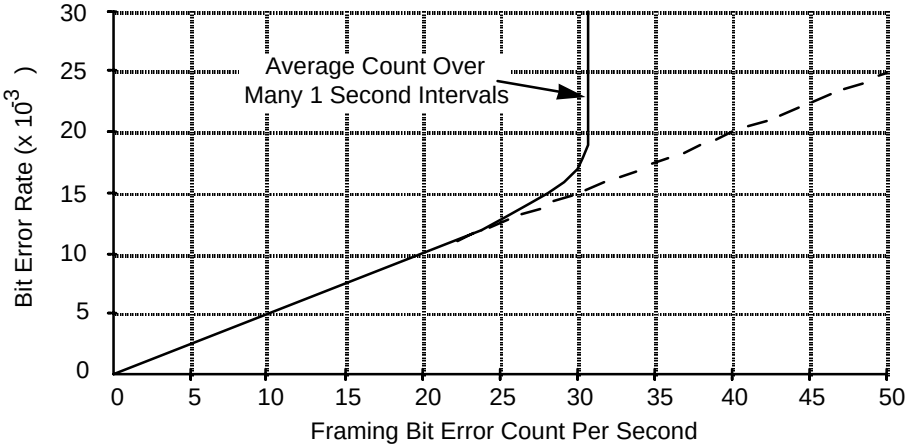
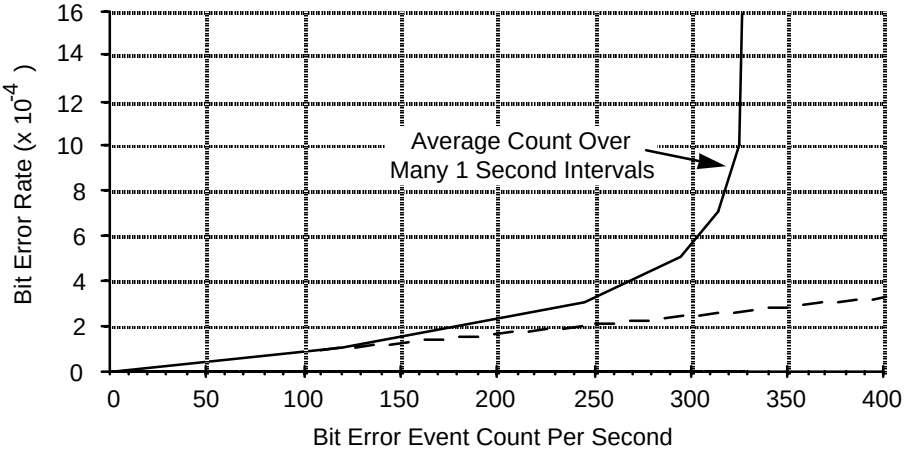



**Figure 49 - BEE Count vs. BER for ESF Framing Format**




Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below $10^{-4}$, there tends to be no more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above $10^{-4}$, each CRC-6 error is often due to more than one bit error. Thus, the relationship between BER and BEE count becomes non-linear above a $10^{-4}$ BER. This must be taken into account when using ESF CRC-6 counts to determine the BER.

**Figure 50 - BEE Count vs. BER for SF Framing Format**

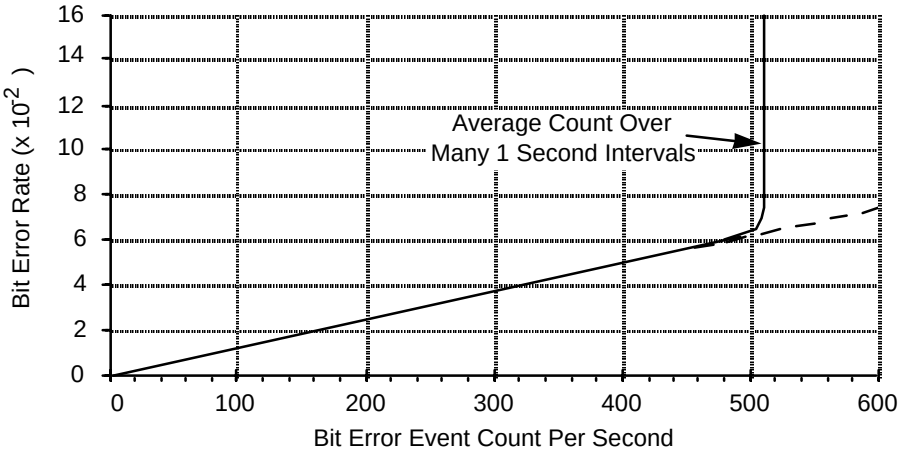



**Figure 51 - BEE Count vs. BER for SLC®96 Framing Format**

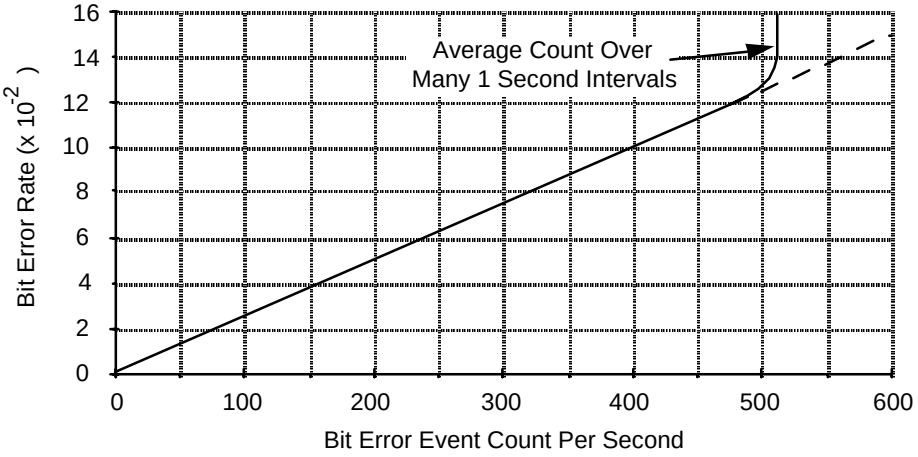
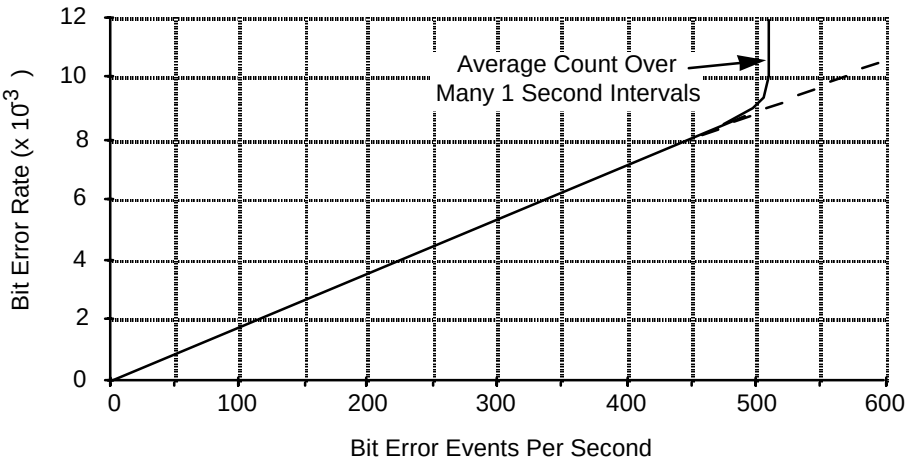
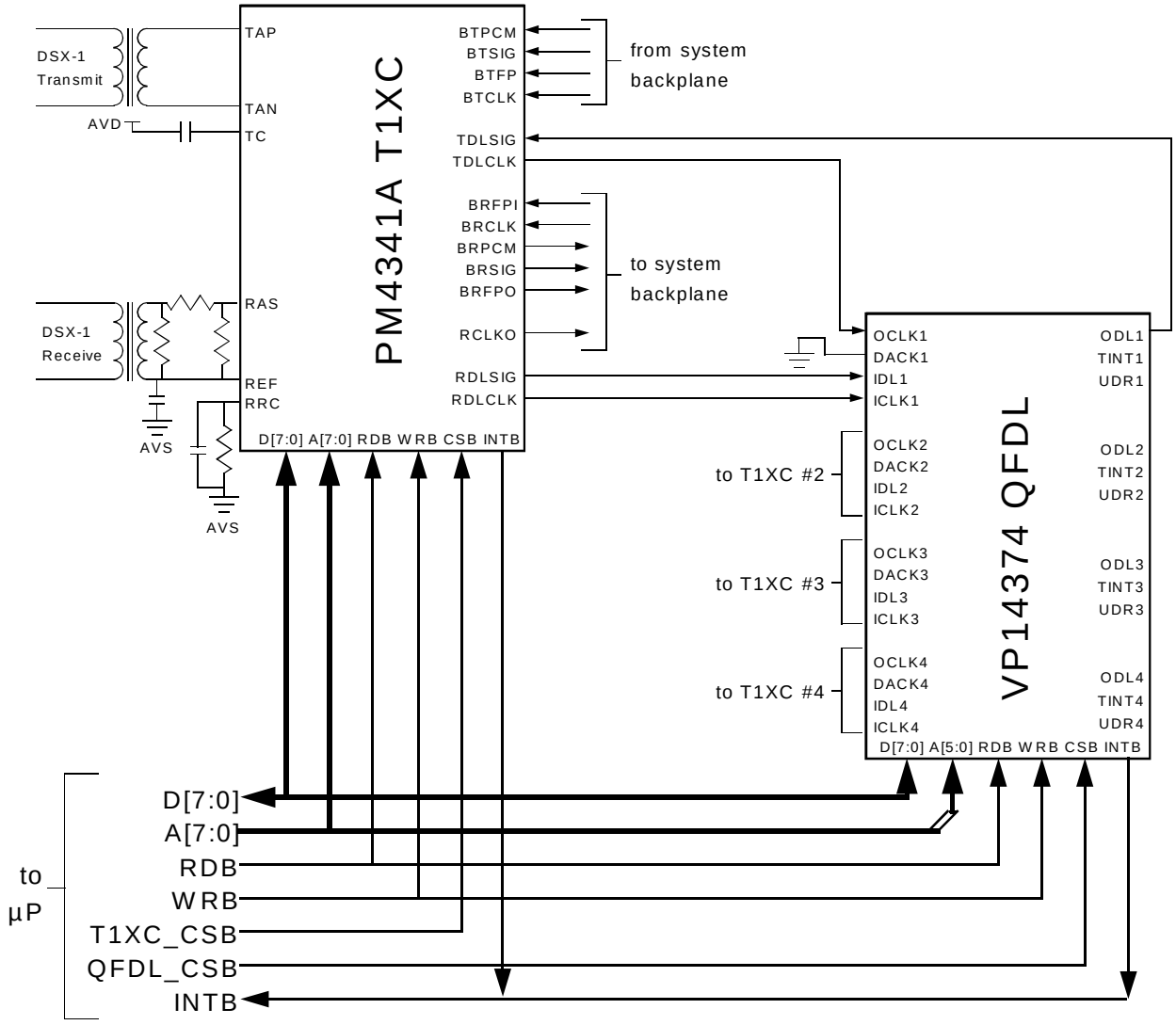


**Figure 52 - BEE Count vs. BER for T1DM Framing Format**



# 14 ADDITIONAL APPLICATIONS

**Figure 53 - Example 4. Terminating ISDN Primary Rate D-Channel with QFDL**




Example 4 is an application utilizing up to four transceivers to terminate four ISDN Primary Rate D-channels through the VLSI Technology VP14374 Quad Facility Datalink transceiver, QFDL. The T1XC chips are programmed to receive and generate the ESF framing format, with the internal HDLC controllers assigned to terminate the ESF 4 kHz datalink. The HDLC data link controllers within VP14374 QFDL are operated identically to those within the T1XC.

To set up the T1XC to process the D-channel, the following registers must be written:

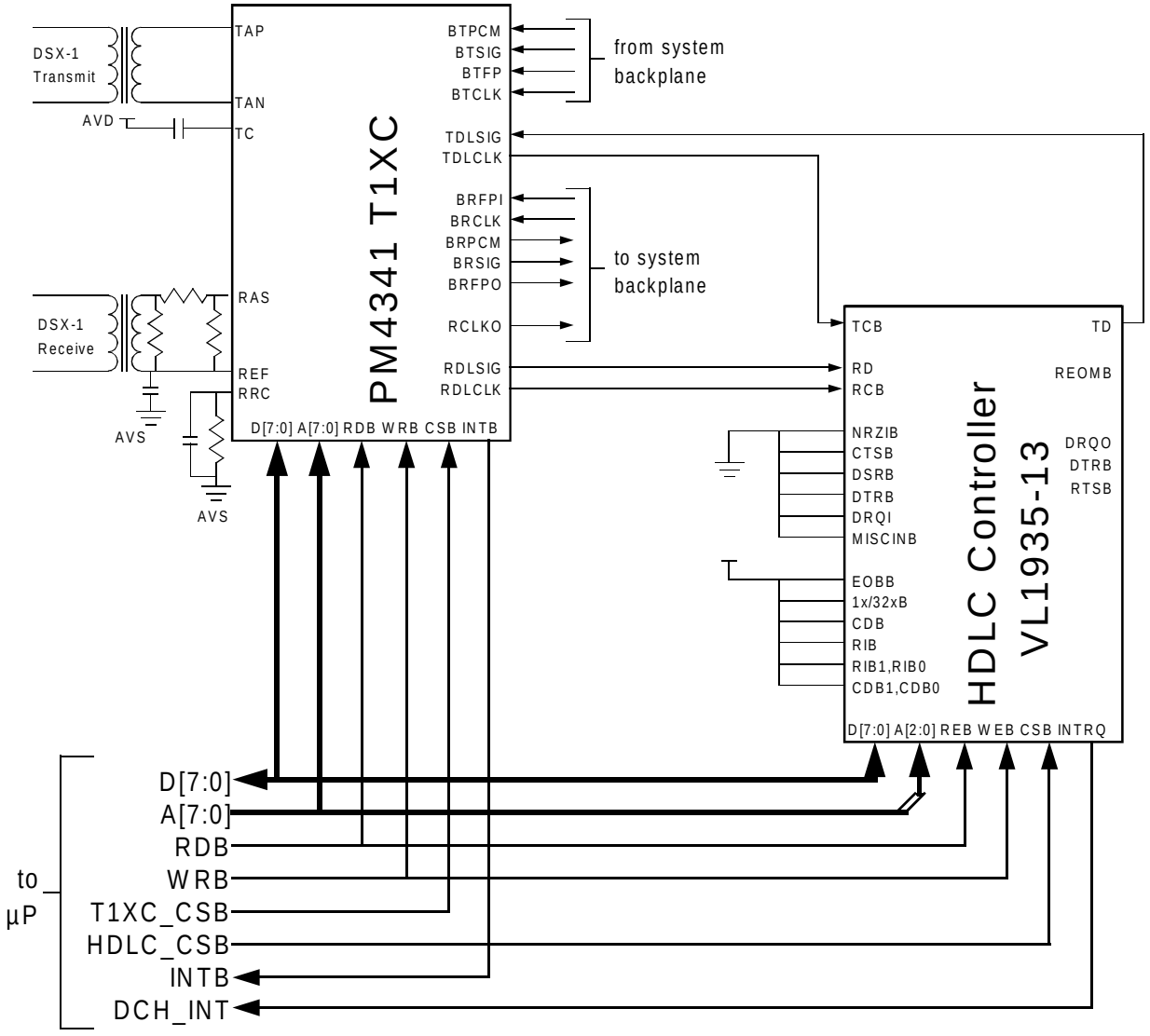
**Table 35 - Setting Up T1XC to Process the D-Channel**

| Action | Addr | Data | Effect |
|---|---|---|---|
| Write CDRC Configuration Register | 10H | 00H | Select B8ZS line code for receiver |
| Write XBAS Configuration Register | 44H | 3XH | Select B8ZS, enable for ESF in transmitter (bits defined by 'X' determine the FDL data rate & Zero Code suppression algorithm used) |
| Write FRMR Configuration Register | 20H | 1XH<br>or<br>5XH<br>or<br>9XH | Select ESF, 2 of 4 OOF threshold<br><br>Select ESF, 2 of 5 OOF threshold<br><br>Select ESF, 2 of 6 OOF threshold<br>(bits defined by 'X' determine the FDL data rate, should be same as those written to XBAS) |
| Write RBOC Enable Register | 2AH | 00H<br>or<br>02H | Enable 8 out of 10 validation<br><br>Enable 4 out of 5 validation |
| Write ALMI Configuration Register | 2CH | 1XH | Select ESF (bits defined by 'X' determine the ESF YELLOW data rate, should be same as those written to FRMR) |
| Write IBCD Configuration Register (optional) | 3CH | 00H | Enable Inband Code detection |
| Write IBCD Activate Code Register (optional) | 3EH | 08H | Program Loopback Activate Code pattern |
| Write IBCD Deactivate Code Register (optional) | 3FH | 44H | Program Loopback Deactivate Code pattern |
| Write SIGX Configuration Register | 40H | 1XH | Select ESF (bits defined by 'X' should be same as those written to FRMR) |
| Write T1XC Datalink Options Register | 02H | 5FH | Enable RFDL & XFDL to process the ESF Facility Datalink. The DMA signals normally available on RDLINT, RDLEOM, TDLINT, TDLUDR outputs are internally configured to generate interrupts on the common INTB interrupt (the interrupt source can be determined by reading registers 8&9). The Primary Rate D-channel is made available on RDLSIG, RDLCLK, TDLSIG, TDLCLK. |

Once this configuration is done, the system will be able to receive and generate ESF formatted data while processing the ESF data link and extracting and

processing the ISDN D-channel. The µP will be required to service interrupt requests from up to five XFDL or RFDL blocks. Note that the more frequent interrupts will be from the QFDL, since it is processing the 64 kbit/s D-channel.

**Figure 54 - Example 5. Terminating ISDN Primary Rate D-Channel with VL1935**




Example 5 is an application utilizing one T1XC transceiver to terminate the ISDN Primary Rate D-channel through the VLSI Technology, Inc. VL1935 Synchronous Data Line Controller. The VL1935 is a single HDLC controller; however, its operation is similar to that of QFDL. The speed of the VL1935 must be able to

support the bursty nature of the transmit clock on TDLCLK, which can have an instantaneous frequency of 2.048 MHz when the transmit backplane is configured for the 2.048 MHz data rate. The VL1935-13 is specified, since its operating clock frequency is 2 MHz.

The T1XC is configured identically as for Example 4.

## 15 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Ambient Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on VDD with Respect to GND | -0.5V to +VDD |
| Voltage on Any Pin | -0.5V to +VDD |
| Static Discharge Voltage | ±500 V |
| Latch-Up Current ($T_A$ = -40°C to +85°C) | ±100 mA |

## 16 CAPACITANCE

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| Cin | Input Capacitance | 10 | pF | $T_A$ = 25°C, f = 1 MHz (sampled only) |
| Cout | Output Capacitance | 10 | pF | $T_A$ = 25°C, f = 1 MHz (sampled only) |
| Cbidir | Bidirectional Capacitance | 10 | pF | $T_A$ = 25°C, f = 1 MHz (sampled only) |

## 17 D.C. CHARACTERISTICS

**TA= -40° to +85°C, VDD=5V ±10%**

**Typical Cond. TA = 25°C , VDD = 5.0 V**

**Table 36 - D.C. Characteristics**

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$,$RA_{VD}$, $TA_{VD}$ | Power Supply | 4.5 | 5.0 | 5.5 | Volts | |
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.8 | Volts | Guaranteed Input LOW Voltage |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{DD}$+ 0.5 | Volts | Guaranteed Input HIGH Voltage |
| $V_{RAS}$ | Analog Input Voltage | $RA_{VS}$ -0.6 | | $RA_{VD}$ +0.6 | Volts | |
| $V_{OL}$ (TTL) | Output or Bidirectional Low Voltage | | 0.1 | 0.4 | Volts | $V_{DD}$ = 5.0 V, $I_{OL}$ = -4 mA for Data Bus Pins and -2 mA for others, Note 3 |
| $V_{OH}$ (TTL) | Output or Bidirectional High Voltage | 2.4 | 4.7 | | Volts | $V_{DD}$ = 5.0 V, $I_{OH}$ = 4 mA for Data Bus Pins and 2 mA for others, Note 3 |
| $V_{T+}$ | Reset Input High Voltage | 3.5 | | | Volts | |
| $V_{T-}$ | Reset Input Low Voltage | | | 1.0 | Volts | |
| $V_{TH}$ | Reset Input Hysteresis Voltage | | 1.0 | | Volts | |
| $I_{ILPU}$ | Input Low Current | +20 | +83 | +200 | µA | $V_{IL}$ = GND, Notes 1, 3 |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{IHPU}$ | Input High Current | -10 | 0 | +10 | µA | $V_{IH} = V_{DD}$, Notes 1, 3 |
| $I_{IL}$ | Input Low Current | -10 | 0 | +10 | µA | $V_{IL}$ = GND, Notes 2, 3 |
| $I_{IH}$ | Input High Current | -10 | 0 | +10 | µA | $V_{IH} = V_{DD}$, Notes 2, 3 |
| IDDOP | Operating Current | | 69 | 90 | mA | VDD = 5.5 V, Outputs Unloaded, XCLK = 37.056 MHz<br>BTCLK = 1.544MHz, Note 4 |

**Notes on D.C. Characteristics:**

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. $I_{DDOP}$ is the sum of all power supply currents when transmitting all ones from XPLS, producing 2.7 Volt pulses across a 50 ohm load. RSLC is active.
5. Typical Values are given as an aid to the system designer. Product is not tested to the typical values given in the data sheet.

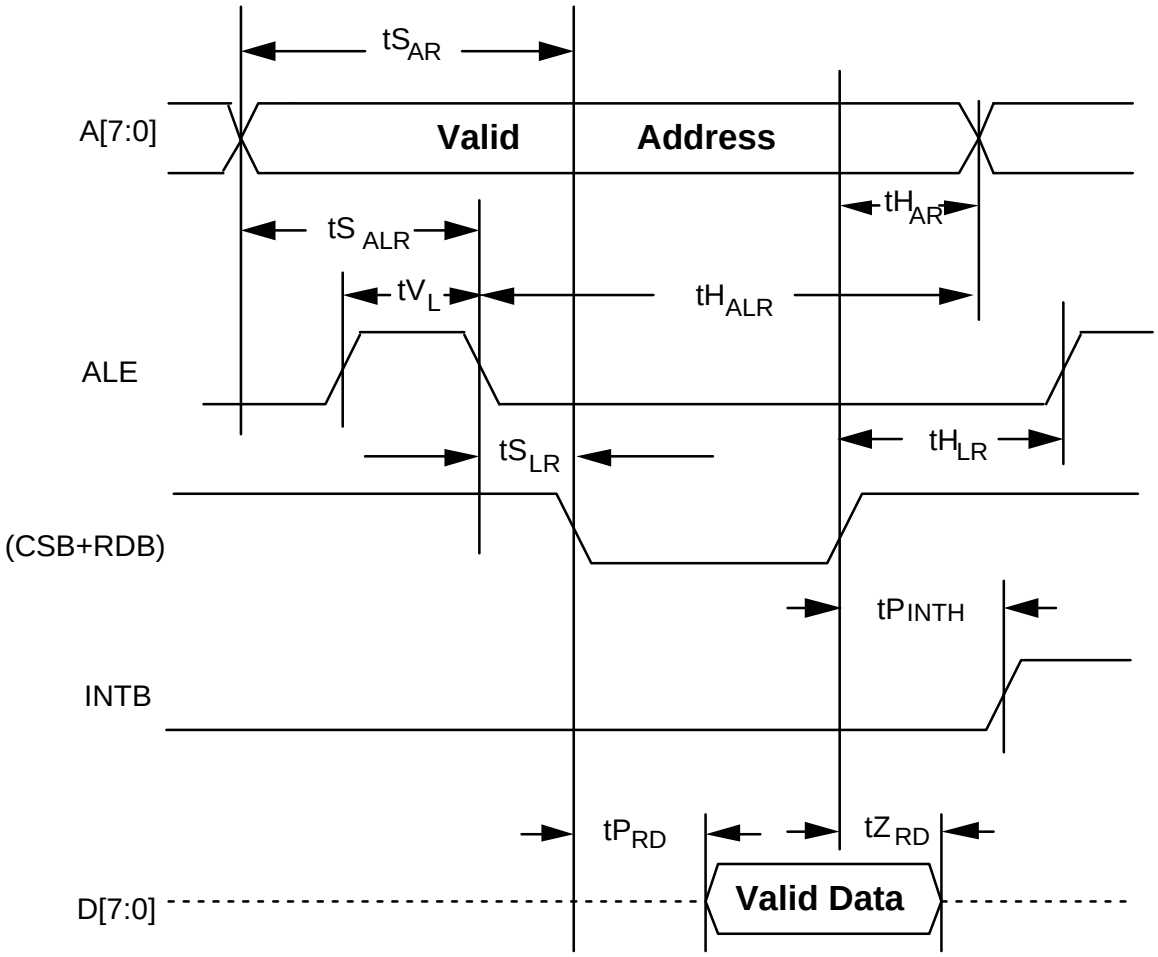
# 18 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

**TA= -40° to +85°C, VDD=5V ±10%**

**Table 37 - Microprocessor Read Access**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $tS_{AR}$ | Address to Valid Read Set-up Time | 10 | | ns |
| $tH_{AR}$ | Address to Valid Read Hold Time | 5 | | ns |
| $tS_{ALR}$ | Address to Latch Set-up Time | 20 | | ns |
| $tH_{ALR}$ | Address to Latch Hold Time | 10 | | ns |
| $tV_{L}$ | Valid Latch Pulse Width | 20 | | ns |
| $tS_{LR}$ | Latch to Read Set-up | 0 | | ns |
| $tH_{LR}$ | Latch to Read Hold | 10 | | ns |
| $tP_{RD}$ | Valid Read to Valid Data Propagation Delay | | 80 | ns |
| $tZ_{RD}$ | Valid Read Deasserted to Output Tri-state | | 20 | ns |
| $tP_{INTH}$ | Valid Read Deasserted to INTB High | | 50 | ns |

**Figure 55 - Microprocessor Read Access Timing**




**Notes on Microprocessor Read Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

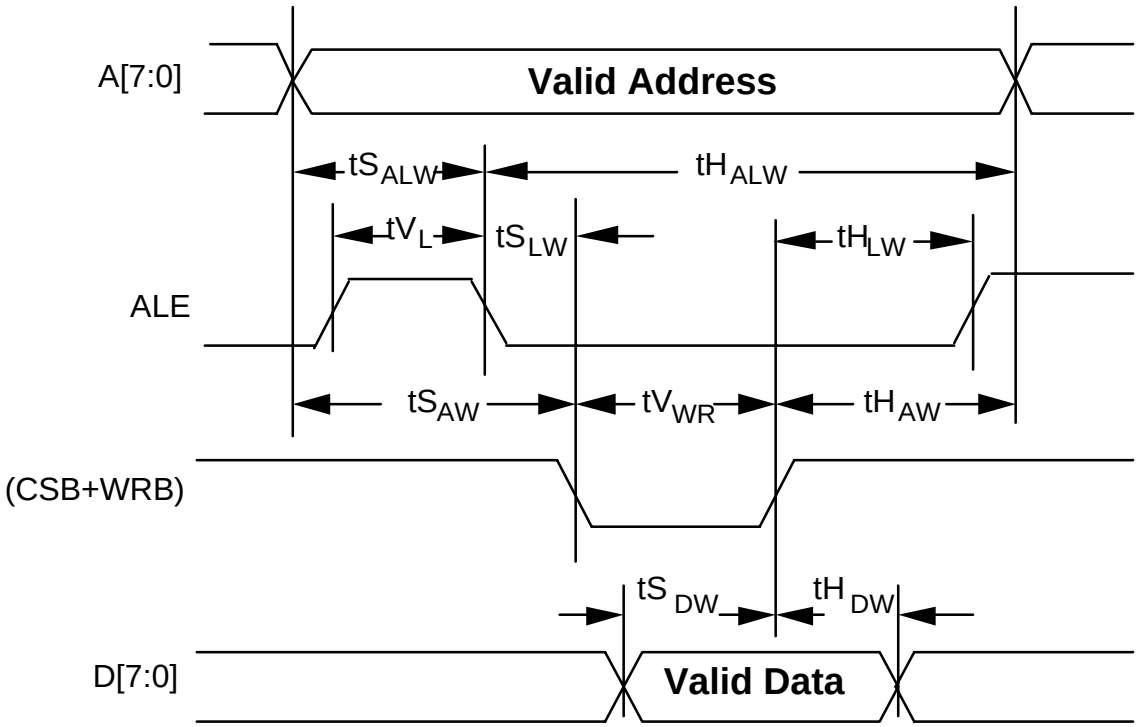
7. In non-multiplexed address/data bus architectures ALE should be held high; parameters $tS_{ALR}$, $tH_{ALR}$, $tV_L$, $tS_{LR}$, and $tH_{LR}$ are not applicable.

8. Parameter $tH_{AR}$ is not applicable when address latching is used.

**Table 38 - Microprocessor Write Access**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $tS_{AW}$ | Address to Valid Write Set-up Time | 10 | | ns |
| $tS_{DW}$ | Data to Valid Write Set-up Time | 10 | | ns |
| $tS_{ALW}$ | Address to Latch Set-up Time | 15 | | ns |
| $tH_{ALW}$ | Address to Latch Hold Time | 15 | | ns |
| $tV_L$ | Valid Latch Pulse Width | 20 | | ns |
| $tS_{LW}$ | Latch to Write Set-up | 0 | | ns |
| $tH_{LW}$ | Latch to Write Hold | 10 | | ns |
| $tH_{DW}$ | Data to Valid Write Hold Time | 10 | | ns |
| $tH_{AW}$ | Address to Valid Write Hold Time | 10 | | ns |
| $tV_{WR}$ | Valid Write Pulse Width | 40 | | ns |

**Figure 56 - Microprocessor Write Access Timing**




**Notes on Microprocessor Interface Write Timing:**

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters $tS_{ALW}$, $tH_{ALW}$, $tV_L$, $tS_{LW}$, and $tH_{LW}$ are not applicable.
4. Parameter $tH_{AW}$ is not applicable if address latching is used.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

## 19 T1XC I/O CHARACTERISTICS

**TA= -40° to +85°C, VDD=5V ±10%**

**Table 39 - Backplane Transmit Input Timing (Figure 57)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | Backplane Transmit Clock Frequency | 1.5 | 2.1 | MHz |
| | Backplane Transmit Clock Duty Cycle | 30 | 70 | % |
| $tS_{TCLK}$ | BTCLK to Backplane Input Set-up Time | 20 | | ns |
| $tH_{TCLK}$ | BTCLK to Backplane Input Hold Time | 20 | | ns |

**Figure 57 - Backplane Transmit Input Timing Diagram**

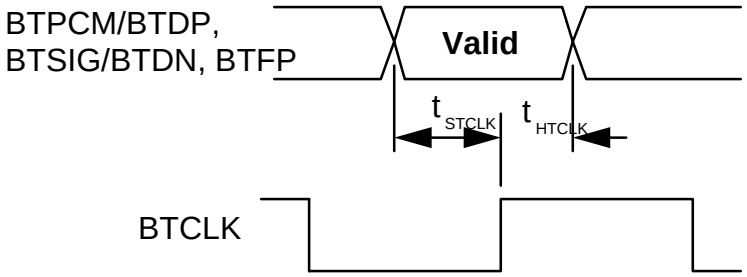
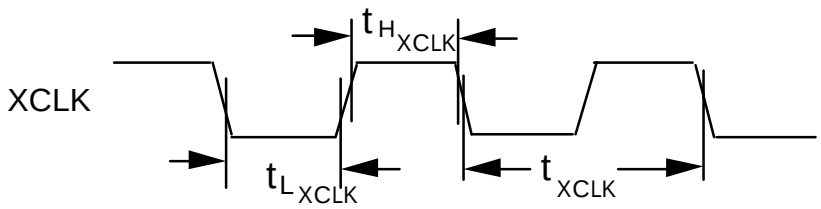


**Table 40 - XCLK=37.056MHz Input (Figure 58)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{LXCLK}$ | XCLK Low Pulse Width (note 1) | 10 | | ns |
| $t_{HXCLK}$ | XCLK High Pulse Width (note 1) | 10 | | ns |
| $t_{XCLK}$ | XCLK Period (typically 1/37.056 MHz or 27 ns) | 20 | | ns |
| | XCLK Duty Cycle (note 2) | 40 | 60 | % |

**Figure 58 - XCLK=37.056MHz Input Timing**




**Notes on XCLK=37.056MHz Timing:**

1. Input Clock high pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the rise and fall ramps.

3. Duty cycle is measured at the 50% points of the rise and fall ramps.

**Table 41 - TCLKI Input (Figure 59)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | TCLKI Frequency (when used for DJAT REF or for mux operation), typically 1.544MHz | | 3.11 | MHz |
| | TCLKI Frequency (when DJAT PLL not used), typically 12.352MHz | | 12.8 | MHz |
| $t_{HTCLKI}$ | TCLKI High Duration (TCLKI=1.544MHz) | 160 | | ns |
| $t_{LTCLKI}$ | TCLKI Low Duration (TCLKI=1.544MHz) | 160 | | ns |

**Figure 59 - TCLKI Input Timing**

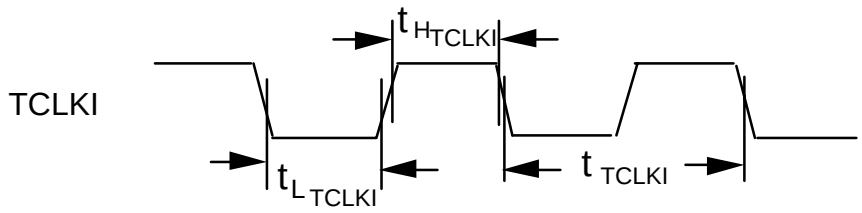
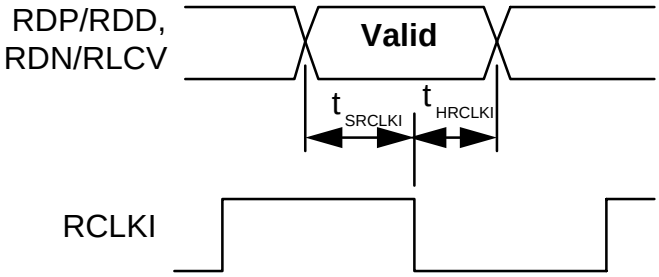


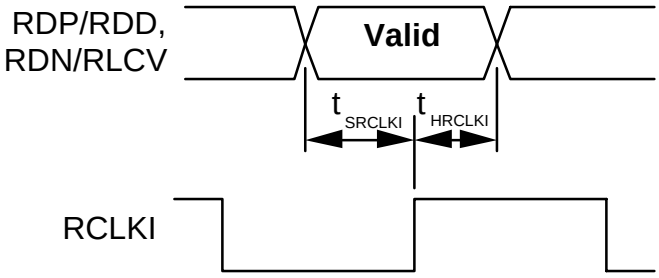

**Table 42 - Digital Receive Interface Input Timing (Figure 60)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | Digital Receive Clock Frequency (nom. 1.544) | | 1.6 | MHz |
| $tHI_{RCLKI}$ | Digital Receive Clock High Duration | 250 | | ns |
| $tLO_{RCLKI}$ | Digital Receive Clock Low Duration | 250 | | ns |
| $tS_{RCLKI}$ | RCLKI to NRZ Digital Receive Input Set-up Time | 20 | | ns |
| $tH_{RCLKI}$ | RCLKI to NRZ Digital Receive Input Hold Time | 20 | | ns |
| $tW_{RDPN}$ | RZ Digital Receive Input Pulse Width | 250 | 400 | ns |

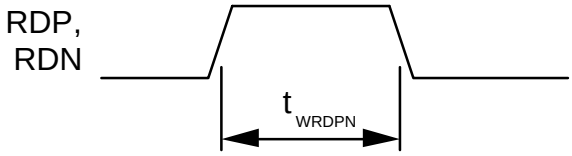
**Figure 60 - Digital Receive Interface Input Timing Diagram**




**With RFALL bit =1, RRZ=0**




**With RFALL bit =0, RRZ=0**




**With RRZ=1**

**Table 43 - Transmit Data Link Input Timing (Figure 61)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $tS_{DIN}$ | TDLCLK to TDLSIG Input Set-up Time | 80 | | ns |
| $tH_{DIN}$ | TDLCLK to TDLSIG Input Hold Time | 20 | | ns |

**Figure 61 - Transmit Data Link Input Timing Diagram**

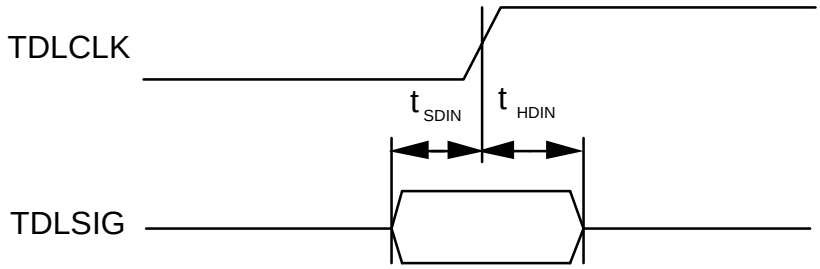
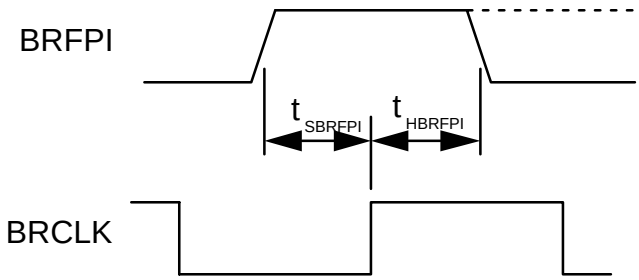



**Table 44 - Backplane Receive Input Timing (Figure 62)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $tS_{BRFPI}$ | BRCLK to BRFPI Input Set-up Time | 20 | | ns |
| $tH_{BRFPI}$ | BRCLK to BRFPI Input Hold Time | 20 | 1 frame -680ns | ns |

**Figure 62 - Backplane Receive Input Timing Diagram**



**Notes on Input Timing:**

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

**Table 45 - Receive Data Link Output Timing (Figure 63)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{PRDLCLK}$ | RDLCLK to RDLSIG Propagation Delay | | 50 | ns |

**Figure 63 - Receive Data Link Output Timing Diagram**

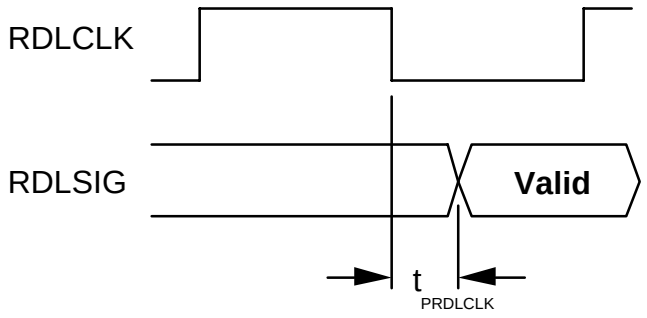


**Table 46 - Backplane Receive Output Timing (Figure 64)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{PBRCLK}$ | BRCLK to Backplane Output Signals Propagation Delay | | 50 | ns |

**Figure 64 - Backplane Receive Output Timing Diagram**

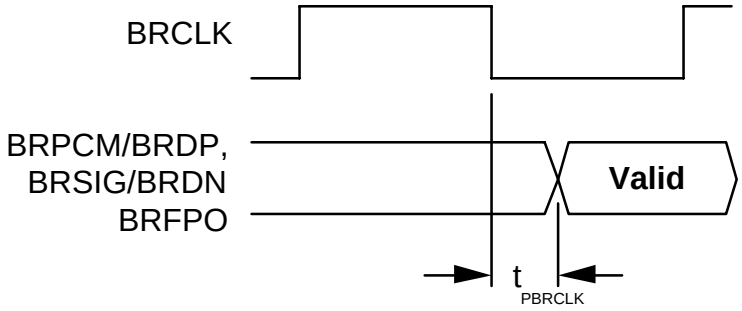



**Table 47 - Recovered Data Output Timing (Figure 65)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{PRCLKO}$ | RCLKO to Recovered Line Data Output Signals Propagation Delay | | 50 | ns |

**Figure 65 - Recovered Data Output Timing Diagram**

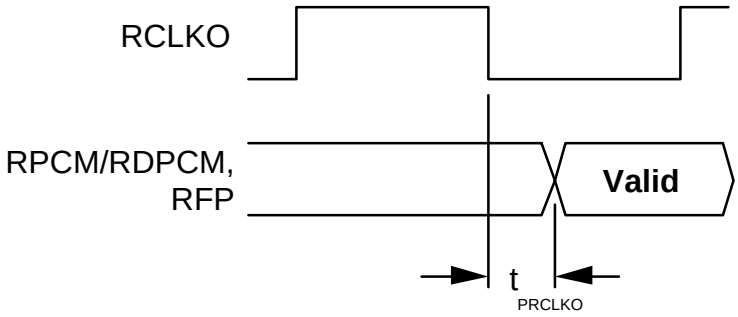
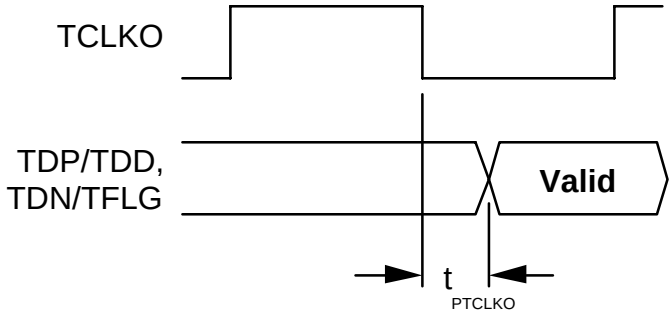


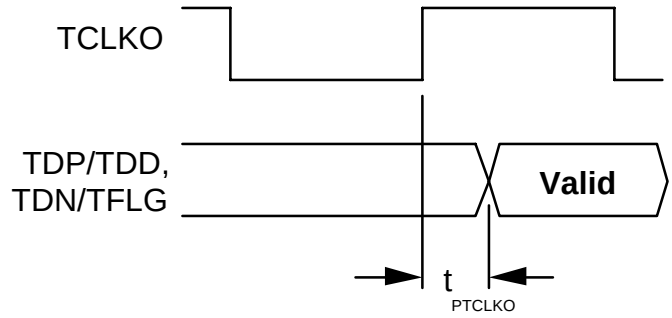
**Table 48 - Transmit Interface Output Timing (Figure 66)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{PTCLKO}$ | TCLKO to Digital Transmit Data Output Signals Propagation Delay | | 50 | ns |

**Figure 66 - Transmit Interface Output Timing Diagram**




**With TRISE bit=0**




**With TRISE bit= 1**

**Table 49 - Transmit Data Link DMA Interface Output Timing (Figure 67)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{P2INT}$ | Transmit Data Register Serviced (WRB low) to TDLINT Low Propagation Delay | | 50 | ns |
| $t_{P2UDR}$ | UDR bit written low (WRB high) to TDLUDR Low Propagation Delay | | 50 | ns |

**Figure 67 - Transmit Data Link DMA Interface Output Timing Diagram**

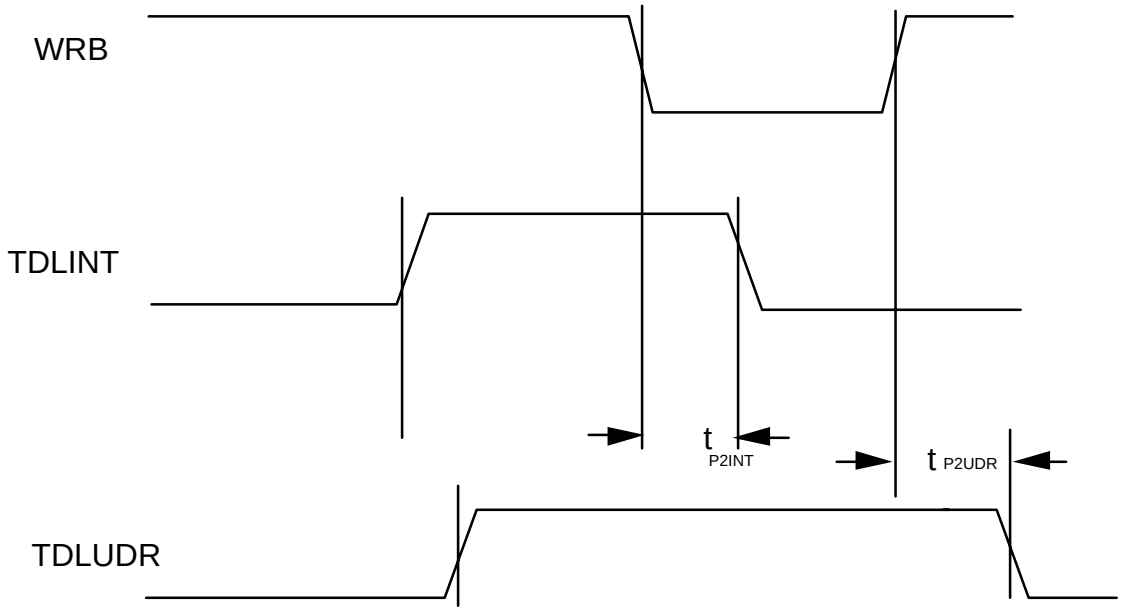
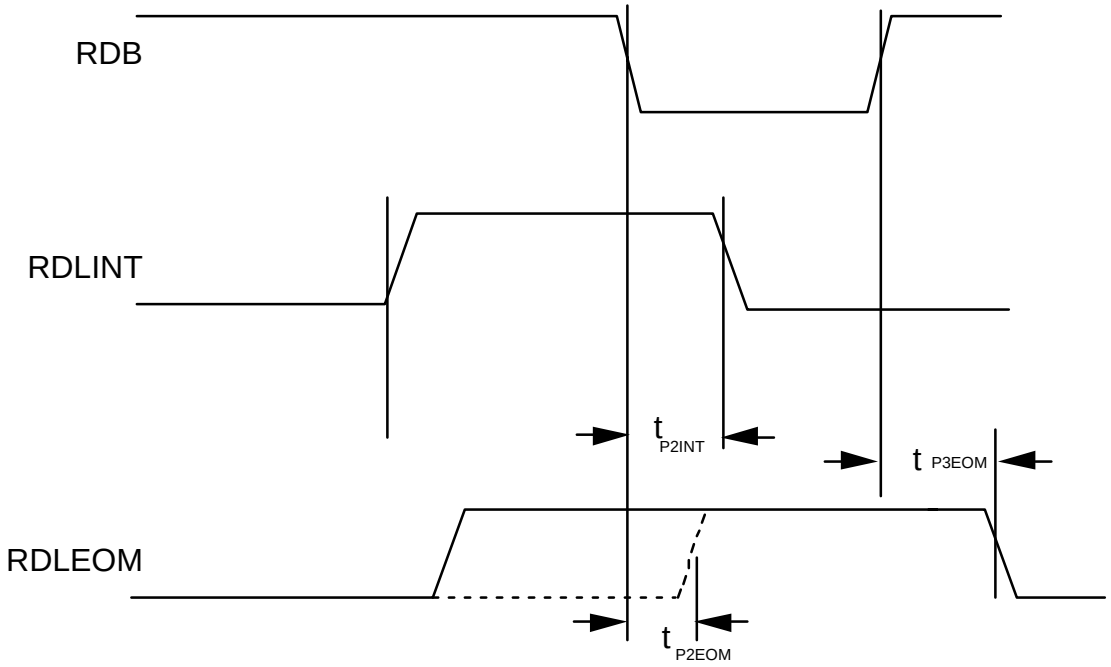


**Table 50 - Receive Data Link DMA Interface Output Timing (Figure 68)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{P2INT}$ | Receive Data Register Serviced (RDB low) to RDLINT Low Propagation Delay | | 70 | ns |
| $t_{P2EOM}$ | Receive Data Register Serviced (RDB low) to RDLEOM High Propagation Delay | | 80 | ns |
| $t_{P3EOM}$ | Receive Status Register Serviced (RDB high) to RDLEOM Low Propagation Delay | | 50 | ns |

**Figure 68 - Receive Data Link DMA Interface Output Timing Diagram**




**Notes on Output Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Output propagation delays are measured with a 50 pF load on the outputs.

# 20 ANALOG CHARACTERISTICS

**TA= -40° to +85°C, VDD=5V ±10%**

**Receive Analog Specifications**

**Table 51 - T1 Slicing Threshold Voltage**

| Symbol | Parameter | Min | Max | Typ. | Units |
|---|---|---|---|---|---|
| | T1 Slicing Threshold Voltage | 62 | 72 | 67 | % of Peak |

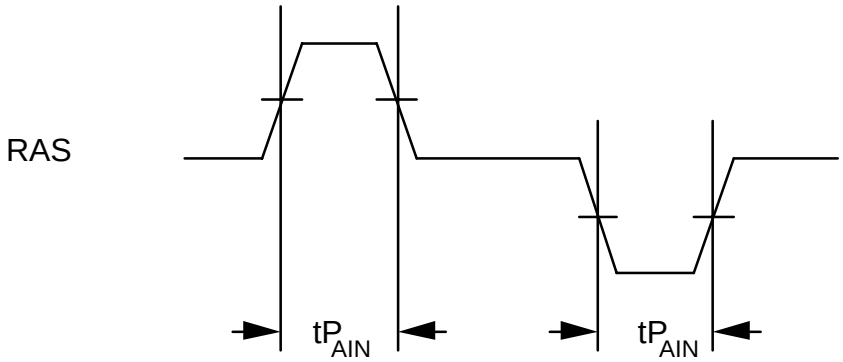
**Notes on Analog Specifications:**

Typical Values are given as an aid to the system designer. Products are not tested to the typical values given in the data sheet.

**Table 52 - Analog Receive Data Input Timing (Figure 69)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $tP_{AIN}$ | Receive Analog Data Signal Pulse Width | 250 | 400 | ns |

**Figure 69 - Analog Receive Data Input Timing Diagram**



## Transmit Analog Specifications

**Typical Cond. TA = 25°C , VDD = 5.0 V**

**Table 53 - TAP/TAN Output Resistance**

| Symbol | Parameter | Min | Typ. | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Ron | TAP/TAN pulse driver output resistance | | 2.6 | | Ω | |

# 21 ORDERING AND THERMAL INFORMATION

**Table 54 - Packaging Options**

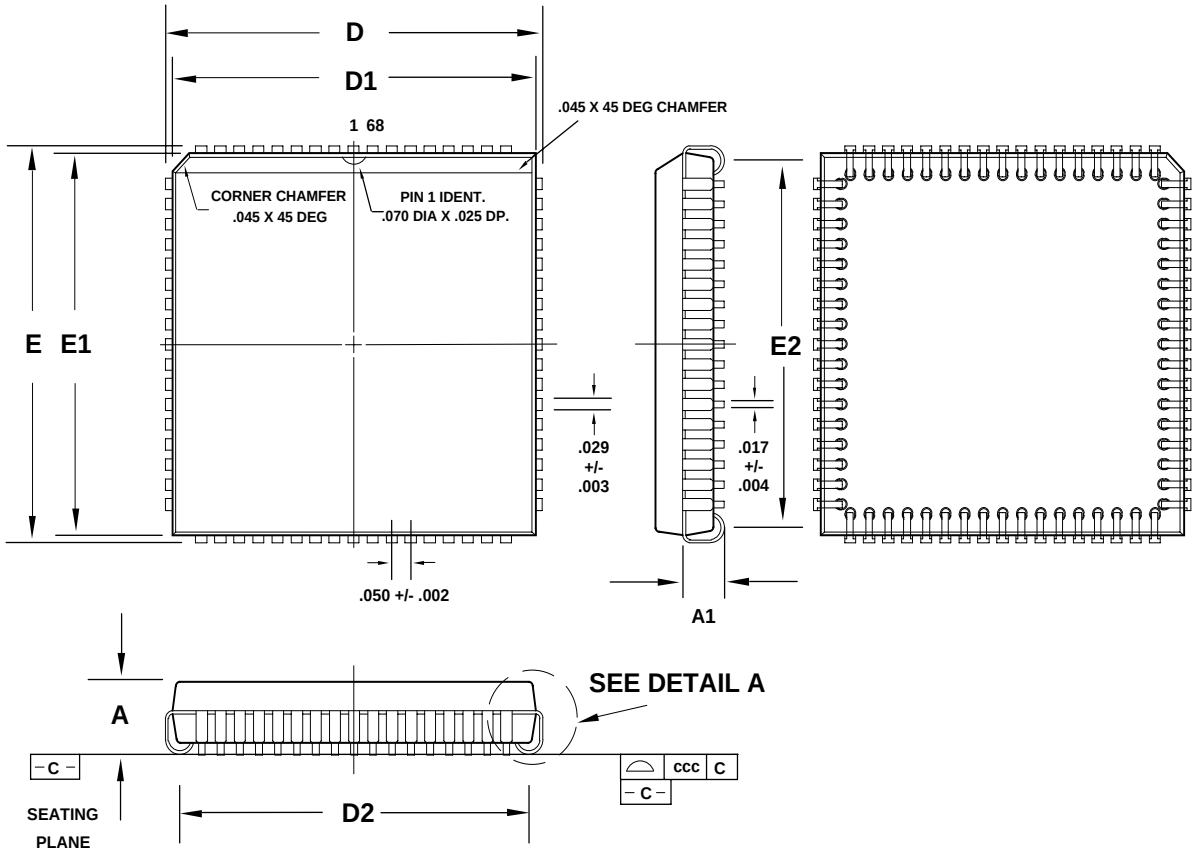
| PART NO. | DESCRIPTION |
|---|---|
| PM4341A-QI | 68 Plastic Leaded Chip Carrier (PLCC) |
| PM4341A-RI | 80 Plastic Quad Flat Pack (PQFP) |

**Table 55 - Thermal Properties**

| PART NO. | AMBIENT TEMPERATURE | Theta Ja | Theta Jc |
|---|---|---|---|
| PM4341A-QI | -40°C to 85°C | 42 °C/W | 12 °C/W |
| PM4341A-RI | -40°C to 85°C | 61 °C/W | 14 °C/W |

# 22 MECHANICAL INFORMATION

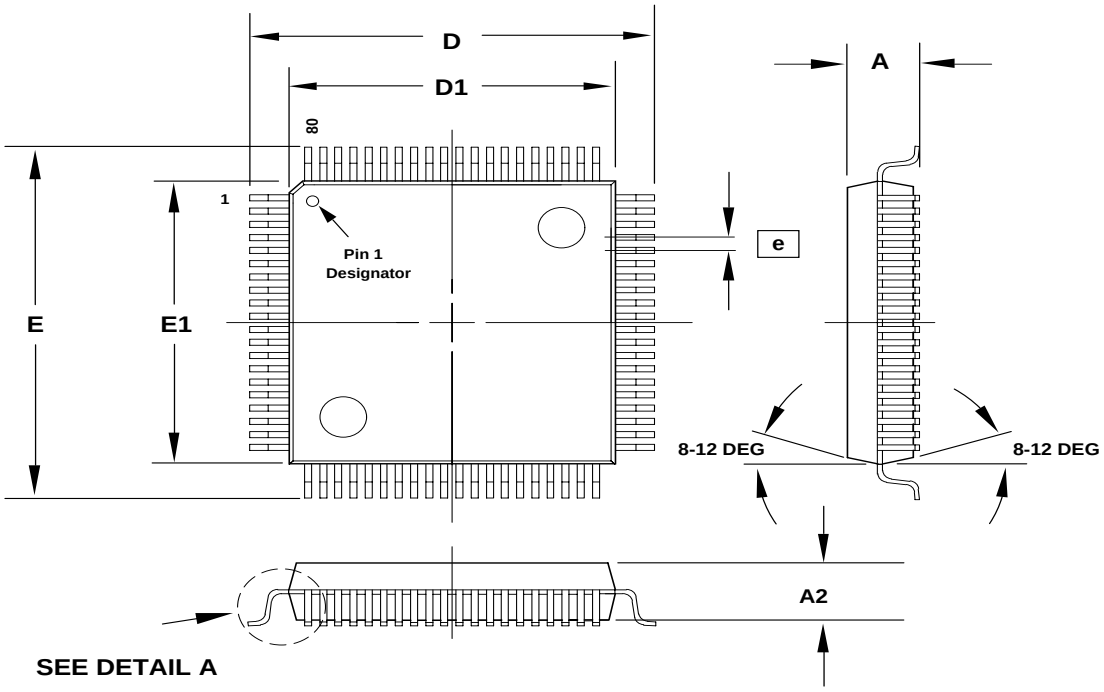
## Figure 70 - 68 Pin Plastic Leaded Chip Carrier (Q Suffix)

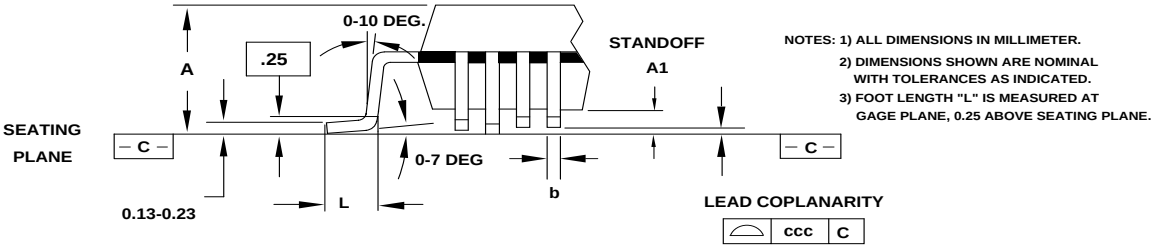



NOTES : 1. ALL DIMENSIONS IN INCHES

| PACKAGE TYPE: 68 PIN PLASTIC LEADED CHIP CARRIER-PLCC | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Dim. | A | A1 | D | D1 | D2 | E | E1 | E2 | ccc |
| Min. | 0.165 | 0.090 | 0.985 | 0.950 | 0.890 | 0.985 | 0.950 | 0.890 | |
| Nom. | 0.175 | | 0.990 | 0.954 | 0.920 | 0.990 | 0.954 | 0.920 | |
| Max. | 0.200 | 0.130 | 0.995 | 0.958 | 0.930 | 0.995 | 0.958 | 0.930 | 0.004 |

## Figure 71 - 80 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix)




NOTES:
1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.
3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE SEATING PLANE.

| PACKAGE TYPE: 80 PIN METRIC PLASTIC QUAD FLATPACK-MQFP | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BODY SIZE: 14 x 14 x 2.0 MM | | | | | | | | | | | |
| Dim. | A | A1 | A2 | D | D1 | E | E1 | L | e | b | ccc |
| Min. | 2.00 | 0.05 | 1.95 | 16.95 | 13.90 | 16.95 | 13.90 | 0.73 | | 0.22 | |
| Nom. | 2.15 | 0.15 | 2.00 | 17.20 | 14.00 | 17.20 | 14.00 | 0.88 | 0.65 | | |
| Max. | 2.35 | 0.25 | 2.10 | 17.45 | 14.10 | 17.45 | 14.10 | 1.03 | | 0.38 | 0.10 |

## NOTES

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PMC-900602 (R7) ref PMC-891007 (R11) Issue date: June 1998