PowerPC 403 to PCI 9060ES Application Note

PCI 9060/403 AN

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Version 0.4

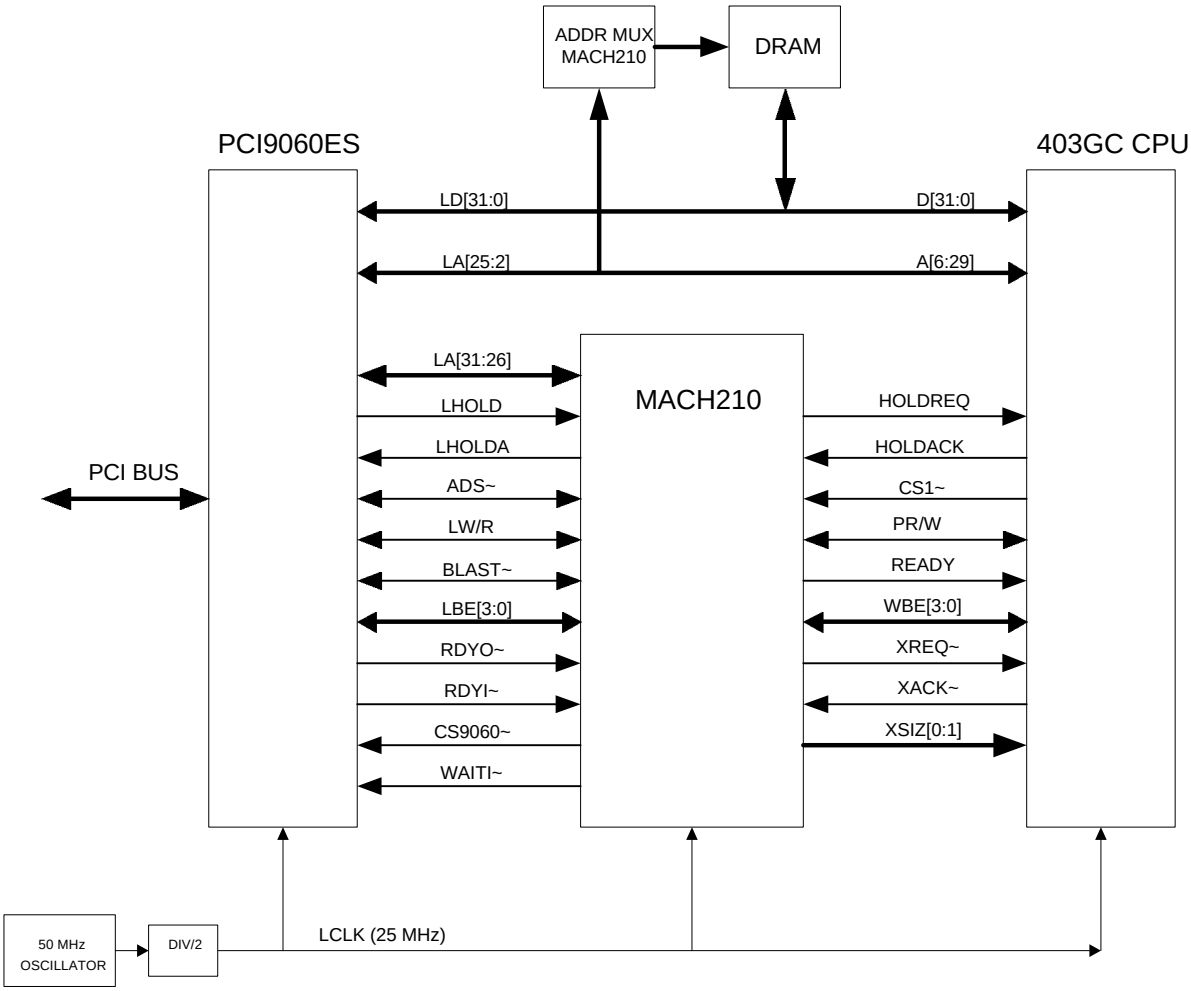
PowerPC 403 to PCIbus Application Note

Features

- Embedded system containing PowerPC 403 with a PCIbus interface
- PCI 9060ES chip supports master, slave and PCI configuration cycles
- 403local bus runs asynchronously to the PCI clock.
- FIFOs in PCI 9060ES support continuous burst transfers between 403 local bus and PCIbus

General Description

This application note describes how to interface the PowerPC 403GC CPU to the PCI bus using the PLX PCI9060ES PCI to Local Bus Bridge chip. The PCI9060ES has both direct master and direct slave transfer capabilities. The direct master mode allows a device (403GC) on the local bus to perform memory, I/O and configuration cycles to the PCI bus. The direct slave mode allows a master device on the PCI bus to access memory (DRAM) on the local bus. **The 403GA may also be used with little or no modification to the design.**



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APPENDIX: SCHEMATICS AND PAL EQUATIONS FOR 16 WORD BURST IMPLEMENTATION

1. Introduction

This application note describes how to interface the PowerPC 403GC CPU to the PCI bus using the PLX PCI9060ES Local Bus Bridge chip. **The 403GA may be used in place of the GC with little or no modification to the design.** (Contact PLX for more information). The PCI9060ES has both direct master and direct slave transfer capabilities. The direct master mode allows a device (403GC) on the local bus to perform memory, I/O and configuration cycles to the PCI bus. The direct slave mode allows a master device on the PCI bus to access memory (DRAM) on the local bus. The PCI9060ES allows the local bus to operate asynchronously to the PCI bus through the use of bi-directional FIFOs. In this application the PCI bus operates at 33 MHz while the local bus is clocked at 25 MHz. The following block diagram shows the basic connections between the major components required for this application.

IMPORTANT NOTE ABOUT REVISION 0.3: The design in Revision 0.3 (this revision) of this application note allows 16 word bursting. In Revision 0.1 the design allowed only four word bursting. To achieve this improvement, the design was changed from using two Mach 210's (Rev 0.1 design) to one Mach 210 and three 16V8's. The PAL equations and schematics included with this application note reflect the changes. However, the text and timing diagrams still reflect the 0.1 (4 word burst) operation. Although the differences are minor, this is noted to avoid confusion. PLX is now updating the text and timing diagrams to reflect the change from four word burst to 16 word burst.

Note that the address and data buses on the 403GC designate bit 0 as the **most** significant bit. Also, the 403GC does not produce the upper 6 address bits, so its maximum addressing range for one bank is 64 Mbytes.

NOTE: PLX provides a "Technical Update", available from the FTP site on the Web page that contains design notes, spec updates and errata on the PLX chips. All designers should obtain this information when performing a design. The web page is atwww.plxtech.com. Contact PLX by e-mail, phone or fax for the FTP passwords.