Schematics and Board Layout Recommendation for PI7C7100

by Glenn Sanders

This application note describes how to properly connect miscellaneous standard PCI and unique control signals to and from Pericom's PI7C7100 3-port PCI-PCI bridge. Listed are all non-standard signals and how to connect them. Also listed are some recommendations for layout as exemplified by our reference board design.

Miscellaneous Signal Connections

Verify that the miscellaneous signals listed below are con nected to the proper value explained in the table following table:

Pin name	Location	Requested Value
P_FLUSH#	W5	pull static high for P_FLUSH#
P_M66EN	V18	depending speed [pull low/pull high]
S_M66EN	D7	pull low
BYPASS	Y4	pull HIGH
PLL_TM	Y3	pull LOW
S_CLKIN	V5	pull low; this signal should not be used.
SCAN_TM#	V4	pull high PI7C7100 with option to pull low
SCAN_EN	U5	tie low
CMP01	U6	filter as sheet 5 our schematics
Reserved	R4	float (no connect)
S1_EN	W3	pull high
S2_EN	W4	pull high
JTAG pins		internally pulled within our bridge chip
for each bus:		
LOCK#		pull up
PERR#		pull up
SERR#		pull up
STOP#		pull up
FRAME#		pull up
TRDY#		pull up
IRDY#		pull up
DEVSEL#		pull up
for each slot:		
REQ#		pull high to Vdd through external resistor
ACK64#		pull up
REQ64#		pull up
SDONE	(A40)	pull up
SBO#	(A41)	pull up

Where **"Pull"** rather than "**tie**" is used, use a 5.1-kohm resistor to corresponding the high/low.

Power Decoupling –For Pericom's bridge, 4 sets of decoupling capacitors, top and bottom, are required positioned as close as possible to each corner of the bridge BGA.

– Bottom: 0.1µF, 0.01µF, 0.001µF

– Top: 10µF, 0.1µF, 0.01µF, 0.001µF

These are in addition to further decoupling at the PCI primary interface and secondary slots, as needed, per PCI spec 2.2 section 4.4.2.1 "***Power Decoupling***."

For add-in cards, add these decoupling capacitors at the edge connector:

– **3.3V and 5V pins**: 0.1µF, 0.01µF, and 0.001µF

– **AVDD and AGND**: 10µF, 0.1µF, 0.01µF, and 0.001µF

(make a little island within your V_{CC} plane to AVDD)

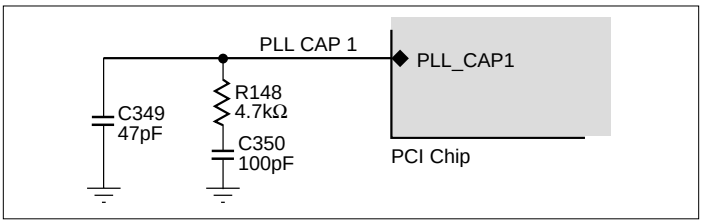
(make a little island within your GND plane to AGND)

Six Layer Board Stacking Recommendation

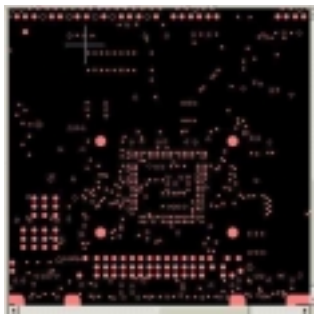
Signal layers should be separated by ground planes and should not be routed between ground and power planes. For board fabrication FR-4 material is preferred. Pericom's reference board is arranged as follows:

Top	For routing clock & other critical signals
Internal Plane 1	Ground
Internal Plane 2	3.3 V
Internal Plane 3	5 V with Analog 3.3 V_{CC} in island under bridge
Internal Plane 4	Ground
Bottom	Signal connections

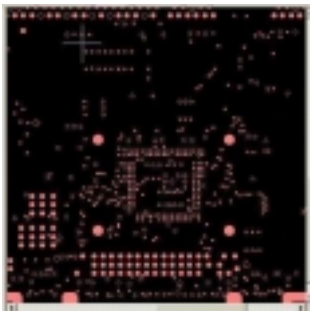
Do **NOT** route high-frequency bus signals under the bridge. Reference schematic is available at the end of Pericom's PI7C7100 data book. Gerber and schematics in electronic format available upon request.



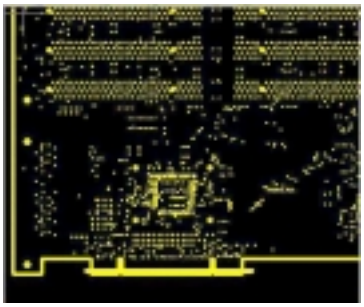
Detail of RC Circuit for CMP01 Analog Out



Internal Ground Plane 1
Notice that this plane is mostly solid under the BGA.



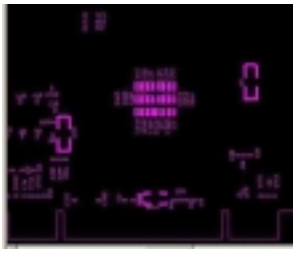
3.3V (Digital) Internal Plane *2*
Between edge connector and BGA are headers that sample the primary bus signals



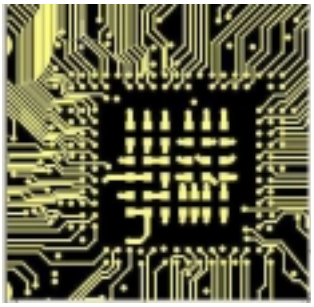
Internal Ground Plane 4
Zoom Out

5V Internal Plane 3
With 3.3V AV_{CC} island

Top Layer Detail on BGA Pads
Notice vias from inner surface mount pads. Large filled region is tied to ground

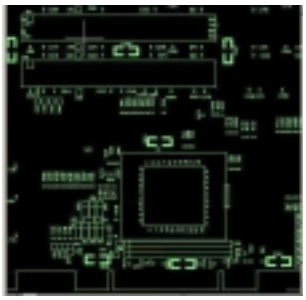


Silkscreen Detail of Bottom
View of Decoupling capacitor placement. Note that capacitors are close to edge connector.



Bottom Layer Under BGA (detail)
Notice decoupling capacitor pads are as close as possible to filter power into the bridge chip.

Top in Red, Bottom in Yellow (detail).
Some traces appear merged at this magnitization. As traces become closer, crosstalk and signal integrity become more important



Top Silkscreen (detail)
Note capacitors at incoming power (edge connector), near each PCI slot, and the PI7C100 chip.

General Layout Guidelines

1. Limit trace lengths. Longer traces display more resistance and induction and introduce more delays. They also limit bandwidth which varies inversely with the square of trace length.
2. Use higher impedence traces. Raising impedence will also increase bandwidth. Use a 65-ohm impedence with ±10% tolerance.
3. Do not use any clock signal loops.When possible, keep clock lines straight.
4. For related clock signals that have skew specifications, match clock trace lengths.
5. Do not route signals in the ground and V_{CC} planes.
6. Do not route signals close to edge of PCB board.
7. Make sure there is a solid ground plane beneath the PI7C7100.
8. The power plane should face the return ground plane. Signals should not be routed between power and ground.
9. Route clock signals on the top layer and avoid vias for these signals. Vias change impedence and introduce more skew and reflections.
10. Do not use any connectors on clock traces.
11. Use wide traces for power and ground.
12. Keep high-speed noise sources away from the PI7C7100.
13. Per PCI spec 2.2 section 4.4.3.1, the PI7C7100 should have a primary PCI edge connector to the BGA pad . The trace distance should not be more than 1.5 inches (37.5 mm) for signals coming from the primary PCI interface. Secondary interface signals would then be limited per PCI motherboard layout rules.

References

1. Pericom Semiconductor Application Note 22 "*Solutions to Current High-Speed Board Design*"
2. PCI Local Bus specification 2.2 section 4.4 "*Expansion Board Specification*" (*decoupling* through *routing recommendations* and *impedence* sections) p150-152.
3. PCI Local Bus specification 2.2 section 4.2.6 *Pinout recommendation* p131.
4. PCI Local Bus specification 2.2 section 4.3.3 *Pull-ups* p136.
5. Compact PCI PICMG 2.0 R3.0 p17-20 "*Electrical Requirements*"