

PowerMOS transistor FREDFET

PHW9ND50

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor incorporating a Fast Recovery Epitaxial Diode (FRED). This gives improved switching performance in half-bridge and full-bridge configurations making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

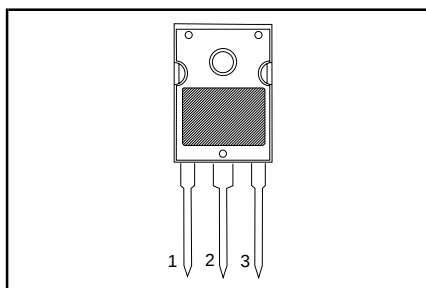
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	8.8	A
P_{tot}	Total power dissipation	147	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.8	Ω
t_{rr}	Source-drain diode reverse recovery time	180 (typ)	ns

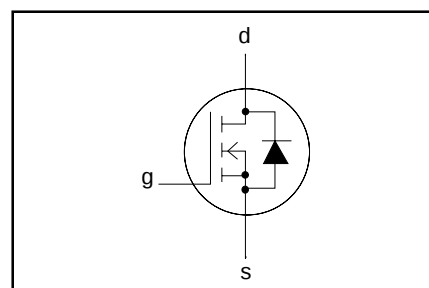
PINNING - SOT429 (TO247)

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}; V_{GS} = 10\text{ V}$	-	8.7	A
		$T_{mb} = 100^\circ\text{C}; V_{GS} = 10\text{ V}$	-	5.5	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	35	A
P_D	Total dissipation	$T_{mb} = 25^\circ\text{C}$	-	147	W
$\Delta P_D / \Delta T_{mb}$	Linear derating factor	$T_{mb} > 25^\circ\text{C}$	-	1.176	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50\text{ V}; \text{starting } T_j = 25^\circ\text{C}; R_{GS} = 50\ \Omega;$ $V_{GS} = 10\text{ V}$	-	510	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50\text{ V}; \text{starting } T_j = 25^\circ\text{C}; R_{GS} = 50\ \Omega;$ $V_{GS} = 10\text{ V}$	-	8	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	0.85	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	60	-	K/W

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ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	500	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	-	0.6	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	$V_{GS} = 10\text{ V}; I_D = 4.8\text{ A}$	-	0.67	0.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	$V_{DS} = 30\text{ V}; I_D = 4.8\text{ A}$	3.5	6.0	-	S
I_{DSS}	Drain-source leakage current	$V_{DS} = 500\text{ V}; V_{GS} = 0\text{ V}$	-	1	25	μA
		$V_{DS} = 400\text{ V}; V_{GS} = 0\text{ V}; T_j = 125^\circ\text{C}$	-	40	250	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 8\text{ A}; V_{DD} = 400\text{ V}; V_{GS} = 10\text{ V}$	-	88	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	47	60	nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}; I_D = 8\text{ A};$ $R_G = 9.1\text{ }\Omega; R_D = 31\text{ }\Omega$	-	18	-	ns
t_r	Turn-on rise time		-	50	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Turn-off fall time		-	60	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1060	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Feedback capacitance		-	90	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	$T_{mb} = 25^\circ\text{C}$	-	-	8.8	A
I_{SM}	Pulsed source current (body diode)	$T_{mb} = 25^\circ\text{C}$	-	-	35	A
V_{SD}	Diode forward voltage	$I_S = 8\text{ A}; V_{GS} = 0\text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_S = 8\text{ A}; V_{GS} = 0\text{ V}; di/dt = 100\text{ A}/\mu\text{s}$ $I_F = 8\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $T_j = 125^\circ\text{C}$	-	180	-	ns
			-	220	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 100\text{ V}$ $V_{GS} = 0\text{ V}; V_R = 100\text{ V}; T_j = 125^\circ\text{C}$	-	0.65	-	μC
I_{rrm}	Source-drain diode peak reverse recovery current	$I_F = 8\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_R = 100\text{ V}; T_j = 125^\circ\text{C}$	-	2.6	-	μC
			-	15	-	A

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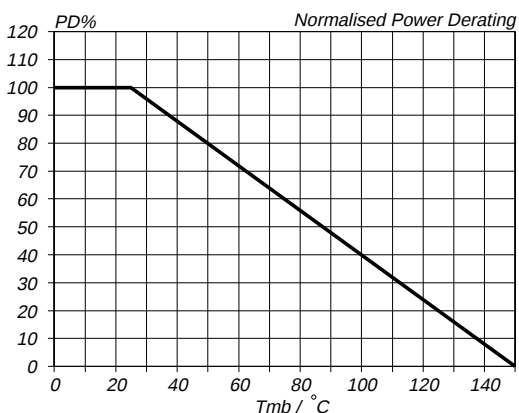


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25^\circ\text{C}} = f(T_{mb})$

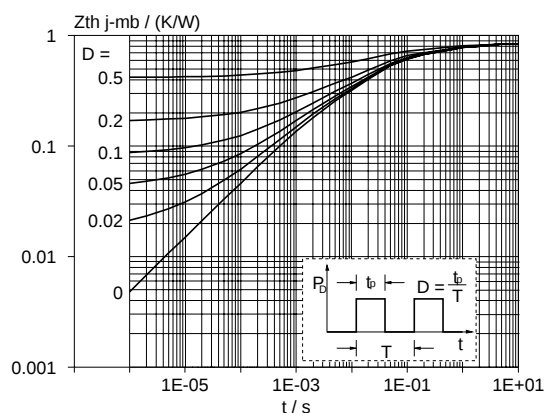


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p / T$

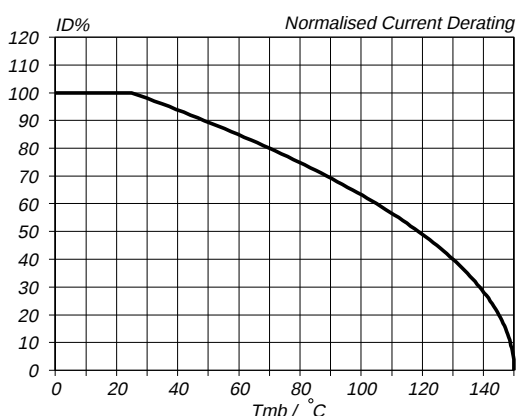


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25^\circ\text{C}} = f(T_{mb})$; conditions: $V_{GS} \geq 10\text{ V}$

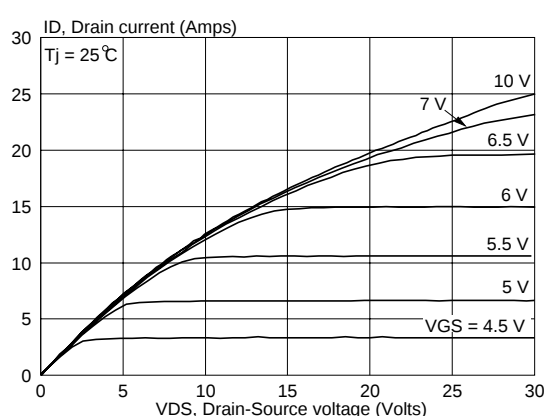


Fig.5. Typical output characteristics.
 $I_D = f(V_{DS})$; parameter V_{GS}

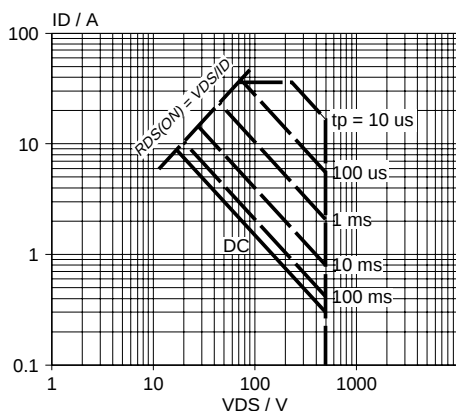


Fig.3. Safe operating area. $T_{mb} = 25^\circ\text{C}$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

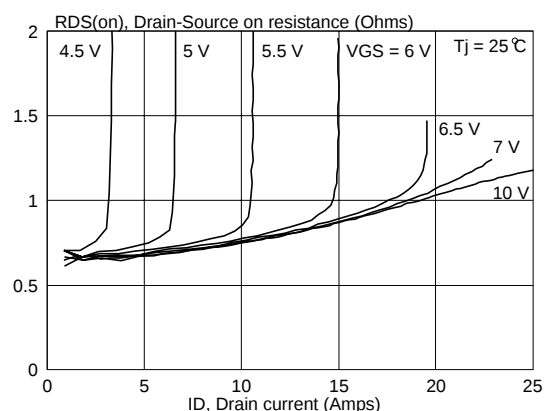


Fig.6. Typical on-state resistance.
 $R_{DS(on)} = f(I_D)$; parameter V_{GS}

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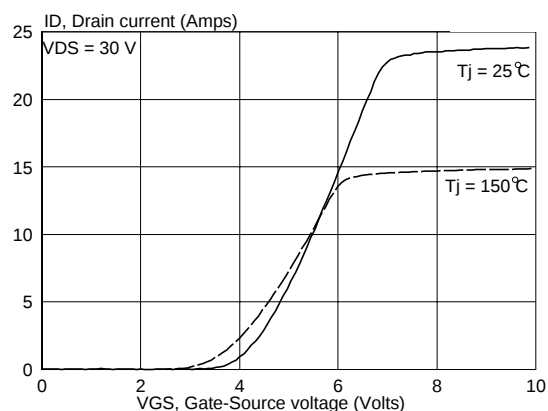


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; parameter T_J

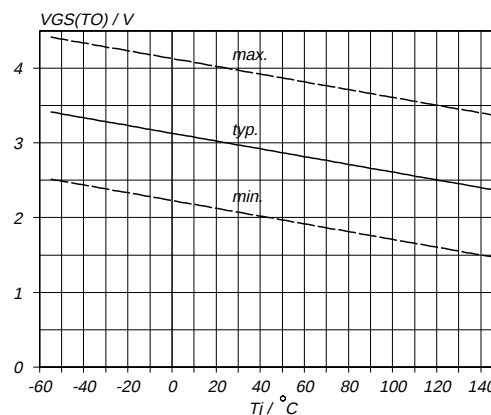


Fig. 10. Gate threshold voltage.
 $V_{GS(T0)} = f(T_J)$; conditions: $I_D = 0.25 \text{ mA}$; $V_{DS} = V_{GS}$

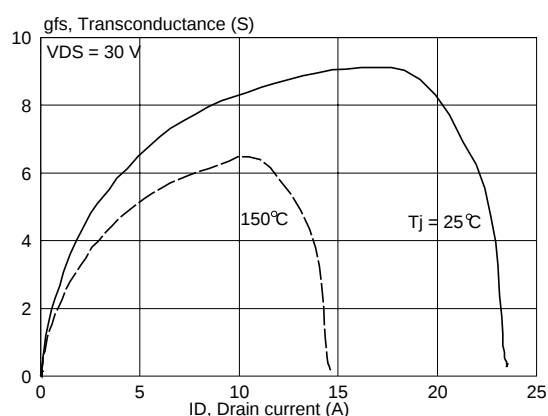


Fig. 8. Typical transconductance.
 $g_{fs} = f(I_D)$; parameter T_J

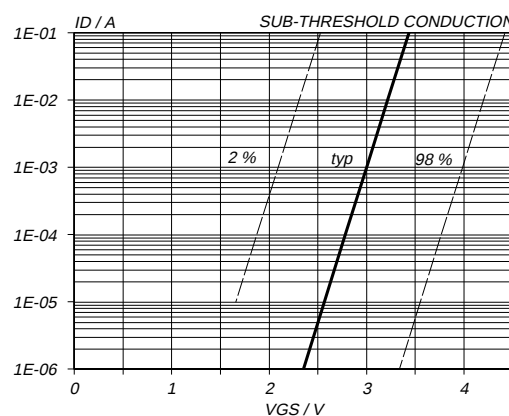


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_J = 25^\circ \text{C}$; $V_{DS} = V_{GS}$

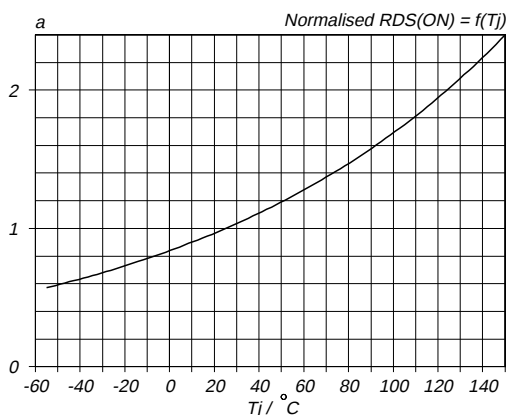


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ \text{C}} = f(T_J)$; $I_D = 4.8 \text{ A}$; $V_{GS} = 10 \text{ V}$

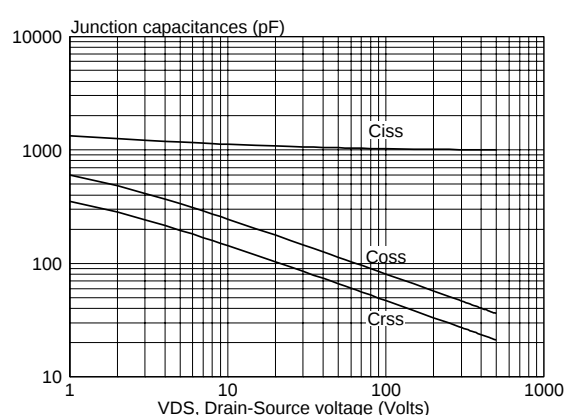
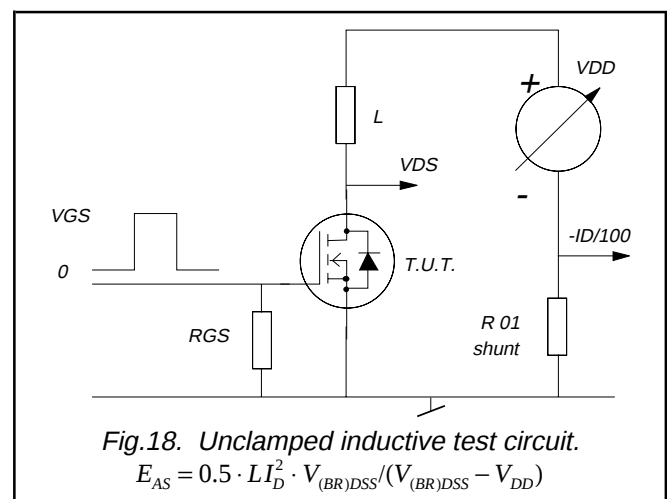
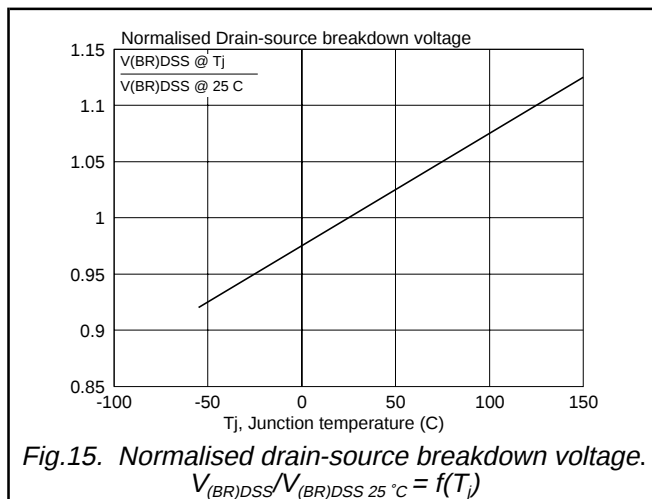
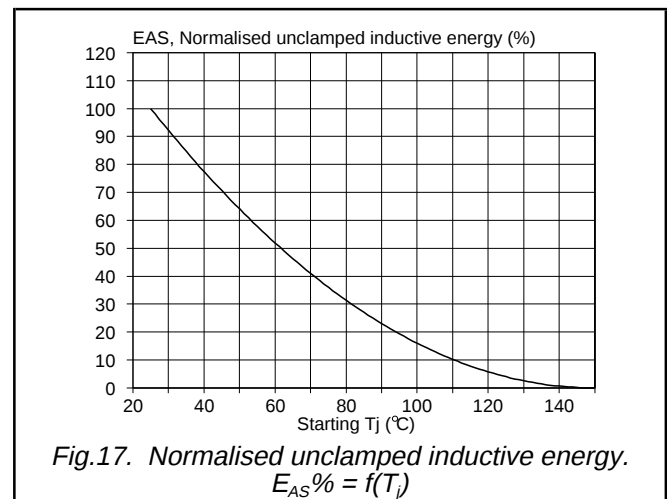
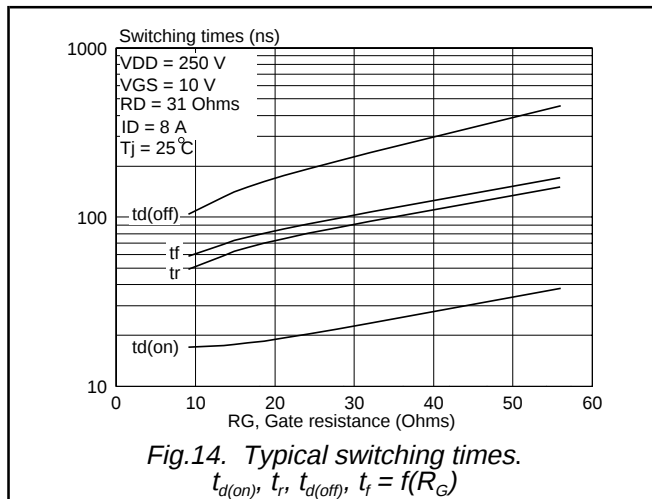
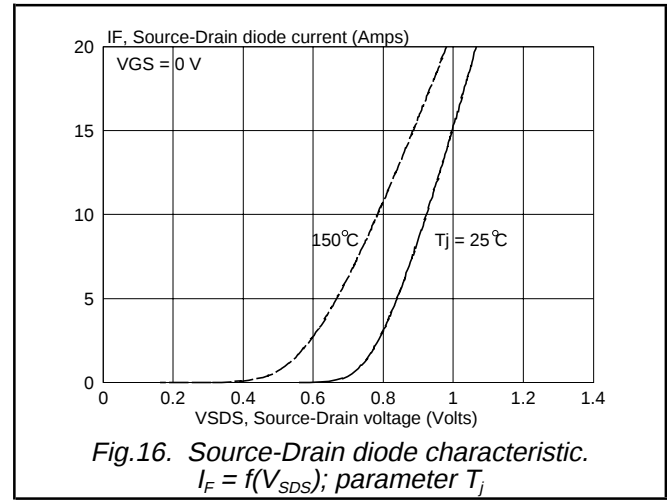
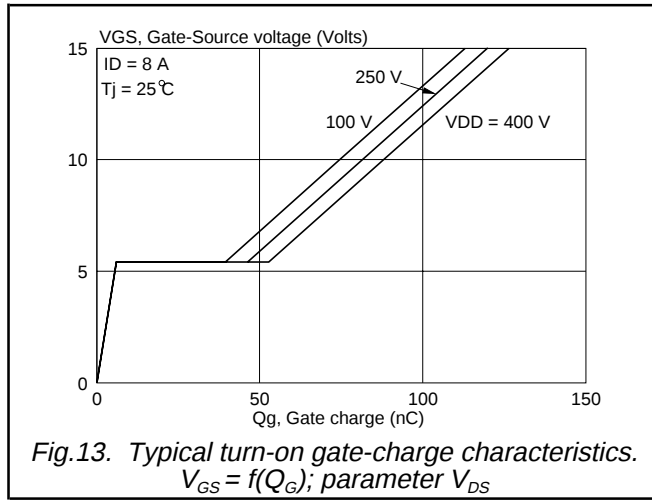


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

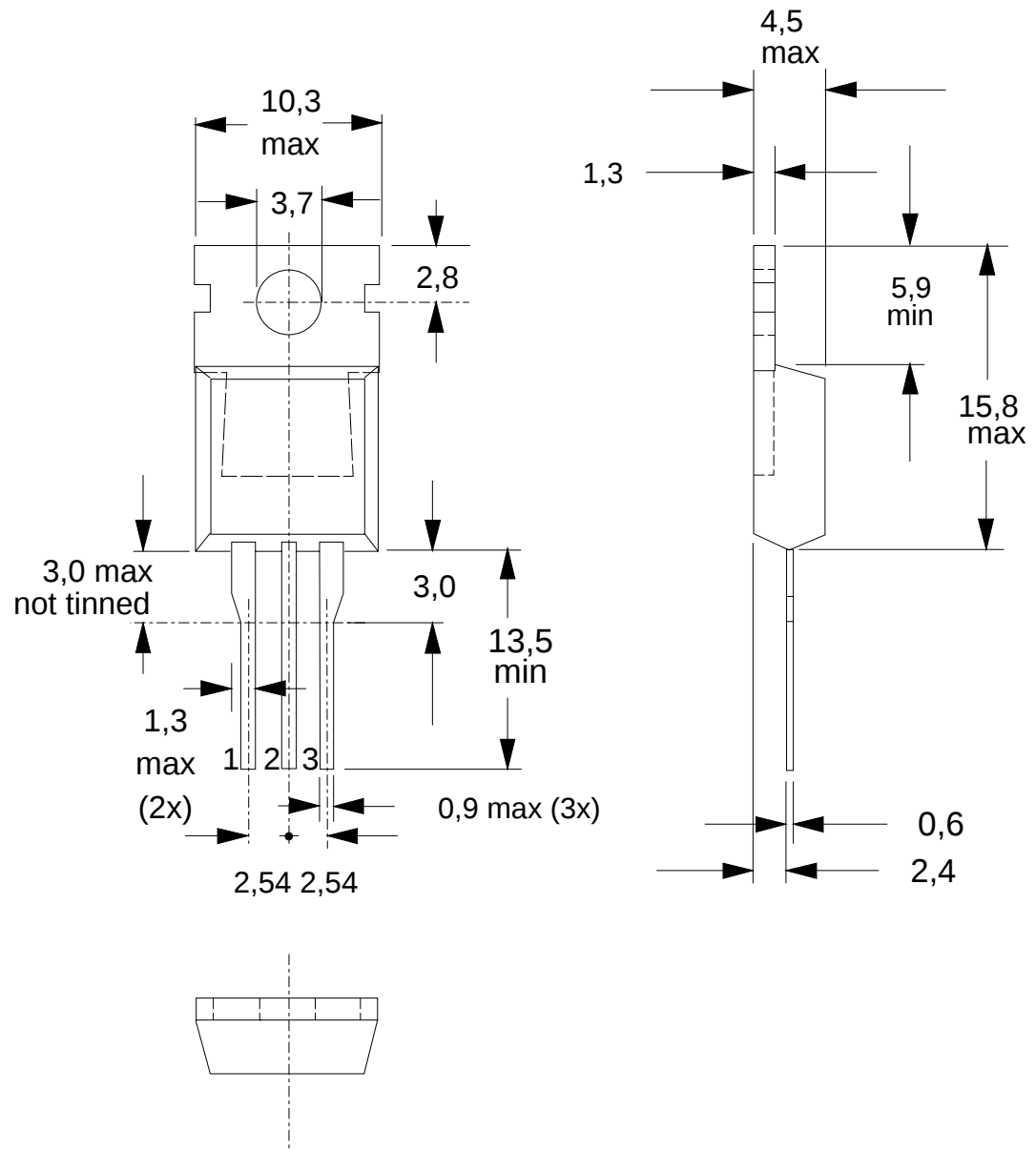


Fig.19. TO220AB; pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for TO220 envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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