Quad ISDN Echocancellation Digital Front End
Quad IEC DFE-T

PEB/PEF 24901 Version 1.2

Quad ISDN Echocancellation Circuit Analogue Front End
Quad IEC AFE

PEB/PEF 24902 Version 2.1

Master Clock Generation on a DFE-T and AFE Line Card

Application Hint 06.99

To enable error-free data transport within the Quad IEC DFE-T, the clocks DCL and FSC from the IOM®-2-interface must be synchronous to the 15,36 MHz signal. Therefore it is recommended to use the same signal for FSC and as input to CLOCK pin at the Quad IEC AFE when the internal PLL is used to generate the 15.36 MHz clock.

If an other clock source is used for CLOCK, e.g. the 2048 kHz DCL, a common time base must be guaranteed. This is usually achieved if FSC is derived from DCL by dividing it directly by 256.

Any constant phase difference between the time bases of both clocks is possible, but the devices have currently been qualified and released only for using the same FSC signal for the Quad IEC DFE-T and for Quad IEC AFE.

Revision History: Previous Version:
Major Changes: