Preliminary

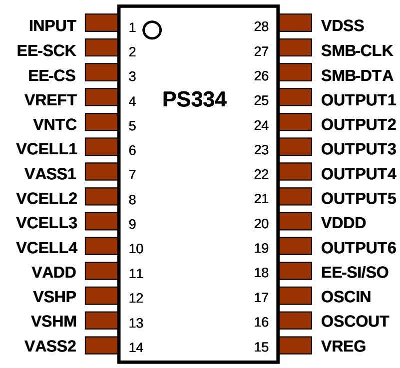
PS334

Li Ion Smart Battery Manager

Features

- Performs all major Li Ion battery management functions including
  - Accurate capacity monitoring
  - Direct control of external charge circuitry (e.g. PWM)
  - Direct control of secondary safety functions
- Six independently programmable output pins can be assigned as SOC LED outputs, direct charge control, or additional levels of safety control
- Fully compliant with industry standard Smart Battery Data Specification V1.1a
  - SMBus V1.1 with PEC / CRC-8 communication with system host
- High accuracy measurement of charge / discharge current, voltage, and temperature with on-chip 14-bit integrating A/D
- Precise capacity reporting for all lithium-based chemistries using PowerSmart patented algorithms and 3D battery cell models
- 3D models and “learned” parameters stored in external EEPROM; fully field re-programmable via SMBus interface
- Supports cell configurations of 1-4 cells in series
- Extremely low power operation:
  - Sleep Mode: < 10 uA typical
  - Run Mode: < 500 uA typical
  - Sample Mode: < 250 uA typical
- PS345X modules available for quick prototyping or production
- Complete hardware and software development tools available

Pin Description



0.209 mil SSOP
28-PIN Package

Pin Summary

Pin Name	Function
Input	LED Switch Input
EE-SCK, EE-CS, EE-SI/SO	SPI Serial EEPROM Interface
VREFT	Reference Voltage Output
VNTC	Temperature A/D Input
VCELL1-4	Single Cell Voltage Inputs
VASS1, VADD, VASS2	Analog Supply Voltage Inputs
VSHP, VSHM	Current Sense Resistor Inputs
VREG	Voltage Reg. Control Output
OSCOUT, OSCIN	Crystal Oscillator Inputs (32 KHz)
OUTPUT1-6	Programmable Output Pins 1-6
VDDD, VDSS	Digital Power Supply Inputs
SMB-CLK, SMB-DTA	SMBus Interface Pins

Product Overview

The PS334 is an advanced Smart Battery IC product from PowerSmart, incorporating the accurate capacity monitoring from the PS330 and PS331 plus six (6) programmable output pins. The PS334’s programmable outputs can be used as LED outputs to display State-Of-Charge (SOC), direct control of external charge circuitry, or to provide additional levels of safety in LiIon packs.

As a result, PowerSmart’s PS334 eliminates the need for additional components normally required for charge control or safety. Using the PS334, OEMs can achieve the highest smart battery data accuracy in a complete battery management solution at an attractive cost. The PS334 delivers both space and total system component cost savings which is especially useful for applications such as PDAs, digital cameras, and notebook computers

Table of Contents

1. General Description

The PS334 is part of PowerSmart's P3 family of ICs whose integrating, self-calibrating 14-bit A/D ensures precise measurements of current, voltage and temperature to enable remaining runtime. The P3 family's patented, self-learning 3-dimensional cell models compensate for self-discharge, temperature, charge/discharge efficiencies and other factors, and an auto-zero offset correction feature automatically compensates for accuracy drift during usage. In addition, an advanced integrated 8-bit RISC microprocessor enables exceptionally fast data computations.

Additional enhancements to the PS334 include more Lithium Ion cell model parameters (now over 250) and control algorithm values. Additional capacity correction and error reducing functions have been added to enhance reliability and improve fuel-gauge and charge control performance.

New capacity correction features have been added to PowerSmart's patented control algorithms. These include new temperature based End-of-Charge trigger conditions as well as capacity correcting conditions using low-discharge (with load), open-circuit, and near End-Of-Charge based voltage trip points.

The PS334 can be easily customized for a particular application's Lithium Ion-based battery cell chemistries using the external EEPROM. Upgrades to previously assembled battery packs are simple via the standard SMBus serial communications interface. The EEPROM also contains the programming information for the configuration of the programmable output pins.

On-chip circuitry includes an internal RC oscillator and watchdog timer that are complemented by a low-cost, low-power external 32 kHz crystal for precise timing. A single external FET voltage regulator circuit is also included for operation from battery voltages greater than 3.3 Volts.

2. Module Versions

Based on the PS334, PowerSmart's PS345X Series Modules provide complete, 'turn-key' subsystems that can be simply integrated in a battery pack or embedded application. As a result, the PS345X Module family supports rapid prototyping and production of complete battery management solutions for all portable computer, communication, medical, industrial, or automotive applications.

Each PS345X module incorporates the PS334 IC, together with reprogrammable EEPROM and complete safety circuitry, and programmable output pins. The PS3452, PS3453, and PS3454 battery management boards. Respectively, they support Lithium Ion configurations of 2, 3, and 4-cell applications.

Please refer to the PowerSmart web site for ordering information (www.powersmart.com).

3. Development Tool Summary

PowerSmart provides all the necessary hardware and software to enable easy tailoring of battery control algorithm parameters and cell performance models to meet specific application requirements and attain the highest accuracy available anywhere. Table 1 summarizes the development tool offering from PowerSmart to support the PS334. Please refer to the PowerSmart web site for ordering information and design documentation (including schematics) at www.powersmart.com.

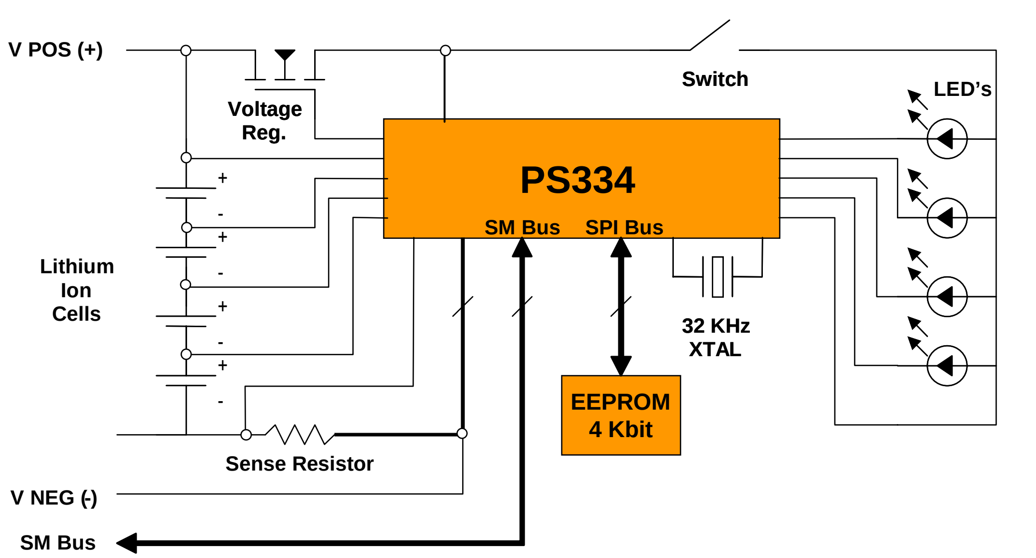
4. Reference Documents

This data sheet provides an overview of the PS334 as well as features that apply to the entire P3 family. It also provides a detailed description of features and specifications that

Table 1: P3 Family Development Tool Summary

Tool	Description
P3 Li Ion Workbook	Microsoft Excel ™ based tool used to edit the initial configuration of a P3 battery pack and create a .p3i file for programming into the EEPROM. Available for download at www.powersmart.com.
SBTool Software	Development software package of multiple programs for configuration, calibration, and testing of P3-based battery packs including: - PROG: Programs and verifies external serial EEPROM - CAL: Calibration software that can automatically calibrate up to 4 packs at once - WINFO: Read/write of 34 Smart Battery Data values - FTEST: Final Test program to verify end-of-line module/pack values Supplied with all of the hardware tools listed below:
P3 Eval System (PS033N-500)	Low cost platform for the P3 family of IC's for immediate evaluation of P3 functionality. Supplied with a PS331 and circuitry for PC COM port to SMBus translation to facilitate communication over the SMBus. Can be connected to an external lithium ion battery cells to emulate final battery pack operation.
P3 Cal System (PS010N-150)	Cost effective, single board calibration system used for programming and calibration of a P3 battery pack. Provides circuitry for PC COM port to SMBus translation to facilitate communication between a P3 battery pack and the PC. Also provides A/D and D/A hardware for calibrating the P3 on-chip A/D converter.
Info / Test Board (PS011-501)	The INFO/FTEST hardware interface board is a simple circuit that permits a PC's serial COMx port to be used as an SMBus interface.

Figure 1: PS334 Applications Circuit – Removable Smart Battery Block Diagram



are unique to the PS334. For further information on P3 device and development tool operations, please refer to the following documents available for download at www.powersmart.com:

PS331 Data Sheet
P3 Family User's Guide
PS345X Data Sheet
Applications Notes:
- P3 Ex. Connection Diagrams
- P3 PC Board Layout Guide
- P3 Temperature Alarm Operation
- P3 Calibration Explanations

Development Tool Documentation:
- Lithium Ion Workbook Guide
- SBTool User's Guide
- P3 Eval System Data Sheet
- P3 Cal System Data Sheet
- P3 Info / Test Board Data Sheet
- SBToolBox Data Sheet

5. PS334 Programmable Features

Functions that are programmable within the PS334 are configured through values written to the external EEPROM memory during the battery pack programming process. The PS334 supports all of the programmable features as in the PS330 / PS331. Functions that have been added to the PS334 or enhanced from PS330 / PS331 are documented below. Refer to the P3 User's Guide for complete programming information of all P3 products.

6. Output Pin Configuration

The PS334 programmable output pins operate in one of three states:

1) As an LED for State-of-Charge display
2) As a Secondary Safety Condition output
3) As a Charge Condition output

Each of the output pins is configured to perform one of the above functions through the programming of the Output Pin Configuration registers shown in Table 3.

For each output pin, there is an associated bit in both the LED_CFG(L) and LED_CFG(H) registers. The two bits for each output pin can be programmed to select one of four operating modes for that pin as shown in Table 4.

Once the operating mode for output pin is selected, the logical activation condition for the pin is programmed using the LEDx_AND and LEDx_OR register associated with that pin.

The location within the EEPROM of the logical activation control registers for each of the programmable output pins is summarized in Table 5.

The programming of these registers depends upon the activation mode selected for the output pins as described in the following sections.

6.1. Output Pin Initialization

OUTPUT6 is initialized to a low immediately following a hardware reset. Output pins OUTPUT1-5 are not initialized at this time. However, once the internal firmware begins execution, the remaining outputs will be initialized according to the programming of the LED_INIT variable within the EEPROM as shown in Table 6.

The firmware sets the associated pin to the value (0 or 1) programmed into the register.

6.2. Safety Control Configuration

For safety, any combination of the pins can be set to activate on over-voltage, over-temperature, cell imbalance, under-voltage, under-temperature, over-current or other safety related condition. Each pin can be programmed separately for any AND/OR combination of conditions.

When the configuration of an output pin is set for Safety control as described above (LED_CFGH:L = 00), then the activation condition for the pin is defined through the programming of the LEDx_AND and LEDx_OR register as shown in Table 7.

6.3. Charge Control Configuration

For charge control applications, the OUTPUTx pins can be set to activate due to TerminateCharge, FullyCharged, over-temperature, over-voltage, pre-charge, or other charge related conditions. Each pin can be programmed separately for any AND/OR combination of conditions.

When the configuration of an output pin is set for Safety control as described above (LED_CFGH:L = 00), then the activation condition for the pin is defined through the programming of the LEDx_AND and LEDx_OR register for the operates as shown in Table 8.

6.4. LED Control Pin Configuration

One or more of the output pins can be configured to operate as an LED 'bar-graph' that displays SOC. This option is selected for an individual pin when its LED_CFGH:L bits are set to 10 or 11. The LED_STEP value in EEPROM must be programmed for the number of LED's used in the bar graph display, as shown below:

LED_STEP = 100 / number of LEDs

example: For 5 LED's, set LED_STEP=20

The value of the display segments from highest to lowest are assigned to the output pins selected for LED function from highest to lowest. For example, if contiguous output pins (e.g. OUTPUT5-1) are used for LED outputs, the segments will be assigned as follows:

OUTPUT Pin #:	**5**	**4**	**3**	**2**	**1**
SOC Value:	100%	80%	60%	40%	20%

Also as an example, if non-contiguous pins are used (e.g. OUTPUT5, OUTPUT3-1), the segments will be assigned as:

OUTPUT Pin #:	**5**	**3**	**2**	**1**
SOC Value:	100%	75%	50%	25%

"MSB" of the display will be assigned to 5 and the LSB will be assigned to non-contiguous LED's.

In all cases, the least significant output pin assigned as an LED output will always flash if the SOC value is below 10%.

The "Polarity" bit in LED_POLARITY is used to select an active high or active low output. Normal polarity for an LED SOC bar-graph requires this bit be set to active low output. LED_POLARITY is valid for all methods described below (bar graphs, conditional outputs). In case that an output is calculated to 0 and the polarity bit was set to 1, then the output is inverted and will become HIGH.

Two modes of operation are possible for a pin configured as an LED output, depending on the programming of the LED_CFG register as described in Table 4. In both modes, the LED "bar graph" will be displayed on the pins when the SWITCH input is pulled low. When LED_CFGH:L = 10, then the SOC value for a duration of time determined by the programming of the N_DISPLAY value in EEPROM. When LED_CFGH:L = 11, then the SOC will be continuously displayed on the LED outputs, so long as the battery pack is undergoing a charge with a charge current greater than or equal to the LED_CURRENT value.

7. RM Correction and FCC Relearn

As in other P3 Family devices, the PS334 performs a RemainingCapacity (RM) correction when an End-Of-Discharge (EOD) condition is reached according to the values programmed into the Residual Capacity Look-Up Table (LUT). Other parameters dependent on RemainingCapacity are updated at this time, including RelativeStateOfCharge and AbsoluteStateOfCharge. In addition, a FullChargeCapacity (FCC) relearn is performed at EOD as well.

For increased accuracy of RemainingCapacity, the PS334 provides 3 additional options for voltage-based correction of this parameter. With one of the options, an FCC relearn is also performed. The options are summarized as follows:

- Near-EOD Correction / Relearn: RM correction and FCC relearn during discharge before the End-Of-Discharge (EOD) point is reached
- Open-Circuit Correction: RM correction at a mid-point voltage during open-circuit conditions when the accumulated RemainingCapacity error exceeds a threshold.
- Nearly Charged Correction: RM Correction during charging at a voltage point prior to a fully charged, End-Of-Charge condition.

Operation of each of these options is described below:

7.1. Near EOD Correction / Relearn

During discharge, The PS334 provides an optional RemainingCapacity correction and FullChargeCapacity relearn at a programmable voltage point above the end-of-discharge (EOD) voltage. This optional feature is in addition to the RemainingCapacity correction and relearn function that is performed when EOD is reached as in other P3 family devices. This feature

Table 2: PS334 Pin Description

PIN #	NAME	DESCRIPTION
1	INPUT	(Input) Edge triggered input pin typically used for LED activation. May also be used for 'Sleep Mode' wake-up comparator input.
2	EE-SCK	(Output) External serial EEPROM Clock . Connect to SCK pin on external serial EEPROM.
3	EE-CS	(Output) External serial EEPROM Chip Select . Connect to CS pin on external serial EEPROM.
4	VREFT	(Output) Reference voltage output for use with temperature measuring A/D circuit . This 150 mV output is the top leg of a voltage divider thermistor circuit.
5	VNTC	(Input) Temperature measurement A/D input for use with temperature circuit. This is the mid-point connection of a voltage divider where the upper leg is a thermistor (103ETB-type) and the lower leg is a 3.65K ohm resistor . This input should not go above 150 mV.
6	VCELL1	(Input) Lowest level input for A/D measurement of cell voltages.
7	VASS1	Analog ground reference point.
8	VCELL2	(Input) Second to lowest level input for A/D measurement of cell voltages.
9	VCELL3	(Input) Second to highest level input for A/D measurement of cell voltages .
10	VCELL4	(Input) Highest level input for A/D measurement of cell voltages.
11	VADD	(Input) Analog supply voltage input.
12	VSHP	(Input) Current measurement A/D input from positive side of the current sense resistor.
13	VSHM	(Input) Current measurement A/D input from negative side of the current sense resistor.
14	VASS2	Analog ground reference point.
15	VREG	(Output) Used to control an external small signal MOSFET to provide a regulated voltage to the IC . Only required for battery packs with voltages greater than 3.6V.
16	OSCOUT	(Output) Oscillator connection for an external low-power 32.768 kHz crystal which provides accurate timing for self-discharge and capacity calculations.
17	OSCIN	(Input) Other oscillator connection . (See OSCOUT description.)
18	EE-SI/SO	(Bidirectional Input /Output) External SPI serial EEPROM data input/output. Connect to the SI and SO pins on external SPI serial EEPROM.
19	OUTPUT6	(Output) Programmable Output #6
20	VDDD	(Input) Digital supply voltage input.
21	OUTPUT5	(Output) Programmable Output #5
22	OUTPUT4	(Output) Programmable Output #4
23	OUTPUT3	(Output) Programmable Output #3
24	OUTPUT2	(Output) Programmable Output #2
25	OUTPUT1	(Output) Programmable Output #1
26	SMB-DTA	SMBus Data pin connection.
27	SMB-CLK	SMBus Clock pin connection.
28	VDSS	Digital ground reference point.

provides a more precise prediction of RemainingCapacity and an opportunity to relearn FullChargeCapacity prior to a full EOD condition.

The Near EOD Correction / Relearn voltage trip point is defined as V_CAPRST and is programmed into the external EEPROM. An additional look-up table (CAPRST) has been added to support the additional function. The function is enabled/disabled via the CAPRST control bit in the VSOC_CFG byte in external EEPROM.

When the voltage measured on the VPACK4 pin is below V_CAPRST for a duration of CAPRST_RE_CHECK x TWS periods, then a valid V_CAPRST trip point has occurred. RemainingCapacity is loaded with a correction value from the CAPRST Look-Up-Table. The structure of this LUT is illustrated in Table 9. Also, to maintain accurate prediction ability, a Near EOD Correction / Relearn is only performed during a discharge that has reached a valid V_CAPRST trip point after a previous valid fully charged "End-Of-Charge" (EOC) condition. If a partial charge occurs before reaching a valid V_CAPRST voltage, then no correction / relearning will occur. In addition, the correction will not occur if the discharge rate at V_CAPRST is greater than the 'C-rate' adjusted value in HDISCHARGE.

When a valid Near EOD Correction / Relearn condition does occur according to the criteria described above, RemainingCapacity will be loaded with a correction value from the CAPRST table determined by the current temperature and discharge current conditions. In addition, the FullChargeCapacity value will be relearned. Also, the error calculations represented by the SBData value of MaxError will be reduced to amount programmed into the ERR_RED_CAPRST variable in external EEPROM.

Overall, the function of the Near EOD Correction / Relearn is very similar to operation at End-of-Discharge. The main difference is that the it is based on pack voltage and does not generate an alarm as in the case of EOD.

Table 3: Output Pin Configuration Registers – LED_CFG(L) and LED_CFG(H)

EEPROM Register										
Pg.	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	C6	LED_CFG(L)	0	0	OUTPUT6	OUTPUT5	OUTPUT4	OUTPUT3	OUTPUT2	OUTPUT1
0	C7	LED_CFG(H)	0	0	OUTPUT6	OUTPUT5	OUTPUT4	OUTPUT3	OUTPUT2	OUTPUT1

Note: Bits 6 and 7 in both registers must be set to 0 for proper operation.

Table 4: Output Pin Activation Configuration Registers – LED_CFG(L) and LED_CFG(H)

LED_CFG(H) OUTPUTx	LED_CFG(L) OUTPUTx	Activation Method
0	0	Safety Conditions in LEDx_AND:LEDx_OR bytes cause activation
0	1	Charge Conditions in LEDx_AND:LEDx_OR bytes cause activation
1	0	LED 'bar-graph' SOC display activated for a programmable duration (N_DISPLAY) when SWITCH input is pulled LOW
1	1	LED 'bar-graph' SOC display "permanently" activated, so long as the charging current remains above the programmed LED_CURRENT value.

Table 5: Output Pin Logical Activation Condition Control Register Summary

EEPROM Location			
Page	Address (Hex)	Register Name	Pin Name
0	98	LED1_AND	OUTPUT1
0	99	LED1_OR	
0	9A	LED2_AND	OUTPUT2
0	9B	LED2_OR	
0	9C	LED3_AND	OUTPUT3
0	9D	LED3_OR	
0	9E	LED4_AND	OUTPUT4
0	9F	LED4_OR	
0	A0	LED5_AND	OUTPUT5
0	A1	LED5_OR	
0	A2	LED6_AND	OUTPUT6
0	A3	LED6_OR	

Table 6: LED_INIT Register Description

Address										
Pg.	Hex	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	A4	LED_INIT	0	0	OUTPUT6	OUTPUT5	OUTPUT4	OUTPUT3	OUTPUT2	OUTPUT1

7.2. Open Circuit RM Correction

The PS334 provides the ability to correct RM when the battery pack is at a mid-point voltage, in an open-circuit condition, and a high error has been accumulated. Such a condition could occur if the battery pack has been removed for a long period of time, resulting in an incorrect determination of RemainingCapacity.

Open Circuit RemainingCapacity correction is enabled / disabled through the MIDRST bit in the VSOC_CFG location in external EEPROM. The voltage trip point value for Intermediate RemainingCapacity correction is programmed using the V_MIDRST parameter and a tolerancevoltage for the trip point is programmed using V_CATCH. A valid trip point will occur when the pack voltage is within the programmed

Table 7: Safety Conditions Definitions for LEDx_OR and LEDx_AND bytes

LEDx_AND		LEDx_OR	
Bit #	Test Condition	Bit #	Test Condition
7	Vcellx > VCELL_MAX	7	Vcellx > VCELL_MAX
6	Vcellx < VCELL_MIN	6	Vcellx < VCELL_MIN
5	Vcell_Diff > VDIFF_MAX	5	Vcell_Diff > VDIFF_MAX
4	Vpack > VPACK_MAX	4	Vpack > VPACK_MAX
3	Temperature > TEMP_MAX	3	Temperature > TEMP_MAX
2	Temperature < TEMP_MIN	2	Temperature < TEMP_MIN
1	Current( ) > IMAXC (charging)	1	Current( ) > IMAXC (charging)
0	Current( ) > IMAXD (discharging)	0	Current( ) > IMAXD (discharging)

Operation:
_AND byte: Desired trigger conditions are selected with a "1" in the control bit. All selected conditions must be true for a true "AND" condition. If no conditions are desired, 0FFh must be written to the byte.

_OR byte: Desired trigger conditions are selected with a "1" in the control bit. Any selected condition which is true will cause a true "OR" condition. If no conditions are desired, 00h must be written to the byte.

OUTPUTx pin activation results when all "AND" condition OR any "OR" condition is true.

Example:
If _AND byte is set to 088h, and _OR byte is set to 010h, then the OUTPUTx pin is active only if:

[(Vcellx > VCELL_MAX) AND (Temperature > TEMP_MAX)] OR [Vpack > VPACK_MAX]

Table 8: OUTPUT1-6 Charge Control using LEDx_OR and LEDx_AND bytes

LEDx_AND		LEDx_OR	
Bit #	Test Condition	Bit #	Test Condition
7	Vcellx > VCELL_MAX	7	Vcellx > VCELL_MAX
6	TermChargeAlarm	6	TermChargeAlarm
5	Fully_Charged Flag	5	Fully_Charged Flag
4	SOC > MAXSOC	4	SOC > MAXSOC
3	Temperature > TEMP_MAX	3	Temperature > TEMP_MAX
2	PRECHARGE condition true	2	PRECHARGE condition true
1	INPUT pin activated	1	INPUT pin activated
0	Vcellx > V_EOC	0	Vcellx > V_EOC

Operation:
_AND byte: Desired trigger conditions are selected with a "1" in the control bit. All selected conditions must be true for a true "AND" condition. If no conditions are desired, 0FFh must be written to the byte.

_OR byte: Desired trigger conditions are selected with a "1" in the control bit. Any selected condition which is true will cause a true "OR" condition. If no conditions are desired, 00h must be written to the byte.

OUTPUTx pin activation results when all "AND" condition OR any "OR" condition is true.

Example:
If _AND byte is set to 088h, and _OR byte is set to 010h, then the OUTPUTx pin is active only if:

[(Vcellx > VCELL_MAX) AND (Temperature > TEMP_MAX)] OR [SOC > MAXSOC]

tolerance of V_MIDRST and when MaxError is larger than a preset limit (ERR_LIM_MIDRST), and the discharge current is zero for a preset time (N_MIDRST x TWS). RemainingCapacity is then loaded with the appropriate correction value from the SOC_MIDRST table (illustrated in Table 10) based on the present temperature. The MaxError register itself is then re-loaded with ERR_RED_MIDRST.

V_CATCH is the tolerance of the V_MIDRST voltage value.

7.3. Near EOC RM Correction

The PS334 supports a voltage-based RemainingCapacity correction point near a fully charged, End-Of-Charge condition. Near EOC RemainingCapacity correction is enabled / disabled via the NEARFULL bit in the VSOC_CFG location in external EEPROM. The voltage trip point is programmed using the V_NEARFULL parameter.

When the pack voltage reaches the V_NEARFULL threshold during charging and the charge current begins to taper, RM will be corrected with a value from the VNF table (shown in Table 11) based the charge rate and temperature. Also, MaxError will be loaded with the value contained in ERR_RED_VNF in EEPROM memory.

8. Lithium Ion Taper Currents during EOC

The PS334 expands the Lithium Ion Taper current programmability from one value in previous P3 implementations to six values based on temperature as shown in Table 12. As a result, improved charging performance is achieved over varying temperature conditions.

9. Pre-Charge Limit Conditions

The PS334 provides the ability to program lower initial charge rates when both low voltage or low temperature conditions occur.

If charging is desired but Temperature < PCHRG_T then the PRECHARGE value will be used for ChargingCurrent. When the condition is no longer true, ChargingCurrent will be set to the previous defined CHARGING_CURR value, if Vcellx voltage limits are met (see below.)

If charging is desired but any Vcellx < PCHRG_V then the PRECHARGE value will be used for ChargingCurrent. When the condition is no longer true, ChargingCurrent will be set to the previous defined CHARGING_CURR value, if temperature limits are met (see above.)

Table 9: Near EOD RemainingCapacity Correction Table Structure

C-Rate \ Temp.	< CAPRST_T1	< CAPRST_T2	< CAPRST_T3	< CAPRST_T4	< CAPRST_T5	< CAPRST_T6	≥ CAPRST_T6
CAPRST_CR1	CR_RM11	CR_RM12	CR_RM13	CR_RM14	CR_RM15	CR_RM16	CR_RM17
CAPRST_CR2	CR_RM21	CR_RM22	CR_RM23	CR_RM24	CR_RM25	CR_RM26	CR_RM27
CAPRST_CR3	CR_RM31	CR_RM32	CR_RM33	CR_RM34	CR_RM35	CR_RM36	CR_RM37
CAPRST_CR4	CR_RM41	CR_RM42	CR_RM43	CR_RM44	CR_RM45	CR_RM46	CR_RM47
CAPRST_CR5	CR_RM51	CR_RM52	CR_RM53	CR_RM54	CR_RM55	CR_RM56	CR_RM57
CAPRST_CR6	CR_RM61	CR_RM62	CR_RM63	CR_RM64	CR_RM65	CR_RM66	CR_RM67
CAPRST_CR7	CR_RM71	CR_RM72	CR_RM73	CR_RM74	CR_RM75	CR_RM76	CR_RM77
CAPRST_CR8	CR_RM81	CR_RM82	CR_RM83	CR_RM84	CR_RM85	CR_RM86	CR_RM87

Table 10: Open Circuit RemainingCapacity Correction Table Structure

Temperature:	≥ T_MIDRST1	≥ T_MIDRST2	≥ T_MIDRST3	≥ T_MIDRST4	< T_MIDRST5
RM Value:	RM_MIDRST1	RM_MIDRST2	RM_MIDRST3	RM_MIDRST4	RM_MIDRST5

Table 11: Near EOC RemainingCapacity Correction Table Structure

C-Rate \ Temp.	< VNF_T1	< VNF_T2	< VNF_T3	< VNF_T4
VNF_CR1	VNF_RM11	VNF_RM12	VNF_RM13	VNF_RM14
VNF_CR2	VNF_RM21	VNF_RM22	VNF_RM23	VNF_RM24
VNF_CR3	VNF_RM31	VNF_RM32	VNF_RM33	VNF_RM34
VNF_CR4	VNF_RM41	VNF_RM42	VNF_RM43	VNF_RM44
VNF_CR5	VNF_RM51	VNF_RM52	VNF_RM53	VNF_RM54
VNF_CR6	VNF_RM61	VNF_RM62	VNF_RM63	VNF_RM64
VNF_CR7	VNF_RM71	VNF_RM72	VNF_RM73	VNF_RM74

Table 12 : Taper Currents Table Structure

Temperature:	≥ TEOC1	≥ TEOC2	≥ TEOC3	≥ TEOC4	< TEOC5
Taper Current Value:	CRHEOC1	CRHEOC2	CRHEOC3	CRHEOC4	CRHEOC5

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{ADD}-$V_{ASS1,2}$	Supply voltage - Analog section	2.5	7.0	V
V_{DDD}-V_{DSS}	Supply voltage - Digital section	2.5	7.0	V
V_{CELLx}	Voltage at any VCELLx pin	-0.5	20	V
V_{PIN}	Voltage directly at any pin (except VCELLx)	-0.5	7.0	V
T_{BIAS}	Temperature under bias	-25	85	°C
$T_{STORAGE}$	Storage temperature (package dependent)	-35	150	°C

Note: These are stress ratings only. Stress greater than the listed ratings may cause permanent damage to the device. Exposure to absolute maximum ratings for an extended period may affect device reliability. Functional operation is implied only at the listed Operating Conditions below.

10.2. DC Characteristics

(TA=-20°C to 85°C; VCC =3.3V ± 10%)

Symbol	Description	Min	Typ.	Max	Units	Notes
V_{ADD}	Supply voltage – Analog section	2.7	3.3	5.0	V	
V_{DDD}	Supply voltage – Digital section	2.7	3.3	5.0	V	
I_{DD}	Current consumption (See modes below)	8	270	600	µA	
	Run Mode	375	500	600	µA	1
	Sample Mode	190	250	375	µA	1,2
	Low-Voltage Sleep	8	12	15	µA	3
	Shelf Sleep	10	12	18	µA	3,4
V_{SENSE}	Sense resistor voltage input	-152		152	mV	
V_{REFT}	NTC Reference voltage output at V_{REFT} pin		150		mV	
LED0..4	Output voltage for 5 mA current output			0.5	V	
$V_{IN-CELL4}$	Voltage at VCELL4	-0.5		20	V	
I_{IN}	Input current at any VCELLx (only for V_{time})			200	µA	
SCL,SDA	Output voltage for 350 µA output current			35	mV	
$I_{PULLDOWN}$	Pull down current at SCL,SDA		0.5	1.0	µA	
I_{LO}, I_{HI}	Current at SCL,SDA			10.0	µA	
$V_{LO,IN}$	Input voltage for LOW at SCL,SDA	-0.5	0.4	0.6	V	
$V_{HI,IN}$	Input voltage for HIGH at SCL,SDA	1.4	2	5.5	V	
$V_{LO,OUT}$	Output voltage for LOW at SCL,SDA		0.2	0.4	V	
I_{SINK}	Device sink current	100		350	µA	

Notes:

1. During LED illumination, currents may peak at 10mA but average individual LED current is typically 5 mA (using low-current, high-brightness devices.)
2. Sample Mode power consumption is variable and dependent on threshold and timing settings for Sample Mode operation.
3. Power consumption in Low-Voltage Sleep and Shelf Sleep Modes are dependent on the pack voltage. Connecting the SWITCH pin to the VDDD or VADD pin for more than 0.5 second causes the IC to recover from Shelf-Sleep Mode.AC Characteristics.

10.3. AC Characteristics

(TA=-20°C to 85°C; VCC =3.3V ± 10%)

Symbol	Description	Min	Typical	Max	Units	Notes
f_{RC}	Internal RC oscillator frequency	410	465	530	kHz	
f_{XTAL}	External crystal frequency		32.768		kHz	
$f_{A/D}$	Internal A/D operating clock frequency		$f_{RC}/10$		kHz	
f_{CPU}	Internal CPU operating clock frequency		$f_{RC}/4$		kHz	
V_{time}	Voltage measurement time, 10 bit		$2^{11}/f_{A/D}$		ms	
T_{time}	Temperature measurement time, 10 bit		$2^{11}/f_{A/D}$		ms	
I_{time}	Current measurement time, 13 bit+sign		$2^{14}/f_{A/D}$		ms	
C_{SMB}	Bus capacitance @ 100 kHz			160	pF	

11. AC Characteristics – SMBus

(TA=-20°C to 85°C; VCC =3.3V ± 10%)

Symbol	Description	Min	Typical	Max	Units	Notes
f_{SMB}	Clock operating frequency	<1.0		100	kHz	
$f_{SMB\text{-}MASTR}$	Broadcast bit frequency (Note 1)	50	$f_{RC}/8$	68	kHz	1
t_{free}	Free time between START and STOP	4.7			µ s	
t_{SHLD}	Hold time after START condition	4.0			µ s	
$t_{RSSETUP}$	Setup time before repeated START	250			n s	
t_{PSETUP}	Setup time STOP condition	4.0			µs	
t_{HLD}	Data hold time	0			n s	
t_{SETUP}	Data setup time	250			n s	
$t_{LOW:SEXT}$	Message buffering time			24	m s	
$T_{TIMEOUT}$	Timeout period	25		35	m s	
t_{LOW}	Clock low period	4.7			µ s	
t_{HIGH}	Clock high period	4.0			µ s	
t_{HL}	Clock / data fall time			300	n s	
t_{LH}	Clock / data rise time			1000	n s	

Notes:

1. Used when broadcasting AlarmWarning, ChargingCurrent, and/or ChargingVoltage values to either a SMBus Host or a SMBus Smart Battery Charger. This is only used when the PS334 becomes a SMBus Master for these functions. The receiving (Slave) device may slow the transfer frequency. See *SMBus/I²C Tutorial* in PS331 data sheet for additional information.

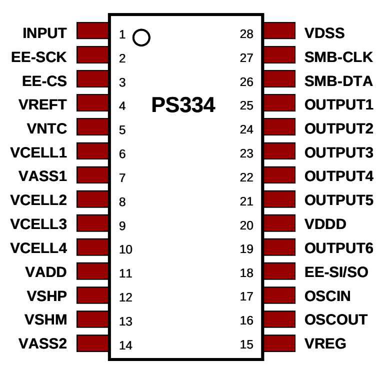
11.1. Granularity

(TA=-20°C to 85°C; VCC =3.3V ± 10%)

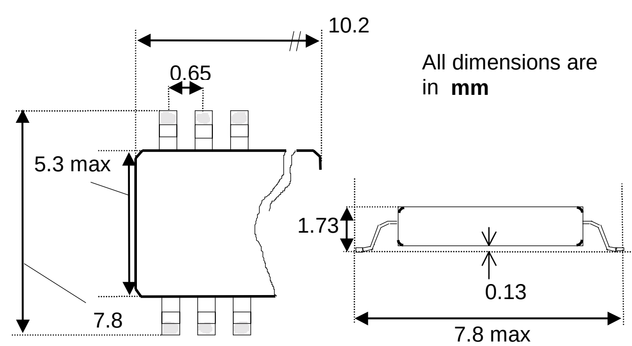
Symbol	Description	Min	Typical	Max	Units	Notes
$G_{ranularity}$	Voltage granularity, @Max = 17000 mV		16.5		mV/bit	
$T_{granularity}$	Temperature granularity, look up tables		0.1		°C/bit	
$I_{granularity}$	Current granularity, @ Rsense = 25 mOhms		0.8		mA/bit	

12. Mechanical Packaging Information

28 pin SSOP package



Mechanical Dimensions



13. Quality Control

PowerSmart, Inc., has received ISO-9001 certification through TUV Rheinland of North America, based in Newtown, Conn. ISO-9001 certification indicates that PowerSmart has met strict international standards of quality control in manufacturing systems including product design, production, training, and inspection and testing. PowerSmart received certification for a quality system for the Design and Development of Battery Control Integrated Circuits, Software, Modules, Chargers, and Systems. PowerSmart, Inc., provides smart battery and charger electronics designed for use with all battery chemistries, bringing a new level of accuracy, reliability and customization not available before with other smart battery ICs.

14. Errata and Revisions

14.1. PS334 - Version 4.1 Firmware

The following errata applies to PS334 silicon with version 4.1 firmware. :

1. Writing DesignCap / FullCap / AtRate / RemCapAlarm while CAPACITY_MODE is active (10mWh or “power mode”) results in incorrect capacity calculations (e.g. RemainingCapacity) anytime the actual capacity is above 256 mAh. As 256 mAh is a very low amount of capacity in real world conditions, users should refrain from using CAPACITY_MODE on this silicon revision of the PS334.
2. If an output pin is selected through the _AND and _OR registers for safety option Current() > IMAXC (charging) and another output pin is selected for safety option Current() > IMAXD (discharging) then there is a possibility that the pin selected for activation on Current() > IMAXD will toggle on and off for a period of ~ ¼ second when the pin selected for Current() > IMAXC is activated.
3. Learning of FCC is inhibited when discharge current is greater than the threshold defined by the LEARN_LIM parameter. On the PS334 with v4.1 firmware when the CycleCount is > 255, this limit check will not be performed.

14.2. PS334 Data Sheet Revision History

6/23/00:
The following revisions have been made to this data sheet from the previous version dated 6/18/00:

1. Addition of errata for the current version of the silicon and corrections to the previous data sheet.
2. Bits 5 and 6 of the programmable outputs in safety mode were swapped. This has been corrected in this data sheet revision. Also, the Lithium Ion Workbook v1.0 handles this properly.
3. Correction of minor formatting and spelling.

7/14/00:
Minor editing of “Features” list.

9/20/00:
Addition of “Notice” section.

15. Notice

PowerSmart products are not authorized for use as critical components of life support devices or systems. Seller disclaims any warranty or responsibility for such usage, which shall be at buyer’s sole risk, notwithstanding any prior notice to seller of such usage or intended usage.

As used herein, “life support devices or systems” are devices or systems that are intended for implant into the body to support of sustain life, or to assist such an implant, and whose failure to perform in such function can be reasonably expected to result in significant injury to the user. A “critical component” is any component of a life support device or system whose failure to perform can reasonably be expected to cause or result in the failure of performance of a life support device or system or to adversely affect its safety or effectiveness.