PMIC-DVC-101

4 Channel PCM Integrated Circuit

FEATURES

- 4 analog inputs
  - expandable to 128 using the SCIC-DVC-101
- 12 bit A/D converter (480 KSPS)
- User configurable including sub-commutation and super commutation
- 3 Digital Configurable Ports (16-bit inputs)
- Serial Input Port (115K baud)
- PCM NRZ-L or RNRZ-L (IRIG-106) output
- Selectable internal/external clock
- Provides time delay with external memory
- Single 5 Volt Operation
- 176 Lead Thin Quad Flatpack
- Available In Die Form

APPLICATIONS

- Munitions Testing
- Industrial Instrumentation
- Patient Monitoring
- System Health Monitoring

GENERAL DESCRIPTION

The 4 Channel PCM IC is a fully integrated, programmable, and expandable data acquisition system. It accepts four signal-conditioned analog input channels and performs pulse code modulation (PCM) non-return to zero level (NRZ-L) encoding to the IRIG-106-96 PCM standard. It has 16 discrete inputs, parallel and serial interfaces, can use an internal or external clock, optional memory delay, configuration memory for programmability, and power management capabilities for low power battery operation. A block diagram of the 4 Channel PCM IC is shown in Figure 1.

The 4 Channel PCM IC has a four-input analog multiplexer and a 12-bit successive approximation register (SAR) architecture analog-to-digital (A/D) converter that samples the input signal waveforms. The 4-to-1 analog multiplexer can pass four conditioned analog signals, each with a maximum bandwidth of 0 to 60 KHz. Signals may be captured by the on-chip (internal) SAR A/D converter or by an external A/D converter, or both. An external multiplexer control port provides system expansion to a maximum of 128 analog channels.

The 4 Channel PCM IC has digital configuration ports that can be configured to receive 16-bit parallel data, 16-bit A/D converter inputs, and 16 discrete inputs. A serial port supports baud rates greater than 115K.

Once data is captured the digital multiplexer & commutator feed the digital signals into the PCM encoder.

The PCM encoder frames and synchronizes the data according to the IRIG-106-96 Telemetry Standard. This includes a selectable output bit rate from 62.5 kilobits per second (Kbps) to 10 megabits per second (Mbps).

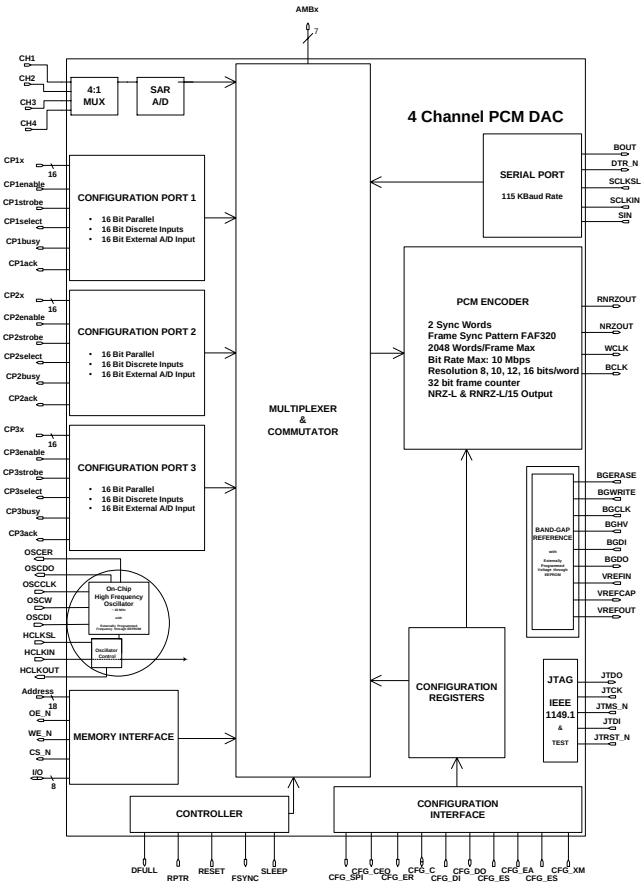

Figure 1: Functional Block Diagram

The PCM output code type is selectable for NRZ-L or RNRZ-L. The default at chip power-up is NRZ-L. The frame synchronization pattern is FAF320 in hexadecimal and is placed at the end of each frame. A 32-bit frame counter will increment per frame. An 8-bit sub-frame counter is available as a sub-frame ID code. The frame format is programmable from 8 to 2048 words-per-frame.

Sub-commutation capability is possible as defined per IRIG-106-96, section 4.3.2 “Frame Structure”. The default mode is 7 words-per-frame and contains the four analog channels, discrete inputs, a frame counter word, and 2 sync words. Word alignment is most significant bit first. Alternative frame formats may be programmed into the configuration memory.

The 4 Channel PCM IC also has the capability to impart a time delay using external SRAM. A 2^{17} maximum addressable memory is supported (125 ms for a single channel).

An externally selectable internal clock or an external reference may be used depending on required system precision.

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HARDENED SUBMINIATURE TELEMETRY AND SENSOR SYSTEM
DATA ACQUISITION CHIPSET

On warm-up, the 4 Channel PCM DAC will generate a PCM output within 50 milliseconds after primary power is applied.

Several power management techniques are used to improve low power battery operation. In operation, the chip selectively clocks only the functions that are needed to perform the task at hand. As well the chip may be powered down into a sleep mode which retains configuration data for quick restart.

PROGRAMMING

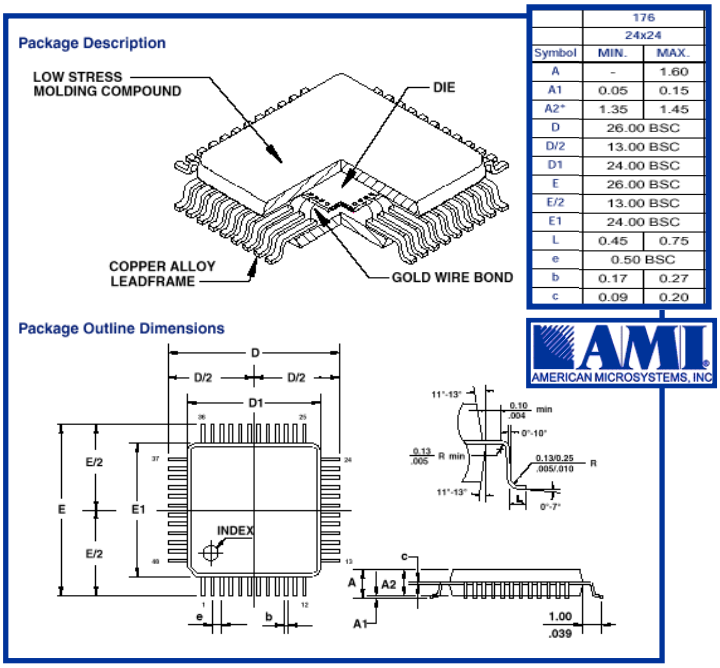
Time Delay

The 4 Channel PCM DAC IC can be configured to delay specific channels. Input pin TRIG synchronizes the delay to an external event.

Configuration Interface

The 4 Channel PCM DAC IC initializes in a power-up default configuration that is hard-coded in the internal logic. If the chip is in an external configuration mode, a configuration file is loaded via the configuration interface from an external PROM. The configuration file contains the configuration data for the device(s).

Multiple Devices with different configurations can be connected together in a “daisy chain”, and a single combined bit stream used to configure the chain of devices.



	176
	24x24
Symbol	MIN. / MAX.
A	- / 1.60
A1	0.05 / 0.15
A2*	1.35 / 1.45
D	26.00 BSC
D/2	13.00 BSC
D1	24.00 BSC
E	26.00 BSC
E/2	13.00 BSC
E1	24.00 BSC
L	0.45 / 0.75
e	0.50 BSC
b	0.17 / 0.27
c	0.09 / 0.20

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SPECIFICATIONS

Parameter		Symbol	Min	Typ	Max	Units
Power Requirements						
Supply Voltage	Digital	V_{DDD}	4.5	5.0	5.5	V
	Analog	V_{DDA}	4.5	5.0	5.5	V
Supply Current	Operating	I_{DD}		TBD		mA
	Low-Power	I_{PD}		TBD		uA
Power Consumption	Operating			TBD		mW
	Low-Power			TBD		uW
Dynamic Specifications						
Operating Ambient Temperature		T_A	-40	25	85.5	°C
External Voltage Reference		V_{REF}	1.5	2.25	2.5	V
Internal Voltage Reference		I_{REF}	2.13	2.25	2.37	V
A/D Converter Resolution		$B_{A/D}$			12	Bits
Clock Frequency		F_C		23		MHz
A/D Converter Conversion Rate		F_S		480	TBD	KSPS
Analog Frequency Response		$BW_{A/D}$	DC	60K	TBD	Hz
Signal to Noise		S/N	54			dB
Total Harmonic Distortion		THD		0.4	1	%
Interchannel Isolation				65		dB
Interchannel Gain Mismatch					±0.5	dB
Absolute Gain Error				± 1	± 2	%
Gain Drift				100	200	ppm/°C
Analog Inputs						
Signal Input Span		V_{pp}	$0.1*V_{REF}$		$1.8*V_{REF}$	V
Input Capacitance		C_{IN}			15	pF
Input Resistance		R_{IN}	1M			Ω
Clock						
Duty Ratio		CLK	45	50	55	%
Clock High Voltage		V_{CLKH}	$0.7xV_{DDD}$		V_{DDD}	V
Clock Low Voltage		V_{CLKL}	0		$0.3xV_{DDD}$	V
Digital Inputs						
Input High Voltage		V_{INHD}	2.4		V_{DDD}	V
Input Low Voltage		V_{INLD}	0		0.8	V
Input Current		I_{IND}			± 1	µA
Input Capacitance		C_{IND}			10	pF
Digital Outputs						
Output High Voltage		V_{OHD}	4.0		V_{DDD}	V
Output Low Voltage		V_{OLD}	0		0.4	V

The PCM configuration data contains the following:

- Serial Port Configuration
- Parallel Port Configuration
- Discrete Port Configuration
- External A/D Port Configuration
- Sample Rate & Configuration
- PCM Coding Configuration
  - Bits Per Word
  - Words Per Minor Frame
  - Minor Frames Per Major Frame
  - Assignment of port data to word location in frame(s)
- Time Delay

Configuration software is available for the PC environment.

PACKAGING

The Thin Quad Flatpack (TQFP) plastic package family is a reduced thickness plastic surface mount package. The 176 lead TQFP packages are constructed using the latest wire bonding and molding technology to provide surface mount packages with a body thickness of 1.0 or 1.4mm. This package finds many applications where size and weight are a critical factor.

The Four Channel PCM IC will be available in die form.

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