P3C1256
HIGH SPEED 32K x 8
3.3V STATIC CMOS RAM

FEATURES

- **3.3V Power Supply**
- **High Speed (Equal Access and Cycle Times)**
  - **— 12/15/20/25 ns (Commercial)**
  - **— 15/20/25 ns (Industrial)**
- **Low Power**
  - **— 360 mW Active**
- **Single 3.3 Volts ±0.3Volts Power Supply**
- **Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
  - **—28-Pin 300 mil DIP and SOJ**

DESCRIPTION

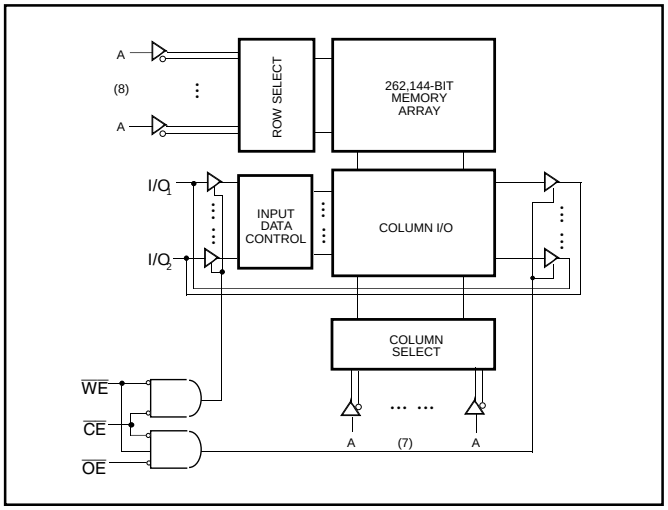
The P3C1256 is a 262,144-bit high-speed CMOS static RAM organized as 32Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 3.3V± 0.3V tolerance power supply.

Access times as fast as 12 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P3C1256 is a member of a family of PACE RAM™ products offering fast access times.

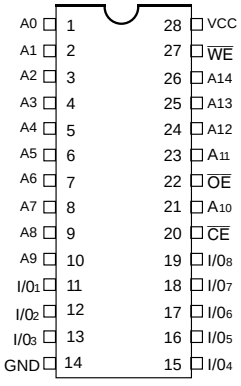
The P3C1256 device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{14}. Reading is accomplished by device selection ($\overline{CE}$ and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

Package options for the P3C1256 include 28-pin 300 mil DIP and SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P5), SOJ (J5)
TOP VIEW

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Temperature Range (Ambient)	Supply Voltage
Commercial (0°C to 70°C)	$3.0V \le V_{CC} \le 3.6V$
Industrial (-40°C to 85°C)	$3.0 \le V_{CC} \le 3.6V$

MAXIMUM RATINGS

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage with Respect to GND	-0.5	7.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	V_{CC} + 0.5	V
T_A	Operating Ambient Temperature	-40	85	°C
S_{TG}	Storage Temperature	-55	125	°C
I_{OUT}	Output Current into Low Outputs		25	mA
I_{LAT}	Latch-up Current	>200		mA

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output High Voltage (I/O_0 - I/O_7)	I_{OH} = –4mA, V_{CC} = 3.0V	2.4		V
V_{OL}	Output Low Voltage (I/O_0 - I/O_8)	I_{OL} = 8 mA I_{OL} = 10 mA		0.4 0.5	V V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	-5	+5	µA
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$ $\overline{CE} = V_{CC}$	-5	+5	µA
I_{SB}	V_{CC} Current TTL Standby Current	V_{CC} = 3.6V, I_{OUT} = 0 mA $\overline{CE} = V_{CC}$		20	mA
I_{SB1}	V_{CC} Current CMOS Standby Current	V_{CC} = 3.6V, I_{OUT} = 0 mA $\overline{CE} = V_{CC}$		3	mA

CAPACITANCES

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	Test Conditions	-12	-15	-20	-25	Unit
I_{CC}	Dynamic Operating Current	Commercial Industrial	* *	110 N/A	100 115	95 110	90 105	mA mA

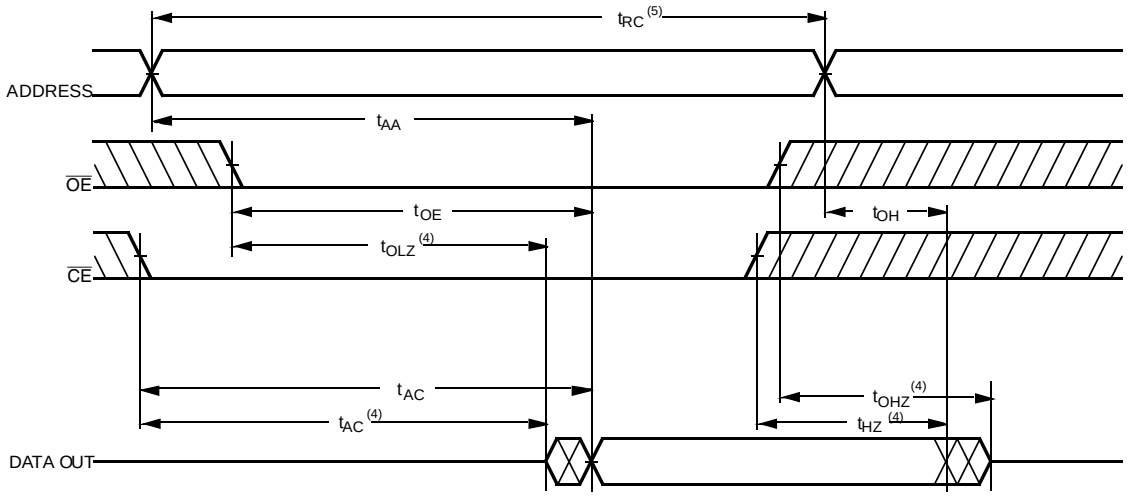
*****Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$, and $\overline{WE} \le V_{IL}$ (max), $\overline{OE}$ is high. Switching inputs are 0V and 3V.

AC ELECTRICAL CHARACTERISTICS - READ CYCLE

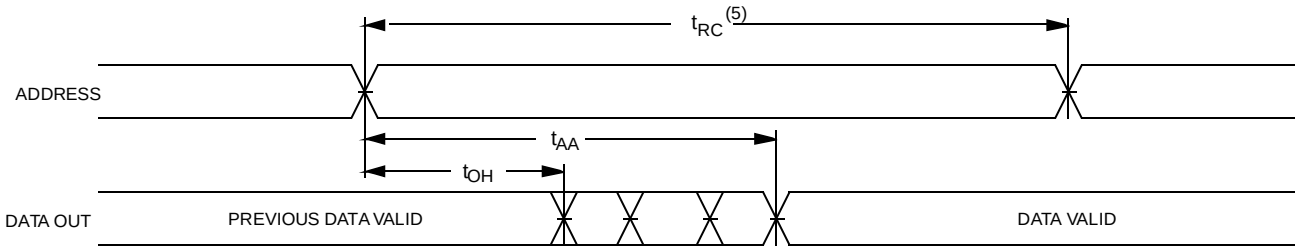
(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address Access Time		12		15		20		25	ns
t_{AC}	Chip Enable Access Time		12		15		20		25	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		7		8		9		10	ns
t_{OE}	Output Enable Low to Data Valid		7		9		11		12	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		6		7		9		10	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		20	ns

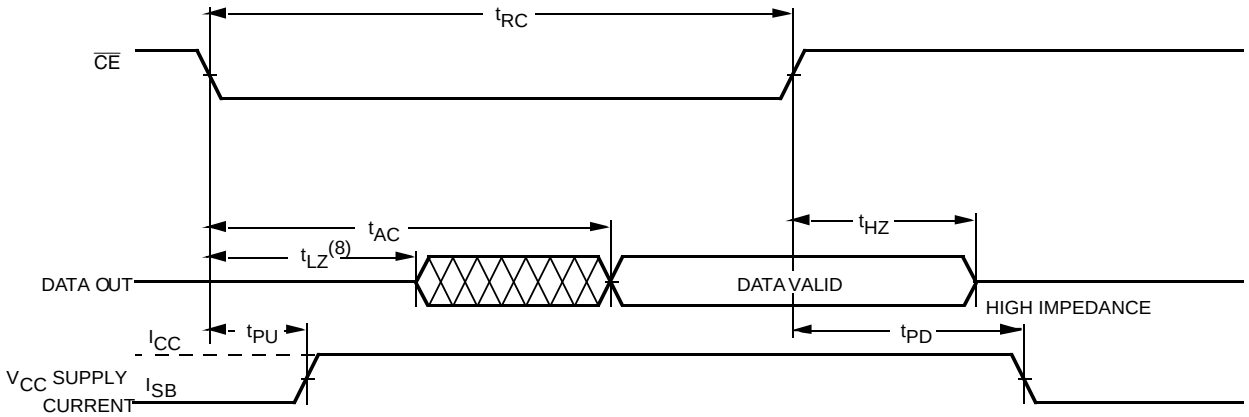
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[1]



READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)



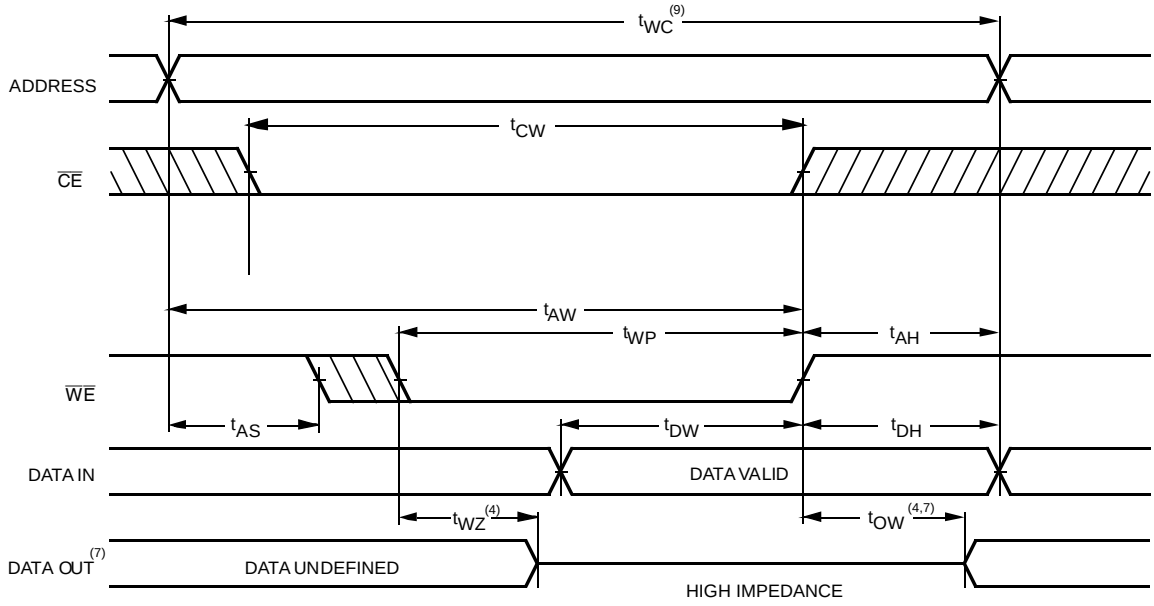
Notes:
1. $\overline{WE}$ is HIGH for READ cycle.
2. $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
3. ADDRESS must be valid prior to, or coincident with $\overline{CE}_1$ transition LOW .
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{CW}	Chip Enable Time to End of Write	10		12		15		18		ns
t_{AW}	Address Valid to End of Write	10		12		15		18		ns
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	9		11		15		18		ns
t_{AH}	Address Hold Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	8		10		12		15		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		8		10		11	ns
t_{OW}	Output Active from End of Write	3		3		3		3		ns

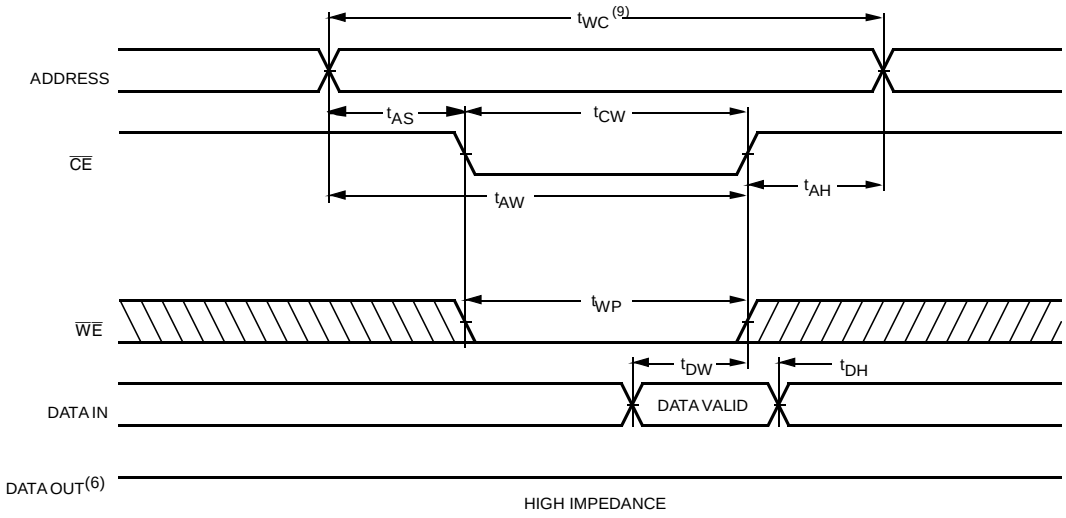
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[6]



Notes:

6. $\overline{CE}_1$ and $\overline{WE}$ must be LOW for WRITE cycle.
7. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
8. If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
9. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[6]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{I/O}$	Power
Standby	H	X	X	High Z	Standby
Standby	X	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	High Z	Active

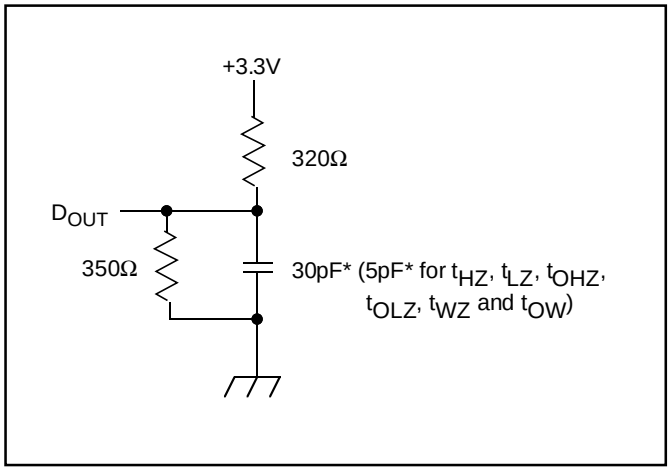


Figure 1. Output Load

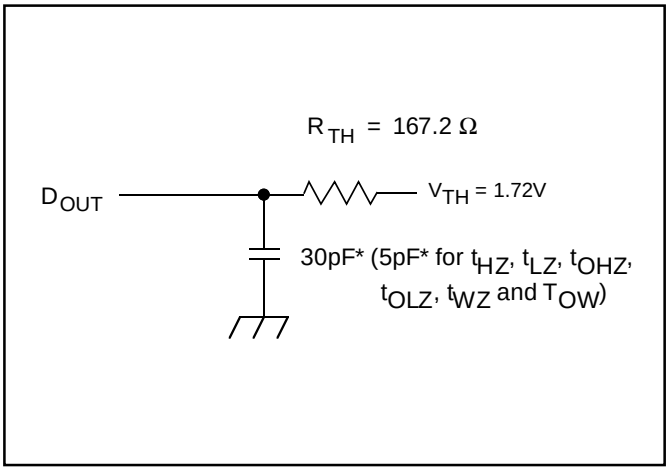


Figure 2. Thevenin Equivalent

* including scope and test fixture.

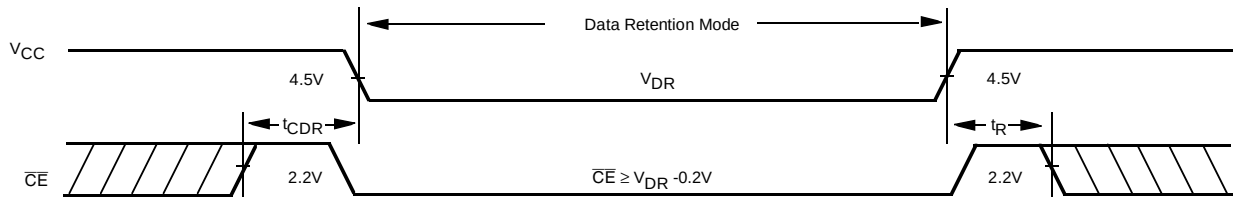
Note:
Because of the ultra-high speed of the P3C1256, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

DATA RETENTION

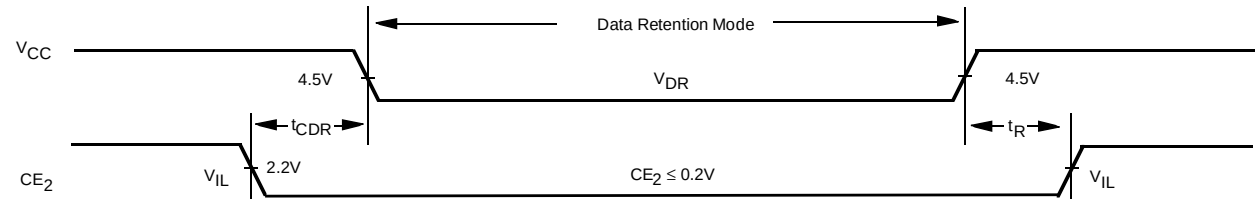
Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CE} \geq V_{CC}$ -0.2V, $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	2.0	3.6	V
I_{CCDR} (1)	Data Retention Current	V_{DR} = 2.0V		600	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operating Recovery Time		t_{RC} (2)		ns

1. $\overline{CE}_1 \geq V_{DR}$ -0.2V, $CE_2 \geq V_{DR}$ -0.2V or $CE_2 \leq 0.2V$; or $\overline{CE}_1 \leq 0.2V$, $CE_2 \leq 0.2V$; $V_{IN} \geq V_{DR}$ -0.2V or $V_{IN} \leq 0.2V$
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE}_1$ CONTROLLED)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE_2 CONTROLLED)



PACKAGE SUFFIX

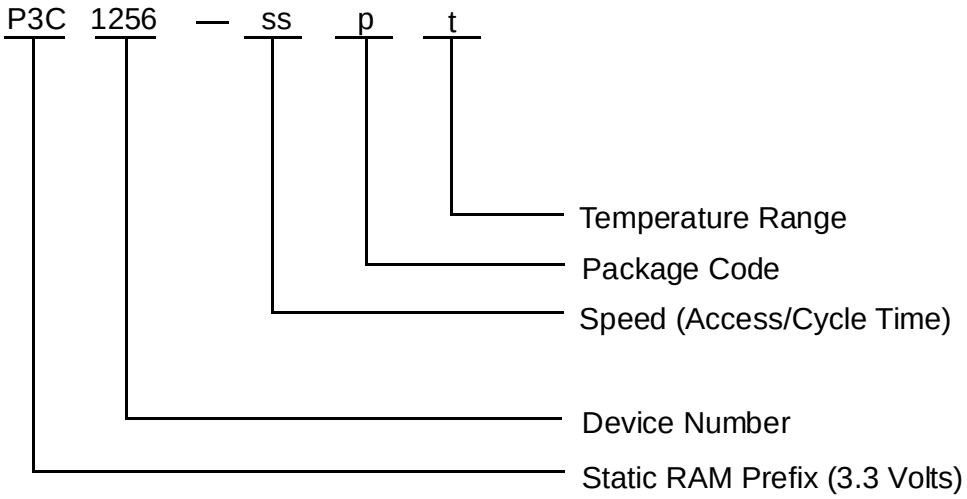
Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
I	Industrial Temperature Range, –40˚C to +85˚C.

ORDERING INFORMATION

Performance Semiconductor's part numbering scheme is as follows:



ss = Speed (access/cycle time in ns), e.g., 12, 15.
p = Package code, i.e., P, J.
t = Temperature range, i.e. C, I.

SELECTION GUIDE

The P3C1256 is available in the following temperature, speed and package options.

Temperature Range	Package \ Speed	12	15	20	25
Commercial	Plastic DIP	-12PC	-15PC	-20PC	-25PC
	Plastic SOJ	-12JC	-15JC	-20JC	-25JC
Industrial	Plastic DIP	N/A	-15PI	-20PI	-25PI
	Plastic SOJ	N/A	-15JI	-20JI	-25JI

N/A = Not Available