PI74FCT399T

Fast CMOS Quad Dual-Port Register

Product Features:

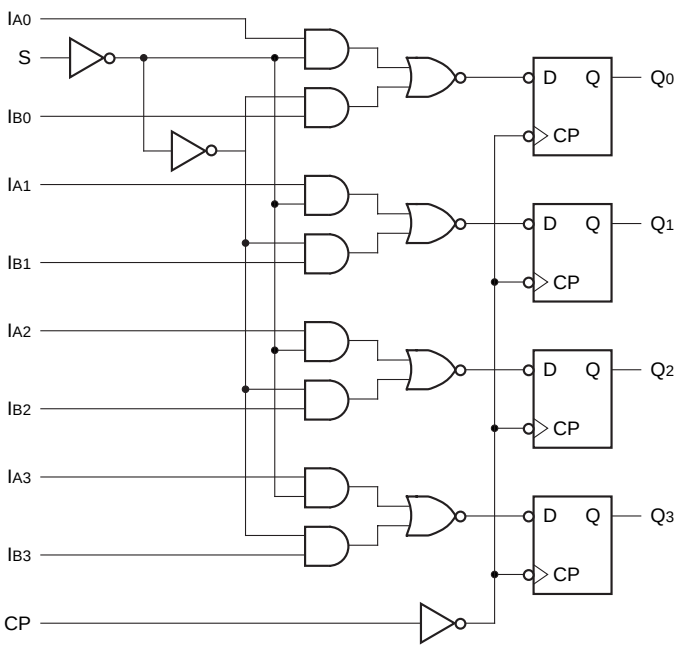
- PI74FCT399T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 16-pin 300 mil wide plastic DIP (P)
  – 16-pin 150 mil wide plastic QSOP (Q)
  – 16-pin 300 mil wide plastic SOIC (S)
  – 16-pin 150 mil wide plastic SOIC (W)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

These high-speed quad dual-port registers select 4-bit wide data from one of the two sources (Ports) under control of a common Select input (S). Synchronous with the LOW-to-HIGH transition of the Clock input (CP), the selected data is transferred to a 4-bit output register. The 4-bit D-type output register is fully edge-triggered. For predictable operation, the Data inputs (I_{AX}, I_{BX}) and Select input (S) must be stable one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input.

Logic Block Diagram



Product Pin Description

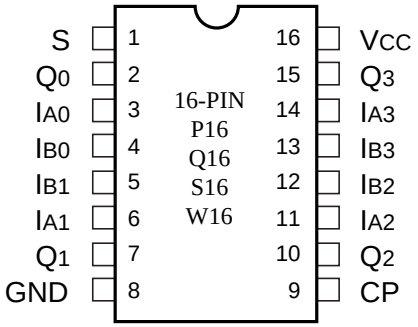
Pin Name	Description
S	Common Select Input
CP	Clock Pulse Input
IA0-IA3	Data Inputs from Source A
IB0-IB3	Data Inputs from Source B
Q0-Q3	Register True Outputs
GND	Ground
V_{CC}	Power

Truth Table[1]

Inputs			Outputs
S	I_A	I_B	Q
I	I	X	L
I	h	X	H
h	X	I	L
h	X	h	H

1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   X = Don't Care

Product Pin Configuration



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open S = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz, 50% Duty Cycle S = GND 50% Duty Cycle One Bit toggling at f_I = 5 MHz	V_{IN} = V_{CC} V_{IN} = GND		1.5	3.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		2.0	5.5[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz, 50% Duty Cycle S = GND Eight Bits toggling at f_I = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND		5.0	12.3[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I (All currents are in milliamps and all frequencies are in megahertz.)

Switching Characteristics over Operating Range

			399T		399AT		399CT		
			Com.		Com.		Com.		
Parameters	Description	Conditions[1]	Min	Max	Min	Max	Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to Q	C_L = 50 pF R_L = 500Ω	3.0	10.0	2.5	7.0	2.5	5.6	ns
t_{SU}	Setup Time, HIGH or LOW D to Q		4.0	—	3.5	—	3.0	—	ns
t_H	Hold Time, HIGH or LOW D to Q		1.0	—	1.0	—	1.0	—	ns
t_{SU}	Setup Time HIGH or LOW S to CP		9.0	—	8.5	—	3.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		5.0	—	5.0	—	4.0	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.