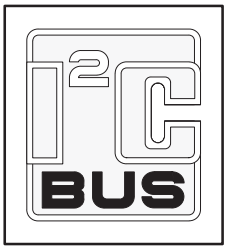
DATA SHEET



PCKV856

70–170 MHz I^2C differential 1:10 clock driver

Preliminary specification

2000 Sep 06

Philips
Semiconductors

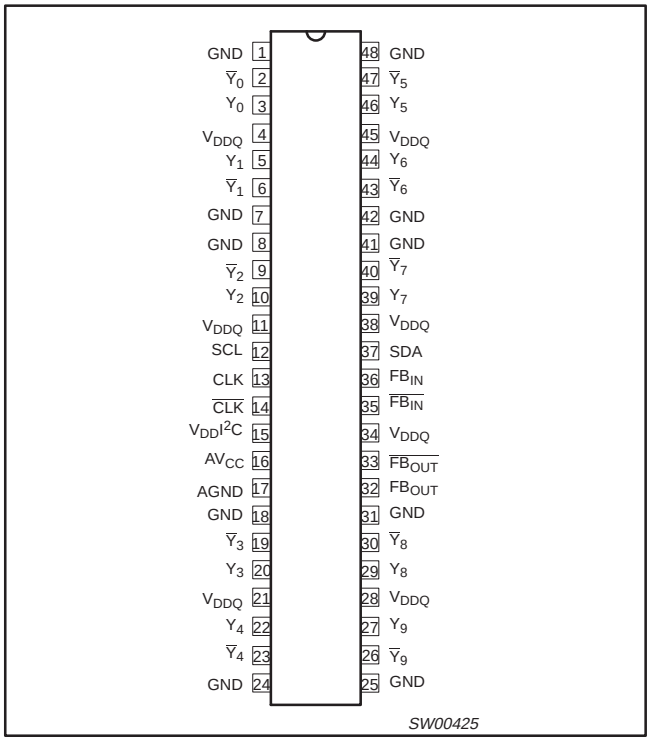
PHILIPS

70–170 MHz I²C differential 1:10 clock driver PCKV856

FEATURES

- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications
- Individual output enable/disable capability via I²C
- Reference inputs selectable between HCSL and SSTL via I²C
- 1-to-10 differential clock distribution
- Very low skew (< 100 ps) and jitter (< 100 ps)
- 2.5 V AV_{CC} and 2.5 V V_{DDQ}
- SSTL_2 interface clock inputs and outputs
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Full DDR solution provided when used with SSTL16877 or SSTV16857
- See PCKV857 for non I²C applications

PIN CONFIGURATION



DESCRIPTION

Zero delay buffer to distribute an SSTL differential clock input pair to 10 SSTL_2 differential output pairs. Outputs are slope controlled. External feedback pin for synchronization of the outputs to the input. A CMOS style Enable/Disable pin is provided for low power disable.

The PCKV856 features I²C compatibility by introduction of SCL (Serial Clock Line) on pin 12 and SDA (Serial Data Line) on pin 37. This provides flexibility in configuring the I/Os of the PCKV856.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0°C to +70°C	PCKV856 DGG	SOT362-1

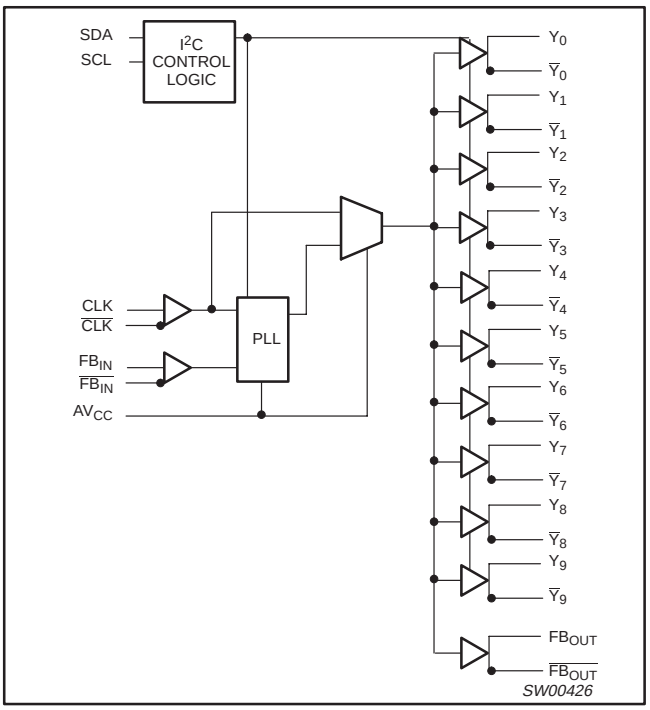
PINS	SYMBOL	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	SSTL_2 ground pins
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47	Y_n, $\overline{Y}_n$, FB_{OUT}, $\overline{FB_{OUT}}$	SSTL_2 differential outputs
4, 11, 21, 28, 34	V_{DDQ}	SSTL_2 power pins
13, 14, 35, 36, 38, 45	CLK_{IN}, $\overline{CLK_{IN}}$, FB_{IN}, $\overline{FB_{IN}}$	SSTL_2 differential inputs
16	AV_{CC}	Analog power
17	AGND	Analog ground
37	SDA	Serial data
12	SCL	Serial clock
15	$V_{DD}I^2C$	I²C power

FUNCTION TABLE

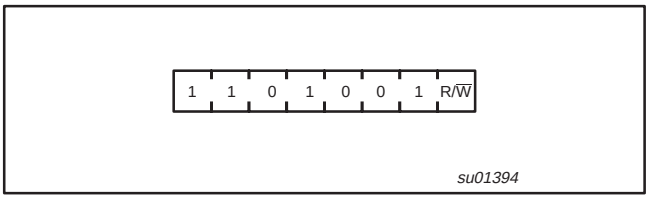
INPUTS			OUTPUTS				PLL ON/OFF
G	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FB_{OUT}	$\overline{FB_{OUT}}$	
L	L	H	Z	Z	Z[1]	Z[1]	OFF
L	H	L	Z	Z	Z[1]	Z[1]	OFF
H	L	H	L	H	L	H	ON
H	H	L	H	L	H	L	ON
X[2]	< 20 MHz	< 20 MHz	Z	Z	Z[1]	Z[1]	OFF

NOTES:
H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
1. Subject to change. May cause conflict with FB_{IN} pins.
2. Additional feature that senses when the clock input is less than 20 MHz and places the part in sleep mode.

BLOCK DIAGRAM



I²C ADDRESS



I²C CONSIDERATIONS

I²C has been chosen as the serial bus interface to control the PCKV856. I²C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I²C devices.

1) Address assignment: The clock driver in this specification uses the single, 7-bit address shown below. All devices can use the address if only one master clock driver is used in a design. The address can be re-used for the CKBF device if no other conflicting I²C clock driver is used in the system.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	1	0	0	1	0

NOTE: The R/$\overline{W}$ bit is used by the I²C controller as a data direction bit. A ‘zero’ indicates a transmission (WRITE) to the clock device. A ‘one’ indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/$\overline{W}$ bit of the address will always be seen as ‘zero’. Optimal address decoding of this bit is left to the vendor.

2) Options: It is our understanding that metal mask options and other pinouts of this type of clock driver will be allowed to use the same address as the original CKBF device. I²C addresses are defined in terms of function (master clock driver) rather than form (pinout, and option).

3) Slave/Receiver: The clock driver is assumed to require only slave/receiver functionality. Slave/transmitter functionality is optional.

4) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

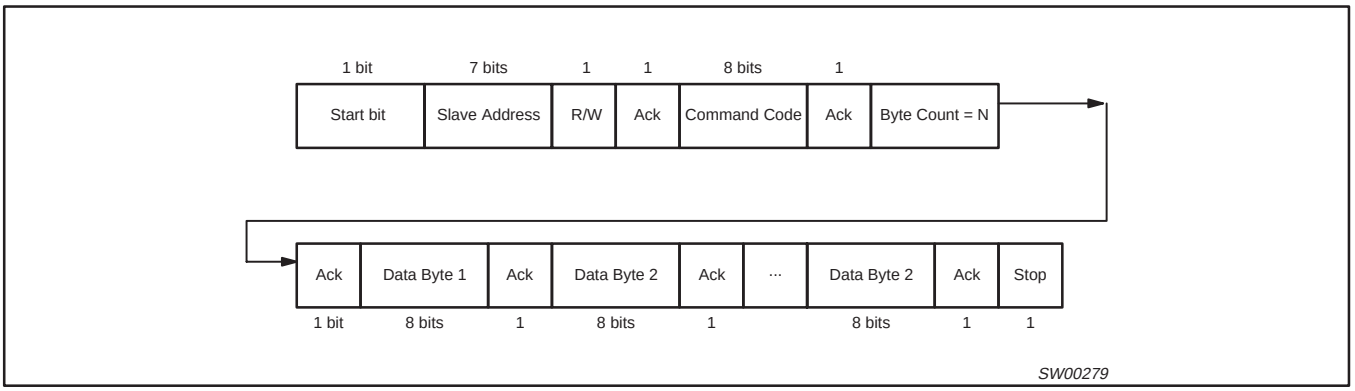
5) Logic Levels: I²C logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

6) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

7) Data Protocol: To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the SMBus controller has a more specific format than the generic I²C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller “writes” to the clock driver and if possible would “read” from the clock driver (the clock driver is a slave/receiver only and is incapable of this transaction.)

“The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes.”



NOTE: The acknowledgement bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required to transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement.

For example:

Byte count byte		Notes:
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte.
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data. (byte 0 then byte 1)
0000	0011	Reads first three bytes (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)
0000	0110	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0000	0111	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle. A clock vendor may choose to discard any number of bytes that exceed the defined byte count.

8) Clock stretching: The clock device must not hold/stretch the SCLOCK or SDATA lines low for more than 10 ms. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

9) General Call: It is assumed that the clock driver will not have to respond to the ‘‘general call.”

10) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I2C specification.

a) Pull-Up Resistors: Any internal resistors pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100 kΩ is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5–6 kΩ range. Assume one I2C device per DIMM (serial presence detect), one I2C controller, one clock driver plus one/two more I2C devices on the platform for capacitive loading purposes.

(b) Input Glitch Filters: Only fast mode I2C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

11) $\overline{\text{PWR DWN}}$: If a clock driver is placed in $\overline{\text{PWR DWN}}$ mode, the SDATA and SCLK inputs must be 3-Stated and the device must retain all programming information. I_{dd} current due to the I2C circuitry must be characterized and in the data sheet.

For specific I2C information consult the Philips I2C Peripherals Data Handbook IC12 (1997).

SERIAL CONFIGURATION MAP

The serial bits will be read by the clock buffer in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 2 – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (Reserved and N/A) should be desined as “Don’t Care”. It is expected that the controller will force all of these bits to a “0” level.

All register bits labeled “Initialize to 0” must be written to zero during intialization. Failure to do so may result in a higher than normal operating current. The controller will read back the last written value.

Byte 0: Active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	INITIAL VALUE	DESCRIPTION
7	2, 3	CLK0_bar, CLK0	1	Enable/Disable Outputs
6	5, 6	CLK1_bar, CLK1	1	Enable/Disable Outputs
5	9, 10	CLK2_bar, CLK2	1	Enable/Disable Outputs
4	19, 20	CLK3_bar, CLK3	1	Enable/Disable Outputs
3	22, 23	CLK4_bar, CLK4	1	Enable/Disable Outputs
2	47, 46	CLK5_bar, CLK5	1	Enable/Disable Outputs
1	44, 43	CLK6_bar, CLK6	1	Enable/Disable Outputs
0	40, 39	CLK7_bar, CLK7	1	Enable/Disable Outputs

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 1: Active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	INITIAL VALUE	DESCRIPTION
7	30, 29	CLK8_bar, CLK8	1	Enable/Disable Outputs
6	27, 26	CLK9_bar, CLK9	1	Enable/Disable Outputs
5	—	—	0	Reserved
4	—	—	0	Reserved
3	—	—	0	Reserved
2	—	—	0	Reserved
1	—	—	0	Reserved
0	—	—	0	ACSL Enable/SSTL_2 Enable

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
AV_{CC}	Analog supply voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O supply voltage		2.3	2.5	2.7	V
V_{IL}	Input low voltage		–0.3		V_{ref} –0.35	V
V_{IH}	Input high voltage		V_{ref} + 0.35		V_{DDQ} + 0.3	V
V_{OL}	Output low voltage[1]		0		0.5	V
V_{OH}	Output high voltage[1]		2		V_{DDQ}	V

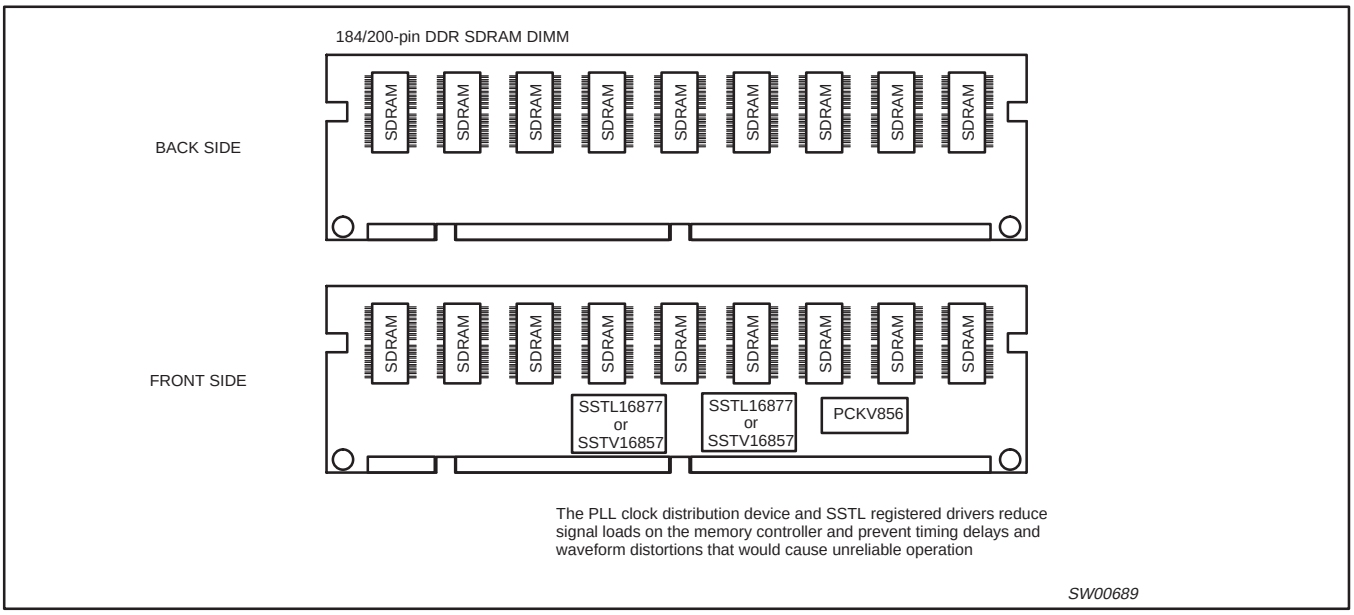
NOTE:
1. This is intended to operate in the SSTL_2 type IV unterminated mode without series resistors on the outputs.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ kΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
f_{CK}	Clock frequency			90	166	195	MHz
$f_{PHASERROR}$	Phase error			–150	0	150	ps
f_{SK}	Output clock skew					200	ps
$fdif_{SK}$	Differential clock skew					100	ps
f_{SL}	Output clock skew			1	1.5		V/ns
$Jitter_{pp}$	Peak-to-Peak jitter (long term)			–100		100	ps
$Jitter_{cc}$	Cycle-to-cycle jitter (short term)			> –100		< 100	ps
O/P impedance	Inherent series resistance				25		Ω
f_{DC}	Duty cycle			45		55	%
C_{in}	Input capacitance			2.5		4	pF
Sync time						100	µs

NOTE:
1. Rise and fall.


184/200-pin DDR SDRAM DIMM
BACK SIDE
FRONT SIDE
SDRAM
SSTL16877 or SSTV16857
SSTL16877 or SSTV16857
PCKV856
The PLL clock distribution device and SSTL registered drivers reduce signal loads on the memory controller and prevent timing delays and waveform distortions that would cause unreliable operation
SW00689

AC WAVEFORMS

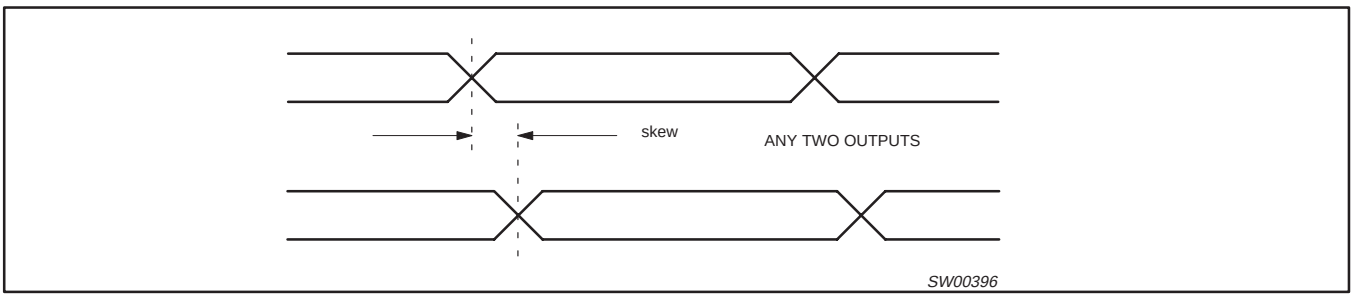


Figure 1. Skew between any two outputs.

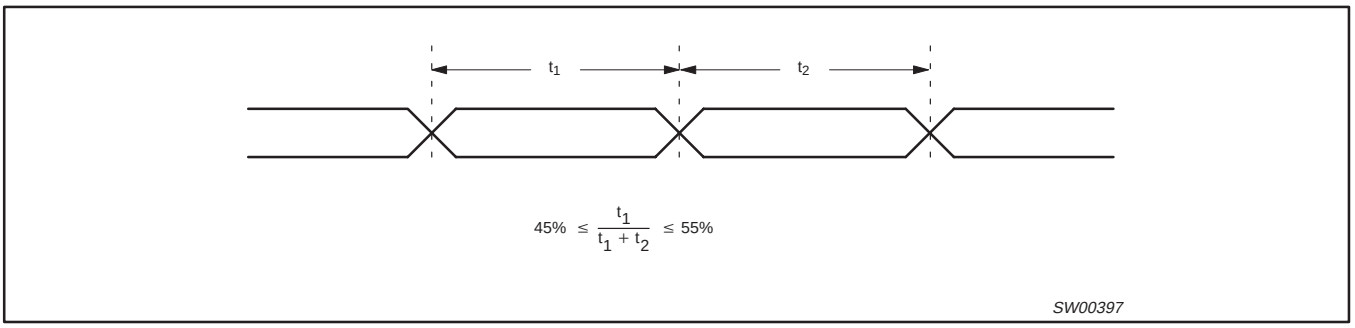


Figure 2. Duty cycle limits and measurement

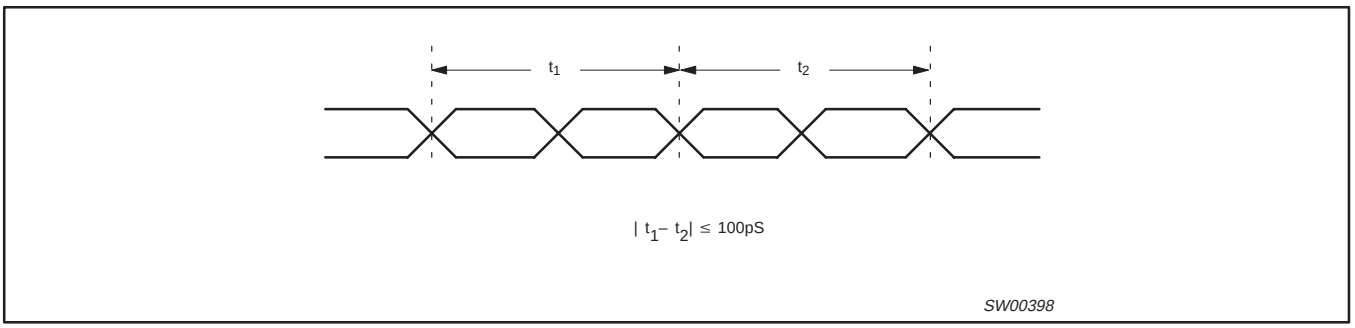
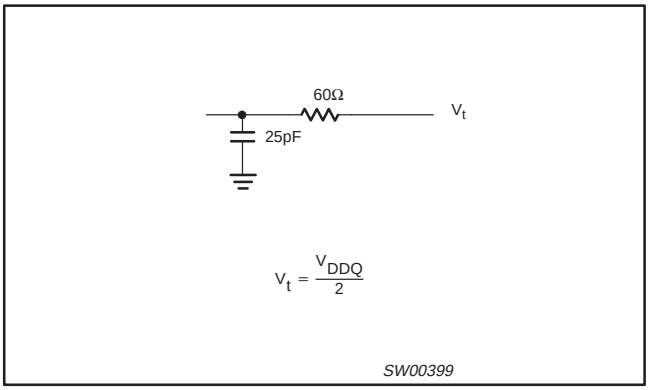
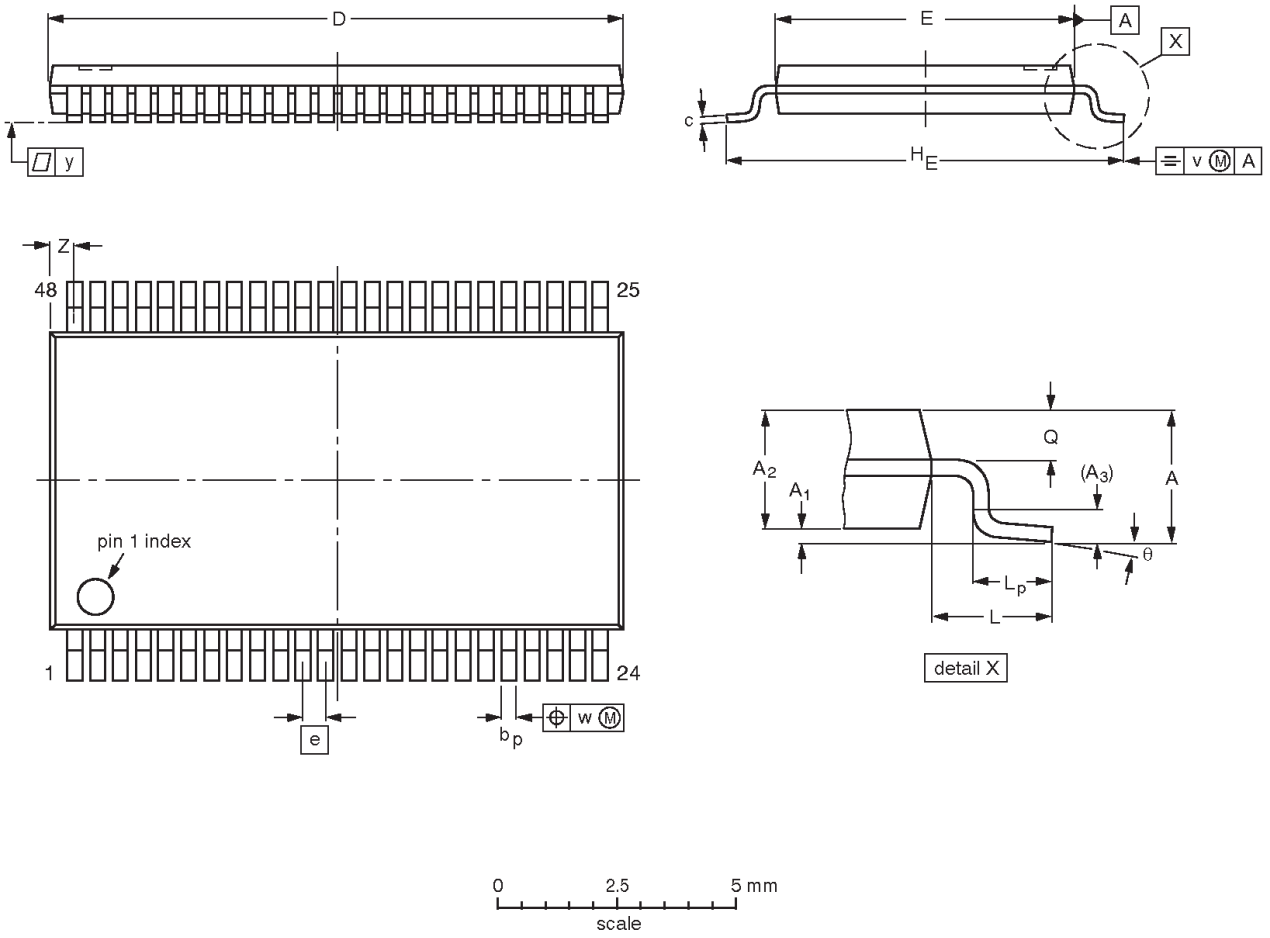


Figure 3. Jitter limit and measurement

TEST CIRCUIT



TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

NOTES

70–170 MHz I²C differential 1:10 clock driver PCKV856

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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