FAST / TTL Buffered I/O 4-Bit Programmable Delay Modules

Electrical Specifications at 25°C

4-Bit FAST Part Number	Delay per Step (ns)	Error ref. to 0000 (ns)	Initial Delay (ns)	Referenced to "0000" - Delay (ns) per Program Setting (P4*P3*P2*P1)															
			0000	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
PLDM8-0.5	0.5 ± .25	± 0.8	8 ± 1	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5
PLDM8-1	1.0 ± 0.5	± 1.0	8 ± 1	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0	14.0	15.0
PLDM8-1.5	1.5 ± 0.6	± 1.5	8 ± 1	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5	12.0	13.5	15.0	16.5	18.0	19.5	21.0	22.5
PLDM8-2	2.0 ± 0.7	± 1.5	8 ± 1	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0	16.0	18.0	20.0	22.0	24.0	26.0	28.0	30.0
PLDM8-2.5	2.5 ± 0.7	± 1.5	8 ± 1	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5	20.0	22.5	25.0	27.5	30.0	32.5	35.0	37.5
PLDM8-3	3.0 ± 0.7	± 2.0	8 ± 1	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0	24.0	27.0	30.0	33.0	36.0	39.0	42.0	45.0
PLDM8-3.5	3.5 ± 0.7	± 2.5	8 ± 1	0.0	3.5	7.0	10.5	14.0	17.5	21.0	24.5	28.0	31.5	35.0	38.5	42.0	45.5	49.0	52.5
PLDM8-4	4.0 ± 0.8	± 3.0	8 ± 1	0.0	4.0	8.0	12.0	16.0	20.0	24.0	28.0	32.0	36.0	40.0	44.0	48.0	52.0	56.0	60.0
PLDM8-4.5	4.5 ± 0.8	± 3.0	8 ± 1	0.0	4.5	9.0	13.5	18.0	22.5	27.0	31.5	36.0	40.5	45.0	49.5	54.0	58.5	63.0	67.5
PLDM8-5	5.0 ± 1.0	± 3.0	8 ± 1	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0	40.0	45.0	50.0	55.0	60.0	65.0	70.0	75.0
PLDM8-10	10 ± 1.5	± 5.0	8 ± 1	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.	110.0	120.0	130.0	140.0	150.0

Electrical Specifications at 25°C

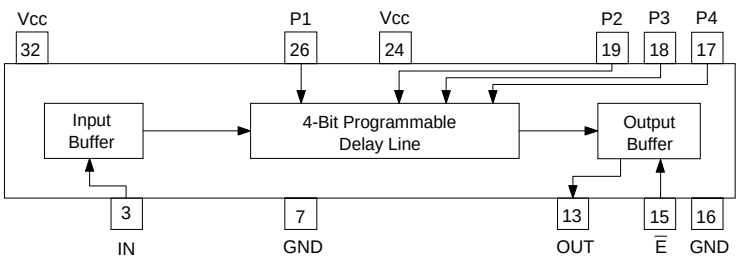
4-Bit TTL Part Number	Delay per Step (ns)	Error ref. to 0000 (ns)	Initial Delay (ns)	Referenced to "0000" - Delay (ns) per Program Setting (P4*P3*P2*P1)															
			0000	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
PLDM15-1	1.0 ± 0.5	± 1.0	15 ± 1	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0	14.0	15.0
PLDM15-2	2.0 ± 0.7	± 1.5	15 ± 1	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0	16.0	18.0	20.0	22.0	24.0	26.0	28.0	30.0
PLDM15-5	5.0 ± 1.0	± 3.0	15 ± 1	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0	40.0	45.0	50.0	55.0	60.0	65.0	70.0	75.0
PLDM15-10	10 ± 1.5	± 5.0	15 ± 1	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.	110.0	120.0	130.0	140.0	150.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays Referenced to Initial Delay, Setting "0000." For example, the setting "1111" delay of PLDM15-1 is 15.0 ± 1.0 referenced to "0000," and 30.0 ± 2.0 referenced to the input.

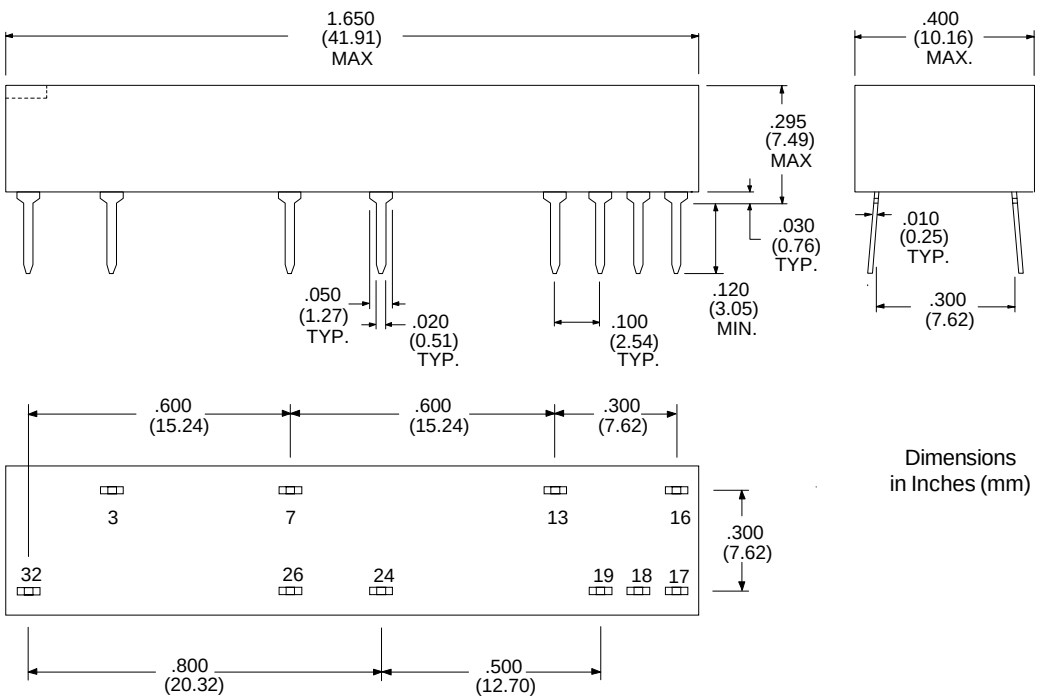
GENERAL: For Operating Specifications and Test Conditions, see Tables I and VI on page 5 of this catalog. Delays specified for the Leading Edge. Buffered input and output.

Operating Temp. Range ..... 0°C to +70°C
Temperature Coefficient ..... ≤ 500ppm/°C typical
Minimum Input Pulse Width ..... 40% max. Delay
Supply Current, I_{CC} ..... 90 mA typ., 105 mA max

FAST / TTL 4-Bit Schematic



ENABLE input (Pin 15) is active low. Output will be disabled (remain low) when " $\overline{E}$ " is high.



Dimensions in Inches (mm)

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

PLDM 1/98

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