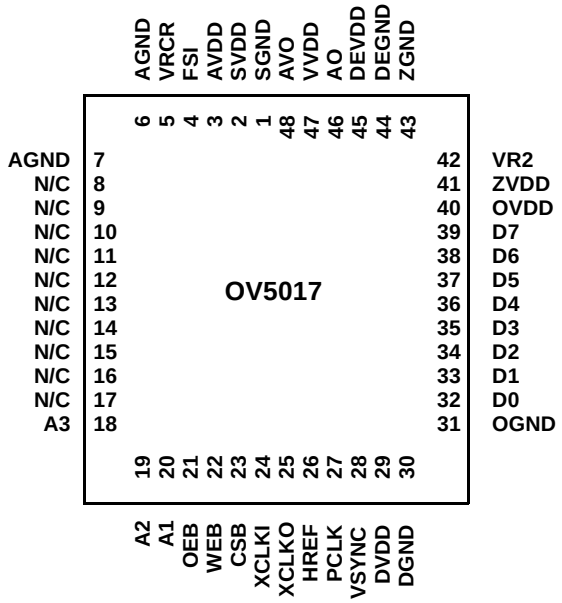
Features

- **Single chip 1/4” video image sensor**
- **Progressive scan**
- **Built-in analog-to-digital (A/D) 8-bit pixel resolution**
- **Programmable features**
- **Frame rate of 50 ~ 0.5 frames per second (fps)**
- **Exposure setting: 1 frame ~ 1/100 frame**
- **Image size: 4.2 mm x 3.2 mm**
- **AGC (auto gain control): 0 ~ 18 dB**
- **Gamma correction: 0.45/1.0**
- **Pixel elements - 384 x 288**
- **Pixel dimension of 11 um x 11 um**
- **External frame sync capability**
- **Signal-to-noise (S/N) ratio > 42 dB**
- **Minimum illumination of 0.5 lux at f1.4 at 50 fps**
- **Single 5-volt supply operation for analog and 5/3.3 volts for digital**
- **Power consumption**
  - — Active: less than 100 mW at 50 fps
  - — Standby: less than 100 µA
- **48-pin package**

Overview

The OV5017 is a black and white digital camera chip that uses OmniVision’s CMOS image core technology. Combining the CMOS sensor technology and an easy to use digital interface, the OV5017 offers a low cost solution for high-quality video image applications.

The digital video port supplies a continuous byte-wide image data. On-chip programmable features include variable frame rate, exposure setting, and image size. All the camera features are register based, accessing the video data and configuring the chip is as easy as read/write of a static memory.



OV5017 PIN ASSIGNMENTS

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The Image Core is a complete analog video camera with 384 x 288 pixel size, which can run at full video speed. The analog video signal complies with CCIR standards. At 50 fps, it may be too fast for many applications; therefore, the frame rate or pixel rate can be programmed to match the external system requirements. The on-chip 8-bit A/D can convert the video signal at 50 fps, and the conversion is synchronized with the actual pixel rate.

The OV5017 also outputs standard timing reference signals such as VSYNC, HREF, PCLK. Databus is shared by negating OEB.

The exposure control can be set to auto or manual operation. Automatic exposure computation is based on full size image array and an exposure range over 100X. The AGC operation is tied to AEC in auto operation. Therefore, use automatic exposure control when selecting full image size. Manual exposure control allows individually adjusting exposure and gain based on actual application. Therefore, use manual exposure time if the window is smaller than full size or if the target object is brighter or darker than the average background.

The frame rate divider can achieve various frame rates on the fly without changing the input clock frequency.

Single frame operation provides one frame data transfer by controlling the assertion of HREF for one complete frame period. Setting FCTL(7) signals the control to assert the HREF in the next frame. Clearing this bit before the new frame cancels the assertion of HREF.

Table 1. Pin Descriptions

Pin #	Class	Pin Name	Description
1	Bias	SGND	Sensor ground. Connect to supply common.
2	Bias	SVDD	Sensor power (+5V) connection.
3	Bias	AVDD	Analog power (+5V) connection.
4	I-0	FSI	External frame sync input. A rising edge on FSI sets the chip vertical sync timing. For proper operation, the frequency of FSI must be half of the programmed frame rate. Internally pulled down with a 100k resistor. Leave open or ground if unused.
5	Bias	VrCR	Internal reference voltage. Requires a 0.1uF external capacitor to AGND.
6	Bias	AGND	Analog ground. Connect to supply common.
7	Bias	AGND	Analog ground. Connect to supply common.
8-17	FT	N/C	Factory test. Leave open.
18, 19, 20, 46	I	A3-A0	Address inputs for internal the registers. Requires CSB = 0 to access the registers.
21	I	OEB	Output enable for the eight bit data bus. OEB = 0 enables the data bus drivers. OEB = 1 puts the data bus in tristate.

Table 1. Pin Descriptions (Continued)

Pin #	Class	Pin Name	Description
22	I	WEB	Write enable input for the internal registers. When the chip is selected (CSB = 0), external data is latched into the registers with the rising edge of WEB.
23	I	CSB	Chip select for the device. CSB = 0 selects the device.
24, 25	OD	XCLKI, XCLKO	Crystal oscillator in/out pins. Nominal clock frequency is 14.31MHz for CCIR 50 Hz timing. The maximum pixel rate is limited to one half of the clock frequency. To connect an external clock to XCLKI, leave XCLKO open.
26	OD	HREF	Horizontal timing reference output. Asserted high during every valid line for the duration of the valid window width. The window sizing function affects the number of valid lines in a frame as well as the number of valid pixels in a line. HREF and status(1), are identical valid pixel timing information.
27	OD	PCLK	Pixel clock output. Defaulted to be a continuous clock. Can be programmed via the internal register to be on during the valid pixel window only. Video data at output bus (D0-D7) is updated with the rising edge of PCLK and is guaranteed to be valid at the falling edge of PCLK.
28	OD	VSYNC	Vertical timing reference output. It is high once per frame for the duration of the vertical sync period. VSYNC and status (2) are identical vertical sync timing information.
29	Bias	DVDD	Digital power (+5V) connection.
30	Bias	DGND	Digital ground. Connect to supply common
31	Bias	OGND	Digital output ground. Connect to supply common
32-39	OD	D0-D7	Bi-directional data bus for video output data and internal register read/write operations.
40	Bias	OVDD	Digital output power (+5V/+3.3V) connection.
41	Bias	ZVDD	Analog power (+5V) connection.
42	Bias	VR2	Internal reference voltage. Requires a 0.1uF external capacitor to AGND.
43	Bias	ZGND	Analog ground. Connect to supply common.
44	Bias	DEGND	Decoder ground. Connect to supply common.
45	Bias	DEVDD	Decoder power (+5V) connection.
47	Bias	VVDD	Video output power (+5V) connection.
48	Q	AVO	Composite video output. It is capable of driving 150 Ω load, Vp-p is 2.0 V.

Pin Type and Default Level:
I: digital input, floating, I-1: digital input, with 100k pull up, I-0: digital input, with 100k pull down, OD: digital CMOS level output, OA: analog CMOS, level output, XI/XO: xtal IO, K: analog input, Q: 75Ω output, FT: factory test, Bias: power supply bias

1. Video Data Bus

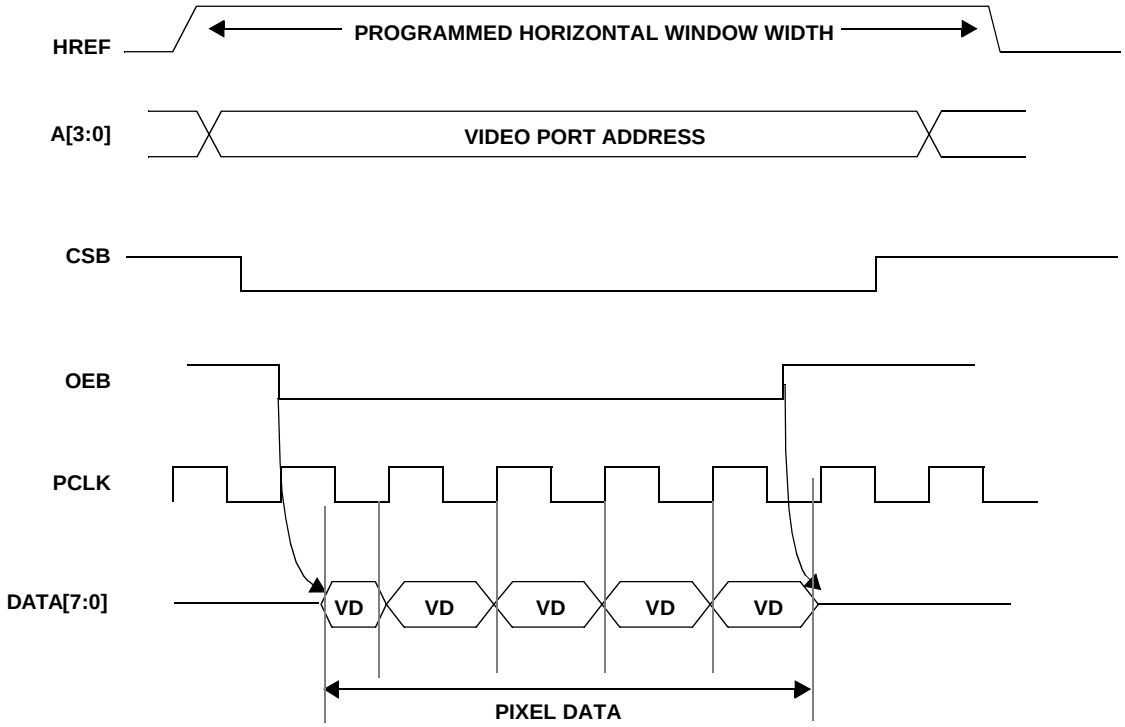


Figure 1. Video Data Timing Showing Continuous Pixel Reading

The eight bit video data from the A/D converter is synchronous to PCLK. The lowest level is ‘h00’ and the highest is ‘hff’, no reserved code for blanking or sync.

PCLK is the pixel clock that is either continuously on or present only during valid pixel window. If the continuous clock is used, HREF is often used to qualify the pixel data. HREF is asserted during the programmed horizontal and vertical window region. Video data is updated at the rising edge of PCLK and can be latched at the falling edge of PCLK.

As shown in Figure 1, reading of the video data is not different from reading other on-chip registers, it requires the assertion of OEB and CSB and the correct address. To maintain uninterrupted video data stream, OV5017 video data will be updated at each pixel clock as long as the OEB, CSB, and correct address are asserted as shown in Figure 1.

Since the video data is continuous during the active window, to prevent new data overruns the previous one, the host has to make sure at least one video data is read in every pixel clock period. The status register bit RDY and OV allows host to perform polling and error detection.

1.1 Register Control

The register read/write is the same as normal memory access, using pins DATA[7:0], A[3:0], WEB, OEB, and CSB. As shown in Figure 2 and Figure 3, the read cycle can be chip select controlled or address controlled. The write cycle also can be chip select controlled or write enable controlled. The memory cycle is fully asynchronous to the frame or pixel timing. Write cycle affects only the registers which are writable, it does not affect read only registers such as video port status register. Since writing to certain

registers affects the basic camera operation, care must be taken when write occurs during the middle of active window. These effects are described in the individual register section. As a guide line, registers affects the frame rate, exposure time, window size, are better updated during the vertical sync

.

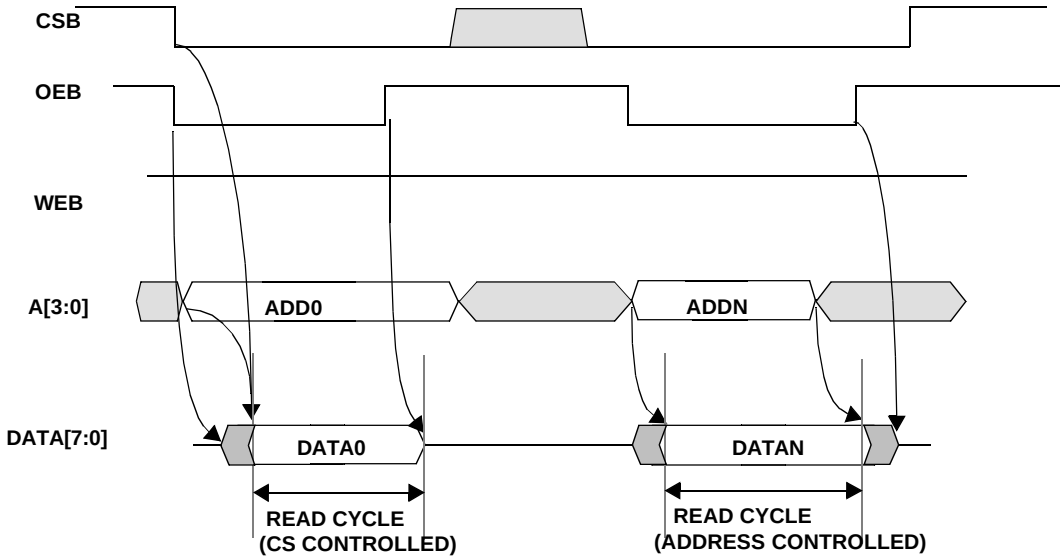


Figure 2. Register Access Showing a Single Byte Read

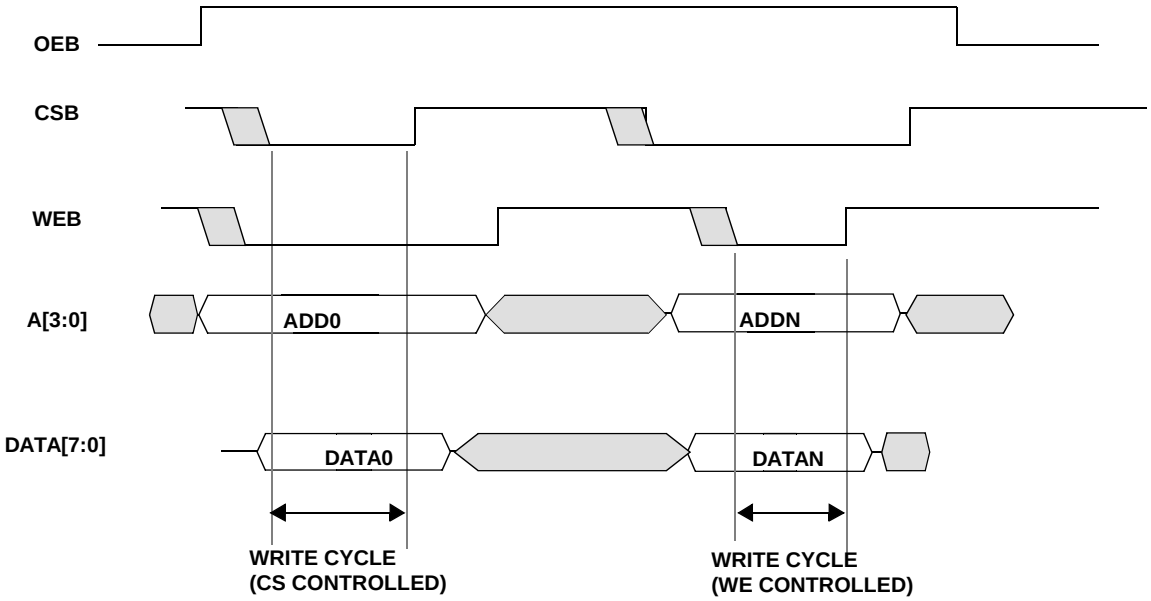


Figure 3. Register Access Showing Single Byte Write

2. Registers

Table 2. Register Sets

A[3:0]	Register Name	R/W	Bit Name	Function	Default Value
10xx	VPORT	R	VD[7:0]	Video data	xxxxxxxx
0000	STATUS	R	TO2,TO1, , ,OV, VSYNC, HREF, RDY	Status register	00xxxxxx
0001	FCTL	W	SFR, FSET, , , SKIP, FBLC, STOP, SRST	Single frame flow control system control	00xx0000
0010	EXCTL	R/W	AUTO, EX[6:0]	Auto or manual exposure value	11111111
0011	GCTL	R/W	GN[2:0]	Gain value	xxxxx000
0100	FRCTL	R/W	FDIV[5:0]	Frame rate divider	xx000000
0101	MCTL	R/W	GAMMA, MIR, DN, BKL, FZEX, PCKS, PCKI, BPSHP	Miscellaneous controls	00000000
0110	HWCTL	R/W	HWS[3:0], HWE[3:0]	Window control	00000000
0111	VWCTL	R/W	VWS[3:0], VWE[3:0]	Window control	00000000
1110	TST	W	TST[7:0]	Reserved for test	xxxxxxxx
1111	TOPT	W	TOPT[7:0]	Reserved for test	xxxxxxxx

Note: Unimplemented bits in all the R/W registers return “0” in the read cycle, no effect in the write cycle.

2.1 Detailed Register Descriptions

The following table describes the function of each bit within a register:

Table 3. Bit descriptions

Register Name	Bit name	Range	Function
VPORT	VD	VD[7:0]	This register selects the video data port. The video data is not latched in this VPORT, as long as VPORT remains selected. The video data is updated as new pixel signals are converted.
STATUS	TO2	STA7	Reserved bit.

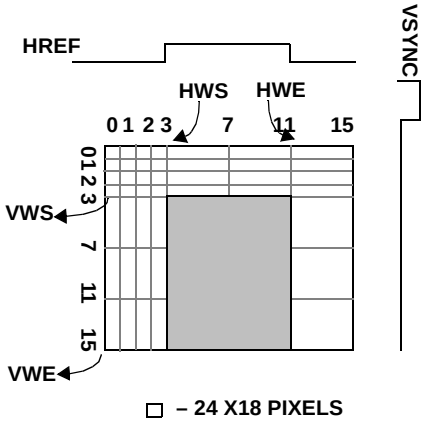
Table 3. Bit descriptions (Continued)

Register Name	Bit name	Range	Function
	TO1	STA6	Reserved bit.
	OV	STA3	Pixel data overrun flag. It is set each time pixel data is updated if STA0 has been set already. Reading of this register clears the bit.
	VSYNC	STA2	This bit duplicates the signal at pin VSYNC.
	HREF	STA1	This bit duplicates the signal at pin HREF.
	RDY	STA0	This bit is set each time pixel data is updated, and is cleared by reading the VPORT register. This bit will not be set if the VPORT register is being read while pixel data is updating.
FCTL	FSET	FCTL[7]	Set to initiate single frame transfer. This bit works only if FCTL[6] is also set. If this bit is set in the middle of a frame, HREF will not be asserted until the next new frame. This bit is cleared automatically at the end of the new frame so that it can be set again.
	SFR	FCTL[6]	Set to enable single frame operation mode. Since the video data is a continuous non-stop byte stream, the validity of the data is qualified only by assertion of HREF. In a continuous frame operation, HREF is asserted in every frame. In a single frame operation, HREF is asserted only for the first frame immediately after setting the FCTL[7]. The actual duration of HREF assertion is programmed by the window size.
	SKIP	FCTL[3]	Makes VSYNC and HREF to skip every other frame. This function does not alter the pixel rate; it simply blocks their assertion in every other frame.
	FBLC	FCTL[2]	Chooses how frequent the black level calibration is performed internally. It is set once every frame and cleared once every line. Line BLC can set the BLC within a fraction of a frame time. This is useful to speed up BLC process after power up or activation after standby mode. However, frame BLC provides better image stability.
	STOP	FCTL[1]	Set to stop chip clock and enter low power standby mode. This function does not alter register content. The chip is put in default state and all image data is lost. Setting this bit does not prevent further register access. Upon clearing this bit, it generally takes about two frames for the chip to become stable.
	SRST	FCTL[0]	Software reset enable. Setting this bit resets all the on-chip registers and puts the chip in default state. Upon clearing this bit, it generally takes about two frames for the chip to become stable.

Table 3. Bit descriptions (Continued)

Register Name	Bit name	Range	Function
EXCTL	AUTO	EXCTL[7]	Enables auto exposure. To select auto exposure mode, set this bit. To select manual exposure mode, clear this bit.
	EX	EXCTL[6:0]	Sets the exposure time, where 7fh is the 1/50s, and 00h is the 1/(50*128*2)s. This register is used in manual exposure mode only. After updates are made to this register, it takes two frames for the chip to become stable.
GCTL	GN	GCTL[2:0]	Selects the post amplifier gain, where 111 is the 18dB gain and 000 is the 0dB in a linear relationship. This register is used in manual exposure mode only. After updates are made to this register, it takes two frames for the chip to become stable.
FRCTL	FDIV	FRCTL[5:0]	Divides the frame rate by 1 to 64 in steps of 1 by using this formula: Frame Rate = F_0 / (FDIV+1) Pixel Rate = f_{osc} / [(FDIV +1)*2] where f_{osc} is the main clock frequency of XCLKi $F_0 = f_{osc}$ / (458*625); F_0=50 @ 14.318Mhz After updates are made to this register, it takes two frames for the chip to become stable.
MCTL	GAMA	MCTL[7]	Set this bit to select gamma = 0.45, and clear this bit for gamma = 1.
	MIR	MCTL[6]	Set this bit to select mirror image.
	NSR	MCTL[5]	Set this bit to turn on indoor mode, and clear for outdoor mode.
	BKL	MCTL[4]	Set this bit to turn on backlight compensation.
	FZEX	MCTL[3]	Set this bit to freeze the exposure setting. This works in auto exposure mode; it has no effect in manual exposure mode.
	PCKS	MCTL[2]	Clear this bit to output continuous pixel clock to PCLK; set to output pixel clock only during the valid pixel window
	PCKI	MCTL[1]	Set this bit to inverse the polarity of PCLK.
	BPSHP	MCTL[0]	Set this bit to disable sharpness function.
HWCTL/ VWCTL	HWS	HWCTL[7:4]	Selects the start of the horizontal window.
	HWE	HWCTL[3:0]	Selects the end of the horizontal window.
	VWS	VWCTL[7:4]	Selects the start of the vertical window.
	VWE	VWCTL[3:0]	Selects the end of the vertical window.

Table 3. Bit descriptions (Continued)

Register Name	Bit name	Range	Function
The array is divided into 16x16 blocks as shown in Figure 1.1. each block is H24xV18 pixels. The method for selecting vertical and horizontal window region is the same. Each direction uses an eight-bit register. Bit [7:4] selects the start block location. Bit [3:0] selects the end block location. For example, to select the shaded area as the active region, use HWCTL=4cH,VWCTL=44H. This window selection feature changes only the assertion time of HREF and does not change the pixel rate or the data rate. If the end location is equal to or less than the start location, the window size is from start location to the end of the right most edge.			 **Figure 4. Windowing**

3. Electrical Specifications

This section provides the electrical parameters descriptions and timing diagrams.

3.1 Electrical Parameters

Table 4. Electrical parameters ($0^oC \leq TA \leq 85^oC$, voltages referenced to GND)

Symbol	Descriptions	Max	Type	Min	Units
Supply					
V_{DD1}	Supply voltage (digital/analog: DEVDD, ZVDD, AVDD, SVDD, VVDD, DVDD)	5.25	5.0	4.75	V
V_{DD2}	Supply voltage (OVDD)	5.5 3.6	5.0 3.3	4.5 3.0	V V
I_{DD1}	Supply Current (@ 50fps, 50pf CMOS load on data bus)	40	-	-	mA
I_{DD2}	Standby supply current	100	-	-	uA
Inputs					
V_{IL}	Input voltage LOW	0.8	-	-	V
V_{IH}	Input voltage HIGH	-	-	2.0	V
Cin	Input capacitor	10	-	-	pF
t_r, t_r	Digital input rise/fall time	25	-	-	ns
Outputs - standard load 25pf, 1.2kΩ to 3.0volts					
V_{OH}	Output voltage HIGH	-	-	2.4	V
V_{OL}	Output voltage LOW	0.6	-	-	V
Clock input / Crystal Oscillator					
f_{osc}	Resonator frequency	-	14.31818	-	MHz
	Load capacitor	-	10	-	pF
	Parallel resistance		1M		W
	Clock input rise/fall time	5	-	25	ns
	Duty cycle if external clock input	60		40	%
Video timing					
t_{PCLK}	PCLK cycle time (@ 50Hz fps)	-	-	139	ns
t_{PHD}	PCLK to HREF delay	25	-	-	ns
t_{PDD}	PCLK to DATA delay	25	-	-	ns

Table 4. Electrical parameters ($0^oC \leq TA \leq 85^oC$, voltages referenced to GND) (Continued)

Symbol	Descriptions	Max	Type	Min	Units
Interface timing					
t_{OE}	Output enable access time	15	-	-	ns
t_{OEZ}	Output enable to Z delay	15	-	-	ns
t_{RC}	Register read cycle time	-	-	100	ns
t_{CS}	Chip select pulse width	-	-	50	ns
t_{CSA}	Chip select access time	30			ns
t_{CSX}	Chip select to data invalid time	15			ns
t_{AA}	Address access time	30			ns
t_{AX}	Address data invalid time	15	-		ns
t_{WC}	Register write cycle time	-	-	100	ns
t_{WE}	Write enable pulse width	-	-	50	ns
t_{AS}	Write cycle address set up time	-	-	0	ns
t_{AH}	Write cycle address hold time	-	-	0	ns
t_{DS}	Write cycle data set up time	-	-	20	ns
t_{DH}	Write cycle data hold time	-	-	0	ns
t_{SYNC}	External FSI cycle time	-	2	-	frame
t_{PD}	Chip power up time	100	-	-	us
DIGIAL/Analog video parameters					
AVO	Composite video level (p-p)	-	2.0	-	V
AV_{SYNC}	sync amplitude	0.55	-	0.6	V
Ravo	Output load resistance		150		Ohm
t_H	horizontal line width		458		pclk
t_{HSYNC}	horizontal sync width		32		pclk
t_{HF}	horizontal blank front porch		9		pclk
t_{HB}	horizontal blank back porch		33		pclk
t_{HACT}	active pixel in one scan line		384		pclk

Table 4. Electrical parameters ($0^oC \leq TA \leq 85^oC$, voltages referenced to GND) (Continued)

Symbol	Descriptions	Max	Type	Min	Units
t_{VB1}	field 2 vertica back equaliztion width		-		t_H
t_V	vertical field width		312.5		t_H
t_{VSYNC}	vertical sync width		2.5		t_H
t_{VF1}	field 1 vertical front equlization width		3		t_H
t_{VB1}	field 1 vertica back equaliztion width		19		t_H
t_{VF2}	field 2 vertical front equlization width		2.5		t_H
t_{VB2}	field 2 vertica back equaliztion width		19.5		t_H
t_{VACT}	active line in a field		288		t_H

3.2 Timing diagrams

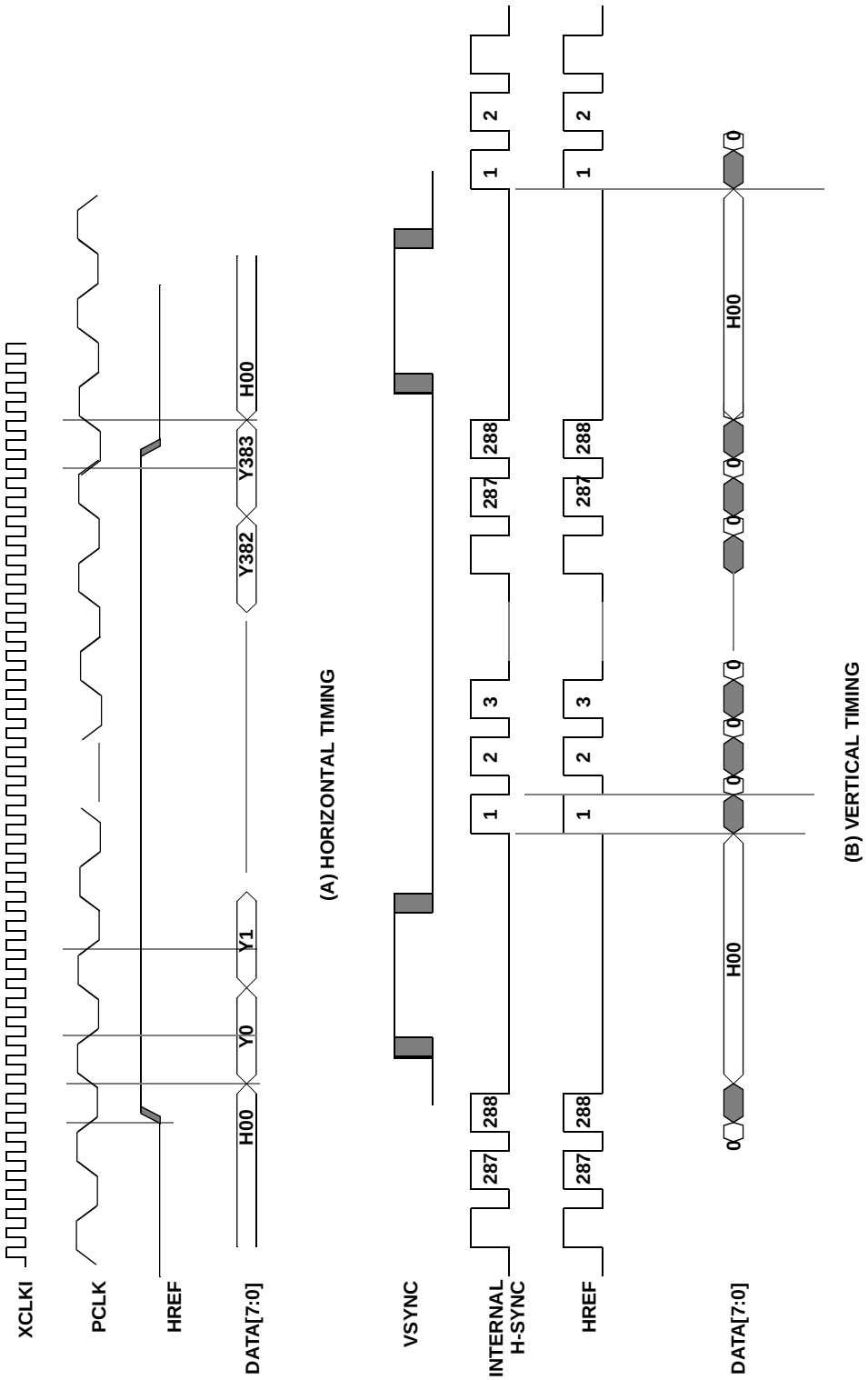


Figure 5. Video Data Timing (384 x 288), PCLK = 1/4 XCLKi

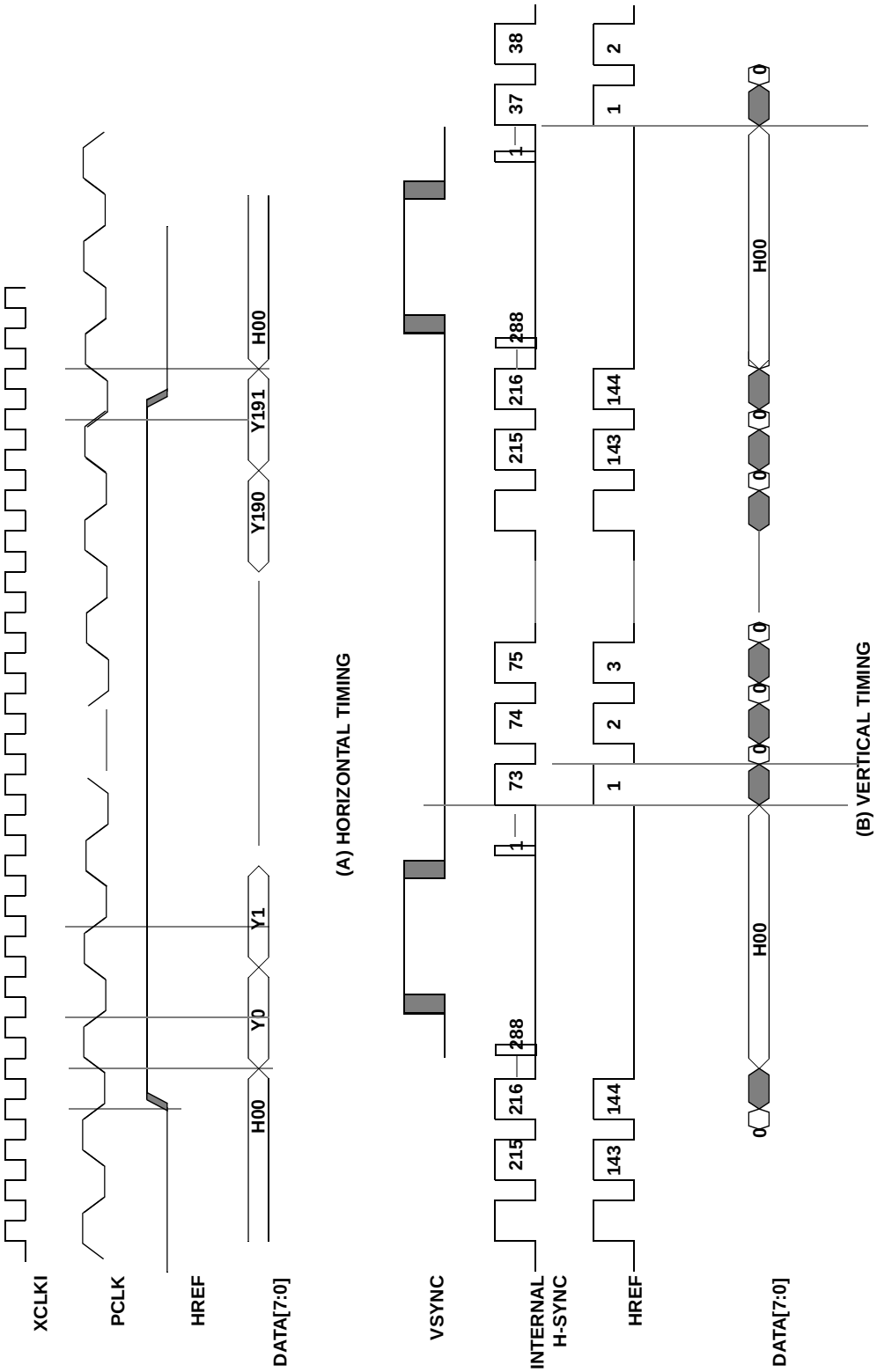


Figure 6. Video Port Timing (192 x 144), PCLK = 1/2 XCLKi

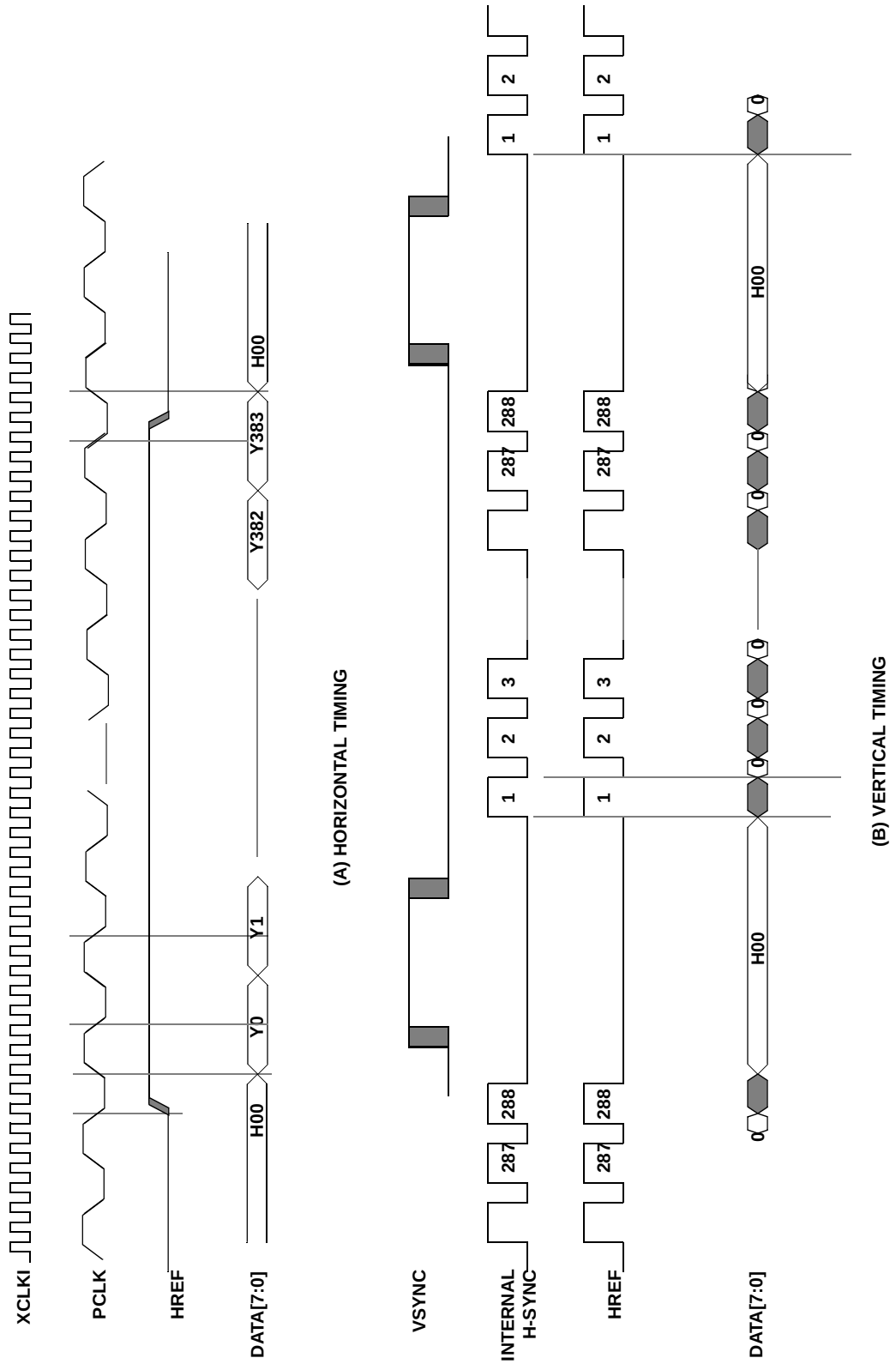

XCLKI
PCLK
HREF
DATA[7:0]
H00
Y383
Y382
Y1
Y0
H00
(A) HORIZONTAL TIMING
VSYNC
INTERNAL H-SYNC
HREF
DATA[7:0]
1
2
3
287
288
0
H00
(B) VERTICAL TIMING

Figure 7. Video Port Timing (384 x 288), PCLK = 1/2 XCLKi

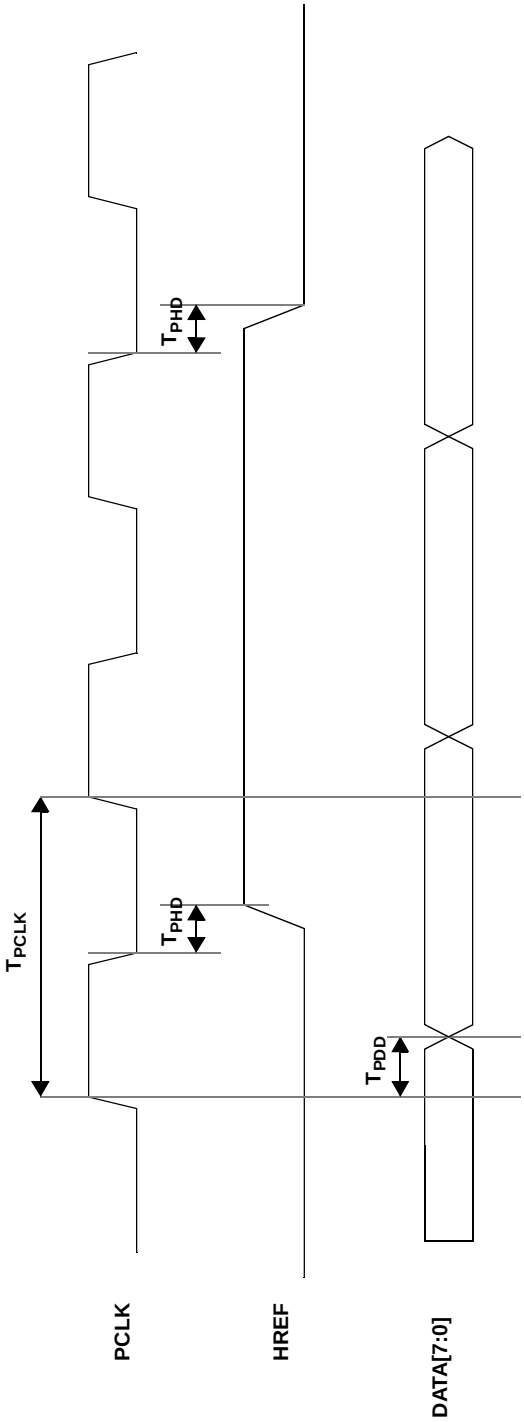


Figure 8. Pixel Timing

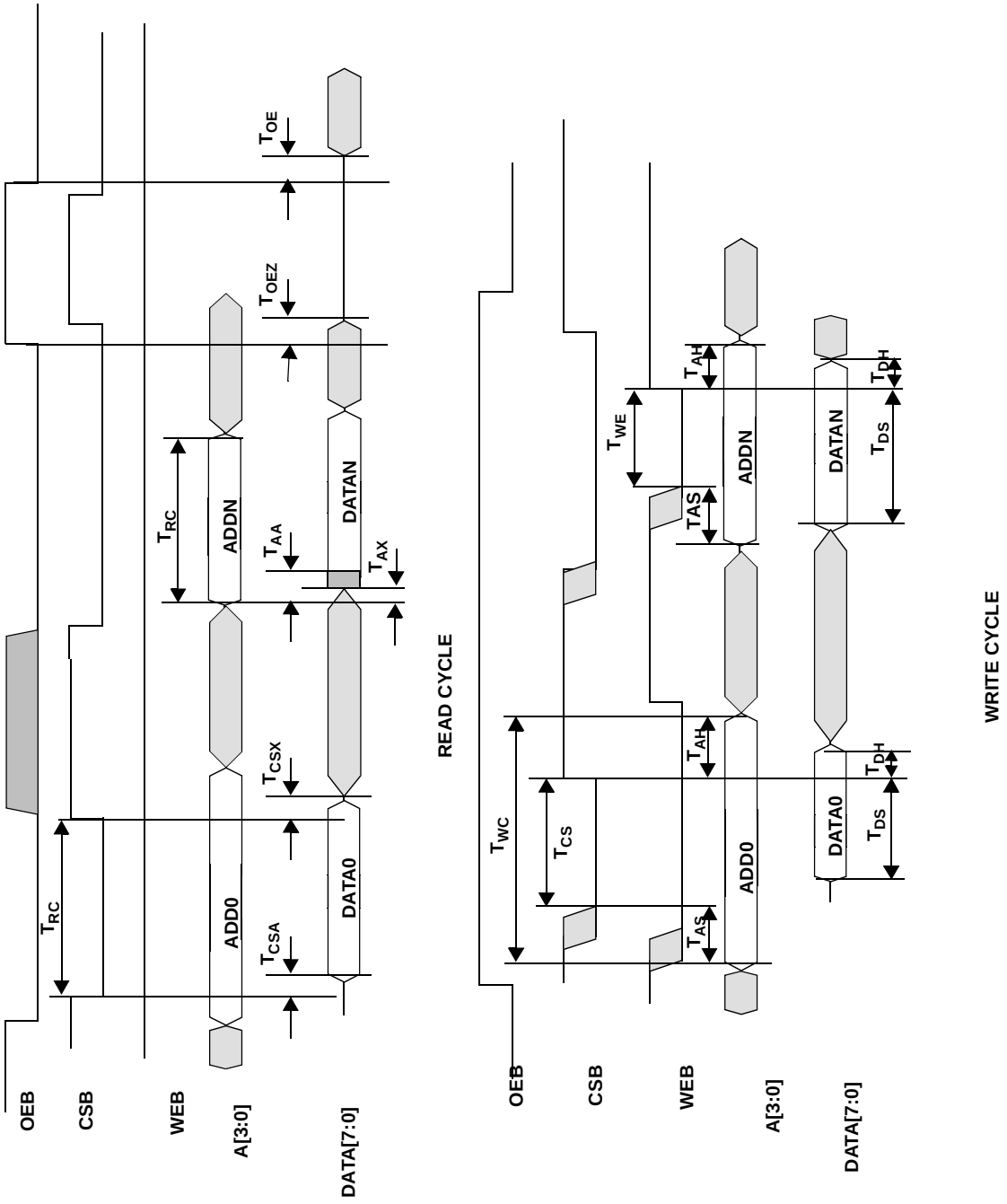


Figure 9. Register R/W Timing

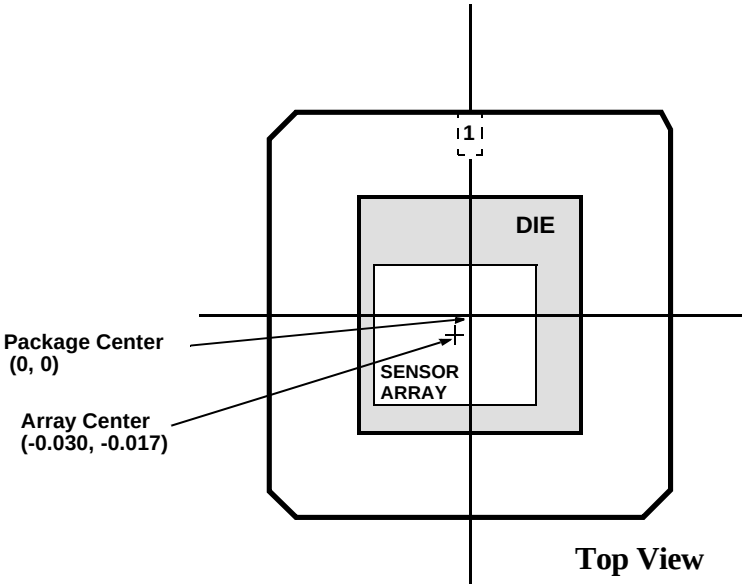


Figure 10. OV5017 Sensor Array Location Dimensions (in inches)

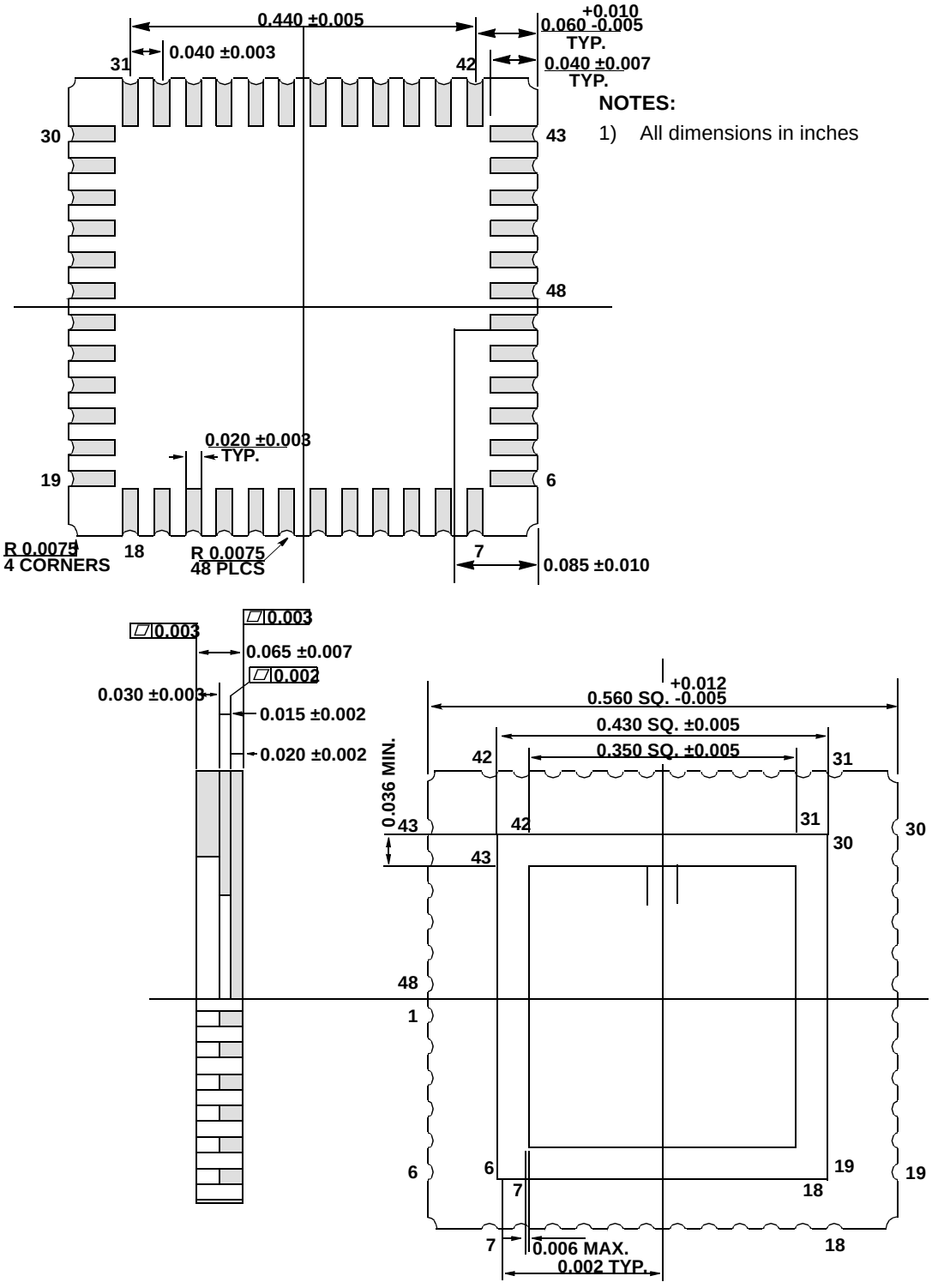


Figure 11. OV5017 Package Outline Dimensions

ERRATA

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1. In default mode, the video data changes on the falling edge of PCLK instead of on the rising edge. We recommand inverting the PCLK pin polarity by setting MCTL(1) so the video data can still be latched on the falling edge of PCLK. All the pclk timing parameters is applied to inverted PCLK.

2. OV5017 default active HREF window width has one extra pixel, 385 instead of 384, the back porch blanking is one less, that is:

   t_{HACT} = 385, t_{HB} = 32.

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3. A glitch (width 1/2 ~ 10 PCLKS) in HREF appears between VSYNC and the first valid HREF if programmed FRCTL(5:0) >= 9.

4. Intensity of lines (32,33,256,257) may be different from the rest of image if programmed FRCTL(5:0)= 4,5,9~11,13~15,17~22,24~63.