AMERICAN MICROSYSTEMS, INC

OP034ID03

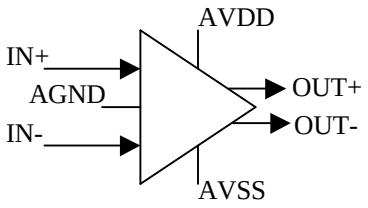
June, 1998 Preliminary

AMI 0.8 micron CMOS
CWL Double Poly

Fully Differential Op Amp

Features

- Settling Time 100us (typ)
- Idd under 1mA



Description

Low power, high-gain fully-differential opamp to be used as a building block in sigma-delta integrators and gain stages with capacitive loads

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
AVDD	Positive Supply	+ 5V Supply
AVSS	Negative Supply	
AGND	Analog Ground	Nominal 2.5 V
In+	Analog Input	Positive Opamp Input
In-	Analog Input	Negative Opamp input
Out +	Analog Output	
Out -	Analog Output	

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
T	Temperature		-40	85	°C
V	Supply Voltage		4.5	5.5	V
IDD	Quiescent Current		320	950	uA
CMErr	Common-Mode Error		-	2.3	mV
SR	Slew-Rate	Cload =4pF	9	28	V/us
Ts	Settling Time	Cload =4pF	60	140	ns
AV0	Openloop DC Gain		94	107	dB
GBW	Gain bandwidth		13	34	MHz
PM	Phase Margin		85	-	degree
PSRRdc	PSRR @DC		162	-	dB
CMIR+	CMIR above AGND	AGND=2.5V	1.9	2.8	V
CMIR-	CMIR below AGND	AGND=2.5V	0.5	1.4	V
Cin	Input Capacitance		-	0.5	pF