OV9630 Color CMOS SXGA (1.3 MPixel) CAMERACHIP™

General Description

The OV9630 CAMERACHIP™ is a low voltage CMOS image sensor that provides the full functionality of a single-chip 1.3 Mega-pixel (MP) SXGA (1280 x 1024) camera and image processor in a small-footprint package. The OV9630 CAMERACHIP provides full-frame, sub-sampled or windowed 10-bit images in a wide range of formats, controlled through OmniVision's Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, white balance and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, blooming, etc., to produce a clean, fully stable color image.

Features

- High sensitivity for low-light operation
- 2.5V/3.3V operating voltage for embedded portable applications
- Standard SCCB CAMERACHIP control interface
- Raw RGB SXGA, VGA (sub-sampled) with complete Windowing control
- Automatic image control functions including Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Brightness Control (ABC), Automatic Band Filter (ABF) for 60 Hz noise and Automatic Black-Level Calibration (ABLC)
- Image quality controls include anti-blooming and zero smearing

Ordering Information

Product	Package
OV09630-C00A (Color)	CLCC-48

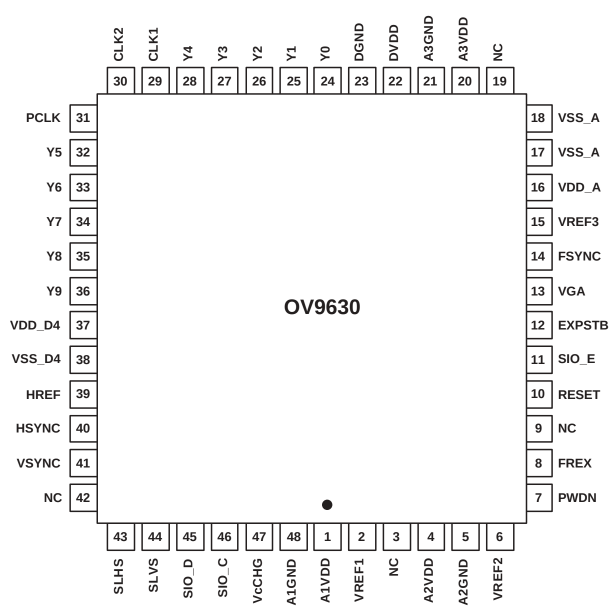
Applications

- Digital still cameras
- Cellular Phones
- Other high-resolution (1280 x 1024) video or snapshot camera applications

Key Specifications

	Array Size	1280 x 1024 (SXGA)
Power Supply	Core	2.5VDC $\pm$ 10%
	Analog	3.3VDC $\pm$ 10%
	I/O	3.3VDC $\pm$ 10%
Power Requirements	Active	150 mW
	Standby	30 µW
Temperature Range	Operation	0°C to 70°C
	Stable Image	0°C to 50°C
	Output Formats (10-bit)	Raw RGB Data
	Lens Size	1/3"
Maximum Image Transfer Rate	SXGA	15 fps
	VGA	30 fps
	Sensitivity	1.0 V/Lux-sec
	S/N Ratio	54 dB
	Dynamic Range	60 dB
	Scan Mode	Progressive/Interlaced
	Maximum Exposure Interval	1048 x t_{ROW}
	Pixel Size	4.2 µm x 4.2 µm
	Dark Current	28 mV/s
	Fixed Pattern Noise	< 0.03% of $V_{PEAK-TO-PEAK}$
	Image Area	5.4 mm x 4.3 mm
	Package Dimensions	.560 in. x .560 in.

Figure 1 OV9630 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV9630 image sensor. The OV9630 includes:

- Image Sensor Array (1280 x 1024 resolution)
- Analog Signal Processor
  - Gain
  - White Balance (WB)
- Dual A/D Converters
- Output Formatter
  - Windowing
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

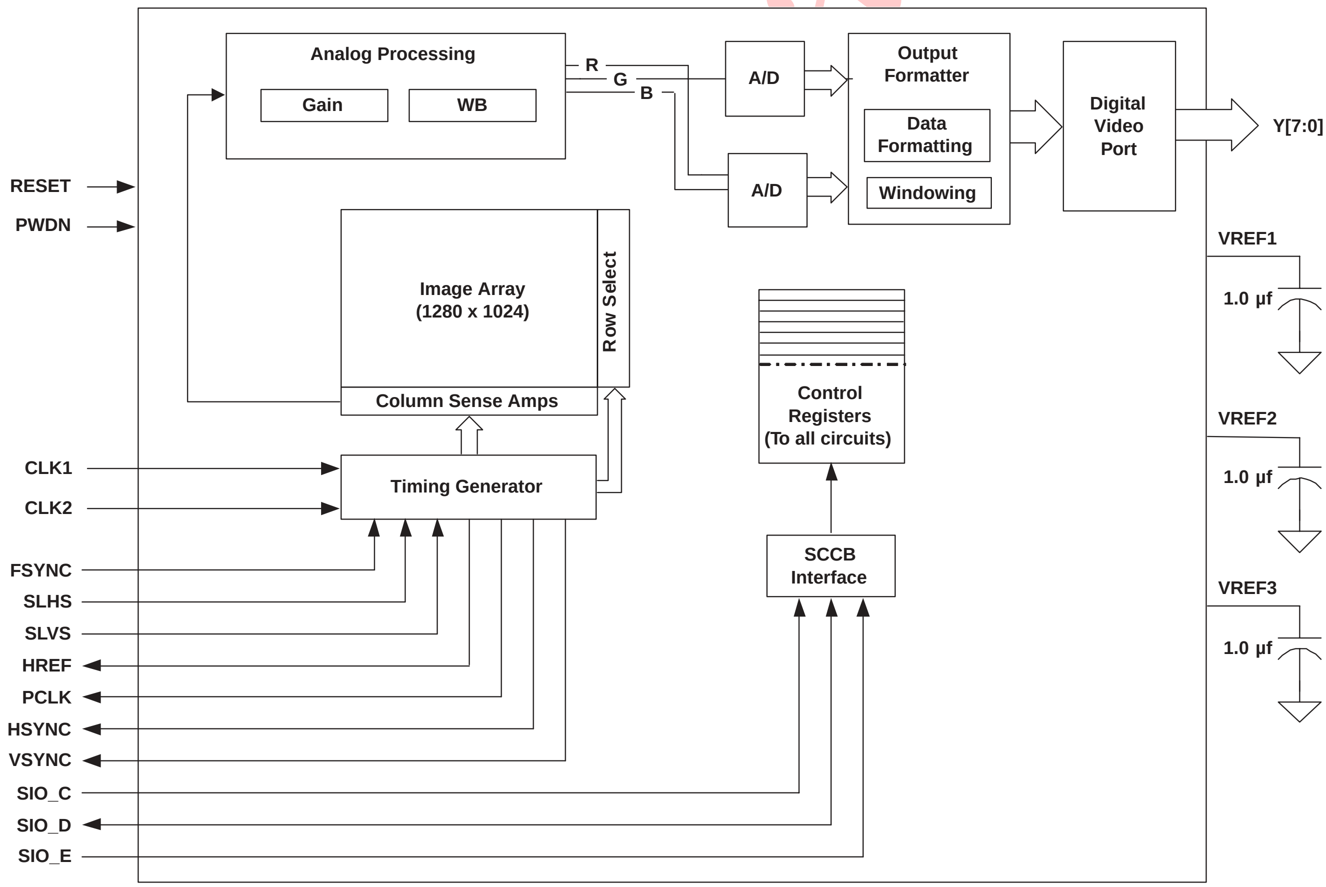
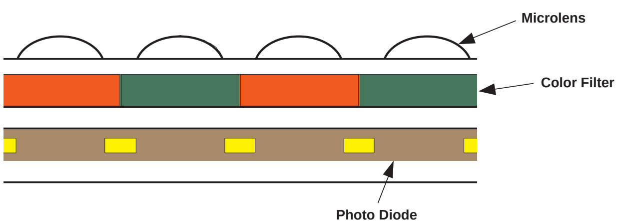


Image Sensor Array

The OV9630 sensor is a 1/3-inch CMOS imaging device. The sensor contains 1,359,232 pixels. However, the maximum output window size is 1296 columns by 1028 rows.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme. Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Analog Signal Processor

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC). The gain adjustment range is 0-24 dB.

White Balance (WB)

The amplified signals are then balanced with a channel balance block. In this block, the Red/Blue channel gain is increased or decreased to match Green channel luminance level. The adjustment range is 54 dB. This function can be done manually by the user or by the internal automatic white balance (AWB) controller.

Dual A/D Converters

The balanced signal is then digitized by the on-chip 10-bit ADC. It can operate at up to 12 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

After the pixel data has been digitized, further alterations to the signal can be applied before the data is output:

- Black level calibration (BLC) - This block subtracts the average signal level of optical black pixels to compensate for the temperature and exposure time generated dark current in the pixel output. The user can disable black level calibration.

Output Formatter

Windowing

The OV9630 allows the user to define window size or region of interest (ROI), as required by the application. Window size setting (in pixels) ranges from 2 x 4 to 1280 x 1024 (SXGA) or 2 x 2 to 640 x 480 (VGA). Note that modifying the window size or window position does not alter the frame or pixel rate. The windowing control merely alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical ROI. The default window size is 1280 x 1024.

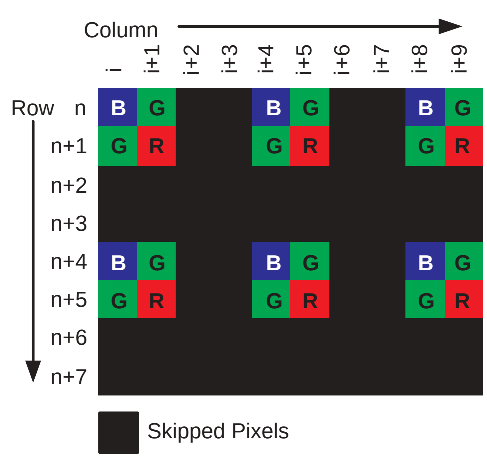
Note that after writing to register COMH (0x12) to change the sensor mode, registers related to the sensor's cropping window will be reset back to its default value.

Data Formatting

Sub-Sampling Mode

The OV9630 can be programmed to output in 640 x 480 (VGA) sized images. In this mode, both horizontal and vertical pixels are sub-sampled to an aspect ratio of 4:2 as illustrated in Figure 4.

Figure 4 Sub-Sampling Mode



Timing Generator

In general, the timing generator controls the following functions:

- Frame Exposure Mode Timing
- Frame Rate Timing
- Frame Rate Adjust

Frame Exposure Mode Timing

The OV9630 supports frame exposure. Typically, frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin 8) is the frame exposure mode enable pin and the EXPSTB pin (pin 12) serves as the sensor's exposure start trigger (1 = Sensor stays in reset mode, 0 = sensor starts exposure - only effect in frame exposure mode). There are two modes of operation for the frame exposure function.

- Control both FREX and EXPSTB pins - Frame Exposure mode can be set by pulling both FREX and EXPSTB pins high at the same time (see Figure 13).
- Control FREX only and keep EXPSTB low - In this case, the pre-charge time is tline and sensor exposure time is the period after pre-charge until the shutter closes (see Figure 12).

When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXPSTB pin goes low (sensor exposure time can be defined as the period between EXPSTB low to shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data output, the OV9630 will output continuous live video data unless in single frame transfer mode. Figure 12 and Figure 13 show detailed timing of the Frame Exposure mode.

For frame exposure, register AEC (0x10) must be set to 0xFF and register GAIN (0x00) should be no larger than 0x10 (maximum 2x gain).

Frame Rate Timing

Default frame timing is illustrated in Figure 10 and Figure 11. Refer to Table 1 for the actual pixel rate at different frame rates.

Table 1 Frame and Pixel Rates

Frame Rate (fps)	15	15	10	7.5	6	5
PCLK (MHz)	48	24	16	12	9.6	8

NOTE:
Based on 48 MHz external clock and internal PLL OFF, and 24 MHz or below external clock and internal PLL ON.

Frame Rate Adjust

The OV9630 offers three methods for frame rate adjustment:

- Clock prescaler:
  By changing the system clock divide ratio, the frame rate and pixel rate will change together.
- Line adjustment:
  By adding a dummy pixel timing in each line, the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
  By adding dummy line periods to the vertical sync period, the frame rate can be altered while the pixel rate remains the same.

After changing registers COML (0x2A) and FRARL (0x2B) to adjust the dummy pixels, it is necessary to write to register COMH (0x12) or CLKRC (0x11) to reset the counter. Generally, OmniVision suggests users write to register COMH (0x12) (to change the sensor mode) as the last one. However, if you want to adjust the cropping window, it is necessary to write to those registers after changing register COMH (0x12). To use COMH to reset the counter, it is necessary to generate a pulse on resolution control register bit COMH[6].

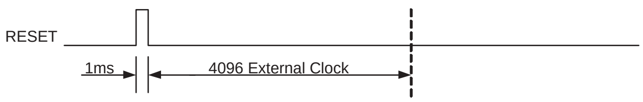
Channel Average Calculator

The OV9630 provides average output level data for the R/G/B channels along with frame-averaged luminance level. Access to the data is provided via the serial control port. Average values are calculated from 128 pixels per line (64 pixels per line in VGA).

Reset

The RESET pin (pin 10) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the RESET pin is low.

Figure 5 RESET Timing Diagram



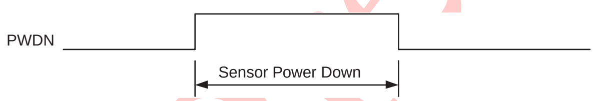
There are two ways for a sensor reset:

1. Hardware reset - Pulling the RESET pin high and keeping it high for at least 1 ms. As shown in Figure 5, after a reset has been initiated, the sensor will be most stable after the period shown as 4096 External Clock.
2. Software reset - Writing 0x80 to register 0x12 (see "COMH" on page 18) for a software reset. If a software reset is used, a reset operation done twice is recommended to make sure the sensor is stable and ready to access registers. When performing a software reset twice, the second reset should be initiated after the 4096 External Clock period as shown in Figure 5.

Power-Down Mode

The PWDN pin is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the PWDN pin is low.

Figure 6 PWDN Timing Diagram



Two methods of power-down or standby operation are available with the OV9630.

- Hardware power-down may be selected by pulling the PWDN pin high. When in hardware power-down, the standby current will be less then 10 µA.
- Software power-down can be effected by setting the COMC[4] register bit high. Standby current will be less then 1 mA when in software power-down.

SCCB Interface

The OV9630 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of OV9630 operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Slave Operation Mode

The OV9630 can be programmed to operate in slave mode (default is master mode).

Digital Video Port

MSB/LSB Swap

The OV9630 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers.

Line/Pixel Timing

The OV9630 digital video port can be programmed to work in either master or slave mode.

Pin Description

Table 2 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	A1VDD	Power	Analog VDD
02	VREF1	Analog	Sensor array reference - connect to ground using a 0.1 µF capacitor
03	NC	—	No connection
04	A2VDD	Power	Analog VDD
05	A2GND	Power	Analog ground
06	VREF2	Analog	Sensor array reference - connect to ground using a 0.1 µF capacitor
07	PWDN	Input (0)[a]	Sets device to power down standby mode, active high
08	FREX	Input (0)	Snapshot trigger
09	NC	—	No connection
10	RESET	Input (0)	Clears all registers and resets them to their default values, active high
11	SIO_E	Input (0)	SCCB interface enable, low to turn on SCCB
12	EXPSTB	Input (0)	Frame exposure start trigger
13	VGA	Input (0)	Sensor Resolution Selection 0: SXGA resolution (1280 x 1024) 1: VGA resolution (640 x 480)
14	FSYNC	Input (0)	Frame synchronization input
15	VREF3	Analog	Sensor array reference - connect to ground using a 0.1 µF capacitor
16	VDD_A	Power	Analog VDD
17	VSS_A	Power	Analog ground
18	VSS_A	Power	Analog ground (substrate)
19	NC	—	No connection
20	A3VDD	Power	Analog VDD
21	A3GND	Power	Analog ground
22	DVDD	Power	Digital VDD (2.5V)
23	DGND	Power	Digital ground
24	Y0	Output	Digital video output bit[0]
25	Y1	Output	Digital video output bit[1]
26	Y2	Output	Digital video output bit[2]
27	Y3	Output	Digital video output bit[3]
28	Y4	Output	Digital video output bit[4]
29	CLK1	Input (0)	Crystal clock input
30	CLK2	Output	Crystal clock output

Table 2 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
31	PCLK	Output	Pixel clock output
32	Y5	Output	Digital video output bit[5]
33	Y6	Output	Digital video output bit[6]
34	Y7	Output	Digital video output bit[7]
35	Y8	Output	Digital video output bit[8]
36	Y9	Output	Digital video output bit[9]
37	VDD_D4	Power	Digital output VDD
38	VSS_D4	Power	Digital output ground
39	HREF	Output	Horizontal reference output
40	HSYNC	Output	Horizontal synchronization output
41	VSYNC	Output	Vertical synchronization output
42	NC	—	No connection
43	SLHS	Input (0)	Slave mode horizontal synchronization input
44	SLVS	Input (0)	Slave mode vertical synchronization input
45	SIO_D	I/O	SCCB serial interface data I/O
46	SIO_C	Input (0)	SCCB serial interface clock
47	VcCHG	Analog	Sensor reference - internal connect to pin 15. Connect to ground using a 0.1 µF capacitor.
48	A1GND	Power	Analog ground

a. Input (0) represents an internal pull-down resistor.

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +125ºC
Supply Voltages (with respect to Ground)	V_{DD-A}	3.6V
	V_{DD-C}	2.75V
	V_{DD-IO}	3.6V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead Temperature, Surface-mount process		+230ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 4 DC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	3.3V ± 10%	3.0	3.3	3.6	V
V_{DD-IO}	DC supply voltage – Digital I/O	3.3V ± 10%	3.0	3.3	3.6	V
V_{DD-C}	DC supply voltage – Digital Core	2.5V ± 10%	2.25	2.5	2.75	V
I_{DDA}	Active (Operating) Current	See Note [a]		40	60	mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS (I_{OH} / I_{OL})	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. $V_{DD-A} = V_{DD-IO}$ = 3.3V, V_{DD-C} = 2.5V
$I_{DDA} = \Sigma\{I_{DD-A} + I_{DD-IO} + I_{DD-C}\}$, SXGA, f_{CLK} = 24MHz at 15 fps, 25 pF plus TTL loading

b. $V_{DD-A} = V_{DD-IO}$ = 3.3V, V_{DD-C} = 2.5V
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ to 3V

Table 5 Functional and AC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Resolution		10		Bits
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			21	dB
	Red/Blue Adjustment Range		12		dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	8	24	48	MHz
t_{CLK}	Input Clock Period	12	42	21	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
AC Conditions:	• V_{DD}: $V_{DD\text{-}C}$ = 2.5V, $V_{DD\text{-}A}$ = $V_{DD\text{-}IO}$ = 3.3V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 7 SCCB Timing Diagram

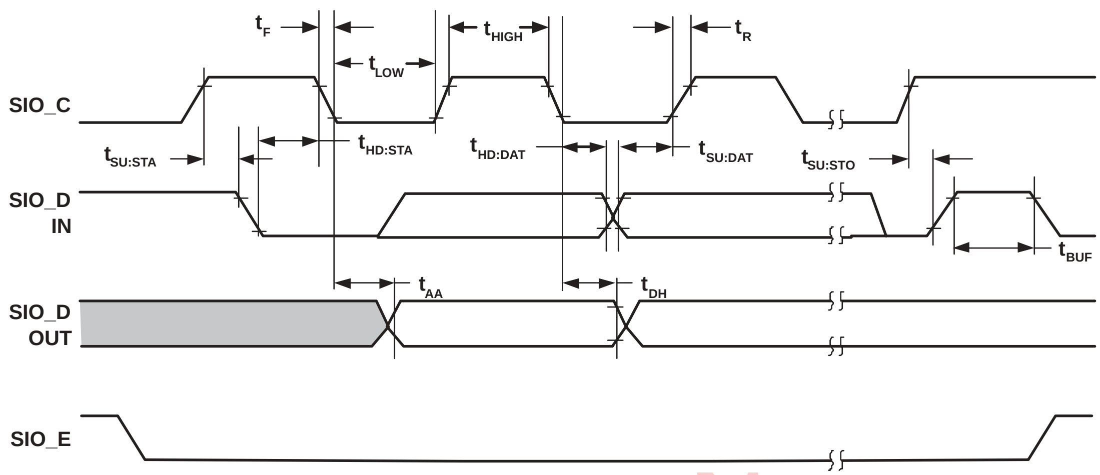


Table 6 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 8 SXGA Line/Pixel Output Timing

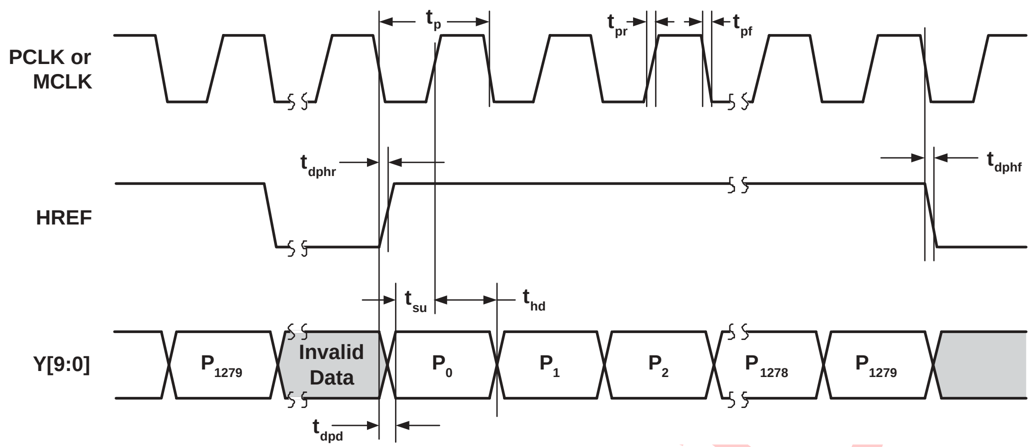


Figure 9 VGA Line/Pixel Output Timing

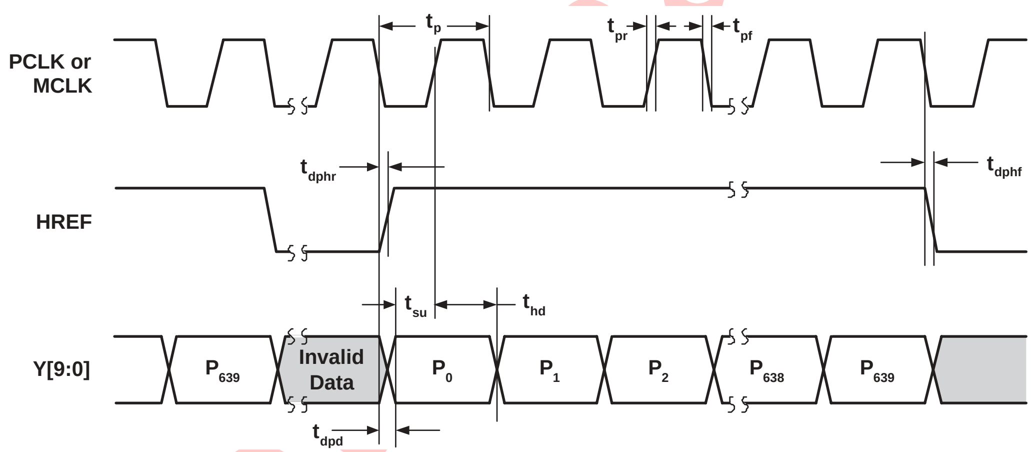


Figure 10 SXGA Frame Timing

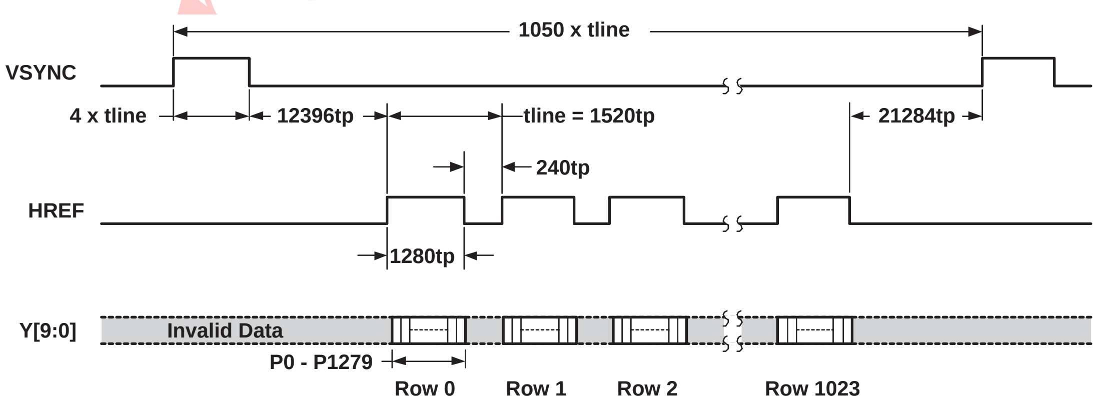


Figure 11 VGA Frame Timing

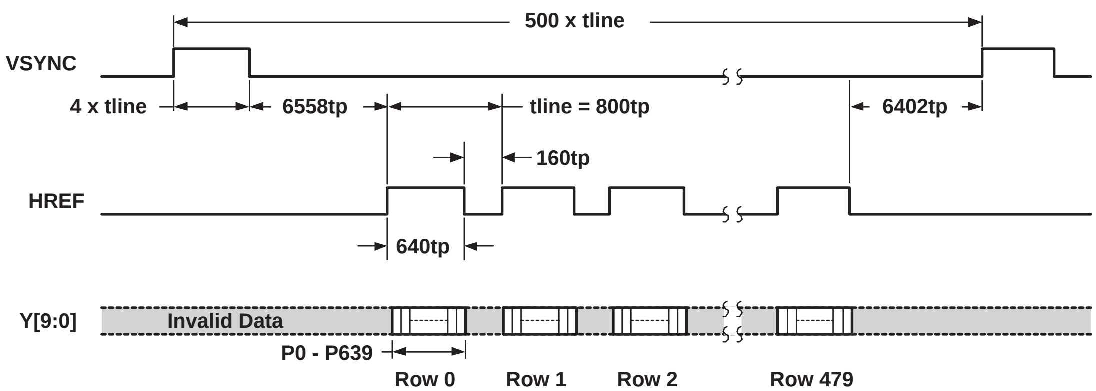


Table 7 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period			41.66	ns
t_{pr}	PCLK rising time		10		ns
t_{pf}	PCLK falling time		5		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 12 Frame Exposure Mode Timing with EXPSTB Staying Low

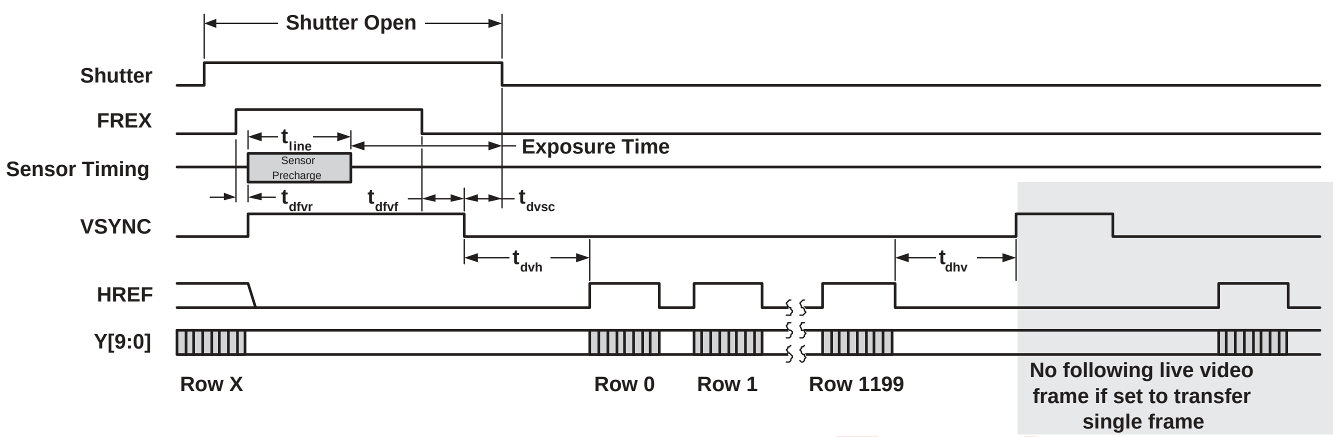


Figure 13 Frame Exposure Mode Timing with EXPSTB Asserted

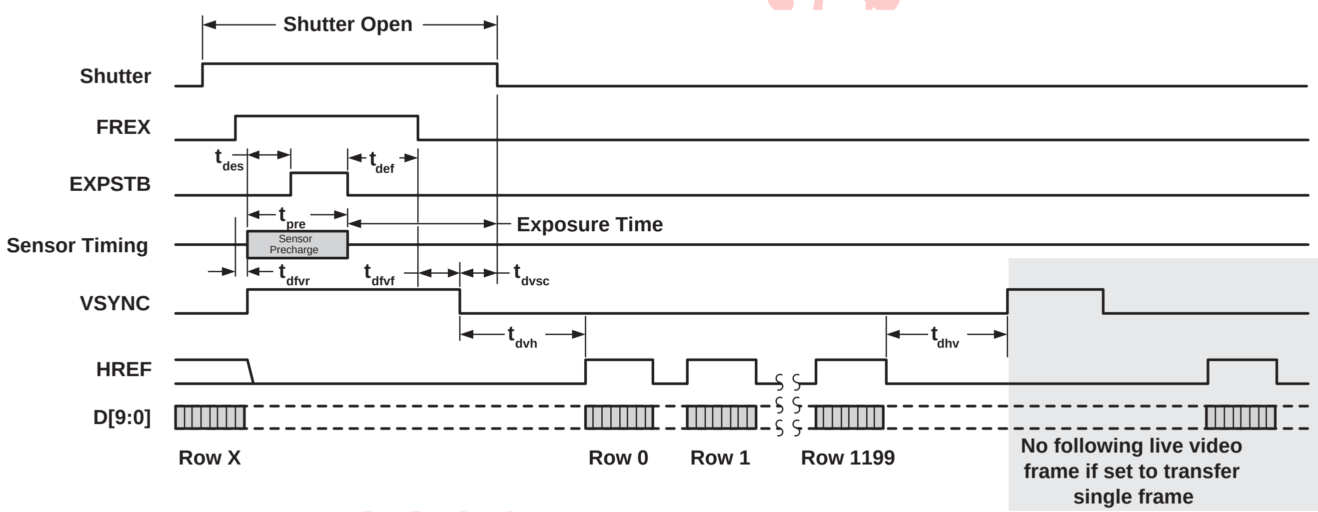


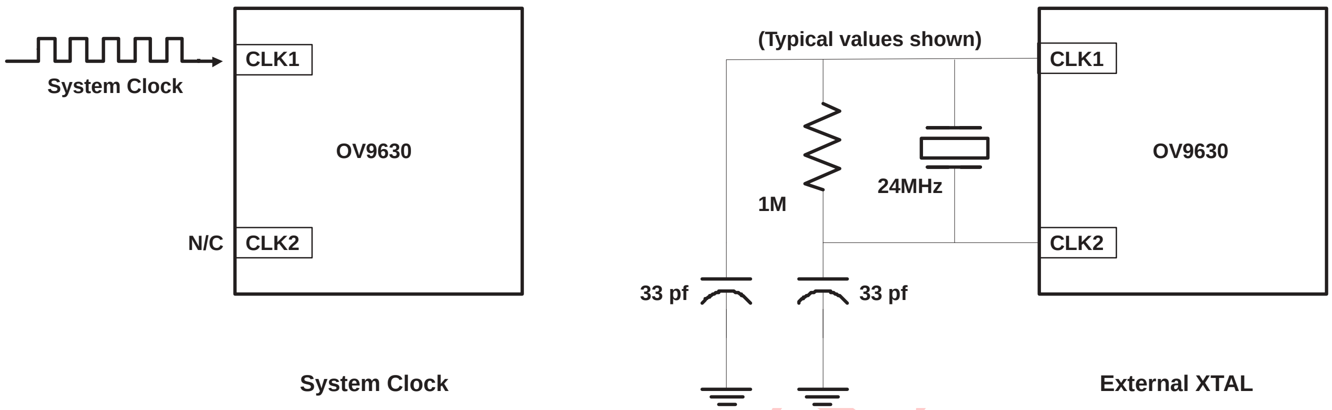
Table 8 Frame Exposure Mode Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		1520 (SXGA)		tp
		800 (VGA)		tp
tvs		4		tline
tdfvr	8		9	tp
tdfvf			4	tline
tdvsc			2	tline
tdhv		21044 (SXGA)		tp
		6402 (VGA)		tp
tdvh		12396 (SXGA)		tp
		6558 (VGA)		tp
tdhso	0			ns

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 3040tp (1600tp for VGA) after VSYNC falling edge.

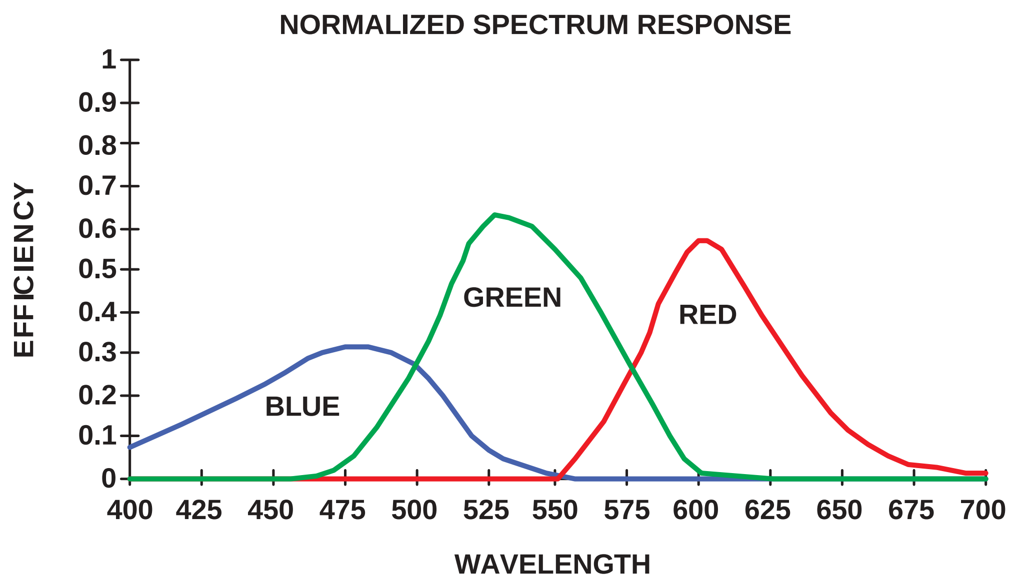
Clock Options

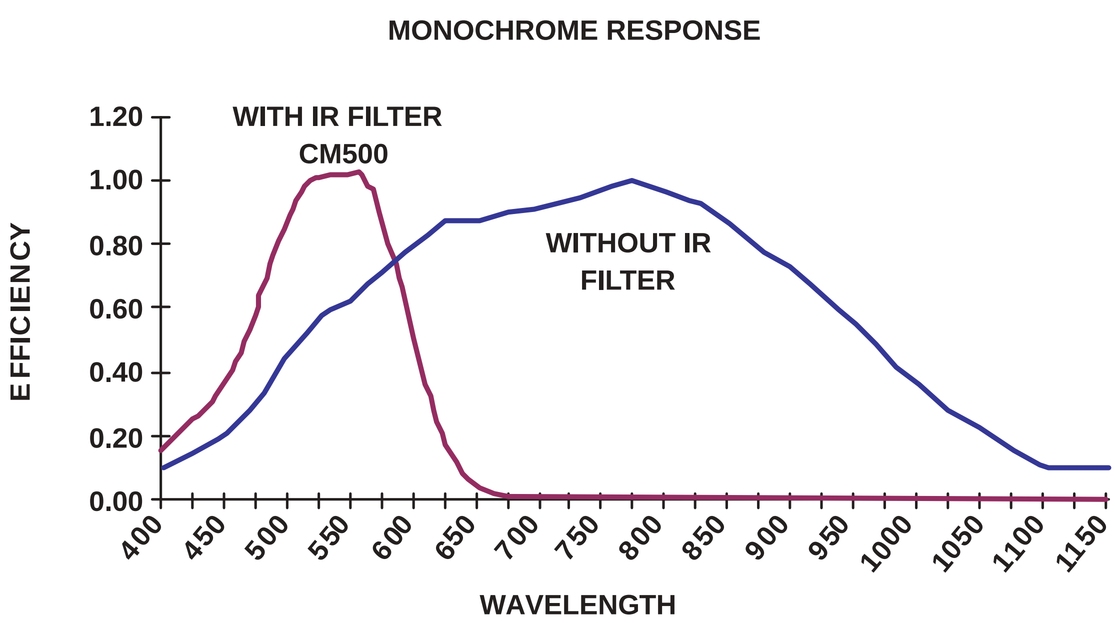
Figure 14 System and External Clock Options



OV9630 Light Response

Figure 15   OV9630 Light Response





Register Set

Table 9 provides a list and description of the Device Control registers contained in the OV9630. The device slave addresses are 60 for write and 61 for read.

Table 9 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting Bit[7:6]: Reserved Bit[5:0]: Gain control gain setting • Range: [00] (Gain = 1X) to [3F] (Gain = 8X) Gain = (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) AGC Enabled: Updated automatically AGC Disabled: User manually stores and updates value
01	BLUEH	80	RW	AWB – Blue channel gain setting • Range: [000] (Gain = x/5) to [3FF] (Gain = 5X) BLUE[9:0] = MSB + LSB = BLUEH[7:0] + COMA[3:2] AWB Enabled: Updated automatically AWB Disabled: User manually stores and updates value
02	REDH	80	RW	AWB – Red channel gain setting • Range: [000] (Gain = x/5) to [3FF] (Gain = 5X) RED[9:0] = MSB + LSB = REDH[7:0] + COMA[1:0] AWB Enabled: Updated automatically AWB Disabled: User manually stores and updates value
03	COMA	40	RW	Common Control A Bit[7:4]: AWB update threshold Bit[3:2]: AWB – BLUE channel LSB Bit[1:0]: AWB – RED channel LSB
04	COMB	00	RW	Common Control B Bit[7:6]: AWB – Step select 00: 1023 steps 01: 255 steps 10: 511 steps 11: 255 steps Bit[5:4]: AWB – Update speed select 00: Slow 01: Slowest 10: Fast 11: Fast Bit[3]: Reserved Bit[2:0]: AEC – Exposure Time LSB
05	BAVG	00	RW	Digital B Channel Average (Automatically updated by AGC/AEC, user can only read the values)
06	GbAVG	00	RW	G Channel Average Picked G pixels in the same line with B pixels.

Table 9 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
07	GrAVG	00	RW	G Channel Average Picked G pixels in the same line with R pixels.
08	RAVG	00	RW	Digital R Channel Average (Automatically updated by AGC/AEC, user can only read the values)
09	COMC	00	RW	Common Control C Bit[7:5]: Reserved Bit[4]: Standby Mode Enable 0: Disable 1: Enable Bit[3:2]: Sensor Sampling Reset Timing Select 00: Normal reset time 01: Long reset time 10: Longer reset time 11: Longest reset time Bit[1:0]: Output Drive Select 00: Weakest 01: Double I_{OL}/I_{OH} 10: Double I_{OL}/I_{OH} 11: Triple I_{OL}/I_{OH}
0A	PIDH	96	R	Product ID Number MSB (Read only)
0B	PIDL	C1	R	Product ID Number LSB (Read only)
0C	COMD	28	RW	Common Control D Bit[7]: Analog half current selection 0: Normal current 1: Half current Bit[6]: Swap MSB and LSB at the output port Bit[5]: Reserved Bit[4]: ADC half current selection 0: Normal current 1: Half current Bit[3:2]: Reserved Bit[1]: Sensor precharge voltage selection 0: Selects internal reference as precharge voltage 1: Selects SVDD as precharge voltage Bit[0]: Frame exposure option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D-0F	RSVD	XX	–	Reserved
10	AEC	43	RW	Automatic Exposure Control Most Significant 8 bits for AEC[10:3] (least significant 3 bits in register COMB[2:0] - see “COMB” on page 16). Bit[10:0]: Exposure time $T_{EX} = t_{LINE} \times AEC[10:0]$ ***Note:*** *Set COMI[2] to 0 to disable the AEC.*

Table 9 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal PLL ON/OFF selection 0: PLL disabled 1: PLL enabled Bit[6]: Digital video port master/slave selection 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLKRC[5:0] + 1)
12	COMH	20	RW	Common Control H Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6]: Resolution selection 0: SXGA 1: VGA Bit[5]: Average luminance value pixel counter ON/OFF 0: OFF 1: ON Bit[4]: Reserved Bit[3]: Master/slave selection 0: Master mode 1: Slave mode Bit[2]: Window output selection 0: Output only pixels defined by window registers 1: Output all pixels Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: Reserved

Table 9 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COMI	87	RW	Common Control I Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: Reserved Bit[5]: Banding filter ON/OFF 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Banding filter option 0: Set to 0, if system clock is 48 MHz and the PLL is ON. 1: Set to 1, if system clock is 24 MHz and the PLL is ON or if the system clock is 48 MHz and the PLL is OFF. Bit[3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	RSVD	XX	–	Reserved
15	COMK	00	RW	Common Control K Bit[7]: HSYNC pin output swap 0: HSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: HSYNC Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data valid on PCLK falling edge 1: Data valid on PCLK rising edge Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	RSVD	XX	–	Reserved

Table 9 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
17	HREFST	1D (13 in VGA)	RW	Horizontal Window start most significant 8 bits, LSB in COMM register (see "COMM" on page 21). Bit[9:0]: Selects the beginning of the horizontal window, each LSB represents two pixels. ***Note:*** *1. HFREFST[9:0] should be less than HREFEND[9:0].* *2. For maximum output window size of 1296x1028, minimum value of this register is 0x1B.*
18	HREFEND	BD (63 in VGA)	RW	Horizontal Window end most significant 8 bits, LSB in COMM register (see "COMM" on page 21). Bit[9:0]: Selects the end of the horizontal window, each LSB represents two pixels. ***Note:*** *1. HREFEND[9:0] should be larger than HREFST[9:0].* *2. For maximum output window size of 1296x1028, maximum value of this register is 0xBD.*
19	VSTRT	01 (02 in VGA)	RW	Vertical Window line start most significant 8 bits, LSB in COMM register (see "COMM" on page 21). Bit[8:0]: Selects the start of the vertical window, each LSB represents four scan lines in SXGA or two scan lines in VGA. ***Note:*** *1. VSTRT[8:0] should be less than VEND[8:0].* *2. For maximum output window size of 1296x1028, minimum value of this register is 0x00.*
1A	VEND	81 (7A in VGA)	RW	Vertical Window line end most significant 8 bits, LSB in COMM register (see "COMM" on page 21). Bit[8:0]: Selects the end of the vertical window, each LSB represents four scan lines in SXGA and two scan lines in VGA. ***Note:*** *1. VEND[8:0] should be larger than VSTRT[8:0].* *2. For maximum output window size of 1296x1028, maximum value of this register is 0x81.* *3. The adjustment range for the vertical window size is from [01] to [122] in SXGA and [01] to [0F4] in VGA.*
1B-29	RSVD	XX	–	Reserved

Table 9 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	COML	00	RW	Common Control L Bit[7]: Line interval adjustment. Interval adjustment value is in COML[6:5] and FRARL[7:0] (see “FRARL” on page 21). 0: Disabled 1: Enabled Bit[6:5]: Line interval adjust value MSB 2 bits Bit[4]: AGC preset initial value for auto gain control 0: Disabled 1: Enabled Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits The frame rate will be adjusted by changing the line interval. Each LSB will add 2/1520 T_{frame} in SXGA and 2/800 T_{frame} in VGA mode to the frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average This register will auto update when COMH[5] = 1 (see “COMH” on page 18). Average Luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] +RAVG[7:0])/4
30-31	RSVD	XX	–	Reserved
32	COMM	0A (0Ffor VGA)	RW	Common Control M Bit[7:6]: Reserved Bit[5]: Vertical window end position LSB Bit[4]: Vertical window start position LSB Bit[3:2]: Horizontal window end position LSBs Bit[1:0]: Horizontal window start position LSBs ***Note:*** *For maximum output window size of 1296x1028, value of this register should be 0x1F.*
33-38	RSVD	XX	–	Reserved

NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.

Package Specifications

The OV9630 uses a 48-pin ceramic package. Refer to Figure 16 for package information and Figure 17 for the array center on the chip.

Figure 16 OV9630 Package Specifications

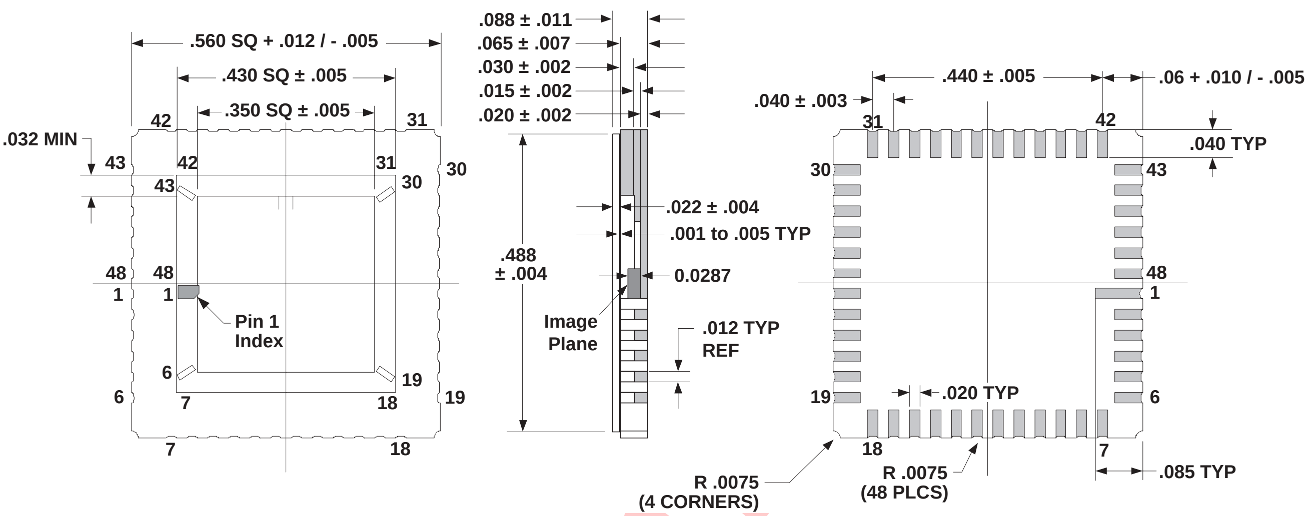
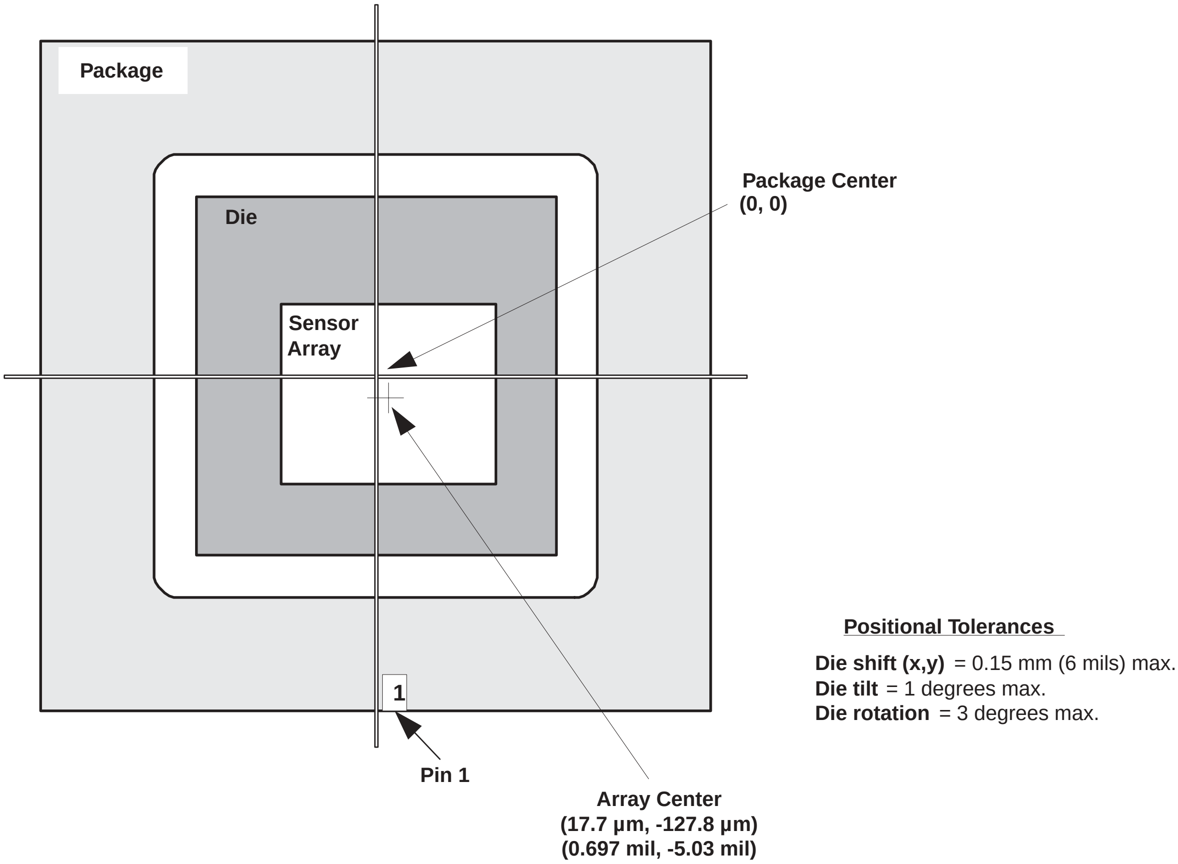


Table 10 OV9630 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 17 OV9630 Sensor Array Center



Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (SVDD) down as shown.

NOTE: Picture is for reference only, not to scale.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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