FAIRCHILD SEMICONDUCTOR™

I-Cube®

OCX160 Crosspoint Switch
Preliminary Datasheet

Features

- 667 Mb/s port data bandwidth, >50Gb/s aggregate bandwidth
- Low power CMOS, 2.5V and 3.3V power supply
- SRAM-based, in-system programmable
- 160 configurable I/O ports
  - 80 dedicated differential input ports
  - 80 dedicated differential output ports
  - Supports LVDS and LVPECL I/O
  - LVTTL control interface
  - Output Enable control for all outputs
- Non-blocking switch matrix
  - Patented ActiveArray™ matrix for superior performance
  - Double-buffered configuration RAM cells for simultaneous global updates
  - ImpliedDisconnect™ function for single cycle disconnect/ connect
- Full Broadcast and multicast capability
  - One-to-One and One-to-Many connections
  - Special broadcast mode routes one input to all outputs at maximum data rate
- Registered and flow-through data modes
  - 333 MHz synchronous mode
  - 667 Mb/s asynchronous mode
  - Low jitter and signal skew
  - Low duty cycle distortion
- RapidConfigure™ parallel interface for configuration and readback
- JTAG serial interface for configuration and Boundary Scan testing
- 420 BGA package with 1.27mm ball spacing

Description

The OCX™ family of SRAM-based devices are non-blocking *n X n* digital crosspoint switches capable of data rates of 667 Megabits per second per port. The I/O ports are fixed as either input or output ports. The input ports support flow-through mode only. The output ports are individually programmable to operate in either flow-through (asynchronous) or registered (synchronous) mode. Each output register may be clocked by a global clock or a next neighbor clock source.

The patented ActiveArray provides greater density, superior performance, and greater flexibility compared to a traditional *n:1* multiplexer architecture. The OCX devices support various operating modes covering one input to one output at a time as well as one input to many outputs, plus a special broadcast mode to program one input to all outputs while maintaining maximum data rates. In all modes data integrity and connections are maintained on all unchanged data paths.

The RapidConfigure parallel interface allows fast configuration of both the Output Buffers and the switch matrix. Readback is supported for device test and verification purposes. The OCX160 also supports the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The JTAG interface can also be used to download configuration data to the device and readback data. A functional block diagram of the OCX160 is shown in Figure 1.

Applications

- SONET/SDH and DWDM
- Digital Cross-Connects
- System Backplanes and Interconnects
- High Speed Test Equipment
- ATM Switch Cores
- Video Switching

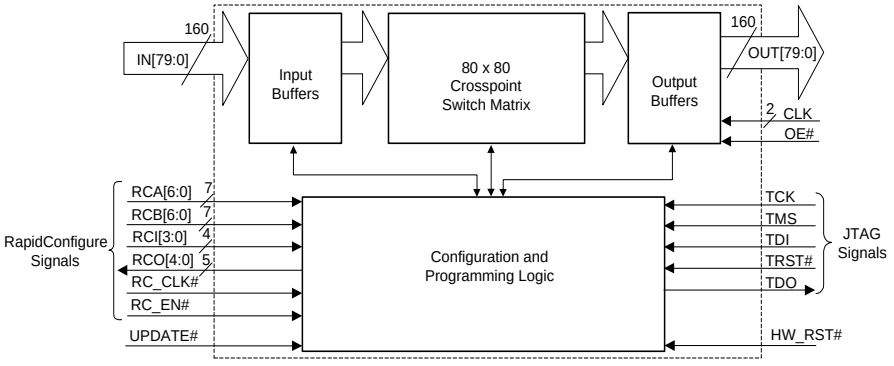

Figure 1 OCX160 Functional Block Diagram

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Tables

1. Introduction

The OCX160 is a differential crosspoint-switching device. The main functional block of the device is a Switch Matrix as shown in Figure 1. The Switch Matrix is a *x-y* structure supporting an input-to-output data flow. Figure 2 shows a conceptual view of the switch matrix with inputs connected to the horizontal trace and outputs to the vertical trace. Connections between vertical and horizontal lines are implemented with a proprietary high-performance buffering circuit. Signal path delays through the Switch Matrix are very well balanced, resulting in predictable and uniform pin-to-pin delays.

Note – For the purpose of clarity, the logic diagrams within this datasheet are conceptual representations only and do not show actual circuit implementation.

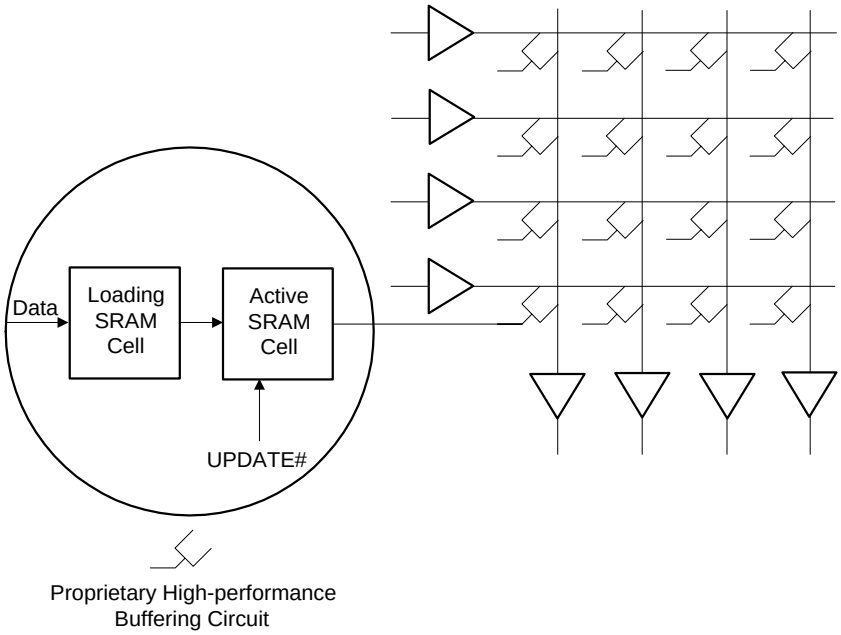


Figure 2 OCX160 Switch Matrix

The Active SRAM cells are responsible for establishing connections in the switch matrix by turning on the interconnect circuit, while the Loading SRAM cell can be used to store a second configuration that can be transferred to the Active SRAM cell at a later time. The two SRAM cells are arranged so that a double buffered scheme can be employed. Through the use of an internal signal (generated automatically during a programming cycle) it is possible to store a second configuration map in the Loading SRAM while the Active SRAM maintains its present connection status. When the UPDATE# signal is asserted low, the contents of the Loading SRAM cell are transferred to the Active SRAM cell and the switch matrix connection is either made or broken.

The UPDATE# signal can be used to control when the switch matrix is reconfigured. For instance, as long as the UPDATE# signal is asserted high, the Loading SRAM cells for the entire switch matrix could be changed without affecting the current configuration of the switch. When the UPDATE# signal is asserted low, the entire switch matrix would be reconfigured simultaneously. If the UPDATE# signal is asserted continuously, all crosspoint programming commands (generated by RapidConfigure or JTAG programming cycles) will take effect immediately, since the Loading SRAM cell's contents will be transferred directly to the Active SRAM cell.

1.1 Input and Output Buffers

All of the input buffers are differential inputs with flow-through mode. The output buffers are programmable for either flow-through or registered mode. Figure 3 shows the basic block diagram of the input and output blocks with the sources for the output control signals (OE# and CLK). The control signals are explained in more details in the following sections.

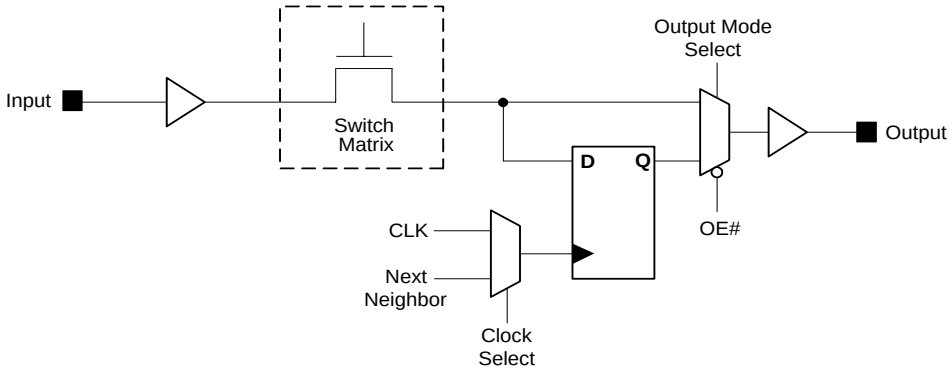


Figure 3 Input and Output Buffer Configuration

1.1.1 Input and Output Port Function Mode

The following legend describes the various modes of the Input and Output Ports and the specification used by the OCXPro™ Software.

Legend:

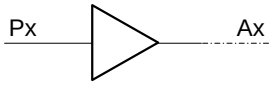
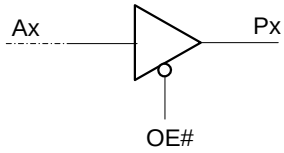
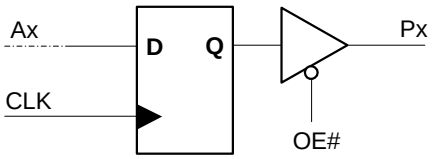
Ax–Switch Matrix Signal

Px–Port Signal

OE#–Output Enable (# means “Active Low”)

CLK–Clock

Table 1 Summary for Programmable I/O Attributes for OCX160

Symbol	I/O Port Function	Mnemonic
	**Input** – The external signal is buffered from the Input Port pin to the corresponding Switch Matrix line.	**IN**
	**Output** – The internal signal is buffered from the corresponding Switch Matrix line to the Output Port pin. In this mode an optional output enable (OE#) can be selected. The default state is logic high with enable set to ON.	**OP**
	**Registered Output –** The internal signal on the Switch Matrix line is registered by an edge-triggered register within the Output Port. A clock source is required in this mode. An output enable (OE#) is available but not required.	**RO**
	**No Connect** – In this mode, the output Port pin is isolated from the Switch Matrix.	**NC**

1.1.2 Broadcast Mode

The OCX160 has a special Broadcast Mode which connects any input to all outputs without performance degradation. The input is selected using RapidConfigure or JTAG and disconnects all other inputs. The Global Update pin (UPDATE#) must be held high during Broadcast Mode. Asserting the UPDATE# pin returns the array to the previous program condition.

1.2 Output Buffer Configuration

Every output port of the OCX160 can be configured as either a flow-through or registered output. In registered mode there are two clock sources that are available:

- Global Clock
- Next Neighbor

Additionally, there are output control signals.

1.2.1 Output Control Signals

Every output port of the OCX has a global Output Enable signal (OE#). All output buffers have output enables that have programmable polarity and are individually configurable.

Additionally each output can be permanently enabled (always ON) or disabled (always OFF) which is useful for applications which need to tri-state outputs (for example when using multiple chips in expansion mode) or for power saving in designs that do not need to use all the outputs available.

Two control bits are used to control the function of the output enable function as described in Table 5.

1.2.2 Neighboring Output Port as a Clock Source

A physically adjacent port can be used as a clock source for an output port configured in registered mode. These outputs are grouped in pairs such that the signal being switched through OUT0 can be used to clock the signal being switched through OUT1, and vice versa. Any single clock or data input signal can be used to clock any other input signal provided they are switched to an appropriate output pair (see Table 2). Figure 4 shows the implementation of next neighbor output port clocking in the OCX160 switch.

For example, IN*x* is used for data input while IN*y* is used for the corresponding clock. IN*x* is connected to OUT0 via the crosspoint array while IN*y* is connected to OUT1 via the crosspoint array. OUT0 is configured in registered output (RO) mode with OUT1 as its next neighbor clock selection. OUT1 will output the clock signal as well as clock the data in OUT0. Adjacent port selection is required for next neighbor clocking in the registered output mode.

This feature is useful in many applications where different types of data switching through the crosspoint array have various associated clocks. To match the delays in the data and corresponding clocks, it is common practice to pass the clocks through the switch along with the data.

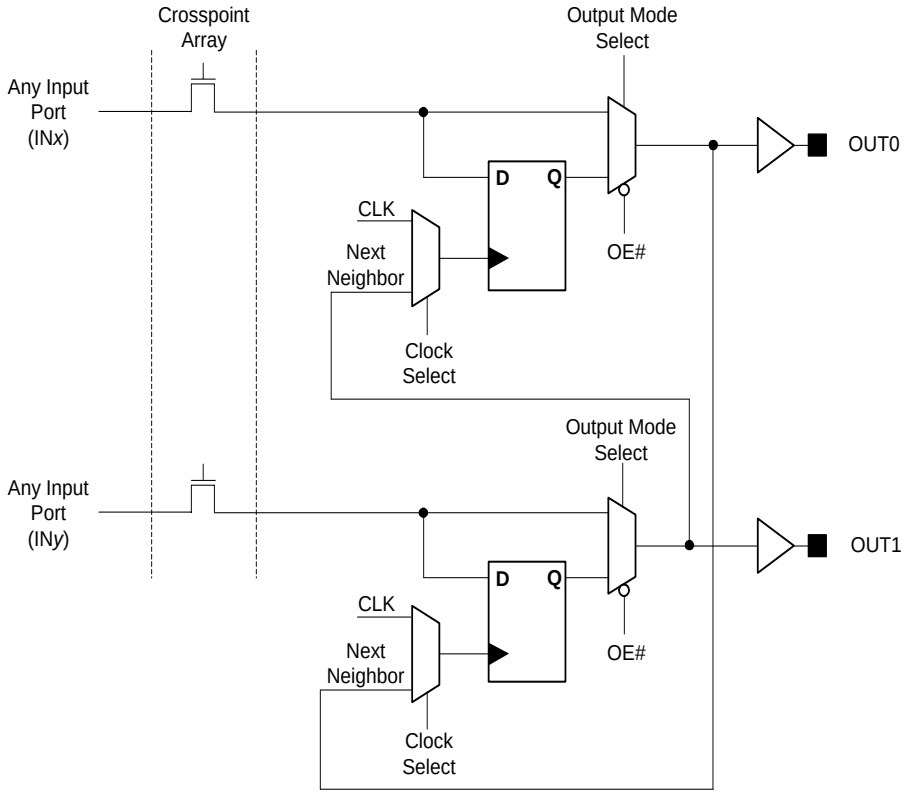


Figure 4 Next Neighbor Clock Block Diagram

The advantages of next neighbor clocking are:

1. Using next neighbor clocking in the registered output (RO) mode helps reduce the skew in outgoing data.
2. For a design with a large number of outputs switching simultaneously, next neighbor clocking mode is useful to stagger outputs for reduced board noise caused by simultaneous switching outputs.

Note – Selecting the next neighbor clock for both outputs at the same time is not recommended. Only one output in the pair at a time can be clocked by its next neighbor.

Table 2 Next Neighbor Outputs

Pairing Sequence for Neighboring Outputs								
Output Next Neighbor Pairs	0,1	2,3	4,5	6,7	8,9	◗◗◗◗	76,77	78,79

Only OUT1 can neighbor with OUT0, OUT3 with OUT2, etc. OUT2 cannot neighbor with OUT1, or OUT4 with OUT3, etc.

1.3 RapidConfigure Interface

RapidConfigure (RC) is a 25 signal parallel interface that is used to program the OCX160 device. The 25 pins are allocated as follows:

RCA[6:0] = RapidConfigure Address A. RCA are input pins.

RCB[6:0] = RapidConfigure Address B. RCB are input pins.

RCI[3:0] = RapidConfigure Instruction Bits

RCO[4:0] = RapidConfigure Readback. RCO are output pins.

RC_CLK# = RapidConfigure Clock (negative edge clock)

RC_EN# = RapidConfigure Cycle Enable (active low)

1.3.1 RapidConfigure Programming Instructions

The RC interface supports both write and read types of operations:

1. Write Operations (reset crosspoint and Input or Output Buffer (IOB), configure an Output Buffer, connect/disconnect crosspoint)
2. Read Operations (Output Buffer and crosspoint configuration read).

Table 3 RapidConfigure Programming Instructions

RCI[3:0]	RCA[6:0]	RCB[6:0]	RCO[4:0]	Instruction	Description
0000				Reserved	
0001				Reserved	
0010	X	X		Reset Crosspoint Array	Reset, along with an Update operation (UPDATE# pin or Update command), resets the entire crosspoint array to no connect. All Output Buffers remain unchanged by this operation.
0011	X	Input Port Address		Set Array to Broadcast mode	Connects the input selected by RCB[6:0] to all output ports and disconnects all other inputs. The Global Update (UPDATE#) pin must be held high during Broadcast mode. Activating the Global Update pin returns the array to the previous program condition.
0100	Output Port Address	Data		Configure an Output Buffer	Program an Output Buffer specified by RCA[6:0]. See Table 5 for RCB[6:0] bit assignment and buffer functionality.
0101				Readback Crosspoint, Output Buffer status	This is a two-cycle instruction.
Cycle 1	Output Port Address	Input Port Address	X		Specify the crosspoint connect status at output location specified by RCB[6:0] to the input location specified by RCA[6:0].

Table 3 RapidConfigure Programming Instructions *(Continued)*

RCI[3:0]	RCA[6:0]	RCB[6:0]	RCO[4:0]	Instruction	Description
Cycle 2	X	X	Output Data		Readback (using RCO[4:0]) the status of the input buffer specified in Cycle 1 by RCA[6:0], the output buffer specified in Cycle 1 by RCO[4:0] and the crosspoint connect status. See Table 4 for RCO[4:0] readback pin assignment.
0110	X	X		Update	Program the Global Update function without the use of the UPDATE# pin.
0111	X	Input Port Address		Disconnect Input	Disconnect the crosspoint cells of the input row location specified by RCB[6:0].
1000	Output Port Address	Input Port Address		Disconnect Input and Output	Disconnect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the source input address or to the same output address remain the same as before.
1001	Output Port Address	Input Port Address		Connect, with ImpliedDisconnect	Connect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the same input address or to the same output address are set to no connect (NC).
1010	Output Port Address	Input Port Address		Connect, without ImpliedDisconnect	Connect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the same input address remain the same as before.
1011				Reserved	
1100				Reserved	
1101	X	X		Reset All	Reset the switch matrix to no connects (NC). Update is forced internally. Sets the Output Buffer to Flow-through mode with Output Enabled.
1110				Reserved	
1111				Reserved	

Note – X = Don’t care.

Table 4 RCO[4:0] Readback Pin Assignment

RCO[4:0]	Readback Location	Signal/Function
O4	Crosspoint	**Connection Status:** 0 = No connection (NC) — (default state at reset) 1 = Connected
O3	Output Buffer	**Clock Select:** 0 = Global Clock — (default state at reset) 1 = Next Neighbor
O2	Output Buffer	**Output Mode:** 0 = Flow-through (OP) — (default state at reset) 1 = Registered (RO)
O1, O0 0,0 0,1 1,0 1,1	Output Buffer	**Output Enable:** Output enabled (ON) – this is the default state at reset Output disabled (OFF) Output controlled by OE (active high) Output controlled by OE# (active low)

Table 5 Programming an Output Buffer using RapidConfigure

RCB[6:0]	Signal/Function
B6, B5, B4	Don’t care
B3	**Clock Select:** 0 = Global Clock 1 = Next Neighbor
B2	**Output Mode:** 0 = Flow-through (OP) 1 = Registered (RO)
B1, B0 0,0 0,1 1,0 1,1	**Output Enable:** Output enabled (ON) – this is the default state at reset Output disabled (OFF) Output controlled by OE (active high) Output controlled by OE# (active low)

1.3.2 ImpliedDisconnect

ImpliedDisconnect is a feature that provides the ability to make fast switch connection changes. When using the RC instruction “Connect, with ImpliedDisconnect” to establish a new connection, any existing connection to that output port is automatically broken. Thus, a connection change, i.e. breaking an existing connection and then making a new one, can be accomplished in one RapidConfigure cycle.

1.4 JTAG Configuration Controller

The Output port attributes and the Switch Matrix connections can be programmed using the JTAG serial bus. The RapidConfigure Interface can be enabled or disabled using the JTAG serial bus.

The JTAG–based serial mode is always available for configuration regardless of whether the RapidConfigure mode is enabled or disabled. However, proper care must be taken when switching between JTAG and RapidConfigure for configuring the devices. Before attempting to change Switch Matrix connections or output port configuration through JTAG, the user must first ensure that the RapidConfigure mode is disabled by using JTAG serial mode to set the RCE bit to zero in the Mode Control Register.

1.4.1 JTAG Interface

The dedicated JTAG TAP interface is designed in compliance with the IEEE-1149.1. The standard interface has five pins: Test Data Out (TDO), Test Mode Select (TMS), Test Data In (TDI), Test Reset (TRST#), and Test Clock (TCK), which allow Boundary Scan Testing as well as device configuration and verification. The Fairchild supplied software will automatically generate the necessary bitstream from a higher-level textual description of the required configuration. Data on the TDI and TMS pins are clocked into the device on the rising edge of the TCK signal, while the valid data appears on the TDO pin after the falling edge of TCK. For more detailed information on JTAG programming, refer to the *OCX160 Register Programming Manual*.

1.4.2 Output Port Configuration

Output port configuration is accomplished by loading the appropriate bitstream into the programming registers present at each Output port. The JTAG serial bus is used to load configuration data into the Output port programming registers, one Output port at a time.

1.4.3 Switch Matrix Configuration

The contents of the SRAM cells controlling Switch Matrix connection can be modified using the JTAG. This is accomplished by loading the configuration data, one word at a time, into the SRAM cells in the Switch Matrix.

1.4.4 Mode Control Register Configuration

The OCX160 contains a single bit Mode Control Register used to store user flags for RapidConfigure Enable (RCE). These are required for proper functioning of the device. The contents of this register can be changed using the JTAG interface and a special JTAG instruction.

Table 6 Mode Control Register

RCE	Mode
0	RapidConfigure interface disabled (OFF)
1	RapidConfigure interface enabled (ON)

1.4.5 JTAG Architecture and Shift Registers

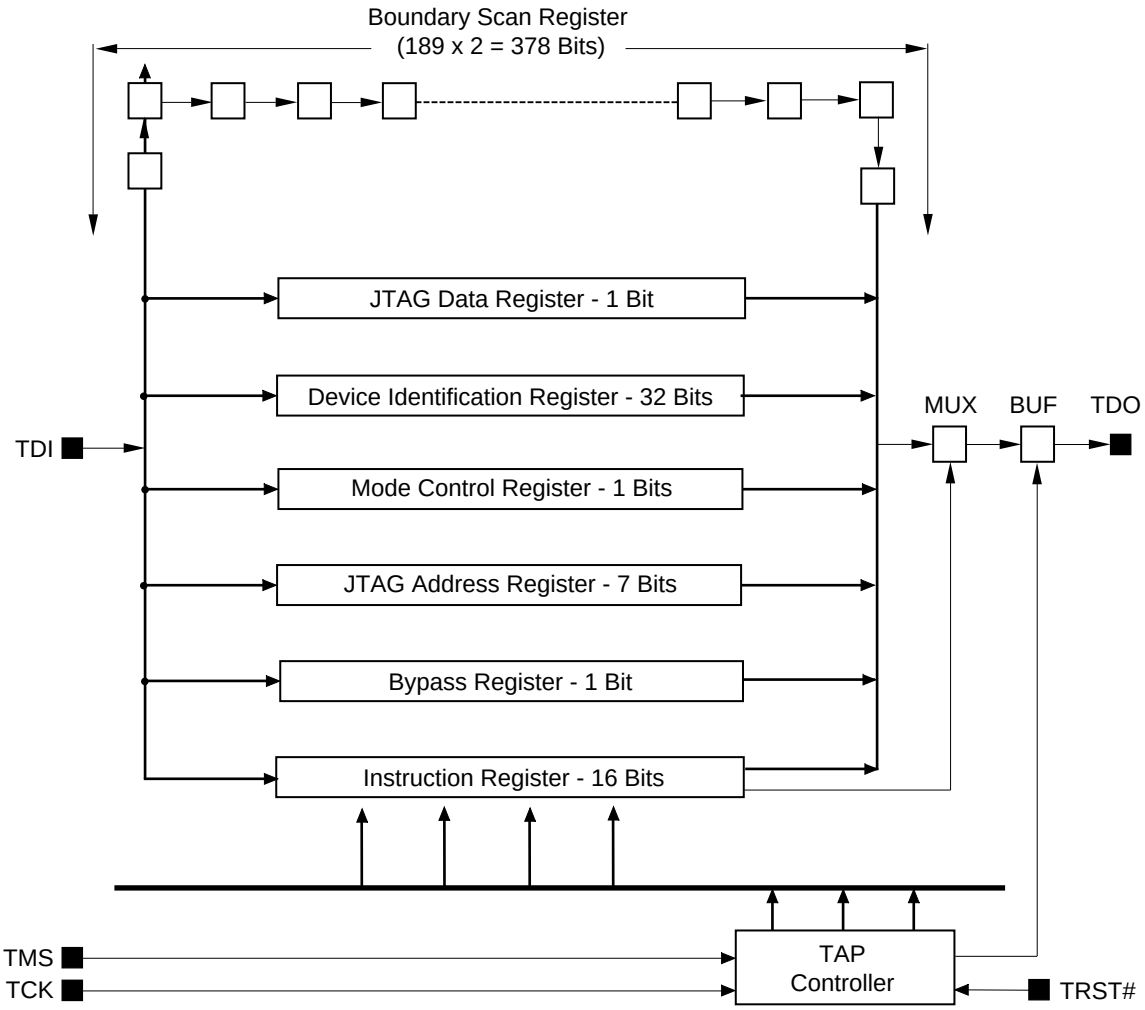


Figure 5 OCX160 JTAG Architecture

1.4.6 JTAG State Machine

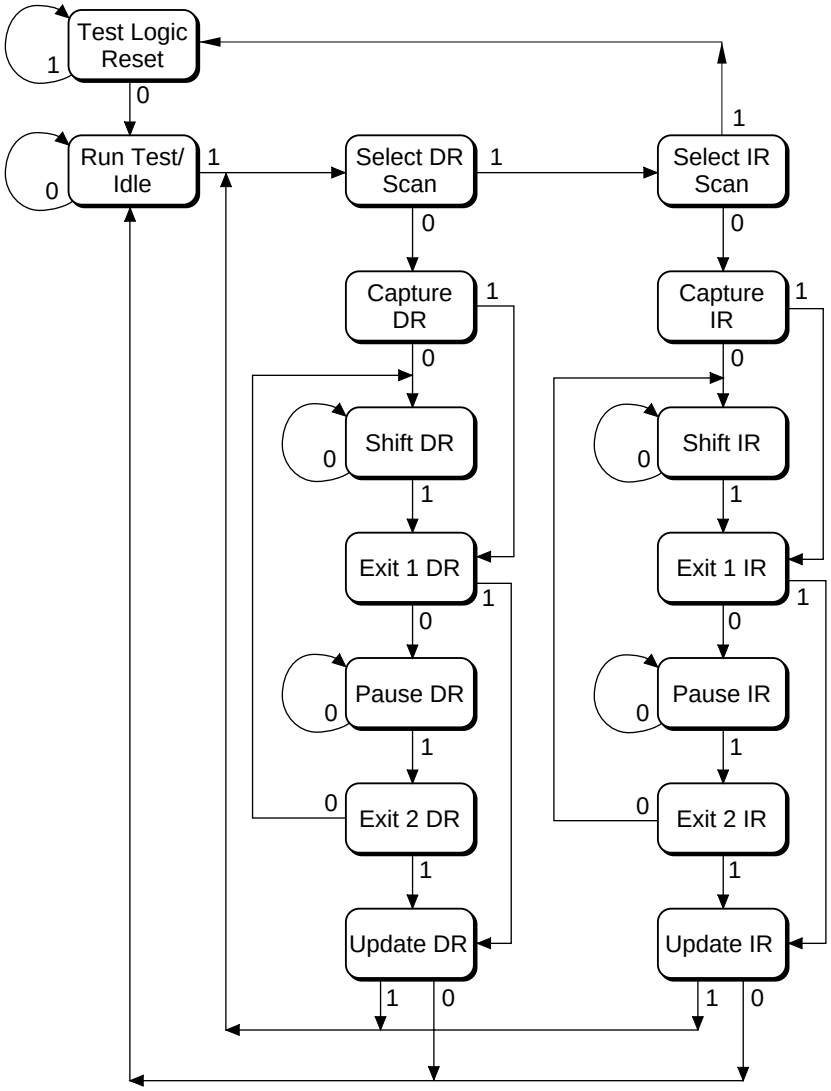


Figure 6 OCX160 JTAG State Machine

1.4.7 JTAG Input Format

Table 7 JTAG Input Format

	Instruction				Data					Address A						
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	I3	I2	I1	I0	BB	BA	B9	B8	B7	A6	A5	A4	A3	A2	A1	A0

1.4.8 JTAG Instructions

Table 8 JTAG Instructions

I [3:0]	BB	BA	B9	B8	B7	A6-A0	Instruction	Description
0 0 0 0	X	X	X	X	X	X	Sample/EXTEST	Places the device in scan mode.
0 0 0 1	X	X	X	X	X	X	Sample/EXTEST	Places the device in scan mode.
0 0 1 0	X	X	X	X	X	X	Reset the Crosspoint Array	Resets the entire Crosspoint Array to no-connect. All other Output Buffer configurations are unchanged by this operation.
0 0 1 1	X	X	X	X	X	X	Set Array for Broadcast mode	Use the JTAG Address Register as the Input address to be the broadcast input Connects the selected Input to all Output cells and disconnects all other Inputs. Activating the Global Update JTAG instruction returns the Crosspoint array from the Broadcast mode to the previous programed state.
0 1 0 0	X	Clock Select	Data Mode	OE	OE	Output Buffer Address	Program a Buffer	Programs the Output Buffer address specified in the JTAG instruction (A6-A0). The configuration data is also specified in the JTAG instruction bits BA-B7. See Table 9 for bit assignment of the Buffer functionality.
0 1 0 1	X	X	X	X	X	Output Address/ Buffer	Configuration readback	Readback the connectivity of the Crosspoint cell with the Input location specified in the JTAG Address Register and the Output location specified JTAG instruction (A0-A6). It also returns the configuration of the Output Buffer addressed in the JTAG instruction (A0-A6). The readback data is shifted out of TDO in the following sequence: 1. Crosspoint Connect (1=connected, 0=no connection) 2. Output Enable—B7 (see Table 9) 3. Output Enable—B8 (see Table 9) 4. Output Data Source—B9 (0=Flow-through, 1=registered) 5. Output Clock Select—BA (0=Global Clock, 1=Next Neighbor) 6. State of Broadcast bit 7. State of the RCE bit NOTE: This instruction does not increment the JTAG Address Register. This instruction also requires two DR cycles
0 1 1 0	X	X	X	X	X	X	Update the Crosspoint Array	Update the programmed connection from the Loading SRAM to the Active SRAM.
0 1 1 1	X	X	X	X	X	X	Disconnect Input cell	Disconnect the Crosspoint connections from the Input address specified in the JTAG Address Register.

Table 8 JTAG Instructions *(Continued)*

I [3:0]	BB	BA	B9	B8	B7	A6-A0	Instruction	Description
1 0 0 0	X	X	X	X	X	Output Address	Disconnect Input and Output	Disconnect the Crosspoint cell at the Input location specified at the JTAG Address Register and the Output location specified in the Disconnect JTAG instruction (A6-A0). All other connections from the same input address or to the same output address remain the same.
1 0 0 1	X	X	X	X	X	Output Address	Connect with ImpliedDisconnect	Connects the Crosspoint cell at the Input location specified on the JTAG Address Register and the output location specified in the Connect JTAG instruction (A6-A0). All other connections from the same Input address or the same Output address are set to no-connects. NOTE: This instruction increments the JTAG Address Register (Input address).
1 0 1 0	X	X	X	X	X	Output Address	Connect—no ImpliedDisconnect	Connects the Crosspoint cell at the Input address specified in the JTAG Address Register and the Output address specified in the Connect JTAG instruction (A6-A0). All other connections from the same input remain the same as before.
1 0 1 1	X	X	X	X	X	Input Address	Set the JTAG Address Register	Sets the 7-bit JTAG Address Register with the 7-bit address (A6-A0) of the JTAG Instruction Register. The 7-bit address of the JTAG Address Register becomes the Input port address for Crosspoint Access.
1 1 0 0	X	X	X	X	X	X	Device ID out	Serialize the device ID and revision history out to TDO. ID for the OCX160 is **0x0000B89F**
1 1 0 1	X	X	X	X	X	X	Reset Output Buffer and Crosspoint Array	Resets the Crosspoint Array to no-connects. Sets the Output buffer to Flow-through mode with Output Enabled. The device ID is serialized to TDO.
1 1 1 0	X	X	X	X	X	X	Set RCE Bit	Sets the RCE bit of the Mode Control Register with the JTAG instruction bit A0. To turn ON the RCE bit, encode bit A0 to 1. To turn OFF the RCE bit, encode bit A0 to 0.
1 1 1 1	X	X	X	X	X	X	Bypass	Places device in a mode to pass TDI data to TDO with one clock delay. Used for programming and testing devices through serial connected JTAG controls.

Table 9 Programming an Output using JTAG

BA, B9, B8, B7	Signal/Function
BA	**Clock Select:** 0 = Global Clock 1 = Next Neighbor
B9	**Output Mode:** 0 = Flow-through (OP) 1 = Registered (RO)
B8, B7 0,0 0,1 1,0 1,1	**Output Enable:** Output enabled (ON) – this is the default state at reset Output disabled (OFF) Output controlled by OE (active high) Output controlled by OE# (active low)

Table 10 Number of JTAG Cycles and Configuration Time

Operation	OCX160
	JTAG Cycles
JTAG Reset Sequence (TMS = “11111”)	7
Enable or Disable RapidConfigure	28
Change attributes of ONE Output Port	28
Change attributes of ALL Output Ports	2,240
Reset JTAG Controller + Reset ALL Output Ports + Clear ALL SRAM cells	35
Connect or disconnect two Ports	56
Configure Entire Switch Matrix	181,440
Completely Configure the Device (All Output Ports and All Switch Matrix Connections)	183,680

1.5 Device Reset Options

The power-on reset, RapidConfigure reset, hardware reset, and JTAG reset functions will program the output buffers to flow-through mode (with Global Clock selected), and Output Enabled (ON). JTAG can be reset via the TRST# pin or by clocking five consecutive one to the TMS pin. The hardware reset pin can be done accomplished through the HW_RST# pin (active low). RC reset can be accomplished by applying the RC instruction 1101 to the RCI[3:0] pins.

Table 11 Device Reset Options

Programming Interface	Reset Method	Output Ports	Switch Matrix	RCE Mode Control	JTAG TAP
Hardware Reset	Power-on Reset	OP	NC	1 (RC Enabled)	TLR[1]
	HW_RST# (low pulse)	OP	NC	1 (RC Enabled)	TLR
JTAG Reset	1. Low Pulse on TRST#	Unchanged	Unchanged	Unchanged	TLR
	2. TMS high for 5 TCLK cycles	Unchanged	Unchanged	Unchanged	TLR
	3. Device Reset (instruction 1101)	OP	NC	1 (RC Enabled)	TLR
	4. Reset Crosspoint Array (instruction 0010)	Unchanged	NC	Unchanged	Unchanged
RapidConfigure Reset	1. Device reset (instruction 1101)	OP	NC	1 (RC Enabled)	Unchanged
	2. Reset Crosspoint Array (instruction 0010)	Unchanged	NC	Unchanged	Unchanged

1. TLR = Test Logic Reset state.

2. Pin Description

Table 12 OCX160 Pin Description

Pin Name	# of Pins	Type	Description
INP[79:0]	80	Input	Non-inverting differential input signals
INN[79:0]	80	Input	Inverting differential input signals
OUTP[79:0]	80	Output	Non-inverting differential input signals
OUTN[79:0]	80	Output	Inverting differential input signals
CLKP	1	Input	Non-inverting differential Global Clock
CLKN	1	Input	Inverting differential Global Clock
OE#	1	Input	Global Output Enable
HW_RST#	1	Input	Hardware Reset
UPDATE#	1	Input	Global Update
RC Pins			
RCA[6:0]	7	Input	RapidConfigure Address A
RCB[6:0]	7	Input	RapidConfigure Address B
RCO[4:0]	5	Output	RapidConfigure Readback
RCI[3:0]	4	Input	RapidConfigure Instruction Bits
RC_CLK#	1	Input	RapidConfigure Clock
RC_EN#	1	Input	RapidConfigure Cycle Enable
JTAG Pins			
TCK	1	Input	JTAG Test Clock
TMS	1	Input	JTAG Test Mode Select
TDI	1	Input	JTAG Test Data In
TRST#	1	Input	JTAG Test Reset
TDO	1	Output	JTAG Test Data Out
Power and Ground Pins			
V_{DD}.CORE	12	2.5V Power	Core Voltage
V_{DD}.PAD (2, 3)	8	2.5V or 3.3V Power	Differential Output Buffer Voltage
V_{DD}.IN (1, 4)	8	3.3V Power	LVTTL Control pins Voltage and Differential Input Buffer Voltage
V_{SS}	36	Ground	Ground

NOTES:

1. Dedicated differential input buffers can receive both LVDS and LVPECL voltage levels using 3.3V supply.
2. V_{DD}.PAD is 2.5V for LVDS outputs or 3.3V for LVPECL outputs.
3. Dedicated differential output buffers can be biased using different supplies for V_{DD}.PAD and external resistors to support both LVDS and LVPECL output voltage levels.
4. The LVTTL control, JTAG pins, and differential input ports are 3.3V—they are not 5V tolerant.
5. The differential output pins powered from 2.5V are 3.3V tolerant.

3. Differential I/O Standards

The OCX160 support the two most popular differential signaling standards: Low Voltage Differential Signaling (LVDS) and Low Voltage Positive Emitter Coupled Logic (LVPECL).

LVDS is typically used in communication systems as high speed, low noise point-to-point links. The OCX160 conforms to the ANSI/TIA/EIA-644 standard covering electrical specifications for output drivers and receiver inputs.

LVPECL is commonly used in video switching applications or those designs requiring transmission of high-speed clock signals.

3.1 LVDS

LVDS is a differential signaling standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage or a board termination voltage is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

Transmitting and receiving circuits for LVDS are shown in Figures 7 and 8.

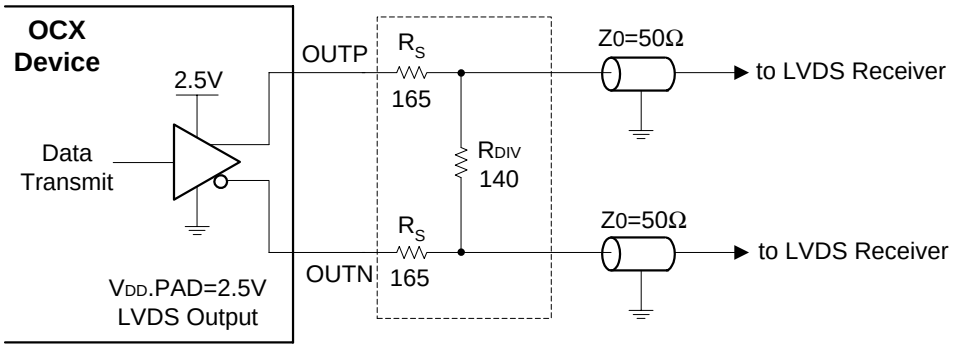


Figure 7 Transmitting LVDS Signal Circuit

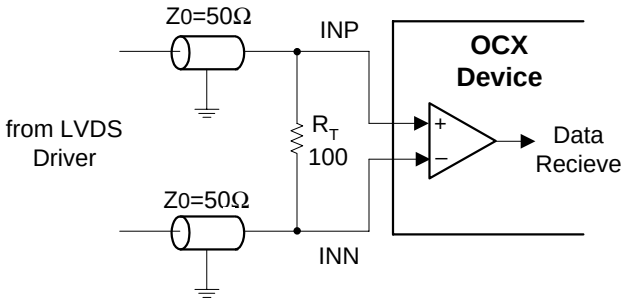


Figure 8 Receiving LVDS Signal Circuit

3.2 LVPECL

LVPECL is another differential signaling standard that specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage or a board termination voltage is not required. The LVPECL standard requires external resistor termination.

Transmitting and receiving circuits for LVPECL are shown in Figures 9 and 10.

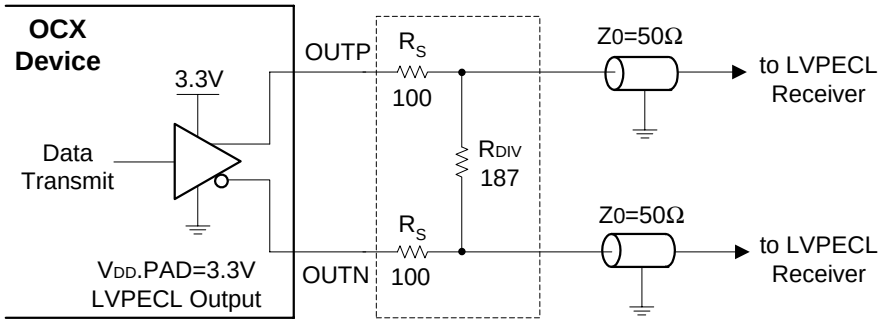


Figure 9 Transmitting LVPECL Signal Circuit

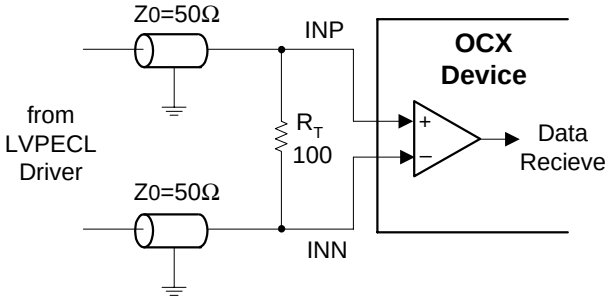


Figure 10 Receiving LVPECL Signal Circuit

3.3 Termination Resistor Packs

Resistor packs are available with the values and the configuration required for LVDS and LVPECL termination from Bourns, Inc. The part numbers are listed in Table 13. For pricing and availability questions, please contact them directly at www.bourns.com.

Table 13 Termination Resistor Packs

Bournes Part Number	Differential I/O Standard	Termination for:	Pairs per Pack	No. of Pins
CAT16-LV2F6	LVDS	Driver	2	8
CAT16-LV4F12	LVDS	Driver	4	16
CAT16-PC2F6	LVPECL	Driver	2	8
CAT16-PC4F12	LVPECL	Driver	4	16
CAT16-PT2F2	LVDS/LVPECL	Receiver	2	8
CAT16-PT4F4	LVDS/LVPECL	Receiver	4	16

3.4 Mixed I/O Systems

The use of different supply voltages and terminating resistors allows the OCX160 to support LVDS / LVPECL translation as well as switching as outlined in Table 14.

Table 14 Supply Voltages and Terminating Resistors

Input	Output	V_{DD}.PAD	R_T	R_S	R_{DIV}
LVDS	LVDS	2.5V	100Ω	165Ω	140Ω
LVPECL	LVDS	2.5V	100Ω	165Ω	140Ω
LVDS	LVPECL	3.3V	100Ω	100Ω	187Ω
LVPECL	LVPECL	3.3V	100Ω	100Ω	187Ω

NOTES:

1. V_{DD}.IN = 3.3V ±10%, V_{DD}.CORE = 2.5V ±5%
2. It is not possible to mix LVDS and LVPECL outputs on a device

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 15 Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{DD}.CORE	Supply Voltage (core)	-0.3 to +3.0	V
V_{DD}.IN	Supply Voltage (inputs)	-0.3 to +3.6	V
V_{DD}.PAD	Supply Voltage (differential outputs)	-0.3 to +3.6	V
V_{IN}[2]	Input Voltage	-0.3 to +3.6[3]	V
T_J	Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_{MAX}	Maximum Power Dissipation	6	W
ESD[6]	Electrostatic Discharge	2000	V

4.2 Recommended Operating Conditions

Table 16 Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}.CORE	Supply Voltage (core)	+2.375 to +2.625	V
V_{DD}.PAD[4]	Supply Voltage (differential output buffers)	3.3V ±10% to 2.5V ±5%	V
V_{DD}.IN	Supply Voltage (inputs)	+3.0 to +3.6	V
T_A	Operating Temperature: Commercial Operating Temperature: Industrial	0 to +70 -40 to +85	°C

4.3 Pin Capacitance

Table 17 Pin Capacitance[5]

Symbol	Parameter	Max	Units
C_{PIN}	Signal Pin Capacitance	10	pF

1. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. A maximum undershoot of 2V for a maximum duration of 20 ns is acceptable. Overshoot to 3.6V is acceptable.
3. All inputs are 3.3V tolerant with the V_{DD} pin at 2.5V or 3.3V.
4. Note that min and max values for V_{DD} for differential outputs are I/O Standard dependent.
5. Capacitance measured at 25°C. Sample tested only.
6. Measured using Human Body Model.

4.4 DC Electrical Specifications

(T_A = -40°C to 85°C, V_{DD}.IN = 3.3V ±10%, V_{DD}.CORE = 2.5V ±5%)

Table 18 LVTTL DC Electrical Specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High-level Input	Ports are 3.3V tolerant	2.0	3.6	V
V_{IL}	Low-level Input	Ports are 3.3V tolerant	-0.3	0.8	V
V_{OH}	High-level Output	V_{DD}.PAD = Min I_{OH} = -4mA	2.4	V_{DD}.PAD+ 0.3	V
V_{OL}	Low-level Output	V_{DD}.PAD = Min I_{OL} = 8mA		0.4	V
IL_{IH}, IL_{IL} (1)	Input Pin Leakage Current	V_{DD}.IN= Max 0.0 < In < $V_{DD.PAD}$		+5 -50	µA
IL_{OZ}	Tristate Leakage Output OFF State	V_{DD}.PAD = Max 0.0 < In < $V_{DD.PAD}$		+5 -5	µA
Power					
P_{DDQ} (2)	Quiescent Power	All V_{DD} = Max		0.5	W

Table 19 LVDS DC Electrical Specifications

DC Parameter	Min	Typ	Max	Units
Output High Voltage for OUTP and OUTN (3)			1.6	V
Output Low Voltage for OUTP and OUTN	0.90			V
Differential Output Voltage (5)	250	350	450	mV
Output Common-Mode Voltage	1.125	1.25	1.375	V
Differential Input Voltage	100	350		mV
Input Common-Mode Voltage	0.25	1.25	2.25	V

1. All LVTTL input pins have pull-up resistors.
2. See section 6 for dynamic power consumption calculation.
3. Refer to Figures 7 and 8 for termination resistor.
4. Refer to Figures 9 and 10 for termination resistor.
5. Maximum capacitive load is 12 pF.

Table 20 LVPECL DC Electrical Specifications

DC Parameters	Min	Max
V_{IH} (4)	V_{DD}.PAD - 1.165	V_{DD}.PAD - 0.880
V_{IL}	V_{DD}.PAD - 1.810	V_{DD}.PAD - 1.475
V_{OH}	1.80	2.40
V_{OL}	0.95	1.55

These values in Table 20 are valid at the output of the source termination pack, as shown in sections 3.2 and 3.3, with a 100Ω differential load only. The V_{OH} levels are 200mV below LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The above table summarizes the DC output specifications of LVPECL.

4.5 AC Electrical Specifications

(V_{DD}.IN = 3.3V ±10%, V_{DD}.CORE = 2.5V ±5%)

Table 21 AC Electrical Specifications

Symbol	Parameter	0°C to 70°C		-40°C to +85°C		Units
		Min	Max	Min	Max	
R_{DATA}	NRZ Data Rate (1)		667		667	Mb/s
F_{RO}	Registered Output Clock Frequency (1)		333		333	MHz
t_{W_RO}	Registered Clock Pulse Width, High or Low (1)	2		2		ns
t_{S_RO}	Registered Output Setup Time to Clock	4		4		ns
t_{H_RO}	Registered Output Clock to Hold Data	0		0		ns
t_{CO_RO}	Registered Output Clock to Data Out Valid		2.5		2.5	ns
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay, Fanout = 1		5.5		6.5	ns
t_{W+}	Input Flow-through Positive Pulse Width	1.5		1.5		ns
t_{W-}	Input Flow-through Negative Pulse Width	1.5		1.5		ns
t_{DCD+}, t_{DCD-}	Duty Cycle Distortion		0.5		0.6	ns
t_{JITTER}	Output Jitter		0.5		0.5	ns
t_{SK}	Skew between Output Ports (1)		0.5		0.6	ns
t_{PHZ_OT}, t_{PLZ_OT}	Output Enable to Valid Data		3		3	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to High Z State		3		3	ns
t_{RC}	RapidConfigure Clock Period	12		12		ns
t_{W+_RC} t_{W-_RC}	RapidConfigure Clock Pulse Width	5		5		ns
t_{S_RC}	RapidConfigure Address Setup to RC_CLK#	3		4		ns
t_{H_RC}	RapidConfigure Address and Enable Hold Time to RC_CLK#	3		4		ns
t_{P_UD}	Update of Crosspoint to Data Out		10		10	ns
f_{JTAG}	JTAG Clock Frequency (TCK)		20		20	MHz
t_{W_JTAG}	JTAG Clock Pulse Width (TCK) @ 20MHz cycle	20	30	20	30	ns
t_{S_JTAG}	JTAG Setup Time	4		4		ns
t_{H_JTAG}	JTAG Hold Time	0		0		ns
t_{P_JTAG}	JTAG Clock to Output Data Valid (TDO)		20		20	ns

NOTES:

1. These parameters are guaranteed but not tested in production.

4.6 Timing Diagrams

Note – For the purpose of clarity, the timing diagrams within this datasheet are conceptual representations only and do not show actual circuit implementation.

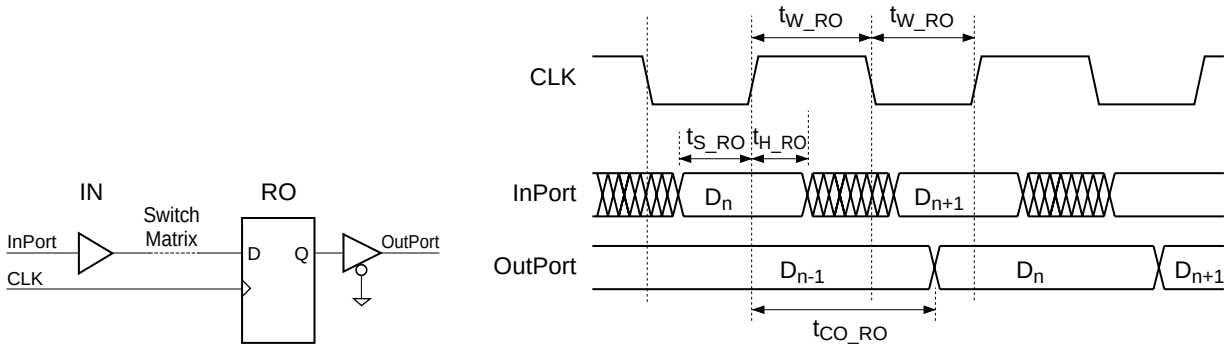


Figure 11 Registered Output Mode Timing

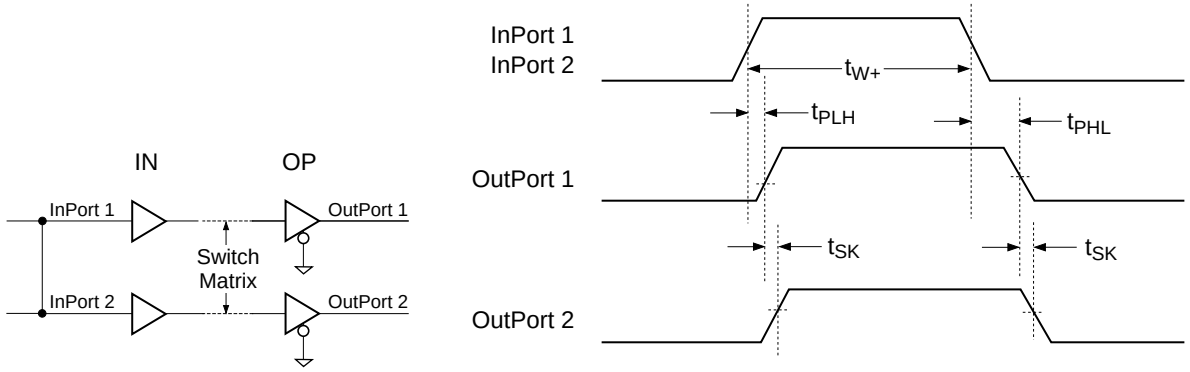


Figure 12 Flow-Through Mode Timing

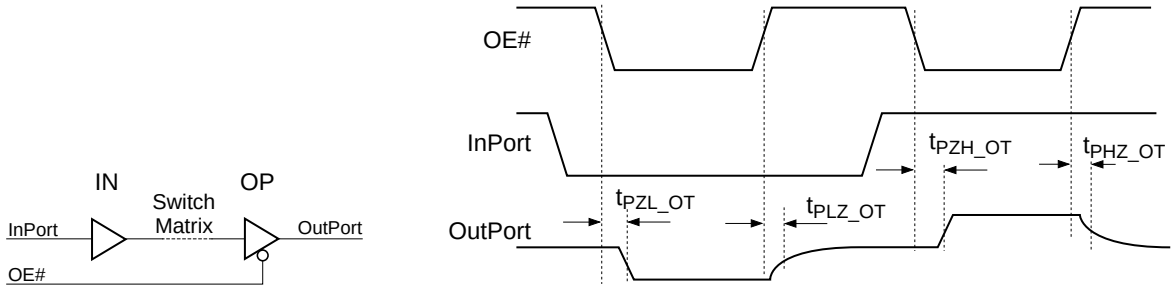


Figure 13 Output Enable Timing

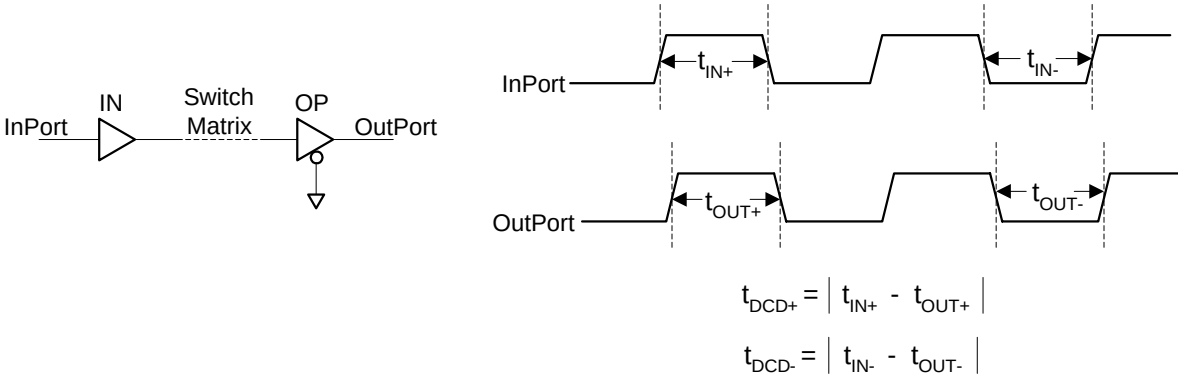


Figure 14 Duty Cycle Distortion

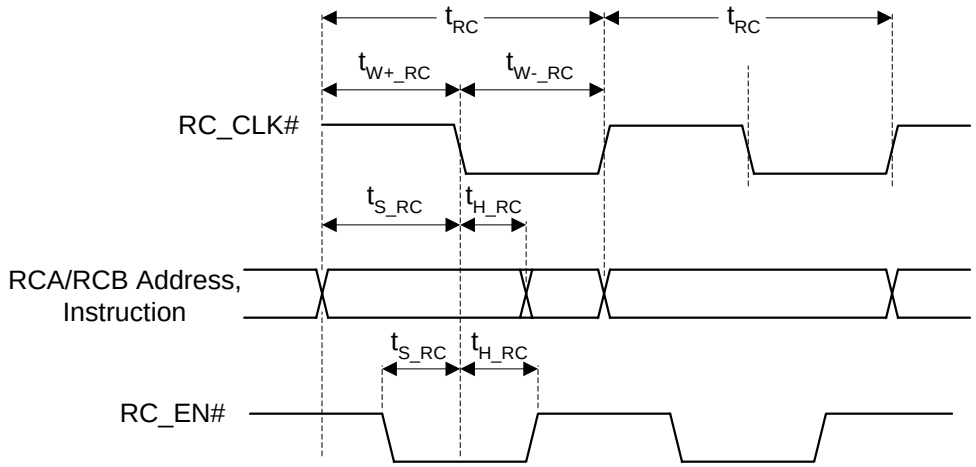


Figure 15 RapidConfigure Write Cycle

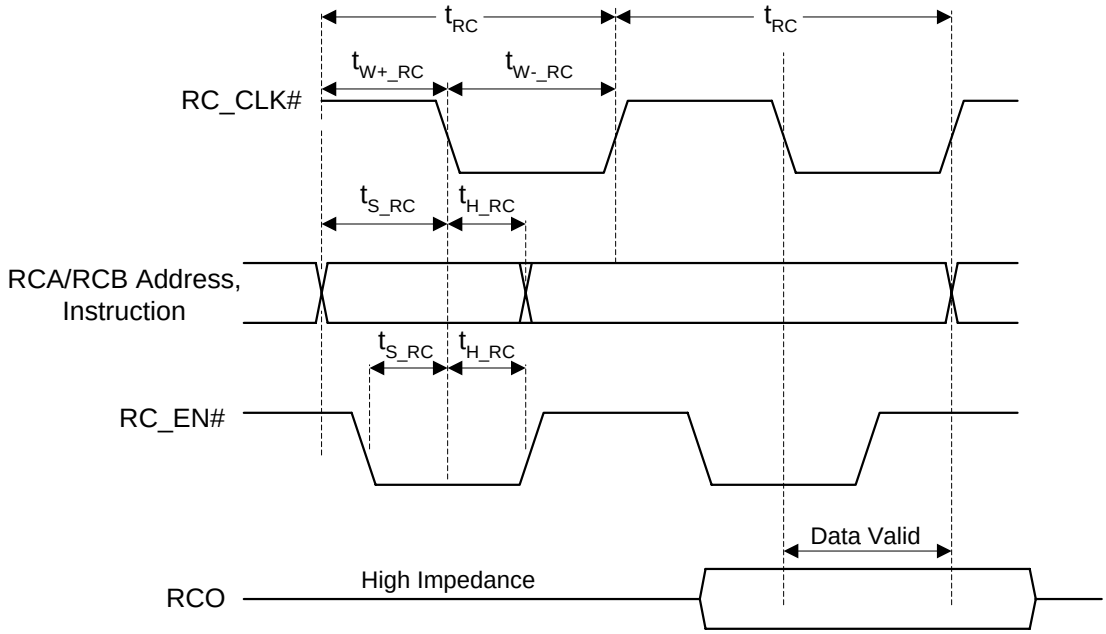


Figure 16 RapidConfigure Read Cycle

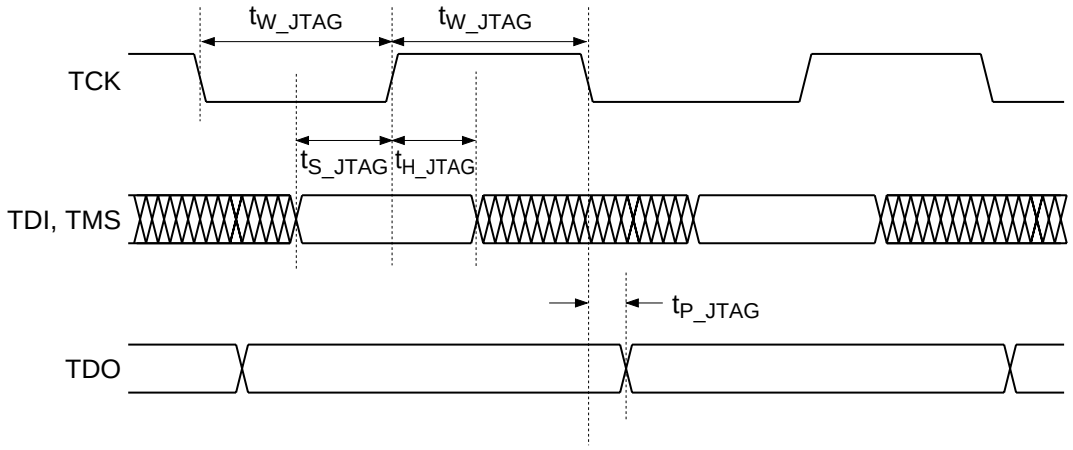


Figure 17 JTAG Timing

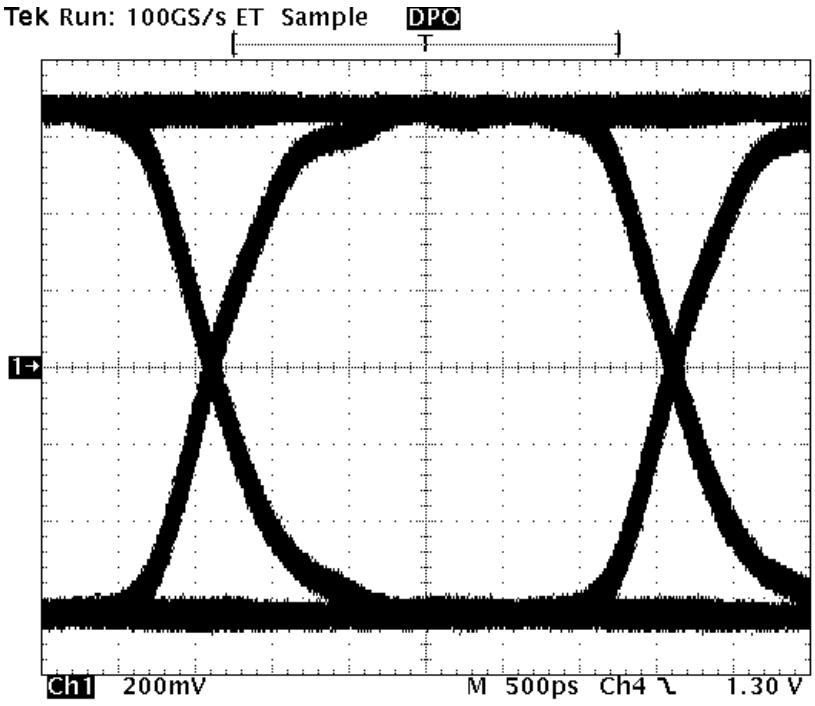


Figure 18 Typical Performance at 667 Mb/s with PRBS Data

5. Package and Pinout

5.1 Package Pinout

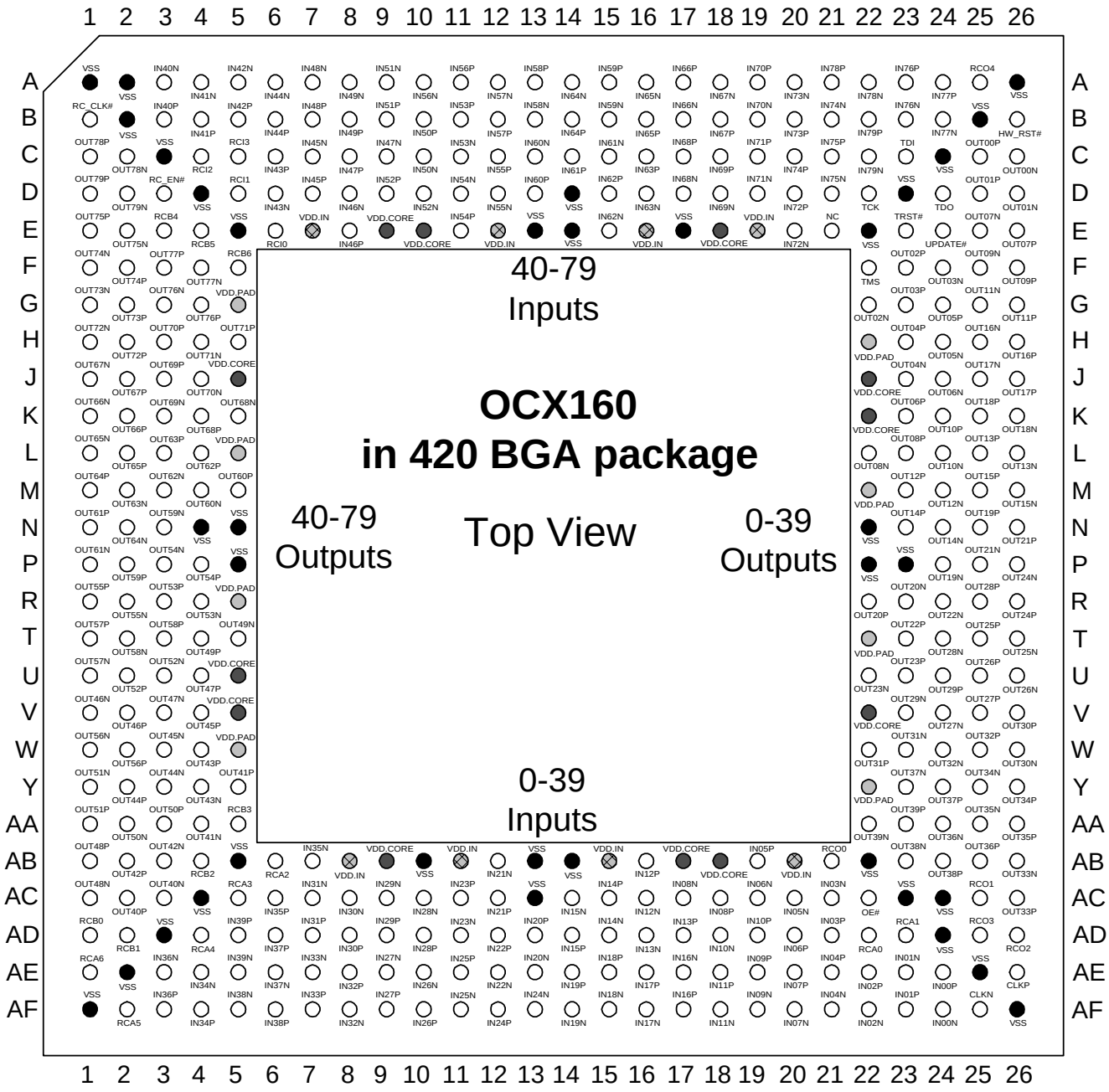


Figure 19 OCX160 Package Pinout

5.2 Pinout by Ball Sequence

Table 22 OCX160 Pinout By Ball Sequence

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A1	V_{SS}	B1	RC_CLK#	C1	OUT78P	D1	OUT79P	E1	OUT75P
A2	V_{SS}	B2	V_{SS}	C2	OUT78N	D2	OUT79N	E2	OUT75N
A3	IN40N	B3	IN40P	C3	V_{SS}	D3	RC_EN#	E3	RCB4
A4	IN41N	B4	IN41P	C4	RCI2	D4	V_{SS}	E4	RCB5
A5	IN42N	B5	IN42P	C5	RCI3	D5	RCI1	E5	V_{SS}
A6	IN44N	B6	IN44P	C6	IN43P	D6	IN43N	E6	RCI0
A7	IN48N	B7	IN48P	C7	IN45N	D7	IN45P	E7	V_{DD}.IN
A8	IN49N	B8	IN49P	C8	IN47P	D8	IN46N	E8	IN46P
A9	IN51N	B9	IN51P	C9	IN47N	D9	IN52P	E9	V_{DD}.CORE
A10	IN56N	B10	IN50P	C10	IN50N	D10	IN52N	E10	V_{DD}.CORE
A11	IN56P	B11	IN53P	C11	IN53N	D11	IN54N	E11	IN54P
A12	IN57N	B12	IN57P	C12	IN55P	D12	IN55N	E12	V_{DD}.IN
A13	IN58P	B13	IN58N	C13	IN60N	D13	IN60P	E13	V_{SS}
A14	IN64N	B14	IN64P	C14	IN61P	D14	V_{SS}	E14	V_{SS}
A15	IN59P	B15	IN59N	C15	IN61N	D15	IN62P	E15	IN62N
A16	IN65N	B16	IN65P	C16	IN63P	D16	IN63N	E16	V_{DD}.IN
A17	IN66P	B17	IN66N	C17	IN68P	D17	IN68N	E17	V_{SS}
A18	IN67N	B18	IN67P	C18	IN69P	D18	IN69N	E18	V_{DD}.CORE
A19	IN70P	B19	IN70N	C19	IN71P	D19	IN71N	E19	V_{DD}.IN
A20	IN73N	B20	IN73P	C20	IN74P	D20	IN72P	E20	IN72N
A21	IN78P	B21	IN74N	C21	IN75P	D21	IN75N	E21	NC
A22	IN78N	B22	IN79P	C22	IN79N	D22	TCK	E22	V_{SS}
A23	IN76P	B23	IN76N	C23	TDI	D23	V_{SS}	E23	TRST#
A24	IN77P	B24	IN77N	C24	V_{SS}	D24	TDO	E24	UPDATE#
A25	RCO4	B25	VSS	C25	OUT00P	D25	OUT01P	E25	OUT07N
A26	V_{SS}	B26	HW_RST#	C26	OUT00N	D26	OUT01N	E26	OUT07P

Table 22 OCX160 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
F1	OUT74N	G1	OUT73N	H1	OUT72N	J1	OUT67N	K1	OUT66N
F2	OUT74P	G2	OUT73P	H2	OUT72P	J2	OUT67P	K2	OUT66P
F3	OUT77P	G3	OUT76N	H3	OUT70P	J3	OUT69P	K3	OUT69N
F4	OUT77N	G4	OUT76P	H4	OUT71N	J4	OUT70N	K4	OUT68P
F5	RCB6	G5	V_{DD}.PAD	H5	OUT71P	J5	V_{DD}.CORE	K5	OUT68N
F22	TMS	G22	OUT02N	H22	V_{DD}.PAD	J22	V_{DD}.CORE	K22	V_{DD}.CORE
F23	OUT02P	G23	OUT03P	H23	OUT04P	J23	OUT04N	K23	OUT06P
F24	OUT03N	G24	OUT05P	H24	OUT05N	J24	OUT06N	K24	OUT10P
F25	OUT09N	G25	OUT11N	H25	OUT16N	J25	OUT17N	K25	OUT18P
F26	OUT09P	G26	OUT11P	H26	OUT16P	J26	OUT17P	K26	OUT18N
L1	OUT65N	M1	OUT64P	N1	OUT61P	P1	OUT61N	R1	OUT55P
L2	OUT65P	M2	OUT63N	N2	OUT64N	P2	OUT59P	R2	OUT55N
L3	OUT63P	M3	OUT62N	N3	OUT59N	P3	OUT54N	R3	OUT53P
L4	OUT62P	M4	OUT60N	N4	V_{SS}	P4	OUT54P	R4	OUT53N
L5	V_{DD}.PAD	M5	OUT60P	N5	V_{SS}	P5	V_{SS}	R5	V_{DD}.PAD
L22	OUT08N	M22	V_{DD}.PAD	N22	V_{SS}	P22	V_{SS}	R22	OUT20P
L23	OUT08P	M23	OUT12P	N23	OUT14P	P23	V_{SS}	R23	OUT20N
L24	OUT10N	M24	OUT12N	N24	OUT14N	P24	OUT19N	R24	OUT22N
L25	OUT13P	M25	OUT15P	N25	OUT19P	P25	OUT21N	R25	OUT28P
L26	OUT13N	M26	OUT15N	N26	OUT21P	P26	OUT24N	R26	OUT24P
T1	OUT57P	U1	OUT57N	V1	OUT46N	W1	OUT56N	Y1	OUT51N
T2	OUT58N	U2	OUT52P	V2	OUT46P	W2	OUT56P	Y2	OUT44P
T3	OUT58P	U3	OUT52N	V3	OUT47N	W3	OUT45N	Y3	OUT44N
T4	OUT49P	U4	OUT47P	V4	OUT45P	W4	OUT43P	Y4	OUT43N
T5	OUT49N	U5	V_{DD}.CORE	V5	V_{DD}.CORE	W5	V_{DD}.PAD	Y5	OUT41P
T22	V_{DD}.PAD	U22	OUT23N	V22	V_{DD}.CORE	W22	OUT31P	Y22	V_{DD}.PAD
T23	OUT22P	U23	OUT23P	V23	OUT29N	W23	OUT31N	Y23	OUT37N
T24	OUT28N	U24	OUT29P	V24	OUT27N	W24	OUT32N	Y24	OUT37P
T25	OUT25P	U25	OUT26P	V25	OUT27P	W25	OUT32P	Y25	OUT34N
T26	OUT25N	U26	OUT26N	V26	OUT30P	W26	OUT30N	Y26	OUT34P
AA1	OUT51P								
AA2	OUT50N								
AA3	OUT50P								
AA4	OUT41N								
AA5	RCB3								
AA22	OUT39N								
AA23	OUT39P								
AA24	OUT36N								
AA25	OUT35N								
AA26	OUT35P								

Table 22 OCX160 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AB1	OUT48P	AC1	OUT48N	AD1	RCB0	AE1	RCA6	AF1	V_{SS}
AB2	OUT42P	AC2	OUT40P	AD2	RCB1	AE2	V_{SS}	AF2	RCA5
AB3	OUT42N	AC3	OUT40N	AD3	V_{SS}	AE3	IN36N	AF3	IN36P
AB4	RCB2	AC4	V_{SS}	AD4	RCA4	AE4	IN34N	AF4	IN34P
AB5	V_{SS}	AC5	RCA3	AD5	IN39P	AE5	IN39N	AF5	IN38N
AB6	RCA2	AC6	IN35P	AD6	IN37P	AE6	IN37N	AF6	IN38P
AB7	IN35N	AC7	IN31N	AD7	IN31P	AE7	IN33N	AF7	IN33P
AB8	V_{DD}.IN	AC8	IN30N	AD8	IN30P	AE8	IN32P	AF8	IN32N
AB9	V_{DD}.CORE	AC9	IN29N	AD9	IN29P	AE9	IN27N	AF9	IN27P
AB10	V_{SS}	AC10	IN28N	AD10	IN28P	AE10	IN26N	AF10	IN26P
AB11	V_{DD}.IN	AC11	IN23P	AD11	IN23N	AE11	IN25P	AF11	IN25N
AB12	IN21N	AC12	IN21P	AD12	IN22P	AE12	IN22N	AF12	IN24P
AB13	V_{SS}	AC13	V_{SS}	AD13	IN20P	AE13	IN20N	AF13	IN24N
AB14	V_{SS}	AC14	IN15N	AD14	IN15P	AE14	IN19P	AF14	IN19N
AB15	V_{DD}.IN	AC15	IN14P	AD15	IN14N	AE15	IN18P	AF15	IN18N
AB16	IN12P	AC16	IN12N	AD16	IN13N	AE16	IN17P	AF16	IN17N
AB17	V_{DD}.CORE	AC17	IN08N	AD17	IN13P	AE17	IN16N	AF17	IN16P
AB18	V_{DD}.CORE	AC18	IN08P	AD18	IN10N	AE18	IN11P	AF18	IN11N
AB19	IN05P	AC19	IN06N	AD19	IN10P	AE19	IN09P	AF19	IN09N
AB20	V_{DD}.IN	AC20	IN05N	AD20	IN06P	AE20	IN07P	AF20	IN07N
AB21	RCO0	AC21	IN03N	AD21	IN03P	AE21	IN04P	AF21	IN04N
AB22	V_{SS}	AC22	OE#	AD22	RCA0	AE22	IN02P	AF22	IN02N
AB23	OUT38N	AC23	V_{SS}	AD23	RCA1	AE23	IN01N	AF23	IN01P
AB24	OUT38P	AC24	V_{SS}	AD24	V_{SS}	AE24	IN00P	AF24	IN00N
AB25	OUT36P	AC25	RCO1	AD25	RCO3	AE25	V_{SS}	AF25	CLKN
AB26	OUT33N	AC26	OUT33P	AD26	RCO2	AE26	CLKP	AF26	V_{SS}

5.3 Pinout by Ball Name

Table 23 OCX160 Pinout By Ball Name

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
CLKN	AF25	IN20N	AE13	IN42N	A5	IN64N	A14	OUT05P	G24
CLKP	AE26	IN20P	AD13	IN42P	B5	IN64P	B14	OUT06N	J24
OE#	AC22	IN21N	AB12	IN43N	D6	IN65N	A16	OUT06P	K23
HW_RST#	B26	IN21P	AC12	IN43P	C6	IN65P	B16	OUT07N	E25
IN00N	AF24	IN22N	AE12	IN44N	A6	IN66N	B17	OUT07P	E26
IN00P	AE24	IN22P	AD12	IN44P	B6	IN66P	A17	OUT08N	L22
IN01N	AE23	IN23N	AD11	IN45N	C7	IN67N	A18	OUT08P	L23
IN01P	AF23	IN23P	AC11	IN45P	D7	IN67P	B18	OUT09N	F25
IN02N	AF22	IN24N	AF13	IN46N	D8	IN68N	D17	OUT09P	F26
IN02P	AE22	IN24P	AF12	IN46P	E8	IN68P	C17	OUT10N	L24
IN03N	AC21	IN25N	AF11	IN47N	C9	IN69N	D18	OUT10P	K24
IN03P	AD21	IN25P	AE11	IN47P	C8	IN69P	C18	OUT11N	G25
IN04N	AF21	IN26N	AE10	IN48N	A7	IN70N	B19	OUT11P	G26
IN04P	AE21	IN26P	AF10	IN48P	B7	IN70P	A19	OUT12N	M24
IN05N	AC20	IN27N	AE9	IN49N	A8	IN71N	D19	OUT12P	M23
IN05P	AB19	IN27P	AF9	IN49P	B8	IN71P	C19	OUT13N	L26
IN06N	AC19	IN28N	AC10	IN50N	C10	IN72N	E20	OUT13P	L25
IN06P	AD20	IN28P	AD10	IN50P	B10	IN72P	D20	OUT14N	N24
IN07N	AF20	IN29N	AC9	IN51N	A9	IN73N	A20	OUT14P	N23
IN07P	AE20	IN29P	AD9	IN51P	B9	IN73P	B20	OUT15N	M26
IN08N	AC17	IN30N	AC8	IN52N	D10	IN74N	B21	OUT15P	M25
IN08P	AC18	IN30P	AD8	IN52P	D9	IN74P	C20	OUT16N	H25
IN09N	AF19	IN31N	AC7	IN53N	C11	IN75N	D21	OUT16P	H26
IN09P	AE19	IN31P	AD7	IN53P	B11	IN75P	C21	OUT17N	J25
IN10N	AD18	IN32N	AF8	IN54N	D11	IN76N	B23	OUT17P	J26
IN10P	AD19	IN32P	AE8	IN54P	E11	IN76P	A23	OUT18N	K26
IN11N	AF18	IN33N	AE7	IN55N	D12	IN77N	B24	OUT18P	K25
IN11P	AE18	IN33P	AF7	IN55P	C12	IN77P	A24	OUT19N	P24
IN12N	AC16	IN34N	AE4	IN56N	A10	IN78N	A22	OUT19P	N25
IN12P	AB16	IN34P	AF4	IN56P	A11	IN78P	A21	OUT20N	R23
IN13N	AD16	IN35N	AB7	IN57N	A12	IN79N	C22	OUT20P	R22
IN13P	AD17	IN35P	AC6	IN57P	B12	IN79P	B22	OUT21N	P25
IN14N	AD15	IN36N	AE3	IN58N	B13	NC	E21	OUT21P	N26
IN14P	AC15	IN36P	AF3	IN58P	A13	OUT00N	C26	OUT22N	R24
IN15N	AC14	IN37N	AE6	IN59N	B15	OUT00P	C25	OUT22P	T23
IN15P	AD14	IN37P	AD6	IN59P	A15	OUT01N	D26	OUT23N	U22
IN16N	AE17	IN38N	AF5	IN60N	C13	OUT01P	D25	OUT23P	U23
IN16P	AF17	IN38P	AF6	IN60P	D13	OUT02N	G22	OUT24N	P26
IN17N	AF16	IN39N	AE5	IN61N	C15	OUT02P	F23	OUT24P	R26
IN17P	AE16	IN39P	AD5	IN61P	C14	OUT03N	F24	OUT25N	T26
IN18N	AF15	IN40N	A3	IN62N	E15	OUT03P	G23	OUT25P	T25
IN18P	AE15	IN40P	B3	IN62P	D15	OUT04N	J23	OUT26N	U26
IN19N	AF14	IN41N	A4	IN63N	D16	OUT04P	H23	OUT26P	U25
IN19P	AE14	IN41P	B4	IN63P	C16	OUT05N	H24	OUT27N	V24

Table 23 OCX160 Pinout By Ball Name *(Continued)*

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
OUT27P	V25	OUT51N	Y1	OUT74P	F2	V_{DD}.CORE	K22	V_{SS}	AB14
OUT28N	T24	OUT51P	AA1	OUT75N	E2	V_{DD}.CORE	U5	V_{SS}	AB22
OUT28P	R25	OUT52N	U3	OUT75P	E1	V_{DD}.CORE	V5	V_{SS}	AC4
OUT29N	V23	OUT52P	U2	OUT76N	G3	V_{DD}.CORE	V22	V_{SS}	AC13
OUT29P	U24	OUT53N	R4	OUT76P	G4	V_{DD}.CORE	AB9	V_{SS}	AC23
OUT30N	W26	OUT53P	R3	OUT77N	F4	V_{DD}.CORE	AB17	V_{SS}	AC24
OUT30P	V26	OUT54N	P3	OUT77P	F3	V_{DD}.CORE	AB18	V_{SS}	AD3
OUT31N	W23	OUT54P	P4	OUT78N	C2	V_{DD}.IN	E7	V_{SS}	AD24
OUT31P	W22	OUT55N	R2	OUT78P	C1	V_{DD}.IN	E12	V_{SS}	AE2
OUT32N	W24	OUT55P	R1	OUT79N	D2	V_{DD}.IN	E16	V_{SS}	AE25
OUT32P	W25	OUT56N	W1	OUT79P	D1	V_{DD}.IN	E19	V_{SS}	AF1
OUT33N	AB26	OUT56P	W2	RCI2	C4	V_{DD}.IN	AB8	V_{SS}	AF26
OUT33P	AC26	OUT57N	U1	RCI3	C5	V_{DD}.IN	AB11		
OUT34N	Y25	OUT57P	T1	RCA0	AD22	V_{DD}.IN	AB15		
OUT34P	Y26	OUT58N	T2	RCA1	AD23	V_{DD}.IN	AB20		
OUT35N	AA25	OUT58P	T3	RCA2	AB6	V_{DD}.PAD	G5		
OUT35P	AA26	OUT59N	N3	RCA3	AC5	V_{DD}.PAD	H22		
OUT36N	AA24	OUT59P	P2	RCA4	AD4	V_{DD}.PAD	L5		
OUT36P	AB25	OUT60N	M4	RCA5	AF2	V_{DD}.PAD	M22		
OUT37N	Y23	OUT60P	M5	RCA6	AE1	V_{DD}.PAD	R5		
OUT37P	Y24	OUT61N	P1	RCB0	AD1	V_{DD}.PAD	T22		
OUT38N	AB23	OUT61P	N1	RCB1	AD2	V_{DD}.PAD	W5		
OUT38P	AB24	OUT62N	M3	RCB2	AB4	V_{DD}.PAD	Y22		
OUT39N	AA22	OUT62P	L4	RCB3	AA5	V_{SS}	A1		
OUT39P	AA23	OUT63N	M2	RCB4	E3	V_{SS}	A2		
OUT40N	AC3	OUT63P	L3	RCB5	E4	V_{SS}	A26		
OUT40P	AC2	OUT64N	N2	RCB6	F5	V_{SS}	B2		
OUT41N	AA4	OUT64P	M1	RC_CLK#	B1	V_{SS}	B25		
OUT41P	Y5	OUT65N	L1	RC_EN#	D3	V_{SS}	C3		
OUT42N	AB3	OUT65P	L2	RCI0	E6	V_{SS}	C24		
OUT42P	AB2	OUT66N	K1	RCI1	D5	V_{SS}	D4		
OUT43N	Y4	OUT66P	K2	RCO4	A25	V_{SS}	D14		
OUT43P	W4	OUT67N	J1	RCO0	AB21	V_{SS}	D23		
OUT44N	Y3	OUT67P	J2	RCO1	AC25	V_{SS}	E5		
OUT44P	Y2	OUT68N	K5	RCO2	AD26	V_{SS}	E13		
OUT45N	W3	OUT68P	K4	RCO3	AD25	V_{SS}	E14		
OUT45P	V4	OUT69N	K3	TCK	D22	V_{SS}	E17		
OUT46N	V1	OUT69P	J3	TDI	C23	V_{SS}	E22		
OUT46P	V2	OUT70N	J4	TDO	D24	V_{SS}	N4		
OUT47N	V3	OUT70P	H3	TMS	F22	V_{SS}	N5		
OUT47P	U4	OUT71N	H4	TRST#	E23	V_{SS}	N22		
OUT48N	AC1	OUT71P	H5	UPDATE#	E24	V_{SS}	P5		
OUT48P	AB1	OUT72N	H1	V_{DD}.CORE	E9	V_{SS}	P22		
OUT49N	T5	OUT72P	H2	V_{DD}.CORE	E10	V_{SS}	P23		
OUT49P	T4	OUT73N	G1	V_{DD}.CORE	E18	V_{SS}	AB5		
OUT50N	AA2	OUT73P	G2	V_{DD}.CORE	J5	V_{SS}	AB10		
OUT50P	AA3	OUT74N	F1	V_{DD}.CORE	J22	V_{SS}	AB13		

5.4 Package Dimensions

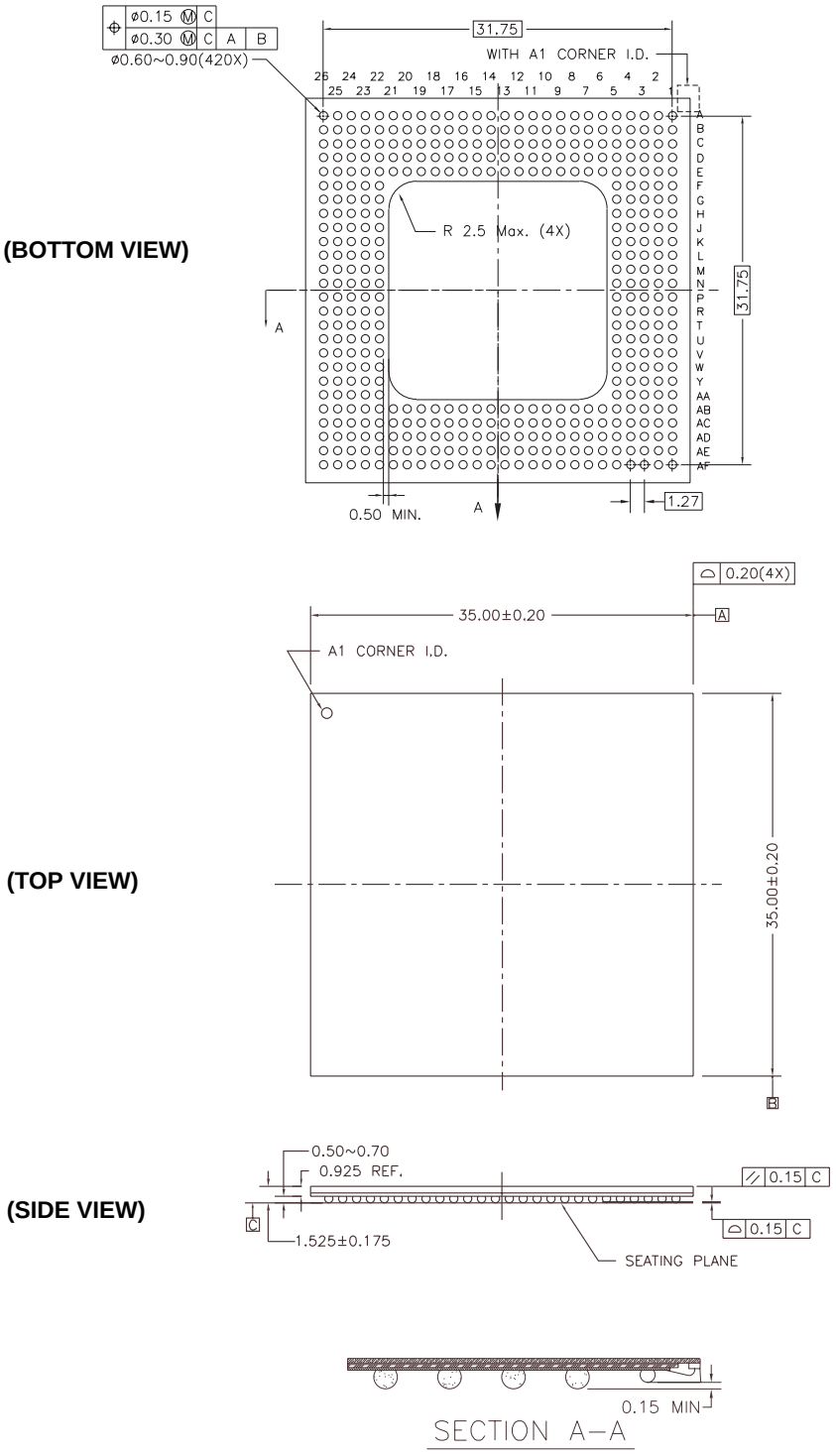


Figure 20 OCX160 Package—Bottom, Top and Side Views

5.5 Package Thermal Characteristics

Table 24 Package Thermal Coefficients

Package	Pin Count	Θ_{JC}(C/W)	Θ_{JA}($^{\circ}$C/W) Still Air
PBGA	420	1.7°C/W	12°C/W

NOTE:

1. Thermal performance values are based on simulation data.

6. Power Consumption

There are two main factors to consider when calculating power consumption for the OCX160:

- Power consumed by the chip
- Power dissipated by the terminating resistors at the switch differential outputs

The first component, chip power, consists of three integral elements (refer to Figure 21):

1. **Input Power**—This element is fixed (always ON) due to the DC current for differential outputs.
2. **Core Power**—This element is the same for LVDS or LVPECL outputs. Core power is a function of data rate (Mb/s) and the number of connection paths through the switch matrix.
3. **Output Power**—This element is a fixed amount for each differential output. The value is zero if the Output Enable (OE#) is disabled or set to OFF.

The second component, termination power, is the power dissipated by the terminating resistors at the switch differential outputs. The value is zero if the Output Enable (OE#) is disabled or set to OFF.

The following diagram shows the chip power elements (as described above), the formulas used for determining chip power, and the total power consumption as determined by the formula [**Chip Power** + **Termination Power**].

6.1 Power for LVDS I/O

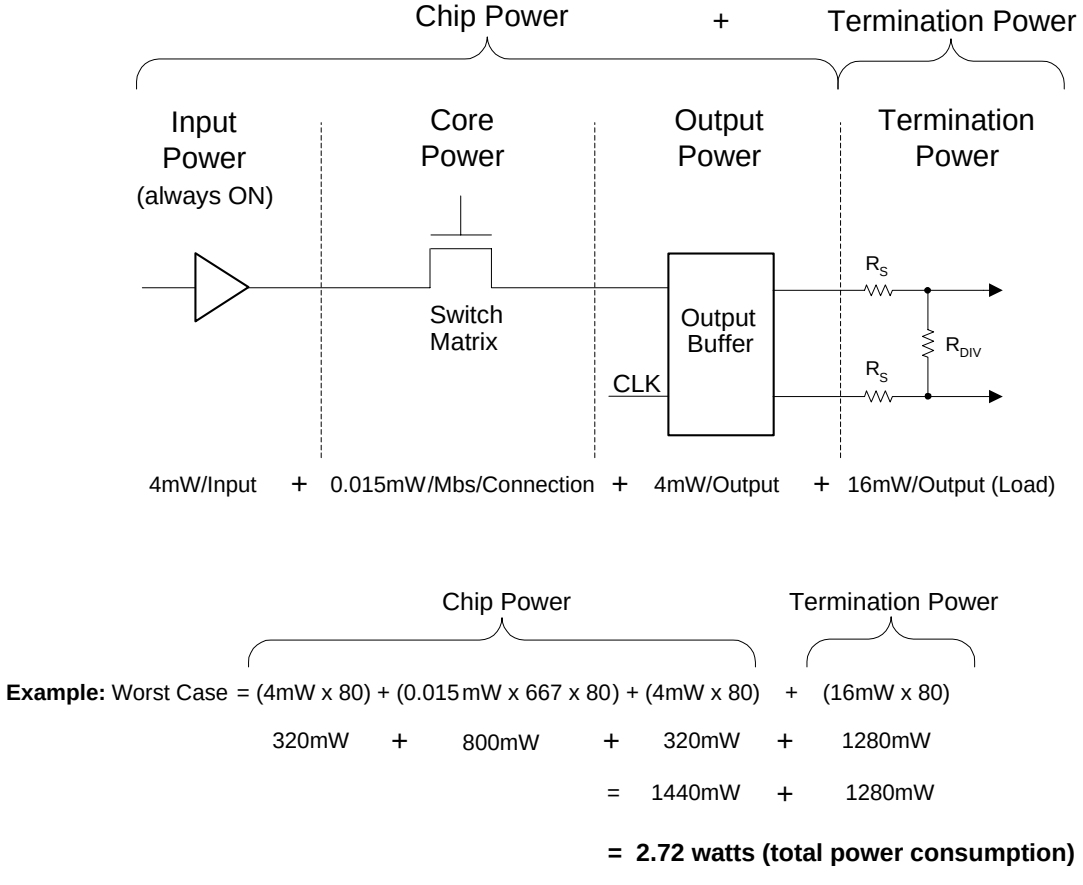


Figure 21 Power Consumption Diagram for the OCX160 using LVDS

6.2 Power for LVPECL I/O

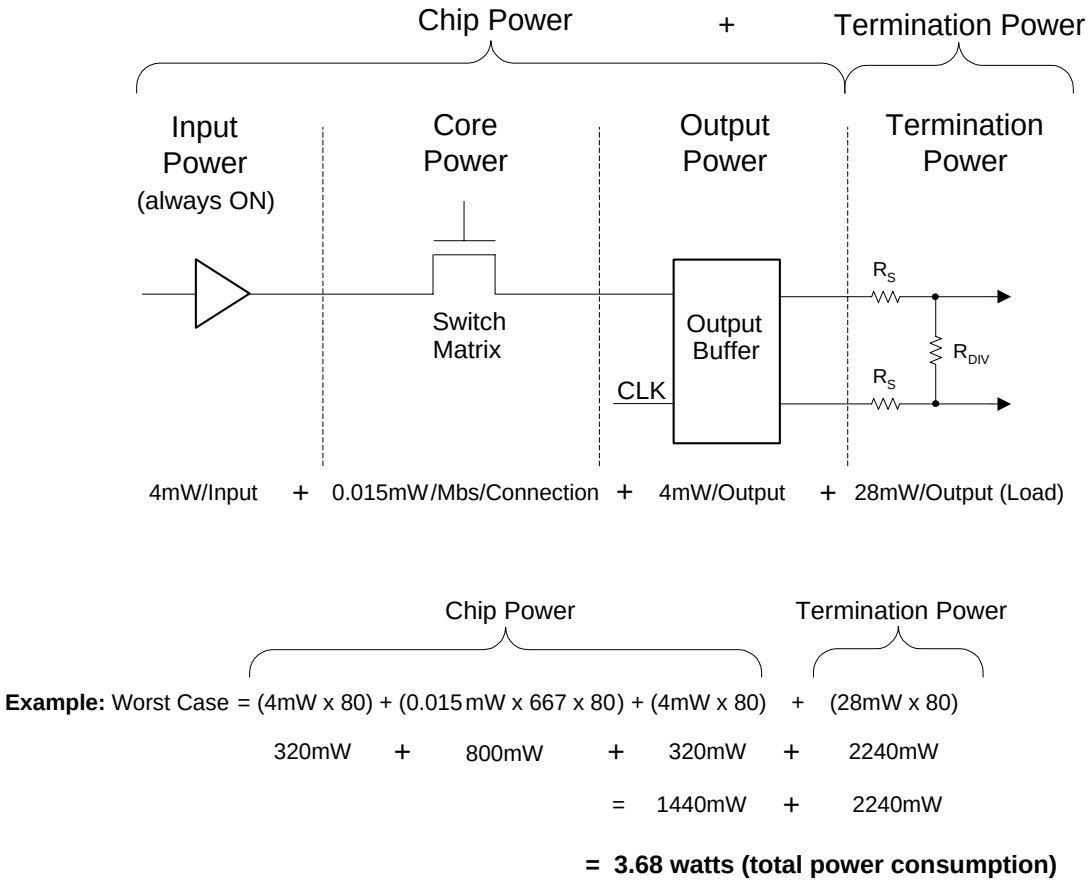
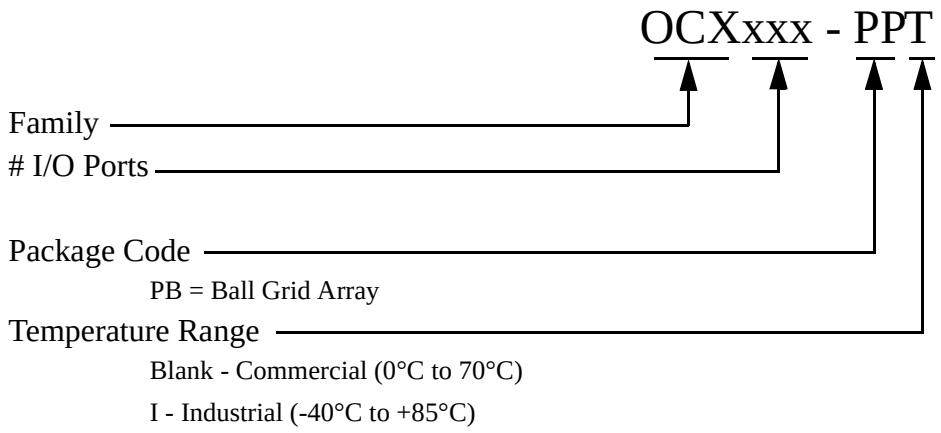


Figure 22 Power Consumption Diagram for the OCX160 using LVPECL

7. Component Availability and Ordering Information



8. Glossary

CLOCK: A single differential input used to gate data into registers in the Output Buffer. The input serves all outputs of the OCX. The neighbor input can also be used as a register clock.

CROSSPOINT: A single cell controlled by two RAM bits. The RAM bits are connected in a master-slave configuration to provide an update for programming and changing program information all at once.

CROSSPOINT ARRAY: An array of Crosspoint cells used to connect any input port to any output port.

INPUT OR OUTPUT PATH: The signal flow from pin to array and array to pin. Each path has a register with selectable clocks, drivers for the loaded outputs with selectable enables, and sense circuits to detect changes on either side of the IO Buffer.

NEXT NEIGHBOR: A physically adjacent port can be used as a clock source for an output configured in registered mode. These outputs are grouped in pairs such that the signal being switched through Output 0 can be used to clock the signal being switched through Output 1, or vice-versa. Any single clock or data input signal can be used to clock any other input signal provided they are switched to an appropriate output pair.

PORT: A name followed by a number to identify a pin on the device.

RAPIDCONFIGURE: A parallel programming method for the OCX devices. The RC mode uses 25 dedicated pins to program the Crosspoint Array and the IO Buffers. The 25 pins consist of an enable, a clock, four instruction bits, two seven-bit address fields, and a five-bit data field.

Revision History

Date/	Version No.	Description
6/16/2000	Revision 1.0	Initial release of “Advanced” datasheet
9/25/00	Revision 1.1	Additions include RCO output pin information, pinout drawing, pinout tables, package dimensions and illustration, duty-cycle diagram, thermal characteristics table, device reset options table, a section on configuring multiple devices, bitstream generation and downloading, JTAG information, and Power Consumption information/illustrations.
10/20/00	Revision 1.2	Corrections to RC Programming table. Additions/corrections to multiple tables and timing diagrams.
11/16/00	Revision 1.3	Updated RapidConfigure Read Cycle timing diagram so that RCO is relative to RC_CLK#; RCO was previously relative to RC_EN#. Replaced “+” on signal names to “P” and “-” to “N”. Corrected RCO[4:0] pin locations. Changed product status definition from Advanced to Preliminary.
11/21/00	Revision 1.4	Corrected Pinout drawing and Pinout tables to reflect that “P” and “N” are reversed on OUT40 to OUT79.
12/14/00	Revision 1.5	Corrections to Table 22 “Pinout By Ball Sequence” to match Pinout drawing—changed ball name on T4 and T5 from OUT49N and OUT49P to OUT49P and OUT49N respectively; ball # for IN07P corrected from AD20 to AE20. Corrections to Table 23 “Pinout By Ball Name” to match Pinout drawing—corrected IN07P ball # from AD20 to AE20; corrected OUT49P (T5) and OUT49N (T4) to be OUT49N (T5) and OUT49P (T4); corrected OUT50P (AA2) and OUT50N (AA3) to be OUT50N (AA2) and OUT50P (AA3).
1/20/2001	Revision 1.6	Changed the V_{IH}, V_{IL}, V_{OH}, and V_{OL} minimum and maximum values for LVPECL DC specifications in Table 20; added a note below table explaining the current values; changed Pass Transistor to proprietary high-performance buffering circuit.
8/6/2001	Revision 1.7	Added Eye diagram for typical performance at 667 Mb/s with PRBS data.
9/14/01	Revision 1.8	Added output jitter specifications.

9. Product Status Definition

Datasheet Identification	Product Status	Definition
Advanced	Formative or In Design	This datasheet contains the design specifications for product development. Specification may change in any manner without notice.
Preliminary	Preproduction Product	This datasheet contains the preliminary data, and supplementary data will be published at a later date. Fairchild reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Full Production	This datasheet contains final specifications. Fairchild reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	No longer in Production	This datasheet contains specifications for a product that has been discontinued by Fairchild. The datasheet is provided for reference information only.