

Introduction

Design constraints are one of the most important aspects of an FPGA design. Along with a good functional design, design constraints are directly tied to the success of device validation on the system board. FPGA designs also require thoughtful constraints to optimize the usage of FPGA resources. In ORCA devices and the ORCA Foundry design flow, device constraints are referred to as preferences. Preferences can be handled at multiple points in the ORCA Foundry design flow. This application note will discuss preferences, the preference file, and how it is used and managed for a successful ORCA design. For full details on any of the preferences covered in this application note please refer to Chapter 4: Logical and Physical Preferences of *Foundry Docs 2001*.

The Preference File (.prf)

The preference file (.prf) is an ASCII file that contains all of the design constraints for a user's ORCA FPGA design. Figure 1 shows a small preference file example.

Figure 1. Sample Preference File

```
FREQUENCY PORT "tx_clk" 50 MHz ;
FREQUENCY PORT "rx_clk" 50 MHz ;
INPUT_SETUP "port1" 1 NS CLKNET "tx_clk";
CLOCK_TO_OUT "port2" 8 NS CLKNET "rx_clk";
LOCATE COMP "port1" SITE "B17" ;
LOCATE COMP "port2" SITE "C16" ;
LOCATE COMP "tx_clk" SITE "B11" ;
LOCATE COMP "rx_clk" SITE "C13" ;
```

There are two types of preferences that users can apply, timing and location. Timing preferences are used to control the timed paths in an FPGA design. Location preferences are used to fix placement of design components in the FPGA array. The most common use of location preferences is fixing the I/O pinout.

Timing preferences can be assigned in two design domains; logical or physical. The logical domain consists of the design elements names in the EDIF. These names are based on the design's hierarchy level and register names. The physical domain consists of the physical ORCA elements that the technology mapper in ORCA Foundry has selected for the device implementation. These names can be cross referenced back to the original logical design, but at great complexity and time for the user. For this reason, most timing constraints in ORCA Foundry are done in the logical domain using logical preferences.

Location preferences in the preference file can only be applied to physical elements or components of the ORCA design. Location preferences are used by the place and routing tool which only works on the physical design after the technology mapper. This is why all location preferences must be in the physical domain. To make this process easier for designers, the technology mapper will keep top-level port names the same as found in the logical design (or EDIF). Fixing I/O pinouts using location preferences can be based on known component names.

The language used in the preference file also supports a feature known as "wildcards." Wildcarding provides the user the ability to assign preferences to multiple design elements without having to assign a preference to each element. For example, if the designer would like to apply a clock_to_out preference on an entire bus outa(31:0) the following preference could be utilized:

```
CLOCK_TO_OUT "outa*" 8 NS CLKNET "rx_clk" ;
```

Wildcarding is a powerful construct of the preference file syntax. More information on all supported wildcards can be found in Chapter 4 of *Foundry Docs 2001*.

It is possible in the preference file to create conflicts between preferences. This typically happens when a global preference covers a path that is covered specifically in another preference. In this situation, the more specific preference will be used for the specified path. If this situation arises where both preferences are at the same level, the preference that is last in the file will be used by the ORCA Foundry tool.

How the Preference File is Used

The preference file is used by ORCA Foundry to guide the tools while implementing the functional design from the EDIF. There are three tools in the ORCA Foundry design flow that use the preference file; MAP, PAR, and Trace (static timing analyzer/reporter).

The ORCA Foundry technology mapper (MAP) takes the logical design from the BUILD process and maps the logical elements to ORCA specific elements such as PFUs and PIOs. The preference file is used as an input to MAP. The mapper will filter the preference file to remove any syntax errors or invalid preferences. Invalid preferences are preferences that do not correspond to any logical or physical elements that are in the design. Invalid preferences are most often caused by a "typo" in the element name.

After the map operation, a new preference file is created by the mapper. This preference file contains all of the valid preferences contained in the input preference file as well as all of the preferences that were included in the EDIF file via the HDL. This preference file should then be used to proceed onto place and route and static timing analysis.

After the map process in the ORCA Foundry, design flow static timing analysis is done by Trace at the first checkpoint. Trace uses the preference file as an input and uses the timing constraints contained here in to produce a report file. The results of this report file should be considered before continuing on to place and route. Considerations include warnings, errors, and potential design issues, for example large logic delays.

Place and Route is done in ORCA Foundry by the tool PAR. PAR uses both location and timing preferences in the preference file as an input to drive the placement and routing of the design in the ORCA device. The output of PAR is a placed and routed design as well as a report and I/O pinout file.

Preference File Creation

Creating design constraints is a process that is continuously evolving throughout the design process. Certain constraints are utilized during the synthesis phase, and again more constraints are applied during place and routing. Finally constraints are added to the reporting tools to obtain more important information on the final design. Preferences can be applied at many points in the design flow process.

OFCC Constraints Editor

ORCA Foundry is driven by the ORCA Foundry Control Center (OFCC), which includes a constraints editor (CE). CE is a GUI-based tool that allows the designer to input logical preferences into a spreadsheet. The entries in the GUI are written out to the preference file being edited. CE can only be opened after the BUILD process and a logical design is available. A listing of design elements extracted from the logical design is provided inside CE. This list of design elements assists the user in identifying all of the elements in the design and applying constraints on them.

CE does not, however, cover all of the typical preferences that need to be assigned to an ORCA design. Typically users begin using CE to understand assigning constraints and the different aspects of their design and then move directly to edit the ASCII .prf file in a text editor.

CE does not support 100% of the preference file language. Do not try to open a preference file not created by CE into CE. Preferences that CE does not support may not be shown correctly or not shown at all. These incorrect preferences may be corrupt if the file is saved. A good rule to remember is that once a design has been modified outside CE, it should not be re-opened back inside CE.

Editing the .prf file in ASCII

Editing the preference file as simple ASCII text is the recommended way of working with the preference file once the user feels comfortable with the preference language and how to identify design elements. The ASCII file gives the user complete control over the types of preferences to assign (logical or physical) and full support of the preference file language.

HDL

Timing and location preferences can be assigned as attributes in HDL code. These preferences will be present in the EDIF file after synthesis and carried onto the preference file created by MAP. It is not recommended to place timing preferences into the HDL source code. It is recommended that if doing ORCA device floorplanning to use location attributes inside the HDL code. This topic is discussed in detail in technical note number TN1010, *ORCA Design Floorplanning*. SCUBA® can be utilized to create design elements in ORCA designs. If SCUBA is used to create a module, SCUBA may place preferences into the HDL code it generates. These preferences will be contained in the EDIF file and ultimately in the preference file after MAP.

Synthesis

Synthesis tools provide a mechanism for assigning design constraints specifically to the synthesis phase of the design. Synthesis results based on these applied constraints vary on the design and synthesis tool that is used. Tools such as Synplify and LeonardoSpectrum have the ability to create a preference file that can be used directly in ORCA Foundry. It is not recommended to use these preference files in ORCA Foundry. The preferences used by the synthesis tools are typically not optimal or up-to-date with current preference techniques and functions. Preference files created by synthesis tools are not compatible with the OFCC constraints editor. Do not try to utilize a synthesis tool preference file inside CE.

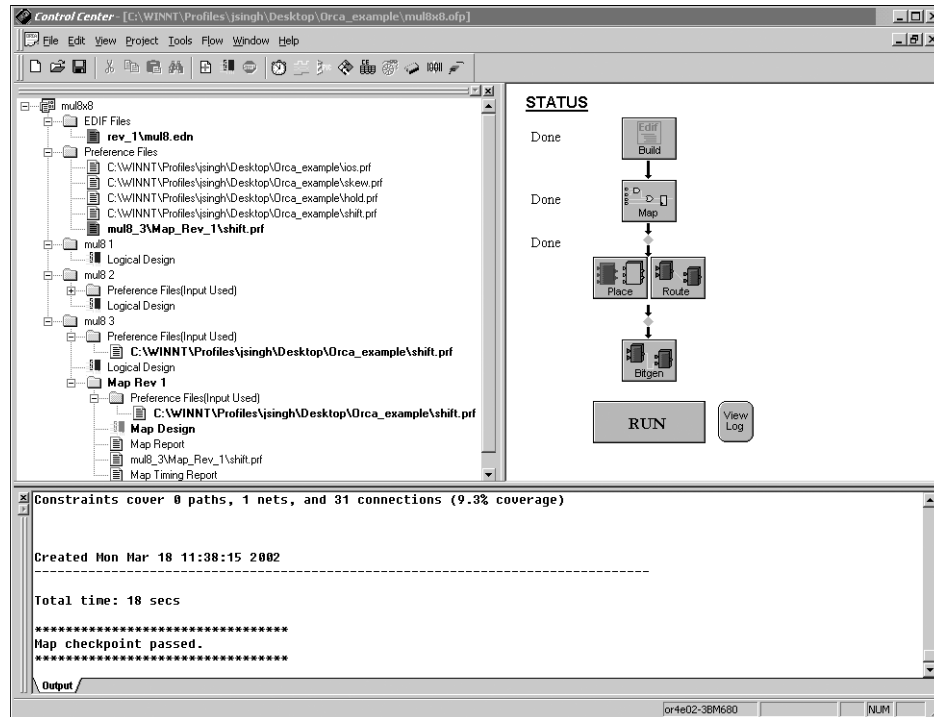
Design Flow Management with OFCC

ORCA Foundry Control Center is the design manager for ORCA Foundry that manages design revisions and tool flows. The preference file is also managed by OFCC in the project view under the section called "Preference Files". In this folder, OFCC will list all of the current preference files that are part of the current project. ORCA Foundry tools can only accept one preference file as an input on a given run. The user must select which of the preference files from the list will be used for a tool run. This preference file is known as the "Active" preference file and its icon is highlighted in red and its text is in bold. All of the other preference files in the project will not be used during the current run.

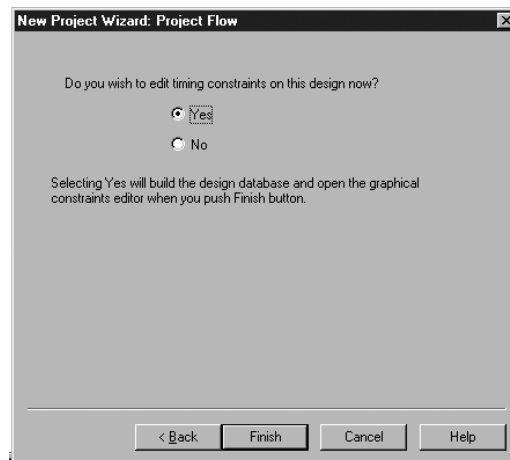
It is highly recommended that users have a master preference file that is located in the same directory as the project file (.ofp). This preference file is where all edits should take place. When the MAP tool is run it will use this preference file and create a new preference file. This new preference file from MAP will now contain all of the design constraints that have been applied in either the HDL or input preference file. All preferences that are produced from the EDIF design are contained in a special section of the preference file between SCHEMATIC START and SCHEMATIC END. This section is where MAP will write out any preferences that are found in the EDIF file. MAP has complete control over this section and the user should not include any preferences inside the block. The preference file from MAP should then be used for PAR since it now contains all of the design constraints.

Preference files can be added and removed from the OFCC project during any phase of the design flow. To add a preference file, select Project > Add File to Project from the menu bar or select the button on the toolbar. To remove a preference file from the preference group right-click on the preference file and in the pop-up menu select Remove. The user can also remove the preference file by simply selecting the preference file and pressing the Delete key on the keyboard. Both of these operations only remove the preference file from the project, they do not delete the file from the file system.

It is very common for users to have several preference files that are used for different aspects of the design. For example, one preference file is used for the basic tool flow (MAP, PAR). Another preference file may be used exclusively for static timing analysis reports for a closer look at I/O timing. OFCC provides the mechanism for this type of analysis to be performed.

Figure 2. OFCC Layout

When creating a new project in OFCC, a preference file can be included along with the EDIF file. Later in the project creation process the user is prompted to edit timing constraints.

Figure 3. New Project Wizard Window

If "Yes" is selected (in the window shown above in Fig. 3), OFCC will start the BUILD process and create the logical design. CE will automatically open allowing the user to input design constraints. When CE is closed the user will be prompted to save the preference file. When the file is saved the preference file will be listed in the "Preference Files" group in the project view and set as Active.

Editing the Preference File in OFCC

There are two methods of editing preference files in OFCC, CE or ASCII. As discussed CE is a good starting place for designers not familiar with the ORCA Foundry tool flow. Using CE users can build a foundation for how to iden-

tify design elements and assign preferences. CE can only be used after the BUILD process has been run. The logical design created by the BUILD process is where CE obtains all of the logical elements in the design.

CE can be opened in several ways:

- On the menu bar select Tools->Constraints Editor. This will open the constraints editor on the current Active preference file.
- On the tool bar select the icon for Constraints Editor. This will open the constraints editor on the current Active preference file.
- Double-Click on a preference file in the project view. This will open the constraints editor on the selected preference file.
- Right-Click on a preference file in the project view and select Open CE from the pop-up menu. This will open the constraints editor on the selected preference file.

Editing the preference file in ASCII mode is the recommended way of working with the preference file once the designer understands the ORCA preference language. To open the preference file for ASCII editing in OFCC, right-click on the preference file and select Open ASCII from the pop-up menu. This will open the selected preference file into a built in ASCII text editor in OFCC. OFCC also allows the user to select a third party text editor under Tools->Preferred Editor. If a third party text editor has been identified then the preference file will be opened externally to OFCC in this editor.

Typical Design Preferences

The full preference language includes many different design constraints from very global preferences to very specific preferences. As a new user this is a very large list to digest and utilize effectively. Listed here are the recommended preferences that should be applied to all designs.

- **Block Asynchronous Paths:** Prevents the timing tools from analyzing any timing paths to or from endpoints that are asynchronous.
- **Block RAM Reads during Write:** If using PFU based RAM, this will prevent timing analysis on a RAM read during a write on the same address in a single clock period.
- **Frequency/Period <net>:** Each clock net in the design should contain a frequency or period preference.
- **Input Setup:** Each clocked input should have an input_setup preference.
- **Clock-to-Out:** Each clocked output should have a clock_to_out preference.
- **Block <net>:** All asynchronous reset nets in the design should be blocked.
- **Multicycle:** The multicycle preference allows the designer to relax the timing constraints on selected paths to make place and route easier.

With these recommendations, the following is a complete example preference file.

Figure 4. Preference File Example

```

SCHEMATIC START ;
LOCATE COMP "tx_clk" SITE "A18" ;
LOCATE COMP "rx_clk" SITE "C15" ;
LOCATE COMP "rxsoc" SITE "D20" ;
LOCATE COMP "rxprty" SITE "B21" ;
LOCATE COMP "rxdata7" SITE "A22" ;
LOCATE COMP "rxdata6" SITE "B22" ;
LOCATE COMP "rxdata5" SITE "C22" ;
LOCATE COMP "rxdata4" SITE "D22" ;
LOCATE COMP "rxdata3" SITE "A19" ;
LOCATE COMP "rxdata2" SITE "B19" ;
LOCATE COMP "rxdata1" SITE "C19" ;
LOCATE COMP "rxdata0" SITE "D19" ;
LOCATE COMP "port_act" SITE "D31" ;
LOCATE COMP "f_sync_in" SITE "W30" ;
LOCATE COMP "txsoc" SITE "D14" ;
LOCATE COMP "txprty" SITE "B13" ;
LOCATE COMP "txdata7" SITE "A11" ;
LOCATE COMP "txdata6" SITE "B11" ;
LOCATE COMP "txdata5" SITE "B12" ;
LOCATE COMP "txdata4" SITE "C12" ;
LOCATE COMP "txdata3" SITE "A10" ;
LOCATE COMP "txdata2" SITE "B10" ;
LOCATE COMP "txdata1" SITE "C10" ;
LOCATE COMP "txdata0" SITE "D10" ;
SCHEMATIC END ;

BLOCK RD_DURING_WR_PATHS ;
BLOCK ASYNCPATHS ;
BLOCK NET "reset_n_int" ;
BLOCK NET "clear_stat" ;

FREQUENCY NET "tx_clk" 50 MHz ;
FREQUENCY NET "rx_clk" 50 MHz ;
FREQUENCY NET "fastclk" 80 MHz ;
FREQUENCY NET "slowclk" 20 MHz ;

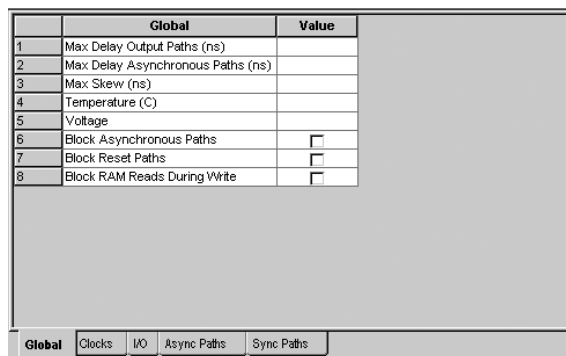
INPUT_SETUP ALLPORTS 1 ns CLKNET "tx_clk";
CLOCK_TO_OUT ALLPORTS 9 ns CLKNET "rx_clk";

MULTICYCLE "M1" START CLKNET "slowclk" END CLKNET "fastclk" 4 X ;
MULTICYCLE FROM CELL "ingress_clk_enable" 10 ns ;
MULTICYCLE TO CELL "rx_main_overhead_pipe*" 4X;

```

Commonly Used Preferences in Constraints Editor and ASCII

CE supports most of the recommended preferences that designers should use when constraining ORCA designs. CE is separated using TABs (Figure 5) into the following pages; Global, Clocks, I/O, Async Paths, and Sync Paths. The preferences supported under the Global TAB assign their constraints to the entire design. The Clocks section lists all of the clocks in the design and assigns preferences to a specific clock. I/O lists all of the top level inputs and output ports of the ORCA design. Pin location and timing constraints can then be assigned to these port names. Async Paths and Sync Paths allow the designer to create paths or select specific nets and assign asynchronous or synchronous preferences.

Figure 5. The Constraint Editor in OFCC

Global

All of the preferences in the Global section of CE are applied to the entire design. These preferences will be overridden by more specific preferences such as clock_to_out and max delay on a specific net or path. The Global CE view and resulting ASCII text is shown in Figure 6.

Figure 6. Global Preferences Assignment in the Constraint Editor and ASCII Editor

	Global	Value
1	Max Delay Output Paths (ns)	
2	Max Delay Asynchronous Paths (ns)	
3	Max Skew (ns)	
4	Temperature (C)	79.0000
5	Voltage	1.5000
6	Block Asynchronous Paths	<input checked="" type="checkbox"/>
7	Block Reset Paths	<input checked="" type="checkbox"/>
8	Block RAM Reads During Write	<input checked="" type="checkbox"/>

```
TEMPERATURE 79.000000 C;
VOLTAGE 1.500000 V;
BLOCK ASYNCPATHS ;
BLOCK RESETPATHS ;
BLOCK RD_DURING_WR_PATHS
```

- **Max Delay Output Paths (ns):** Assigned to all paths that are specified as output paths in the design.
- **Max Delay Asynchronous Paths (ns):** Assigned to all paths that are specified as asynchronous in the design.
- **Max Skew (ns):** Reports the maximum signal skew between a driver and loads. This preference does not constrain the place and route and only serves as a reporting preference for static timing analysis.
- **Temperature (C) (Series 4 only):** Assigns an operating junction temperature to change the derating factor for static timing analysis. If no temperature is provided the default value of 85C is used.
- **Voltage (V) (Series 4 only):** Assigns a value of FPGA array core voltage to change the derating factor for static timing analysis. If no voltage is provided the default value of 1.425V is used.
- **Block Asynchronous Paths:** Blocks input setup for input ports constrained by a clock preference. Input_setup preferences override this preference for specific input ports.
- **Block Reset Paths:** Blocks timing constraints on all reset paths in the design.
- **Block RAM Reads During Write:** Blocks timing constraints on reading a PFU RAM location during a write to the same location. Typically RAMs do not require the ability to write and read the same location in a single clock cycle.

Clocks

The Clocks TAB of CE lists all of the clocks found in the ORCA design. ORCA Foundry identifies any signals that are connected to the clock pin of a synchronous element as a clock. This list can sometimes be surprising to the designer since HDL design can hide the "real" clocks in the design. The second column in the clocks window displays the number of clock loads on the identified clock net. Occasionally CE identifies single fanout clocks in the logical design that are not mapped to the physical design. The Clocks CE view and resulting ASCII text is shown in Figure 7.

Figure 7. Clock Preferences Assignment in the Constraint Editor and ASCII Editor

	Clock Net	Num Clk Loads	Frequency (MHz)	Period (ns)	High (ns)	Max Skew (ns)
1	CLK_c	37	110.0000			
2						

```
FREQUENCY NET "CLK_c" 110.000000 MHz ;
```

- **Frequency:** Assigns the minimum operating frequency for all sequential output to sequential input pins on the specified clock net. Can be used interchangeably with the period preference.
- **Period:** Assigns the minimum clock cycle for all sequential output to sequential input pins on a specified clock net. Can be used interchangeably with the frequency preference.
- **High (ns):** When constraining non-50% duty cycle clocks, this field is set to the number of ns the clock net is high. Can only be used with the period preference, not frequency. Default is a 50% duty cycle clock.
- **Max Skew (ns):** Reports the skew on a specified clock net. This preference does not constrain the place and route and only serves as a reporting preference for static timing analysis.

I/O

The I/O TAB of CE lists all of the top level inputs and outputs in the ORCA design as shown in Figure 8. Using this list the designer can fix the pin locations on the package and also define timing parameters for a specified I/O. CE does not support assigning preferences to I/O busses. In this instance it is easier to use the ASCII file and the wild-carding feature of the preference language. Another approach to grouping I/O ports is the ALLPORTS keyword. This is only supported in ASCII text and applies the timing constraints to all ports clocked on the specified clock net.

Figure 8. I/O Preferences Assignment in the Constraint Editor and ASCII Editor

	Port Name	Location	Input Setup (ns)	Clock To Out (ns)	Clock	Output Load (pF)
1	A_0					
2	A_1	B9	20.0000	10.0000	CLK_c	
3	A_2	C6	20.0000	10.0000	CLK_c	
4	A_3					
5	A_4					
6	A_5					
7	A_6					
8	A_7					
9	B_0					
10	B_1	B8	15.0000	10.0000	CLK_c	
11	B_2	C7	15.0000	10.0000	CLK_c	
12	B_3					
13	B_4					
14	B_5					

```

LOCATE COMP "A_1" SITE "B9" ;
INPUT_SETUP PORT "A_1" 20.000000 ns CLKNET "CLK_c" ;
CLOCK_TO_OUT PORT "A_1" 10.000000 ns CLKNET "CLK_c" ;
LOCATE COMP "A_2" SITE "C6" ;
INPUT_SETUP PORT "A_2" 20.000000 ns CLKNET "CLK_c" ;
CLOCK_TO_OUT PORT "A_2" 10.000000 ns CLKNET "CLK_c" ;
LOCATE COMP "B_1" SITE "B8" ;
INPUT_SETUP PORT "B_1" 15.000000 ns CLKNET "CLK_c" ;
CLOCK_TO_OUT PORT "B_1" 10.000000 ns CLKNET "CLK_c" ;
LOCATE COMP "B_2" SITE "C7" ;
INPUT_SETUP PORT "B_2" 15.000000 ns CLKNET "CLK_c" ;
CLOCK_TO_OUT PORT "B_2" 10.000000 ns CLKNET "CLK_c" ;

```

- **Location:** Assigns a port name to a specific pin location on the package. This package information can be found in the devices data sheet. If the pin location is not provided the place and route will assign this pin at its discretion and provide preferences for the pinout selected in the Pad Layout report.
- **Input Setup (ns):** Constrains the setup time requirement for a selected input port relative to a selected clock net. Hold times can not be specified in CE and must be done in ASCII.
- **Clock To Out (ns):** Constrains the maximum allowable output delay for a selected output port relative to a selected clock net.
- **Output Load (pF):** Assigns an output loading value on a selected output port which drives the place and route. The default output loading for Series 4 is 30pF.

Async Paths

The Async Paths TAB of CE allows the user to create a path or select a net to apply a preference. Typically asynchronous preferences are BLOCK preferences to block specific nets or paths from timing constraints. Examples of nets that can be blocked are asynchronous reset paths, static enables, static status bits, etc. The other preference that can be applied is MAXDELAY on a path or net. MAXDELAY assigns an asynchronous delay to constrain the place and route. Paths can also be created by selecting a from port and a to port. An example of the Async Paths CE view and ASCII text results is shown in Figure 9.

Figure 9. Async Paths Preferences Assignment in the Constraint Editor and ASCII Editor

	From	To	Net	Preference	Delay (ns)
1	A_0	Prod_0		Max Delay	14.0000
2				Max Delay	

```

MAXDELAY FROM PORT "A_0" TO PORT "Prod_0" 14.000000 ns;

```

Sync Paths

The Sync Paths TAB of CE allows the user to assign preferences relative to a specified clock. CE has limited support for the multicycle preference which is utilized for synchronous constraints. In the following examples, the ASCII text will be used to define several synchronous path constraints that are typically used.

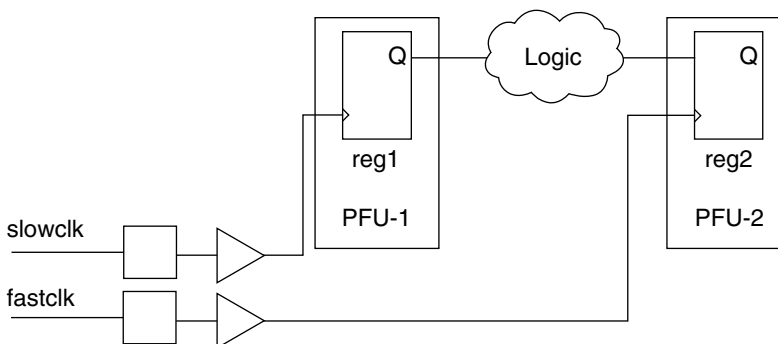
Example 1. Clock to Clock

It is common in today's large FPGA designs to have many clock domains interacting with each other. The static timing analysis tool in ORCA Foundry can constrain based on multiple clocks if given the information on the relationship of the two clocks. The multicycle preference can be used to specify this relationship. For multicycle preferences, all clocks identified in the preference line must also have a frequency or period preference to inform the tools of the frequency of this clock.

```
MULTICYCLE "m1" START CLKPORT "slowclk" END CLKPORT "fastclk" 4 X ;
```

This multicycle preference is used to inform the static timing tool that four clock cycles can be used for timing between the slowclk to the fastclk. Figure 10 shows the schematic view of this relationship. It is common to have a slow clock net for control logic and a fast clock net for the data path. In this example the slow clock to fast clock relationship does not need to occur in a single fast clock period.

Figure 10. Clock to Clock Multicycle Example



Example 2. Timing Relaxation

The multicycle preference is commonly used to relax a timing constraint on a specified path. This occurs when the frequency of the clock is running at a particular rate, but certain paths or nets do not need to run as fast. Typically when a design is having trouble meeting place and route requirements, designers will examine their design for paths that can be relaxed to give the place and route more flexibility with certain paths. This usually helps the place and route tool assign critical paths more resources.

In order to use the multicycle preference based on design elements, the design elements must first be identified. Multicycle preferences can be applied to ports or cells. Ports are I/O ports of the design which are easily identified. Cells are internal cell names that are created from the HDL hierarchy and synthesis. The easiest way to identify cells is via the Trace report (.twr). Figure 11 shows a typical trace report of a frequency preference.

Figure 11. Trace Report for Frequency Preference

```

=====
Preference: FREQUENCY NET "clk" 100.000000 MHz ;
          629 items scored, 0 timing errors detected.
-----

Passed: The following path meets requirements by 0.380ns

Logical Details: Cell type Pin type Cell name (clock net +/-)

Source: IO-FF In Q d_in_ab_p_0io_21 (from clk +)
Destination: FF Data in prbs_chk_inst/compare_ab_5 (to clk +)

Delay: 9.241ns (28.3% logic, 71.7% route), 2 logic levels.

Constraint Details:

    9.241ns physical path delay d_in_ab_21 to PFU_42 meets
    10.000ns delay constraint less
    0.175ns skew and
    0.204ns F4_SET requirement (totaling 9.621ns) by 0.380ns

Physical Path Details:

    Name Fanout Delay (ns) Site Resource
INREG_DEL --- 0.716 E33.SC to E33.INFF d_in_ab_21 (from clk)
ROUTE 3 4.173 E33.INFF to R17C27.K1_2 d_in_ab_p_21
HRIPCO_DEL --- 1.897 R17C27.K1_2 to R17C27.COUT PFU_11
ROUTE 1 2.455 R17C27.COUT to R11C18.K5_1
prbs_chk_inst/un48_compare_abneg3Z0Z_0 (to clk)
-----
          9.241 (28.3% logic, 71.7% route), 2 logic levels.

Clock Skew Details:

Source Clock:
    Delay Connection
    2.893ns ULPLL.MCLK to E33.SC

Destination Clock :
    Delay Connection
    2.718ns ULPLL.MCLK to R11C18.CLK1

Report: 103.950MHz is the maximum frequency for this preference.

```

Under the logical details section of the report is a column titled "Cell name". This column lists the cells, source and destinations, that are covered in this particular path. In this example, cell d_in_ab_p_0io_21 is the source and cell prbs_chk_inst/compare_ab_5 is the destination cell. A multicycle preference to relax this path to twice the delay appears below.

```
MULTICYCLE FROM CELL "d_in_ab_p_0io_21" TO CELL "prbs_chk_inst/compare_ab_5" 2X;
```

When the source or destination of a multicycle preference is an ASIC block such as an embedded block RAM (EBR) the multicycle preference syntax is different. Using the Trace report in Figure 12, the following example of a multicycle preference from a PFU flip-flop to an EBR is created.

Figure 12. Trace Report.

```
=====
Preference: FREQUENCY NET "clk" 100.000000 MHz ;
              734 items scored, 0 timing errors detected.
-----

Passed:  The following path meets requirements by 0.345ns

Logical Details:  Cell type  Pin type      Cell name  (clock net +/-)

Source:          FF          Q          enable_bp_map  (from clk +)
Destination:     BR512X18    Port    inst_qpram_512x18_2/qpram_512x180_0_0  (to clk +)
```

The PIN * wildcards all the pins on the ASIC block. The ASIC block name (the second string inside quotes) can not be wildcarded.

The following three examples reference Figure 13.

The first example relaxes all of the paths from cell "reg1" to cell "reg2" to be timed within four clock cycles of the clock "clk".

```
MULTICYCLE FROM CELL "reg1" TO CELL "reg2" CLKPORT="clk" 4 X;
```

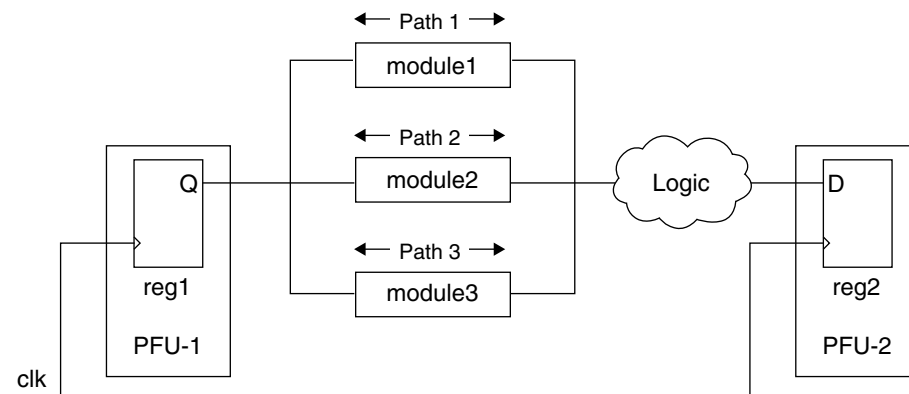
The next example relaxes all of the paths from cell "reg1" to cell "reg2" that also include the path through cell "module1" to be timed within four clock cycles of the clock "clk". This preference results with PATH1 being checked at 4X clk while PATH2 and PATH3 are checked at 1X clk.

```
MULTICYCLE FROM CELL "reg1" TO CELL "reg2" THROUGH CELL "module1" CLKPORT="clk"
4 X;
```

The next example relaxes all of the paths from cell "reg1" to cell "reg2" that do not include the path through cell "module2" to be timed within four clock cycles of the clock "clk". This preference results with PATH1 and PATH3 being checked at 4X clk while PATH2 is checked at 1X clk.

```
MULTICYCLE FROM CELL "reg1" TO CELL "reg2" EXCEPT CELL "module2" CLKPORT="clk" 4
X;
```

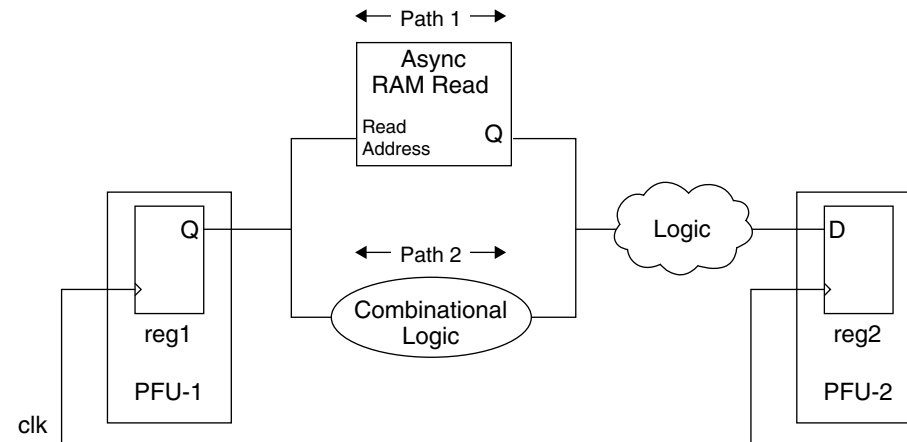
Figure 13. Relaxation Multicycle example for THROUGH and EXCEPT Preference Assignments



The next example references Figure 14 and relaxes all paths from cell "reg1" to cell "reg2" that go through a RAM read. This preference results with PATH1 being checked at 4X clk while PATH2 is checked at 1X clk.

```
MULTICYCLE FROM CELL "reg1" READPATHS TO CELL "reg2" CLKPORT="clk" 4 X;
```

Figure 14. Relaxation Multicycle example for READPATH



The last example shown below relaxes all paths from the bussed cell "rx_main_overhead*" to all of its destinations. In this design example the rx_main_overhead bus contains status information that is updated every 64 clock cycles, but is clocked on the same clock as the data path. This update clearly does not need to route in a single clock cycle and can be relaxed at least over four clock cycles.

```
MULTICYCLE FROM CELL "rx_main_overhead*" 4 X;
```

Example 3. Tightening Timing

The multicycle preference can also be used to tighten the timing constraints on a specified path. The example below is used to constrain all paths from cell "ingress_clk_enable" to 10ns. This cell is covered by a frequency preference of 50Mhz (20ns) on tx_clk. This particular cell and its fanout needs to run at 100Mhz (10ns).

```
MULTICYCLE FROM CELL "ingress_clk_enable" clknet="tx_clk" 10 ns;
```

Note: Please be aware that 0.5X is not interpreted as 1/2 X, but rather as 2X. Do not use a value less than 1X. Rather the absolute time as shown above.

Summary

Preferences can be assigned at a variety of places in the ORCA design flow. It is recommended that new users take advantage of CE in OFCC to start constraining their designs. Once that level of knowledge is acquired, the ASCII text file is the best approach for assigning new preferences. This document should serve as a starting point for understanding constraints in ORCA Foundry. For complete information on all of the preferences discussed here as well as all preferences available consult Chapter 4 Logical and Physical Preferences of *Foundry Docs 2001*.

Technical Support Assistance

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