OTC-045

35-BIT LED DISPLAY DRIVER

DATE：December 5, 2001

■ FEATURES

— CMOS technology
— Continuous brightness control
— Serial data input
— No load signal required
— Optional external data enable and reset
— Wide power supply operation (3.5V to 12V)
— TTL compatibility
— 34 or 35 outputs, 20mA sink capability
— Alphanumeric capability

■ APPLICATIONS

— Products with alphanumeric LED displays such as digital clock, counter, radio, multimeter, etc.
— Industrial control indicator or instrumentation readout
— Relay driver

■ ORDERING INFORMATION

PART NO.	PACKAGE	NOTE
OTC-045	-	CHIP FORM
OTC-045Q	44-PIN LQFP	-

OPTO TECH CORPORATION
NO.8 INNOVATION ROAD 1,
HSINCHU SCIENCE-BASED INDUSTRIAL PARK,
HSINCHU 30077, TAIWAN, R. O. C.

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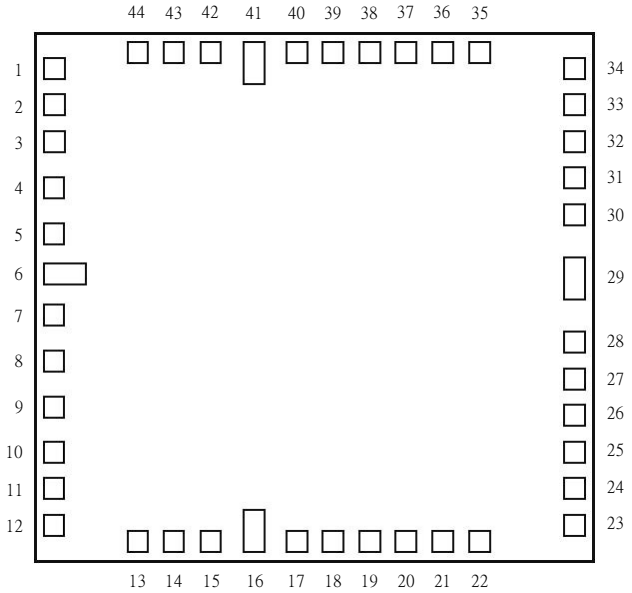
■ ABSOLUTE MAXIMUM RATINGS

Ta=+25℃, UNLESS OTHERWISE SPECIFIED			
CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	VDD	+3.5 ~ +12	V
Clock Frequency	FCLK	4M	Hz
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Input B.C. Current	IBC	700	μA
Output Sustaining Voltage	VDS	10	V
Output Continuous Current	IOUT	25	mA
Power Dissipation Per Output	PDISS	25	mW
Operating Temperature	TOPR	-40 ~ +85	℃
Storage Temperature	TSTR	-60 ~ +150	℃

■ PAD/PIN ASSIGNMENT (TOP VIEW)

— Pad Assignment (Chip Form)



1 :OUT3	16:VSS	31:OUT16
2 :OUT2	17:OUT29	32:OUT15
3 :OUT1	18:OUT28	33:OUT14
4 :RESET	19:OUT27	34:OUT13
5 :B.C.	20:OUT26	35:OUT12
6 :VDD	21:OUT25	36:OUT11
7 :CLK	22:OUT24	37:OUT10
8 :DATA IN	23:OUT23	38:OUT9
9 :$\overline{ENB}$	24:OUT22	39:OUT8
10:OUT35	25:OUT21	40:OUT7
11:OUT34	26:OUT20	41:VSS
12:OUT33	27:OUT19	42:OUT6
13:OUT32	28:OUT18	43:OUT5
14:OUT31	29:VSS	44:OUT4
15:OUT30	30:OUT17	

Die Size：2770um × 2610um (W × H)

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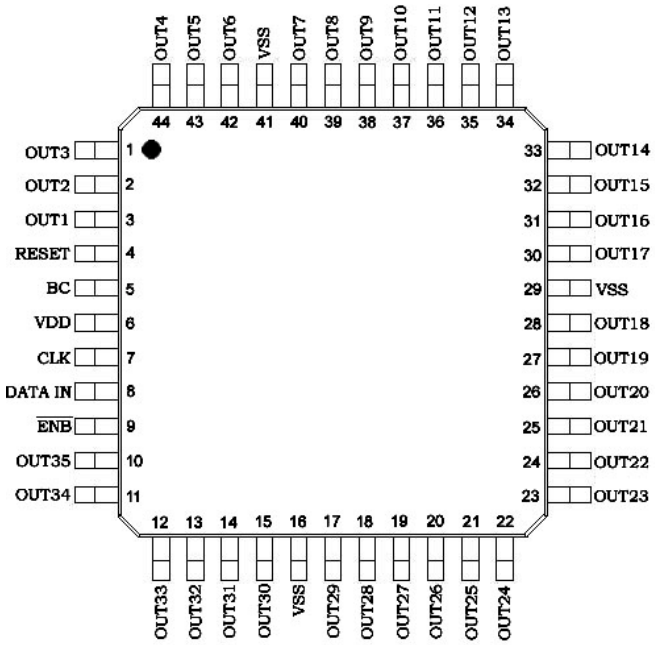
— Pin Assignment (LQFP)



■ PAD/PIN DESCRIPTIONS

PIN NO.	PAD/PIN NAME	TYPE	DESCRIPTION
6	VDD	Power	Power
16,29,41	VSS	Ground	Ground
4	RESET	Input	Reset signal input, (Normally grounded)
5	B.C.	Input	DC current input for LED brightness control
7	CLK	Input	Clock input
8	DATA IN	Input	Serial data input
9	$\overline{\text{ENB}}$	Input	Data input enable, (Normally grounded)
1,2,3;10~15 17~28;30~40 42,43,44	OUT1~OUT35	Output	Open-drain NMOS output drivers

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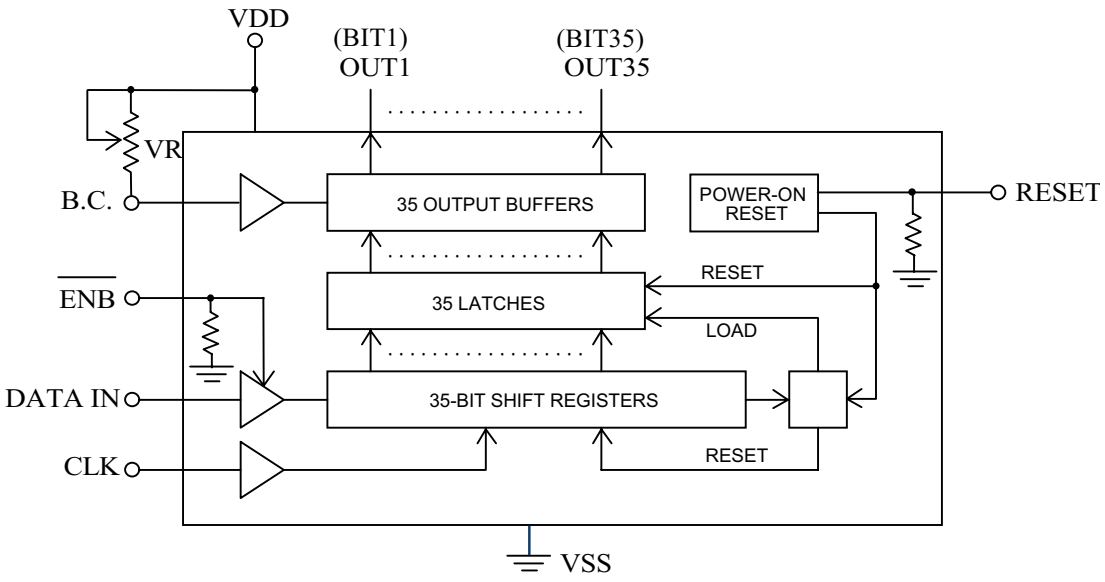
■ FUNCTION BLOCK DIAGRAM



■ FUNCTION DESCRIPTIONS

The OTC-045 is designed to drive either 4 or 5-digit, common anode alphanumeric LED displays with the added benefit of requiring minimal interface with the display or data source.

Data is transferred serially via 2 signals: clock and serial data. Data transfer without the added inconvenience of an external load signal is accomplished by using a format of a leading "1" followed by the allowed 35 data bits. These 35 data bits are latched after the 36th clock has been transferred. This scheme provides non-multiplexed, direct drive to the LED display. Characters currently displayed (thus, data output) changes only if the serial data bits differ from those previously transferred. Display brightness is determined by control of the output current for LED displays. This control function can be achieved by varying the current flowing into B.C. terminal. A simple way is to set an external variable resistor illustrated in the block diagram. Typically, the output current is 36 times greater that current into B.C. terminal.

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Figure 1 shows the input data format. A leading "1" is followed by 35 bits of data. After the 36th had been transferred, a load signal is generated synchronously with the clock high state. This loads the 35 bits of data into the latches. A reset signal is generated consecutively with the clock low, which clears all shift registers for the next set of data. All shift registers are static master-slave, with no clear for the master portion of the first register, allowing continuous operation. There must be a complete 36 clocks or the shift registers will not clear.

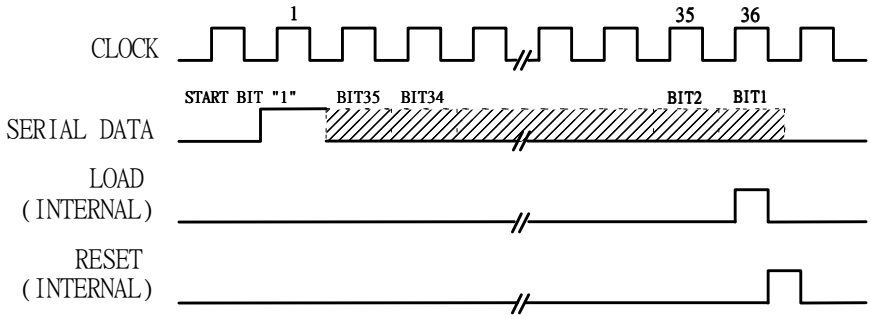
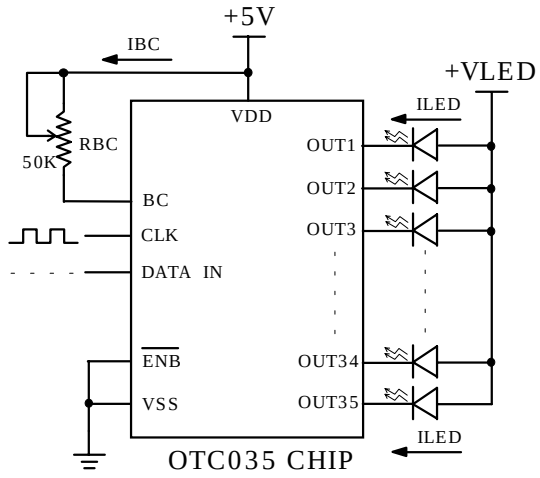


FIG.1 INPUT DATA FORMAT

When the chip first powers on an transient high state of internal power on reset signal is generated which clears all shift registers and latches. The start bit and the first clock return the chip to its normal operation. The 'RESET' input terminal is also available for an option to clear all shift registers and latches by an external pulse.

■ TYPICAL APPLICATION CIRCUIT



IBC = (VDD−VBC) / RBC

ILED = 36 * IBC

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■ RECOMMENDED OPERATING CONDITIONS

VDD=+5V, Ta=+25℃, UNLESS OTHERWISE SPECIFIED					
CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	VDD	4.5	5	9	V
Clock Frequency	FCLK	-	500K	2M	Hz
Input B.C. Current	IBC	0	-	550	μA
Output Sustaining Voltage	VDS	-	-	9	V
Output Continuous Current	IOUT	-	-	20	mA
Power Dissipation Per Output	PDISS	-	-	20	mW

■ DC ELECTRICAL CHARACTERISTICS

VDD=+5V, Ta=+25℃, UNLESS OTHERWISE SPECIFIED					
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply,VDD		3.5	-	12	V
Power Supply Current	VDD=5V, Excluding output	-	-	5	mA
Logic Input Voltages,V_{IH}	VDD=5V	0.8VDD	VDD	VDD+0.3	V
V_{IL}	VDD=5V	VSS-0.3	VSS	0.2VDD	V
Brightness Input,I_{BC}		0	-	550	μA
Brightness Input Voltage	Input Current,I_{BC}=550μA	3.0	3.2	4.0	V
Output Current, $I_{OUT(OFF)}$	VOUT=3.0V	-	-	<0.5	μA
Output Current, $I_{OUT(ON)}$	VOUT=1.0V	0	-	22	mA
	Brightness Input=0μA	0	-	<0.5	μA
	Brightness Input=100μA	3.5	3.6	3.7	mA
	Brightness Input=550μA	20	21	22	mA
Output Matching		-	-	5	%
Clock Input Frequency, F_{CLK}		-	500K	2M	Hz

NOTE 1：Output matching is calculated as the percent variation of each $I_{OUT(ON)}$ to $I_{OUT(AVG)}$, where $I_{OUT(AVG)} = \{\sum_{n=1}^{35} I_{OUT(ON)}[BITn]\} \div 35$

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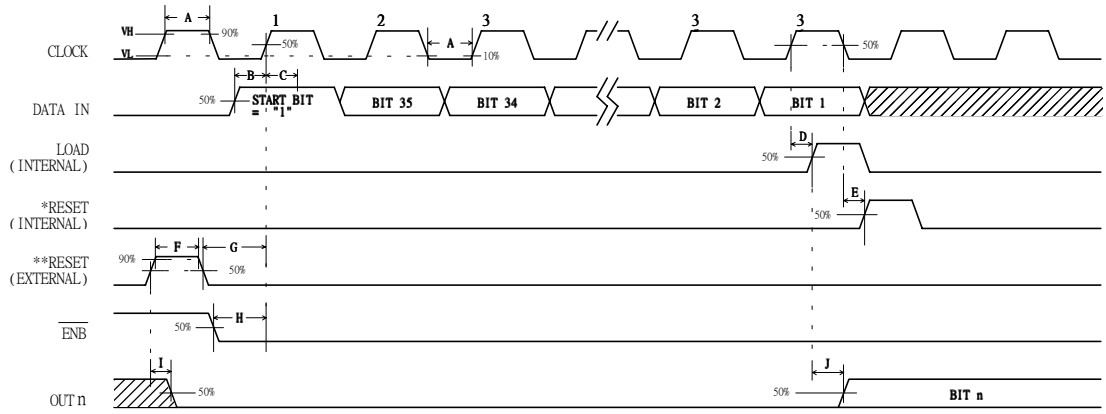
■ TIMING CHART AND TIMING CONDITIONS

— TIMING CHART



* THE INTERNAL RESET ONLY CLEARS ALL INTERNAL SHIFT REGISTERS.

** THE EXTERNAL RESET CLEARS ALL INTERNAL SHIFT REGISTERS AND LATCHES.

— TIMING CONDITIONS

ITEM	DESCRIPTION	MIN	TYP	MAX	UNIT
A	Clock pulse width	250	-	-	nS
B	Serial data setup time	30	-	-	nS
C	Serial data hold time	30	-	-	nS
D	Time between clock activation & internal load pulse activation	35	-	-	nS
E	Time between clock falling & internal reset pulse activation	35	-	-	nS
F	External reset pulse duration	25	-	-	nS
G	External reset inactive setup time	120	-	-	nS
H	Data enable setup time	70	-	-	nS
I	Time between external reset activation & the output off	25	-	-	nS
J	Time between internal load activation & new output states arising	30	-	-	nS

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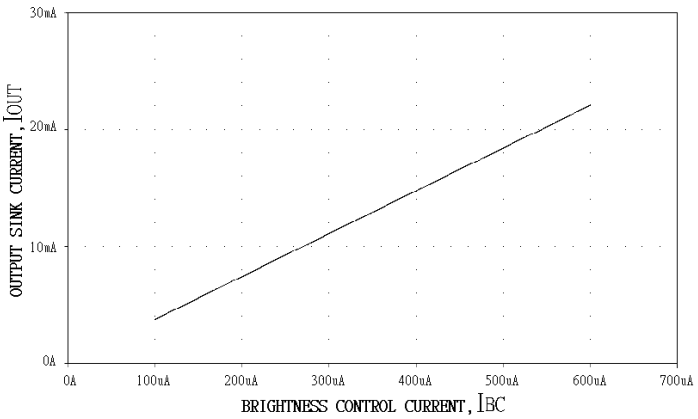
■ TRUTH TABLE

EXTERNAL RESET	$\overline{ENB}$	CLK	SERIAL DATA IN	SHIFT REGISTER CONTENTS I35 I34 I33・・・I2 I1 I0	INTERNAL LOAD	INTERNAL RESET	LATCH CONTENTS I35 I34 I33・・・I2 I1
		↑	H	H R35 R34 ・・・ R3 R2 L	L	L	NO CHANGE
		↑	L	L R35 R34 ・・・ R3 R2 L	L	L	NO CHANGE
L OR F	L OR F	↓	X	R35 R34 R33 ・・・ R2 R1 L	L	L	NO CHANGE
			(1) X	P35 P34 P33 ・・・ P2 P1 H	H	L	P35 P34 P33・・・P2 P1
		(1) (3) ↑↓↑ (2)	(2) X	L L L ・・・ L L L	L	H	P35 P34 P33・・・P2 P1
			(3) H	H L L ・・・ L L L	L	L	P35 P34 P33・・・P2 P1
			(3) L	L L L ・・・ L L L	L	L	P35 P34 P33・・・P2 P1
		↑	X	L R35 R34 ・・・ R3 R2 L	L	L	NO CHANGE
		↓	X	R35 R34 R33 ・・・ R3 R2 L	L	L	NO CHANGE
L OR F	H		(1) X	P35 P34 P33 ・・・ P2 P1 H	H	L	P35 P34 P33・・・P2 P1
		(1) (3) ↑↓↑ (2)	(2) X	L L L ・・・ L L L	L	H	P35 P34 P33・・・P2 P1
			(3) X	L L L ・・・ L L L	L	L	P35 P34 P33・・・P2 P1
H	X	X	X	L L L ・・・ L L L	L	L	L L L ・・・L L

H = HIGH LOGIC LEVEL　　R = PREVIOUS STATE　　X = IRRELEVANT

L = LOW LOGIC LEVEL　　P = PRESENT STATE　　F = FLOATING

■ TYPICAL CHARACTERISTIC CURVES (VDD=5V，VOUT=1V)



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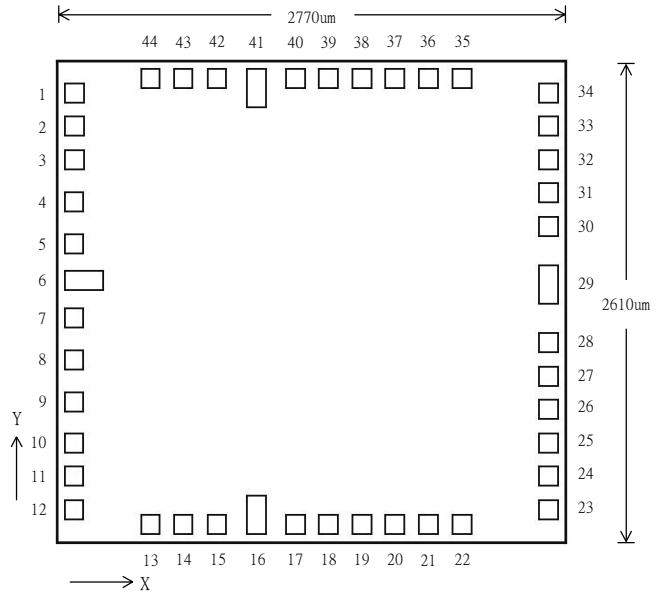
■ PAD LOCATIONS AND PAD SIZE



COORDINATES REFERENCE TO CENTER OF PAD AND PAD SIZE / ORIGION (0,0) AT CENTER OF PAD#12									
Pad No.	Name	X	Y	Pad Size	Pad No.	Name	X	Y	Pad Size
1	OUT3	0	+2184	100X BY 100Y	23	OUT23	+2495	0	100X BY 100Y
2	OUT2	0	+2009		24	OUT22	+2495	+175	
3	OUT1	0	+1834		25	OUT21	+2495	+350	
4	RESET	0	+1616		26	OUT20	+2495	+526	
5	B.C.	0	+1396		27	OUT19	+2495	+702	
6	VDD	+50	+1202	200X BY 100Y	28	OUT18	+2495	+876	
7	CLK	0	+1004	100X BY 100Y	29	VSS	+2495	+1180	100X BY 200Y
8	DATA IN	0	+784		30	OUT17	+2495	+1485	100X BY 100Y
9	$\overline{ENB}$	0	+564		31	OUT16	+2495	+1660	
10	OUT35	0	+350		32	OUT15	+2495	+1834	
11	OUT34	0	+175		33	OUT14	+2495	+2010	
12	OUT33	0	0		34	OUT13	+2495	+2185	
13	OUT32	+400	-76		35	OUT12	+2040	+2260	
14	OUT31	+576	-76		36	OUT11	+1865	+2260	
15	OUT30	+751	-76		37	OUT10	+1690	+2260	
16	VSS	+957	-26	100X BY 200Y	38	OUT9	+1514	+2260	
17	OUT29	+1164	-76	100X BY 100Y	39	OUT8	+1340	+2260	
18	OUT28	+1340	-76		40	OUT7	+1164	+2260	
19	OUT27	+1515	-76		41	VSS	+957	+2210	100X BY 200Y
20	OUT26	+1690	-76		42	OUT6	+750	+2260	100X BY 100Y
21	OUT25	+1865	-76		43	OUT5	+576	+2260	
22	OUT24	+2040	-76		44	OUT4	+400	+2260	

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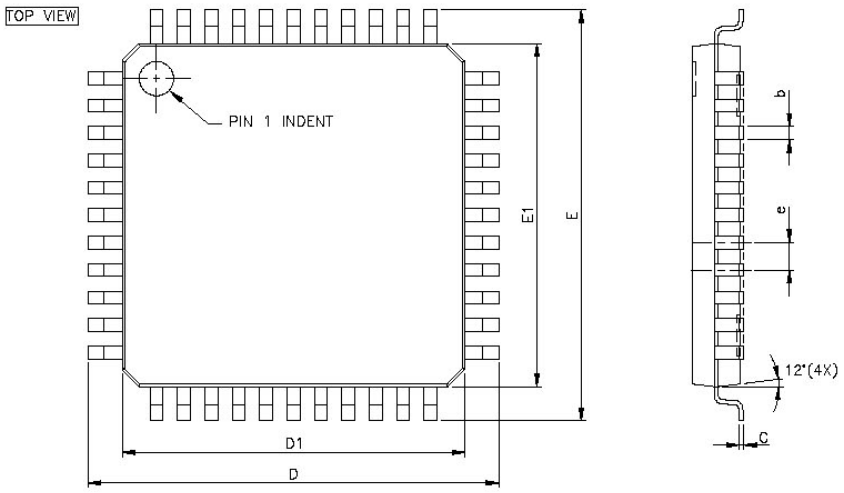
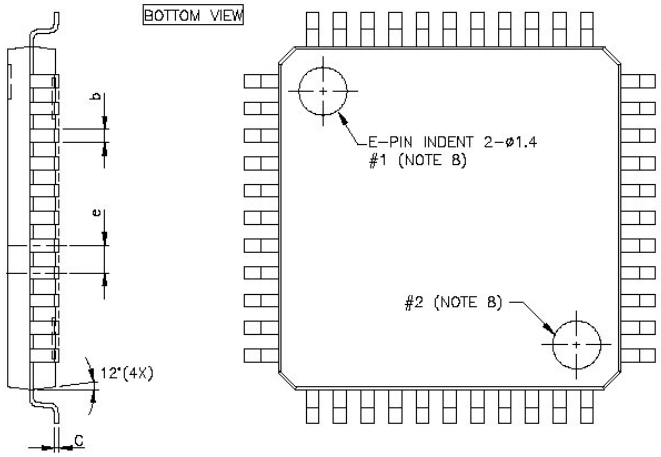
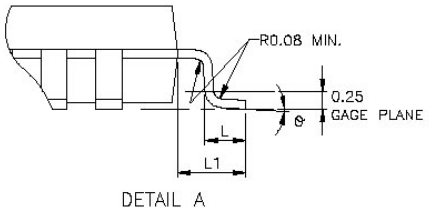
■ PACKAGE INFORMATION





SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.60
A1	0.05	——	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
C	0.09	——	0.20
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
e	——	0.80	——
L	0.45	0.60	0.75
L1	——	1.00	——
θ	0°	3.5°	7°
y	0.0	——	0.08



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