CMOS Single-Supply Rail-to-Rail Input/Output Operational Amplifiers

OP250/OP450

FEATURES

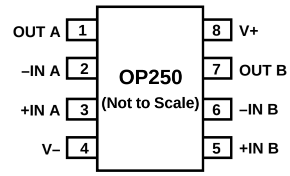
Single-Supply Operation: 2.7 V to 6 V
High Output Current: ±100 mA
Low Supply Current: 800 μA/Amp
Wide Bandwidth: 1 MHz
Slew Rate: 2.2 V/μs
No Phase Reversal
Low Input Currents
Unity Gain Stable

APPLICATIONS

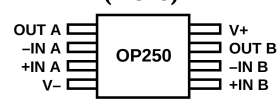
Battery Powered Instrumentation
Medical
Remote Sensors
ASIC Input or Output Amplifier
Automotive

PIN CONFIGURATIONS

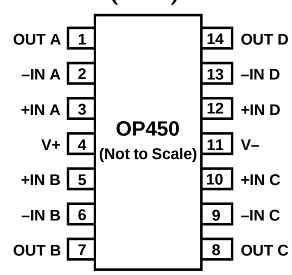
8-Lead Narrow Body SO (SO-8)



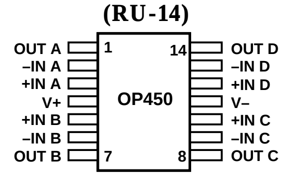
8-Lead TSSOP (RU-8)



14-Lead Narrow Body SO (N-14)



14-Lead TSSOP (RU-14)



GENERAL DESCRIPTION

The OP250 and OP450 are dual and quad CMOS single-supply, amplifiers featuring rail-to-rail inputs and outputs. Both are guaranteed to operate from a +2.7 V to +5 V single supply.

These amplifiers have very low input bias currents. Outputs are capable of driving 100 mA loads and are stable with capacitive loads. Supply current is less than 1 mA per amplifier.

Applications for these amplifiers include portable medical equipment, safety and security, and interface to transducers with high output impedance.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

The OP250 and OP450 are specified over the extended industrial (–40°C to +125°C) temperature range. The OP250, dual, is available in 8-lead TSSOP and SO surface mount packages. The OP450, quad, is available in 14-lead thin shrink small outline (TSSOP) and narrow 14-lead SO packages.

REV. 0

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OP250/OP450–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +3.0 V, T_A = +25°C, V_{CM} = 1.5 V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				8	mV
		–40°C < T_A < +125°C			20	mV
Input Bias Current	I_B			2	40	pA
		–40°C < T_A < +85°C			60	pA
		–40°C < T_A < +125°C			500	pA
Input Offset Current	I_{OS}			0.5	25	pA
		–40°C < T_A < +125°C			60	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	40	55		dB
		–40°C < T_A < +125°C	35			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = 0.3 V to 2.7 V		800		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			1.8		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			0.07		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA		2.99		V
		I_L = 10 mA	2.85	2.94		V
		–40°C to +125°C	2.8			V
Output Voltage Low	V_{OL}	I_L = 100 µA		1		mV
		I_L = 10 mA		55	100	mV
		–40°C to +125°C			125	mV
Output Current	I_{OUT}			100		mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		180		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 6 V	60	80		dB
		–40°C < T_A < +125°C	55			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		700	1,000	µA
		–40°C < T_A < +125°C			1,250	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		1.9		V/µs
Settling Time	t_S	To 0.01%		4		µs
Gain Bandwidth Product	GBP			0.95		MHz
Phase Margin	Øo			46		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V, T_A = +25°C, V_{CM} =2.5 V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	7.5	mV
		–40°C < T_A < +125°C			20	mV
Input Bias Current	I_B			2	40	pA
		–40°C < T_A < +85°C			60	pA
		–40°C < T_A < +125°C			500	pA
Input Offset Current	I_{OS}			0.5	25	pA
		–40°C < T_A < +125°C			60	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	45	60		dB
		–40°C < T_A < +125°C	40			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , Vo = 0.3 V to 4.7 V		1,000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			1.8		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			0.07		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA		4.99		V
		I_L = 10 mA	4.9	4.94		V
		–40°C to +125°C				mV
Output Voltage Low	V_{OL}	I_L = 100 µA		1		V
		I_L = 10 mA		40	100	mV
		–40°C to +125°C			125	mV
Output Current	I_{OUT}			±100		mA
Open Loop Impedance	Z_{OUT}	f =1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 6 V	60	80		dB
		–40°C < T_A < +125°C	55			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		800	1,250	µA
		–40°C < T_A < +125°C		750	1,750	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		100		kHz
Settling Time	t_S	To 0.01%		3		µs
Gain Bandwidth Product	GBP			1		MHz
Phase Margin	Øo			48		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz		10		µV p–p
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . +6 V
Input Voltage[2] . . . . GND to V_S
Common-Mode Input Voltage . . . . ±6 V
Output Short-Circuit
  Duration to GND . . . . Observe Derating Curves
ESD Susceptibility . . . . 2000 V
Storage Temperature Range
  S, RU Package . . . . −65°C to +150°C
Operating Temperature Range
  OP250G/OP450G . . . . −40°C to +125°C
Junction Temperature Range
  S, RU Package . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C

NOTES
[1]Absolute maximum ratings apply at +25°C, unless otherwise noted.
[2]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Units
8-Lead SOIC (S)	158	43	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (N)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

*θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} specified for device soldered in circuit board for surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
OP250GS	–40°C to +125°C	8-Lead SOIC	SO-8
OP250GRU	–40°C to +125°C	8-Lead TSSOP	RU-8
OP450GS	–40°C to +125°C	14-Lead SOIC	N-14
OP450GRU	–40°C to +125°C	14-Lead TSSOP	RU-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP250/OP450 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

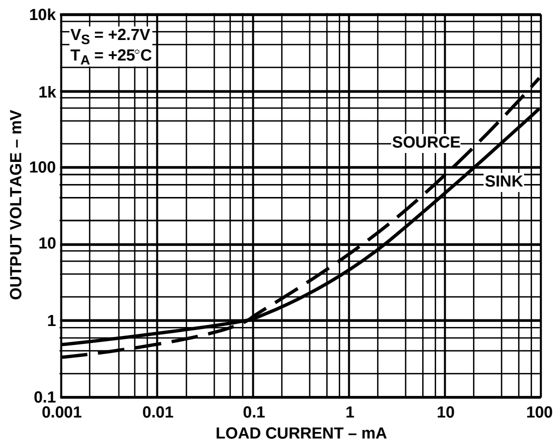


Figure 1. Output Voltage to Supply Rail vs. Load Current

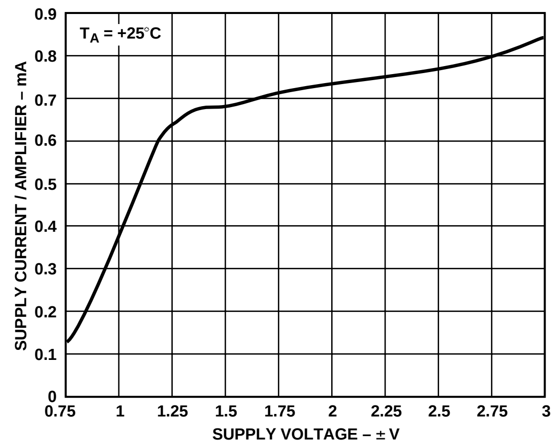


Figure 4. Supply Current per Amplifier vs. Supply Voltage

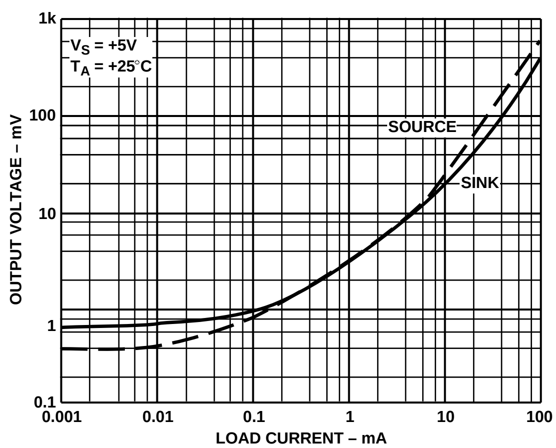


Figure 2. Output Voltage to Supply Rail vs. Load Current

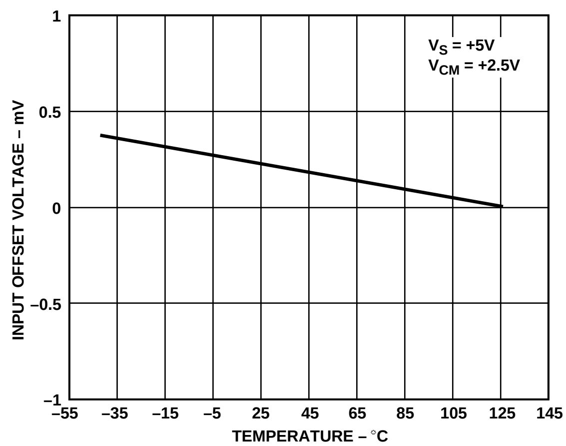


Figure 5. Input Offset Voltage vs. Temperature

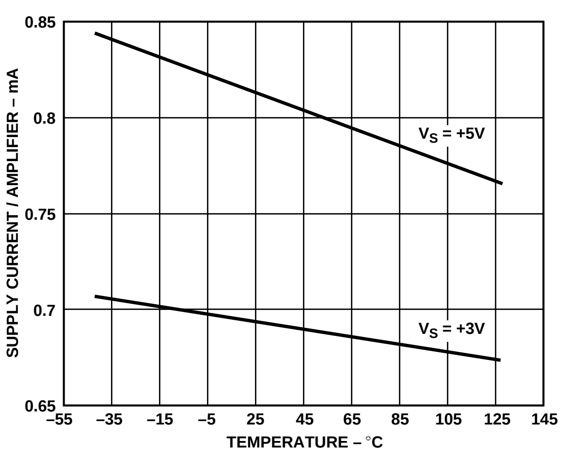


Figure 3. Supply Current per Amplifier vs. Temperature

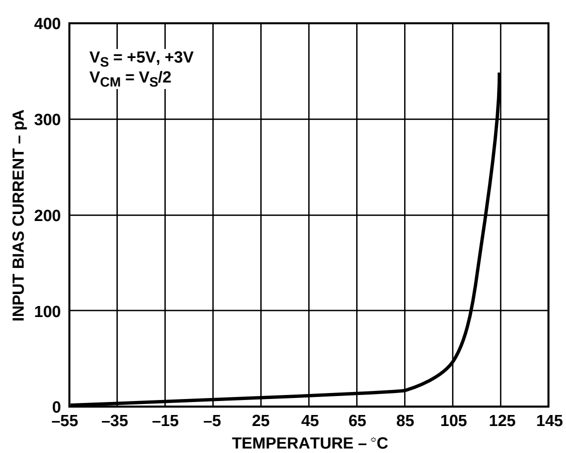


Figure 6. Input Bias Current vs. Temperature

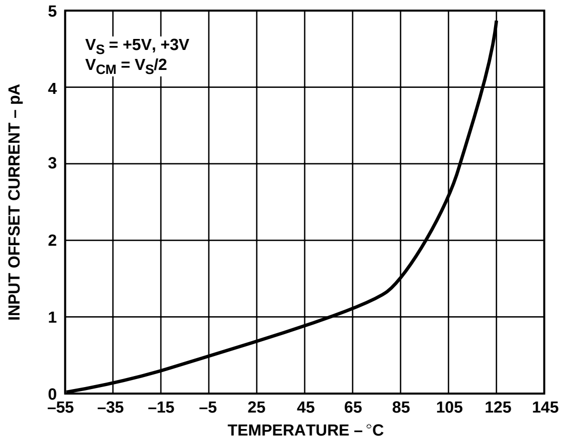


Figure 7. Input Offset Current vs. Temperature

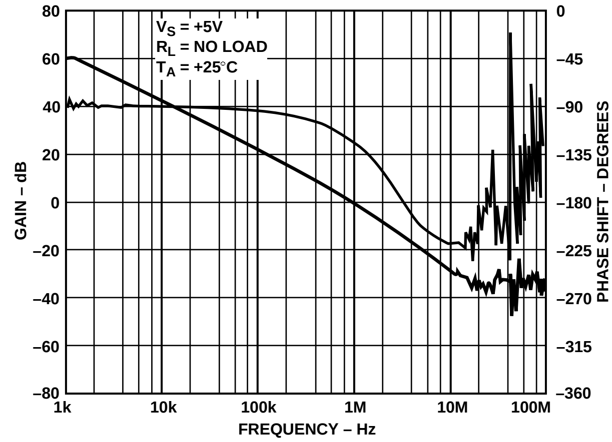


Figure 10. Open-Loop Gain and Phase

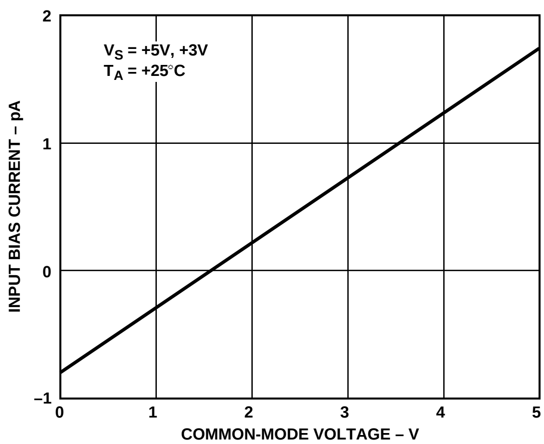


Figure 8. Input Bias Current vs. Common-Mode Voltage

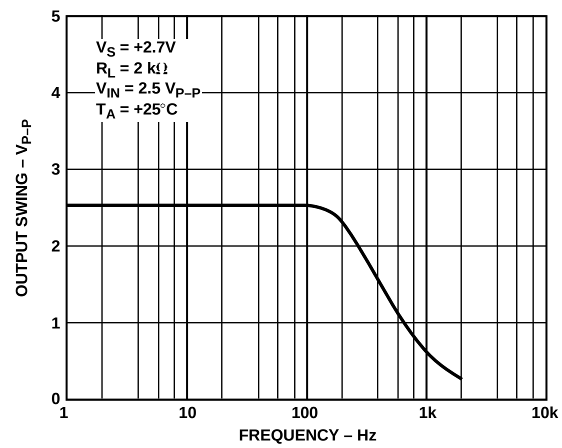


Figure 11. Closed-Loop Output Voltage Swing vs. Frequency

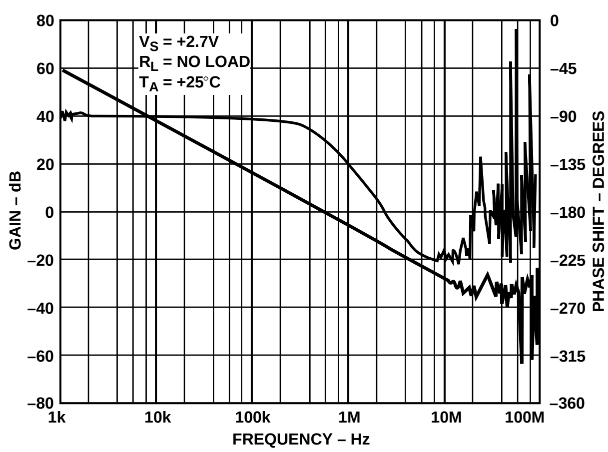


Figure 9. Open-Loop Gain and Phase

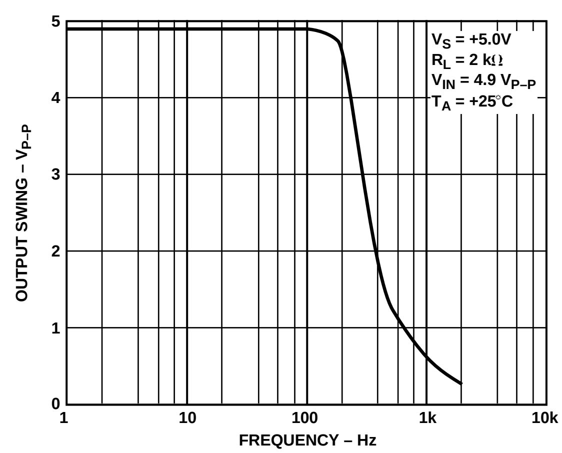


Figure 12. Closed-Loop Output Voltage Swing vs. Frequency

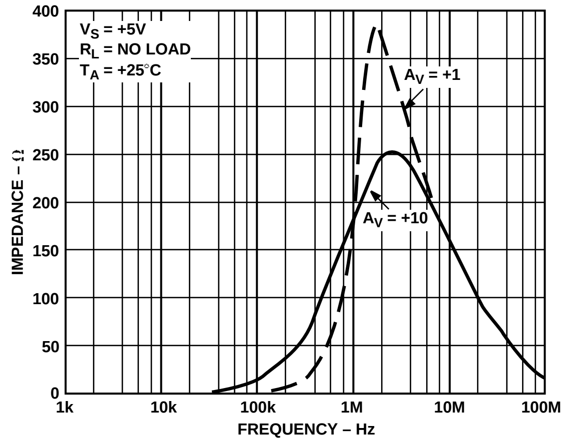


Figure 13. Closed-Loop Output Impedance vs. Frequency

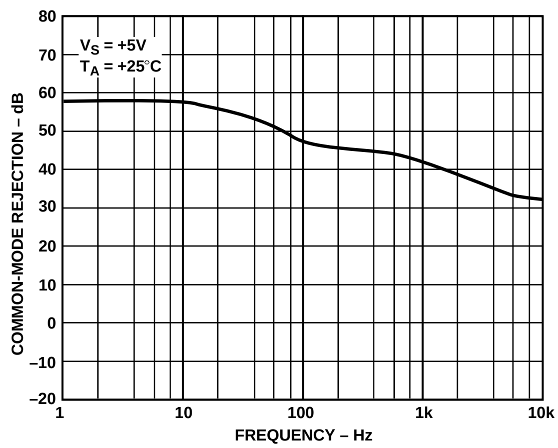


Figure 14. Common-Mode Rejection vs. Frequency

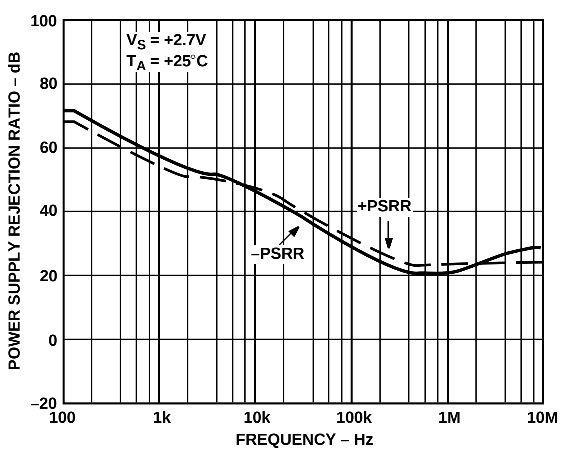


Figure 15. Power Supply Rejection vs. Frequency

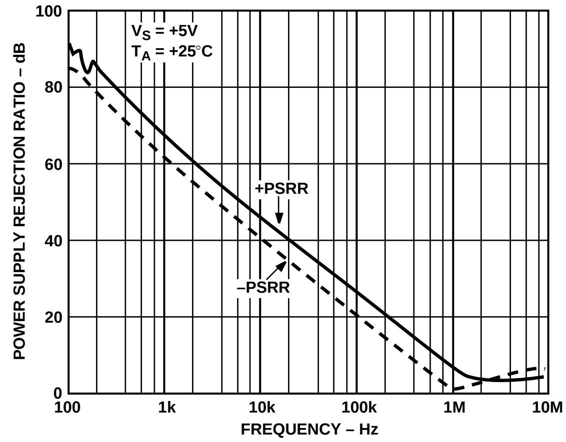


Figure 16. Power Supply Rejection vs. Frequency

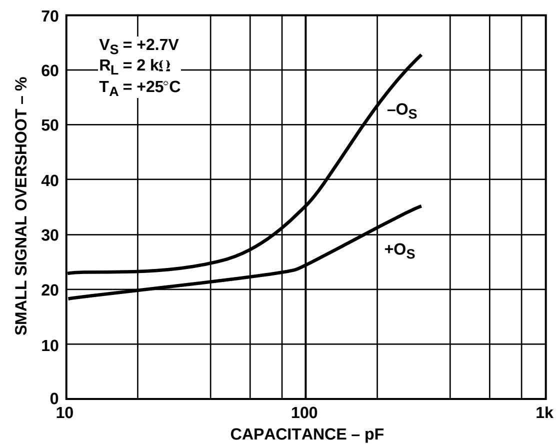


Figure 17. Small Signal Overshoot vs. Load Capacitance

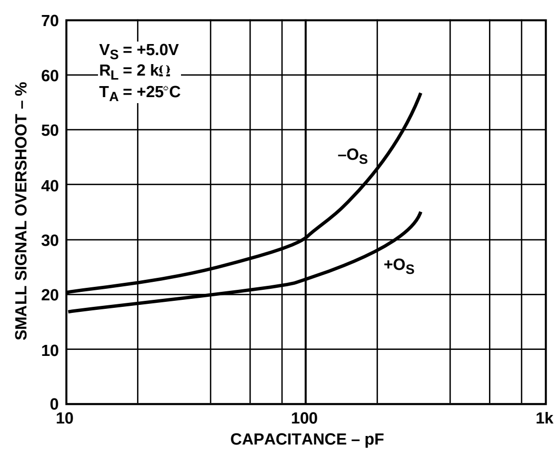
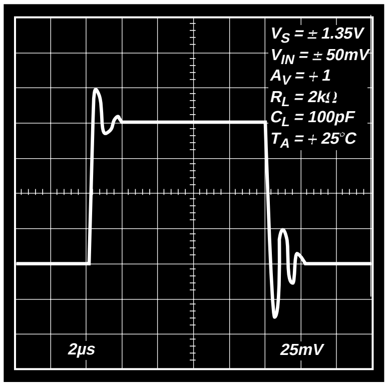


Figure 18. Small Signal Overshoot vs. Load Capacitance



Figre 19. Small Signal Transient Response

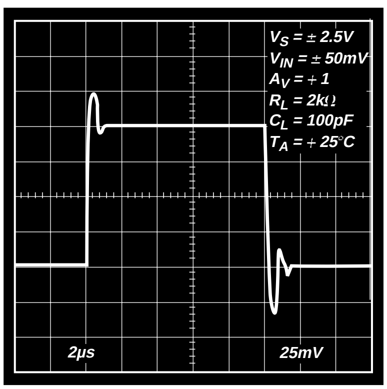


Figure 20. Small Signal Transient Response

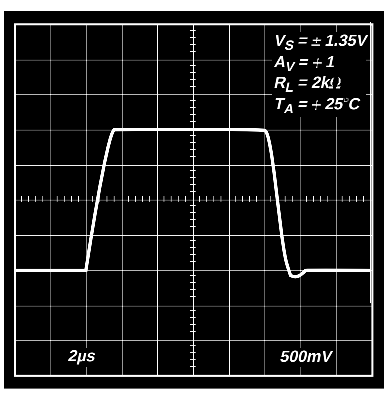


Figure 21. Large Signal Transient Response

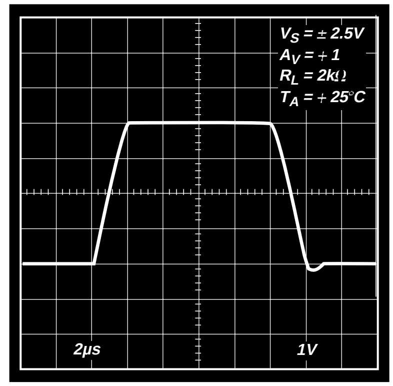


Figure 22. Large Signal Transient Response

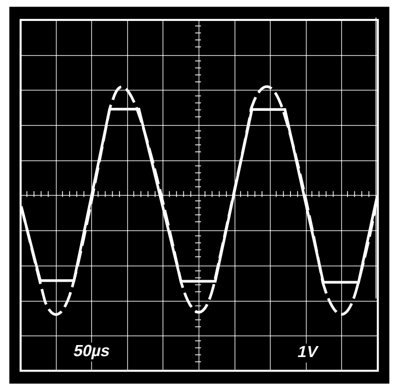


Figure 23. No Phase Reversal

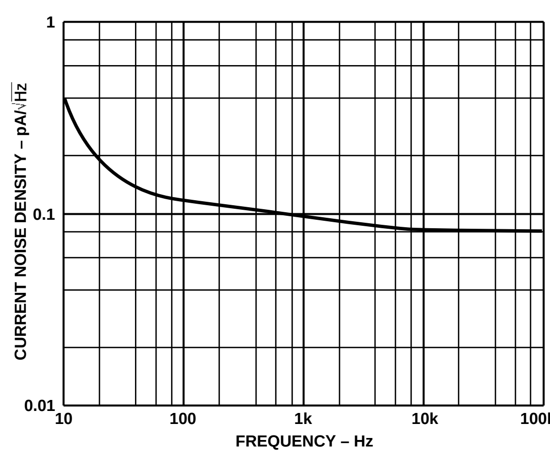


Figure 24. Current Noise Density vs. Frequency

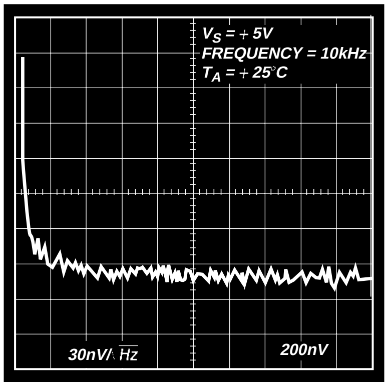


Figure 25. Voltage Noise Density vs. Frequency

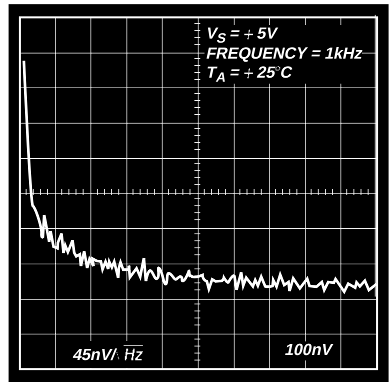


Figure 26. Voltage Noise Density vs. Frequency

THEORY OF OPERATION

The OPx50 family of amplifiers are CMOS rail-to-rail input and output single supply amplifiers designed for low cost and high output current drive. These features make the OPx50 op amps ideal for multimedia and telecom applications.

Figure 27 shows the simplified schematic for an OPx50 amplifier. Two input differential pairs consisting of an n-channel pair (M1–M2) and a p-channel pair (M3–M4) provide a rail-to-rail input common-mode range. The outputs of the input differential pairs are combined in a compound folded-cascode stage, which drives the input to a second differential pair gain stage. The outputs of the second gain stage provide the gate voltage drive to the rail-to-rail output stage.

The rail-to-rail output stage consists of M15 and M16, which are configured in a complementary common-source configuration. As with any rail-to-rail output amplifier, the gain of the output stage, and thus the open loop gain of the amplifier, is dependent on the load resistance. Also, the maximum output voltage swing is directly proportional to the load current. The difference between the maximum output voltage to the supply rails, known as the dropout voltage, is determined by the OPx50's output transistors' on-channel resistance. The output dropout voltage is given in Figures 1 and 2.

Input Voltage Protection

Although not shown on the simplified schematic, there are ESD protection diodes connected from each input to each power supply rail. These diodes are normally reversed biased, but will turn on if either input voltage exceeds either supply rail by more than 0.6 V. Should this condition occur the input current should be limited to less than ±5 mA. This can be done by placing a resistor in series with the input. The minimum resistor value should be:

$$R_{IN} \geq \frac{V_{IN,MAX}}{5\,mA} \tag{1}$$

Output Phase Reversal

The OPx50 is immune to output voltage phase reversal with an input voltage within the supply voltages of the device. However, if either of the device's inputs exceeds 0.6 V outside of the supply rails, the output could exhibit phase reversal. This is due to the ESD protection diodes becoming forward biased, thus causing the polarity of the input terminals of the device to switch.

The technique recommended in the Input Overvoltage Protection section should be applied in applications where the possibility of input voltages exceeding the supply voltages exists.

Output Short Circuit Protection

To achieve high quality rail-to-rail performance, the outputs of the OPx50 family are not short-circuit protected. Although these amplifiers are designed to sink or source as much as 250 mA of output current, shorting the output directly to ground could damage or destroy the device when excessive voltages or currents are applied. If to protect the output stage, the maximum output current should be limited to ±250 mA.

By placing a resistor in series with the output of the amplifier as shown in Figure 28, the output current can be limited. The minimum value for R_X can be found from Equation 2.

$$R_X \geq \frac{V_{SY}}{250\,mA} \tag{2}$$

For a +5 V single supply application, R_X should be at least 20 Ω. Because R_X is inside the feedback loop, V_{OUT} is not affected. The trade-off in using R_X is a slight reduction in output voltage swing under heavy output current loads. R_X will also increase the effective output impedance of the amplifier to $R_O + R_X$, where R_O is the output impedance of the device.

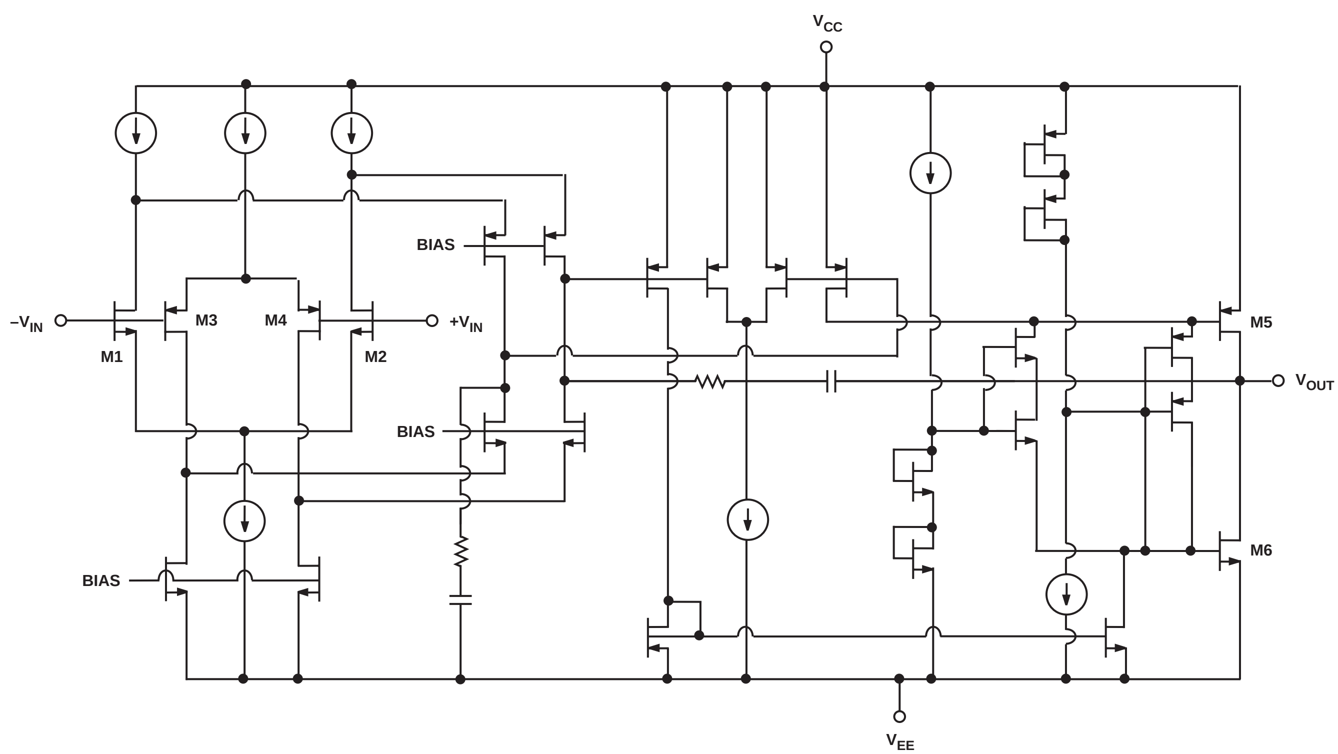


Figure 27. OPx50 Simplified Schematic

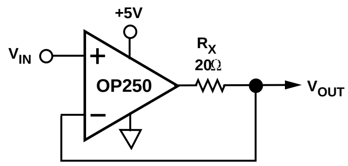


Figure 28. Output Short-Circuit Protection

Power Dissipation

Although the OPx50 family of amplifiers are able to provide load currents of up to 250 mA, proper attention should be given to not exceed the maximum junction temperature for the device. The equation for finding the junction temperature is given as:

$$T_J = P_{DISS} \times \theta_{JA} + T_A \quad (3)$$

Where T_J = OPx50 junction temperature
P_{DISS} = OPx50 power dissipation
θ_{JA} = OPx50 junction-to-ambient thermal resistance of the package; and
T_A = The ambient temperature of the circuit

In any application, the absolute maximum junction temperature must be limited to +150°C. If this junction temperature is exceeded, the device could suffer premature failure. If the output voltage and output current are in phase, for example, with a purely resistive load, the power dissipated by the OPx50 can be found as:

$$P_{DISS} = I_{LOAD} \times \left(V_{SY} - V_{OUT}\right) \quad (4)$$

Where I_{LOAD} = OPx50 output load current
V_{SY} = OPx50 supply voltage; and
V_{OUT} = The output voltage

By calculating the power dissipation of the device and using the thermal resistance value for a given package type, the maximum allowable ambient temperature for an application can be found using Equation 3.

Overdrive Recovery

The overdrive, or overload, recovery time of an amplifier is the time required for the output voltage to return to a rated output voltage from a saturated condition. This recovery time can be important in applications where the amplifier must recover quickly after a large transient event. The circuit in Figure 29 was used to evaluate the recovery time for the OPx50. Figures 30 and 31 show the overload recovery of the OP250 from the positive and negative rails. It takes approximately 0.5 ms for the amplifier to recover from output overload.

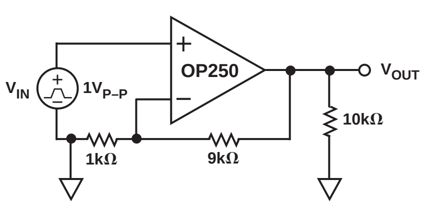


Figure 29. Overload Recovery Time Test Circuit

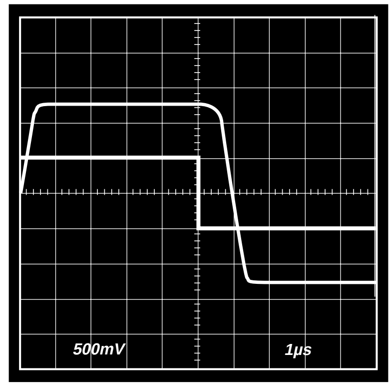


Figure 30. Saturation Recovery from the Positive Rail

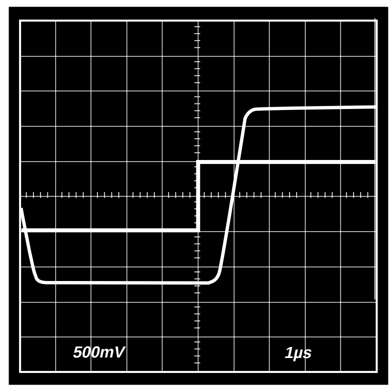


Figure 31. Saturation Recovery from the Negative Rail

Capacitive Loading

The OPx50 family of amplifiers is well suited to driving capacitive loads. The device will remain stable at unity gain even under heavy capacitive load conditions. However, a capacitive load does not come without a penalty in bandwidth. Figure 32 shows a graph of the OPx50 unity-gain bandwidth under various capacitive loads.

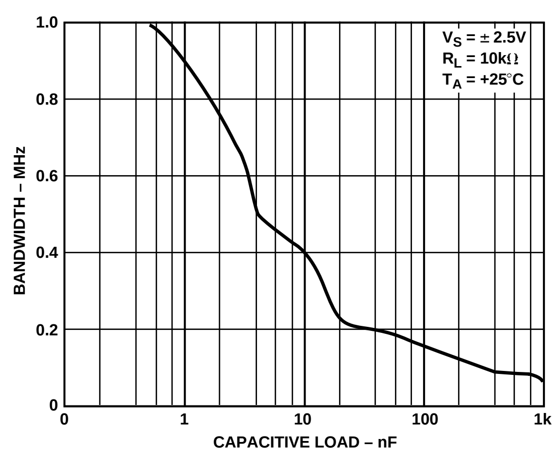


Figure 32. Unity-Gain Bandwidth vs. Capacitive Load

As with any amplifier, an increase in capacitive load will also result in an increase in overshoot and ringing. To improve the output response, a series R-C network, known as a snubber, can be connected from the output to ground in parallel with the capacitive load as shown in Figure 33. The proper snubber network on the output can significantly reduce output overshoot, although it will not increase the bandwidth. Table I shows some snubber network values for a given capacitive load. In practice, these values are best determined empirically based on the exact capacitive load for the application.

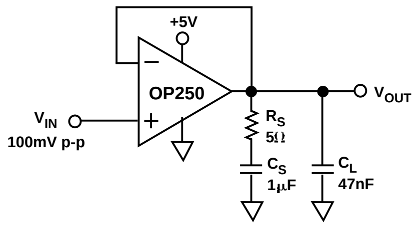


Figure 33. Schematic for Using a Snubber Network

Table I. Snubber Network for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (RS, CS)
1 nF	60 Ω, 30 nF
10 nF	20 Ω, 1 μF
100 nF	3 Ω, 10 μF

Figure 34 shows the output of an OP250 in a unity gain configuration with a 1 nF capacitive load. Figure 35 shows the improvement in the output response with the snubber network added.

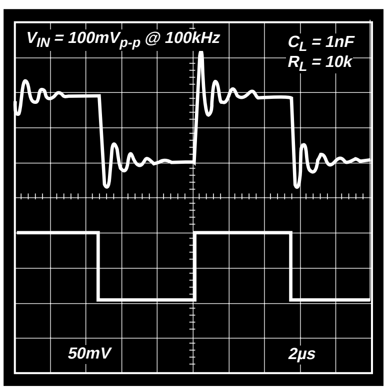


Figure 34. Output of OP250 without Snubber Network

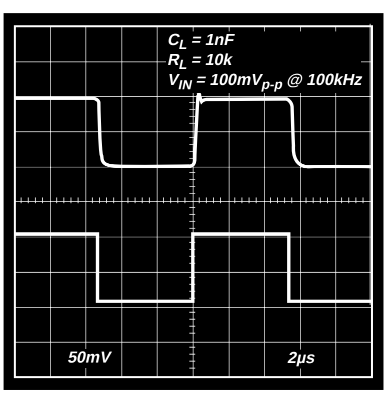


Figure 35. Output of OP250 with Snubber Network

For more information on methods to drive a capacitive load with an op amp, please refer to the *Ask the Applications Engineer* article in *Analog Dialogue*, Vol. 31, Number 2, 1997.

Single Supply Differential Line Driver

Figure 36 shows a single supply differential line driver circuit that can drive a 600 Ω load with less than 0.1% distortion. The design uses an OP450 to mimic the performance of a fully balanced transformer based solution. However, this design occupies much less board space while maintaining low distortion and can operate down to dc. Like the transformer based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1.

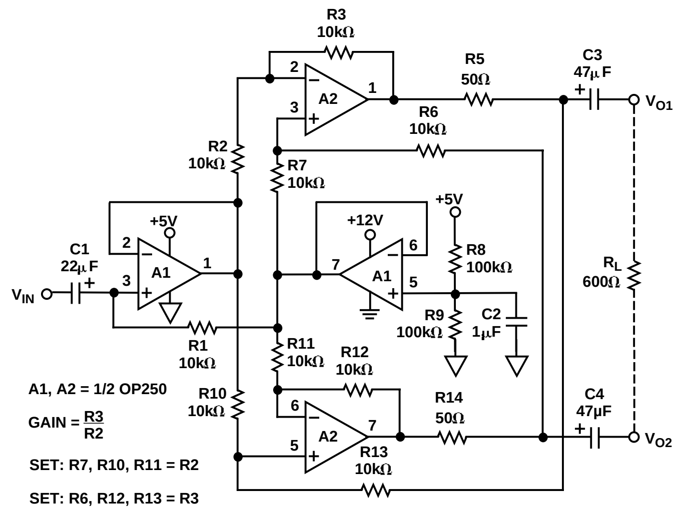


Figure 36. A Low Noise, Single Supply Differential Line Driver

R8 and R9 set up the common mode output voltage equal to half of the supply voltage. C1 is used to couple the input signal and can be omitted if the input's dc voltage is equal to half of the supply voltage.

The circuit can also be configured to provide additional gain if desired. The gain of the circuit is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R3}{R2} \tag{5}$$

Where: $V_{OUT} = V_{O1} - V_{O2}$,
R2 = R7 = R10 = R11 and,
R3 = R6 = R12 = R13

Multimedia Headphone Amplifier

Because of its large output drive, the OP250 makes an excellent headphone amplifier, as illustrated in Figure 37. Its low supply operation and rail-to-rail inputs and outputs can maximize output signal swing on a single +5 V supply. In Figure 37, the amplifier inputs are biased halfway between the supply voltages, which in this application is 2.5 V. A 10 μF capacitor prevents power supply noise from contaminating the audio signal.

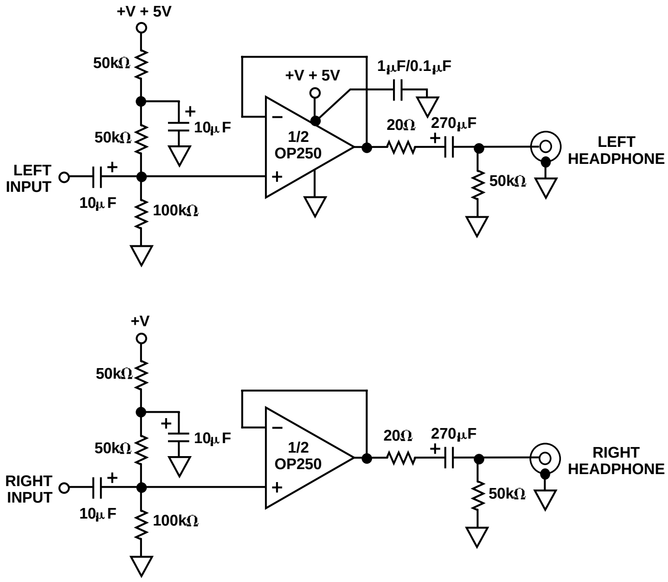


Figure 37. A Single-Supply Stereo Headphone Driver

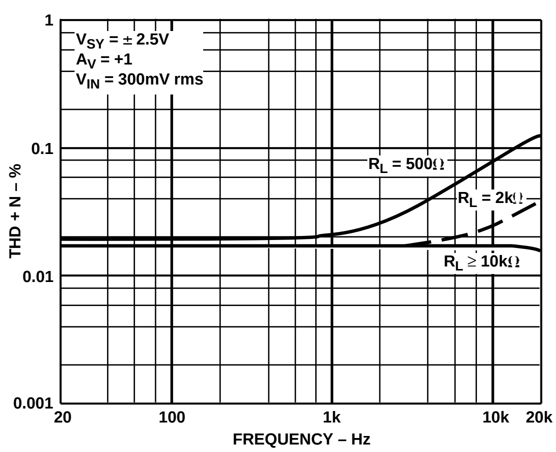


Figure 38. THD vs. Frequency

Headphone Driver

The audio signal is coupled into each input through a 10 μF capacitor. This large value insures the resulting high pass filter cutoff is below 20 Hz, preserving full audio fidelity. If the input already has the proper dc bias, then the coupling capacitor and biasing resistors are not required. A 270 μF capacitor is used at the output to couple the amplifier to the headphone speaker. This value is much larger than the input capacitor because of the low impedance of the headphones, which can range from 32 Ω to 600 Ω or more. An additional 20 Ω resistor is used in series with the output capacitor to protect the op amp's output in the event the output accidentally becomes shorted to ground.

Direct Access Arrangement for Modems

Figure 39 illustrates a +5 V transmit/receive telephone line interface for 600 Ω systems. It allows full duplex transmission of signals on a transformer coupled 600 Ω line in a differential manner. Amplifier A1 provides gain which can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured so as to apply the largest possible signal on a single supply to the transformer. Because of the OP450's high output current drive and low dropout voltages, the largest signal available on a single +5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier for two reasons: (1) It prevents the transmit signal from interfering with the receive signal and (2) it extracts the receive signal from the transmission line for amplification by A4. Amplifier A4's gain can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the OP450 14-lead TSSOP or SOIC footprint and this circuit offers a compact, cost-effective solution.

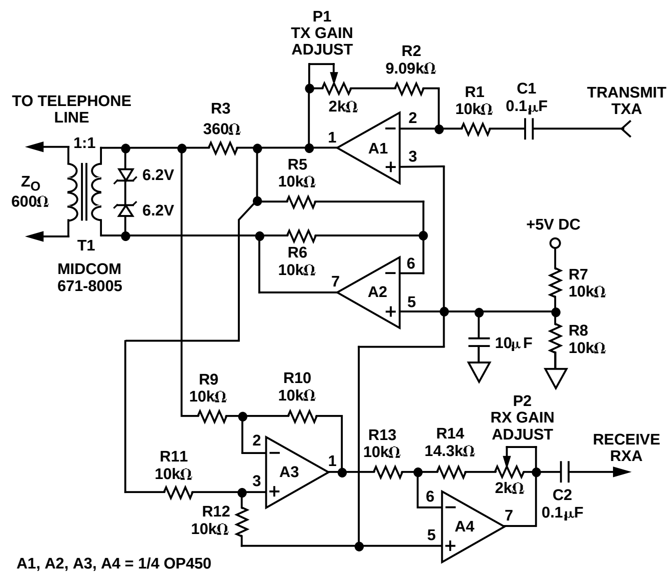


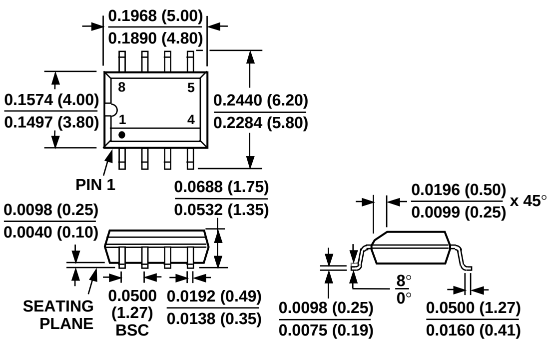
Figure 39. A Single-Supply Direct Access Arrangement for Modems

```
* OP250 SPICE Macro-Model Typical Values
* 10/97, Ver. 1
* TAM / ADSC
*
* Node assignments
*             noninverting input
*             |    inverting input
*             |    |    positive supply
*             |    |    |    negative supply
*             |    |    |    |    output
*             |    |    |    |    |
*             |    |    |    |    |
.SUBCKT OP250 1    2    99   50   45
*
* INPUT STAGE
*
M1  4  3  6 6 MNIN L=2u W=66u
M2  5  2  6 6 MNIN L=2u W=66u
M3  7  3  9 9 MPIN L=2u W=66u
M4  8  2  9 9 MPIN L=2u W=66u
RD1   99  4 5E3
RD2   99  5 5E3
RD3    7 50 5E3
RD4    8 50 5E3
VCM1  10 50 -.3
VCM2  99 11 -.3
D1    10  6 DX
D2     9 11 DX
EOS    3  1 POLY(3) (61,98) (73,98) (81,0) 3E-3
+1 1 1
IOS    1  2 .25E-12
IBIAS1  6 50 700E-6
IBIAS2 99  9 700E-6
*
* CMRR=60 dB, ZERO AT 20kHz
*
ECM1 60 98 POLY(2) (1,98) (2,98) 0 .5 .5
RCM1 60 61 159.2E3
RCM2 61 98 159
CCM1 60 61 50E-12
*
* PSRR=90dB, ZERO AT 200Hz
*
RPS1 70  0 1E6
RPS2 71  0 1E6
CPS1 99 70 1E-5
CPS2 50 71 1E-5
EPSY 98 72 POLY(2) (70,0) (0,71) 0 1 1
RPS3 72 73 1.59E6
CPS3 72 73 500E-12
RPS4 73 98 50
*
* INTERNAL VOLTAGE REFERENCE
*
RSY1 99 91 100E3
RSY2 50 90 100E3
VSN1 91 90 DC 0
EREF 98  0 (90,0) 1
GSY  99 50 POLY(1) (99,50) -1.81E-3 1.5E-5
*
* VOLTAGE NOISE REFERENCE OF 30nV/rt(Hz)
*
VN1 80 0 0
RN1 80 0 16.45E-3
HN  81 0 VN1 30
RN2 81 0 1
*
* POLE AT 1.25MHz
*
G2 98 20 POLY(2) (4,5) (7,8) 0 5E-5 5E-5
R2 20 98 10E3
C2 20 98 12.7E-12
*
* GAIN STAGE
*
G1 98 30 (20,98) 3.5E-4
R1 30 98 6.25E6
CF 30 45 135E-12
D4 31 99 DX
D5 50 32 DX
V1 31 30 0.7
V2 30 32 0.7
*
* OUTPUT STAGE
*
M5  45 41 99 99 MPOUT L=2u W=6660u
M6  45 42 50 50 MNOUT L=2u W=6660u
EO1 99 41 POLY(1) (98,30) .9232 1
EO2 42 50 POLY(1) (30,98) .8914 1
*
* MODELS
*
.MODEL MNIN  NMOS(LEVEL=2,VTO=0.75,
+KP=20E-6,CGSO=0,KF=2.5E-31,AF=1)
.MODEL MPIN  PMOS(LEVEL=2,VTO=-0.75,
+KP=20E-6,CGSO=0,KF=2.5E-31,AF=1)
.MODEL MNOUT NMOS(LEVEL=2,VTO=0.75,
+KP=30E-6,LAMBDA=0.04,CGSO=0)
.MODEL MPOUT PMOS(LEVEL=2,VTO=-0.75,
+KP=20E-6,LAMBDA=0.04,CGSO=0)
.MODEL DX D(IS=1E-16)
.ENDS OP250
```

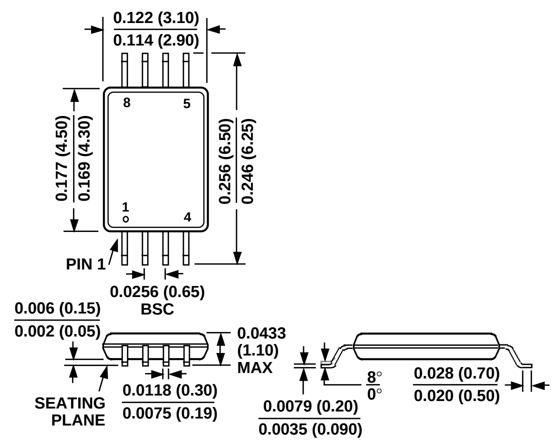
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

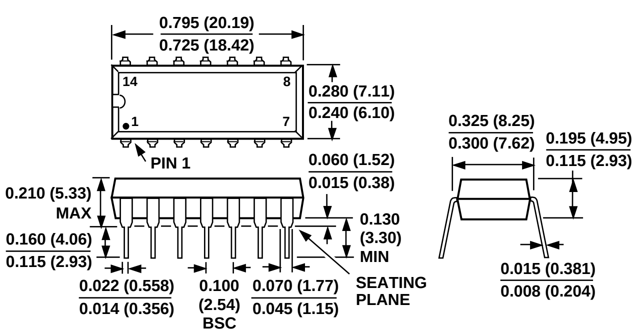
8-Lead SOIC (SO-8)



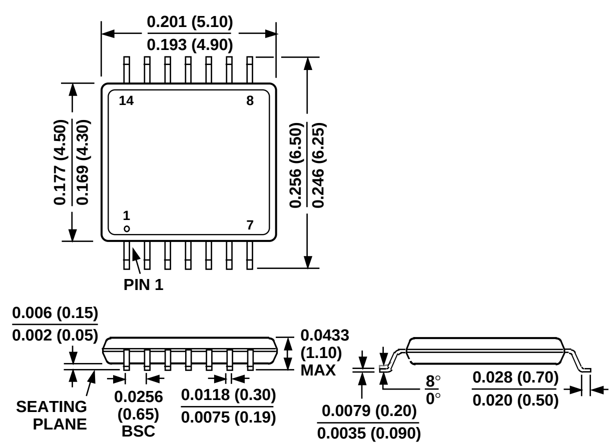
8-Lead TSSOP (RU-8)



14-Lead Plastic DIP (N-14)



14-Lead TSSOP (RU-14)



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