MOST® Bigfoot™ Tx Plastic Fiber Optic Transmitter MOT 003

Preliminary Data Sheet

The 4-Pin MOST optical transmitter (MOT 003) is based on the latest design of the BIGFOOT IC, which is being developed continuously. Therefore the enclosed MOST transmitter data sheet has to be taken as preliminary. Samples which are delivered before the qualification and the production release are engineering samples and do not yet fit all the specified parameter values.

Features

Excellent solution for converting high speed data from TTL to Plastic Optical Fiber (POF)

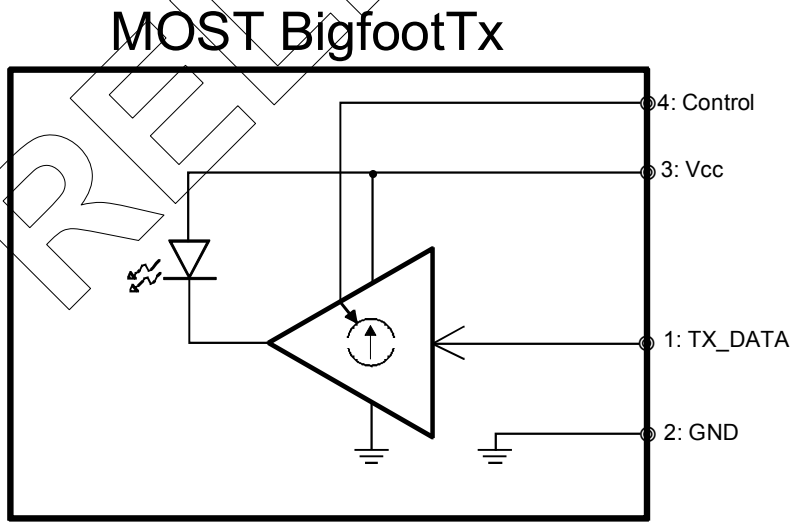
- High speed transmitter up to 50 Mbaud
- TTL Data Input (Logic to Light Function)
- 650 nm for working in a low attenuation range of PMMA Fiber
- High coupled power in1000 micron plastic fiber
- Low cost

Applications

- Optical Transmitter for MOST Systems

Description

The MOST BigfootTx Plastic Fiber Optic Transmitter is a highly integrated CMOS IC combined with a High speed LED designed to transmit up to 25Mbit/sec optical data which is biphase coded at up to 50Mbaud.
The internal peaking circuit minimizes PWD.
The current through the LED will be setup by an external resistor connected to VCC. This makes it possible to control the optical output power of the LED.



Actual design status:

Bigfoot IC Revision	package type	device color	Data sheet is valid since
E	CAI	blue	21-Jul-00

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{STG}	-40	100	°C
Junction Temperature	T_J	-40	100	°C
Soldering Temperature (>1mm from case bottom t≤10s)	T_S	-	260	°C
Power Dissipation (depends on maximum temperature)	P_{TOT}	-	300	mW
Power Supply Voltage	V_{CCMax}	-0.5	6.0	V

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Operating Temperature Range (R_{ext} = 15 kOhm)	T_A	-40	85	°C

All the data in this specification refers to the operating conditions above unless otherwise stated.

Optical Signal Characteristics

(Rext = 15 KOhm / 22.5 MBit MOST Data/ Vcc=4.75 .. 5.25 V)

Parameter	Symbol	Min	Typ	Max	Unit
Peak wavelength at T_A=25°C	λ_{Peak25}	640	650	660	nm
Temperature coefficient λ_{Peak}	$TC\lambda$	-	0.16	-	nm/K
Peak wavelength at T_A=-40..85°C	λ_{Peak}	630	650	670	nm
Spectral bandwidth	Delta λ	-	20	25	nm
Average Output Power coupled into plastic fiber at T_A=25°C, see Note 1	P_{opt25}	-8.2 (150)	-6.5 (225)	-5.2 (300)	dBm (µW)
Temperature coefficient P_{opt}	TC_{Popt}	-	- 0.4	-	%/K
Average Output Power coupled into plastic fiber at T_A=-40..85°C, see Note 1	P_{opt}	-9.4 (115)	-6.5 (225)	-4.7 (340)	dBm (µW)
Optical Rise Time	t_r	-	4.5	7	ns
Optical Fall Time	t_f	-	7.5	10	ns
Extinction Ratio	r_e	10	11	-	dB
Pulse Width Distortion	t_{PWD}	-0.5	0	1	ns
Jitter	t_{PWD}	-	0.5	1	ns

Note 1: The output power coupled into plastic fiber P_{opt} is measured with a large area detector at the end of a short length of a fiber (about 30 cm), which is ideally coupled to the Sidelooker. This value must not be used for calculating the power budget for a fiber optic system with a long fiber because the numerical aperture of plastic fibers decreases on the first meters.
Therefore the fiber seems to have a higher attenuation over the first few meters compared with the specified value.

Due to the direct coupling of the fiber to the LED at the end of the short fiber UMD (uniform mode distribution) will be observed. Therefore the following section of the cable has higher losses compared with EMD (equilibrium mode distribution)

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Low Level Input Voltage	V_{IL}	-0.3	-	1.5	V
High Level Input Voltage	V_{IH}	3.0	-	V_{CC} + 0.3	V
Input Leakage Current (V_{CC}=5.0V, V_I=0.0V or V_I=5.0V)	I_L	-	-	+/- 20	µA
Input Impedance @ 25MHz input data rate	Z_I	3.5	-	-	kOhm
Supply Current (R_{ext} = 15 kOhm) ON state Note 2 Bi phase coded data	I_{CC}	-	25	30	mA
Supply Current (R_{ext} = 15 kOhm) OFF state Note 3	I_{LP2}	-	-	1	mA

Note 2: The current through the LED and therefore the optical output power and overall power consumption depends from the settings of R_{ext}. The nominal value for R_{ext} is 15K. With R_{ext}=30K the optical output power is about –3dB of the nominal value. Typical behavior see figure below.
Important: The external resistor of R_{ext} must be within the range of 13.5K to 33K. For values of R_{ext} out of this range functionality may not be given over the whole temperature range and the device lifetime. Using values below 13K for R_{ext} can damage the transmitter.

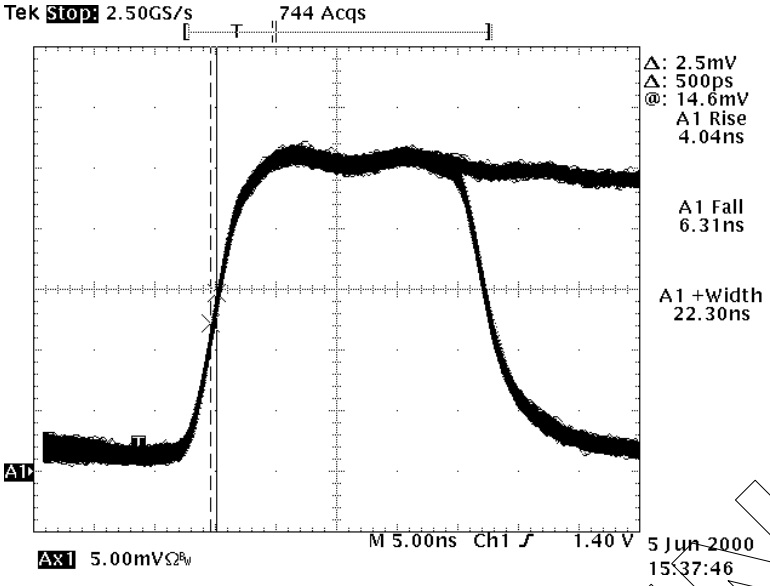
Note 3: The transmitter jumps to low power mode after TX DATA is low for max. 16µsec. If the transmitter is in low power mode it is switched ON 2.5µsec after TX DATA starts toggling.

AC Electrical Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio	25 MHz Power Supply Noise	PSRR	-	30	-	dB
Power Up Time	Zero → MOST Data	T_{PU}	1.0	-	2.5	µs
Power Down Time	MOST Data → Zero	T_{PD}	-	-	16.0	µs
Input Rise Time		t_{TLH}	-	-	5	ns
Input Fall Time		t_{THL}	-	-	5	ns

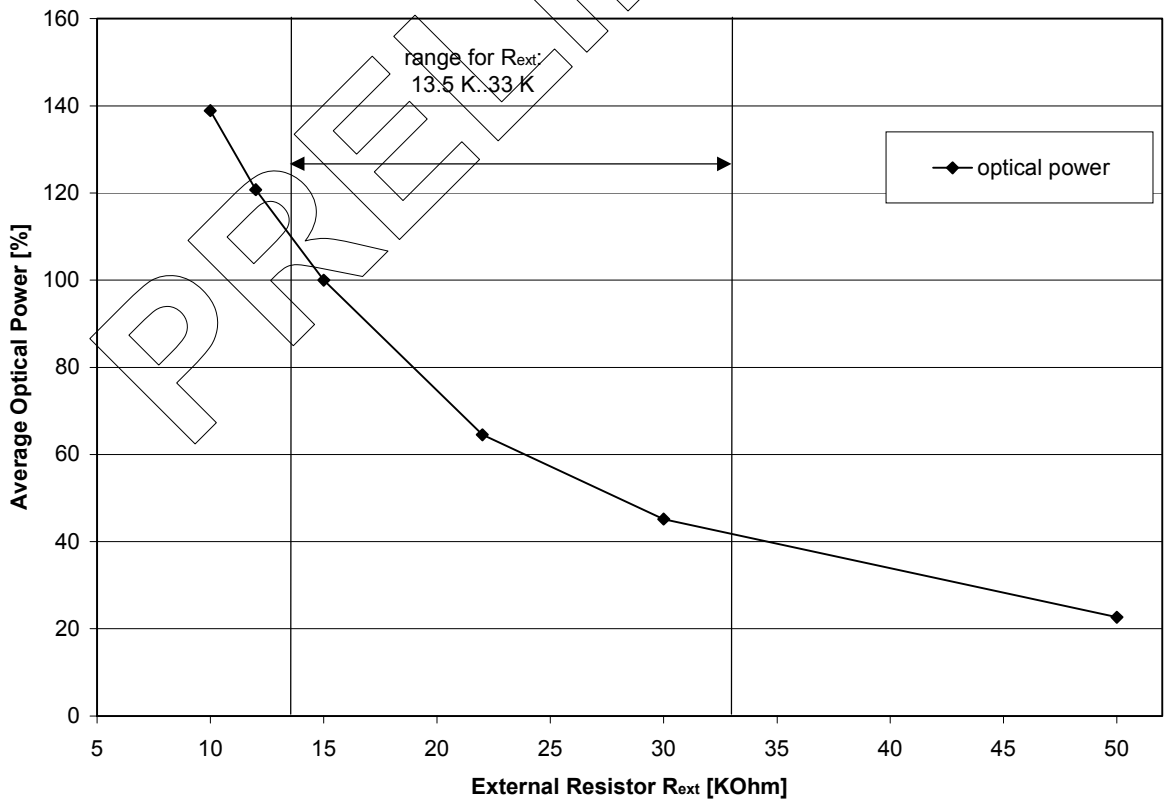
Typical Output Signal

Measured with fast optical receiver (Graviton SPD-1) with 15 kOhm external resistor and 22.579 Mbit/s MOST Data at T_A=25°C.

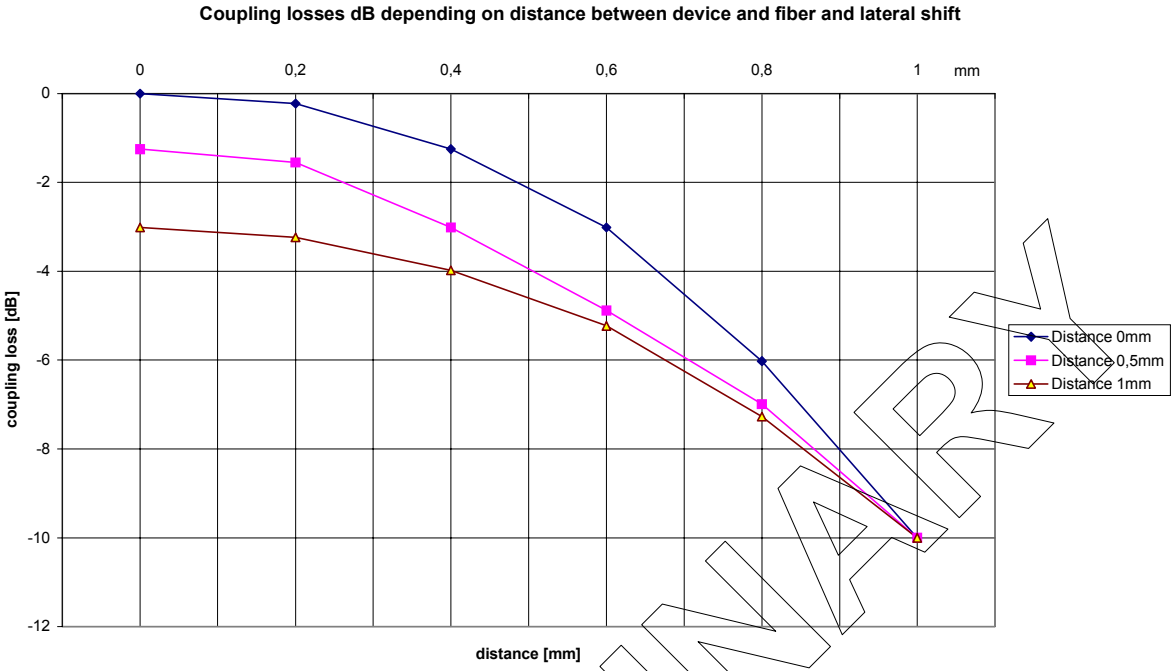


Typical Dependency of Average Output Power P_{opt} on external Resistor R_{ext}

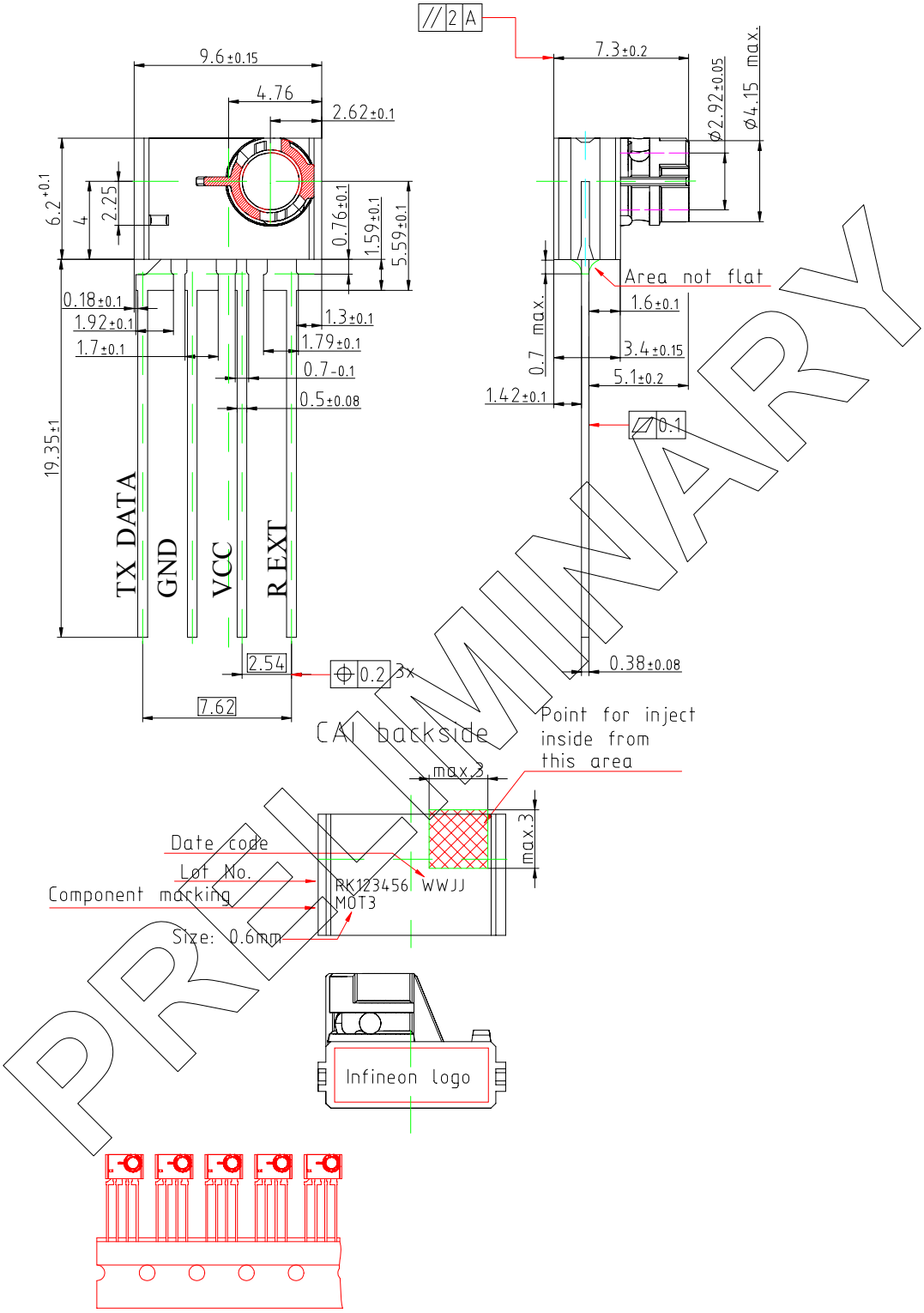
(22.5 MBit MOST Data/ V_{CC}=5 V / T_A=25°C)



Fiber Coupling

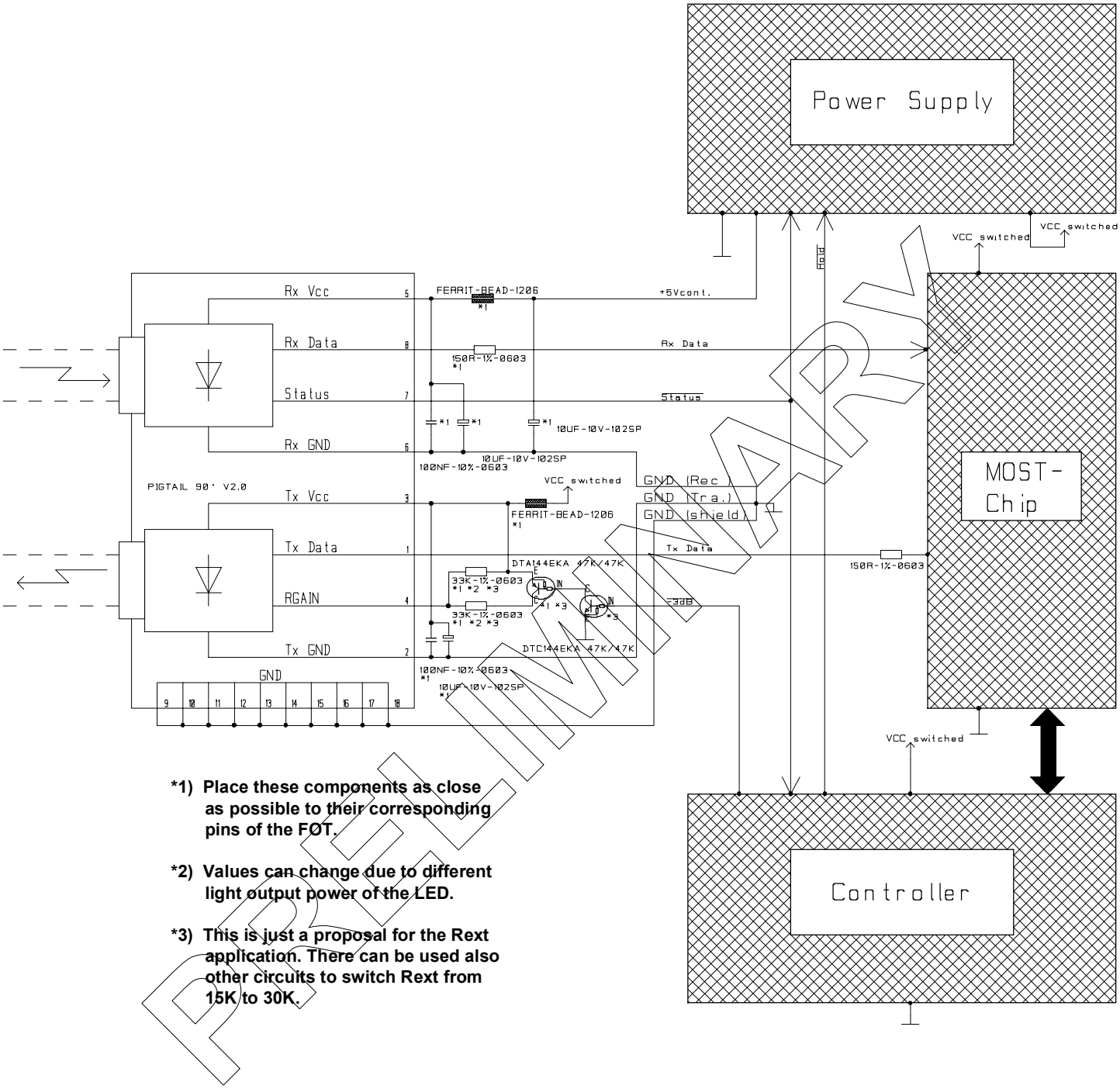


Mechanical Design MOT 003: CAI package (cavity as interface)



Device Color: Blue (Bigfoot IC Rev E), dot on backside

Application Circuit:



***1) Place these components as close as possible to their corresponding pins of the FOT.**

***2) Values can change due to different light output power of the LED.**

***3) This is just a proposal for the Rext application. There can be used also other circuits to switch Rext from 15K to 30K.**

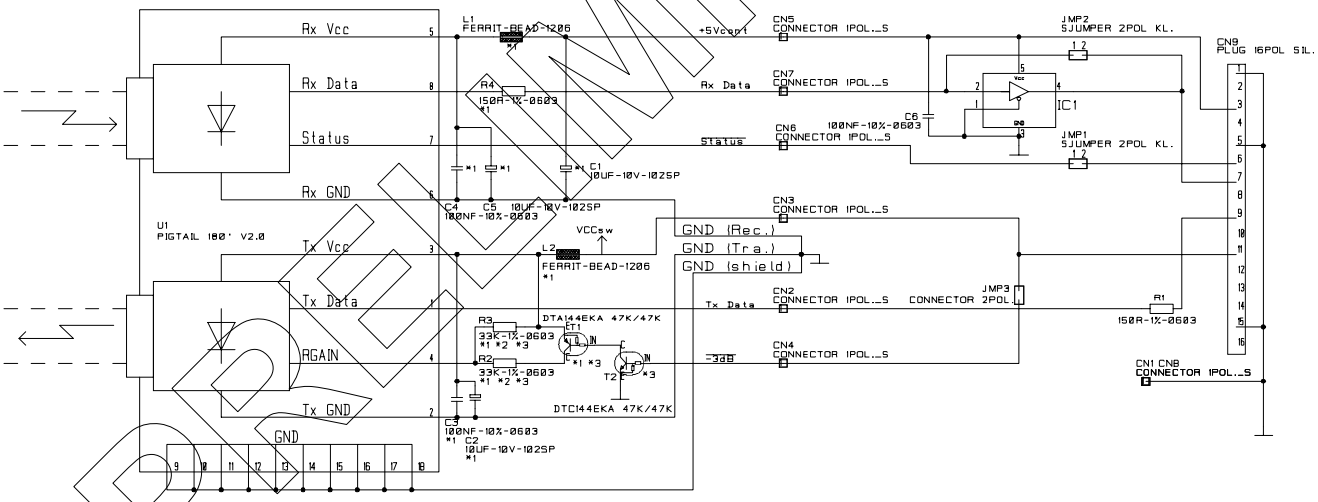
Design & Layout rules:

- The 100NF bypass capacitors of the FOTs must be located as close as possible between the pins Vcc and GND of the FOTs. Use ceramic caps and tantalum caps with low ESR.
- Also the inductor/ferrite bead (receiver) and the -3dB - control circuit (transmitter) must be placed as close as possible to the FOTs. We prefer ferrite beads (e.g. type 74279214 Würth Elektronik) since the D.C. resistance is very low. If other inductors are used the D.C. resistor should be less than 3Ohm.
- For EMC a ferrite bead should be connected to the power supply close to the transmitter and the receiver. Do not use only one ferrite bead together for receiver and transmitter!

- For the ground connection a ground plane is recommended (Y-structure). That means the ground planes of the transmitter, the receiver and the shielding must be separated. The three ground planes should be connected together behind the bypass capacitors (refer to the PCB design below). This ground signal should be connected directly to the ground plane of the MOST controller (e.g. OS8104) and the power supply on the top layer and/or bottom layer and ground layer as it is indicated in the example below.
- If a multi layer design is used the ground layer must have the same ground separation like shown for the top layer!
- A serial resistor in the Rx/Tx data line will also reduce EMC - problems. For Rx the resistor must be placed near the receiver - for Tx the resistor must be placed near the MOST controller chip. The value depends from the distance between the FOTs and the MOST chip (< 5cm) and can be in the range of up to 150R. Higher values for the resistors will increase jitter and can therefore cause locking problems of the MOST PLL!
- The Rx/Tx signals should not be routed parallel over a long distance but may be embedded with ground copper, if possible.
- The GND pin and the pin of Rext (15K - resistor) of the transmitter are used for heat dissipation. Therefore there should be a good connection to the PCB → no isolation gaps! Both pins should dip into a copper area (see layout example below).

Layout example:

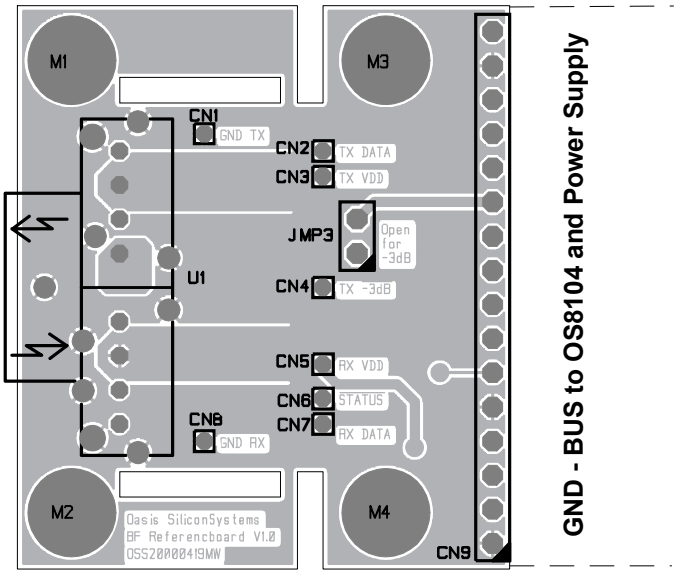
The reference board from OASIS Silicon Systems follows the requirements above. The schematic is very similar to the example above, but does not include the connection to the power supply, the OS8104 or the micro controller.



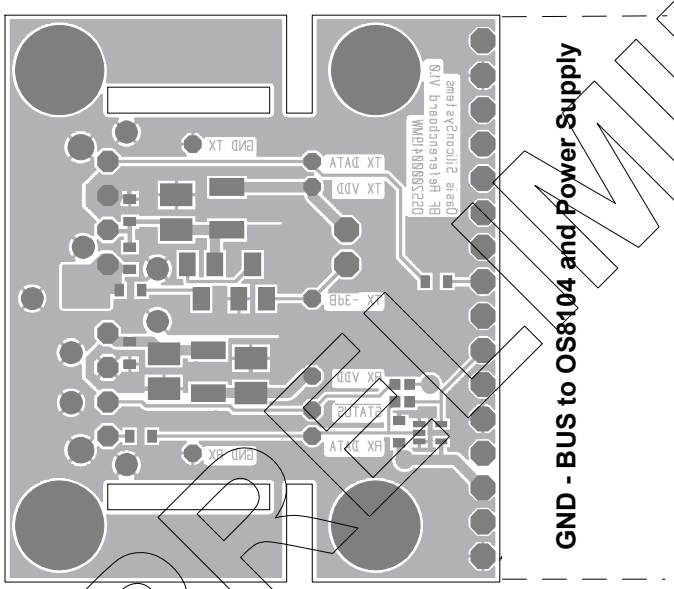
The examples below for top- and bottom layer is the layout of the reference design board and shows how the layout around the optical receiver and transmitter should look like.
It is strongly recommended to follow this examples in your design to get best performance!

Note:
The buffer circuit (IC1), the connectors and jumpers in the middle to the right section of the schematic are only for use of the reference board and will not be necessary for your HW - design.

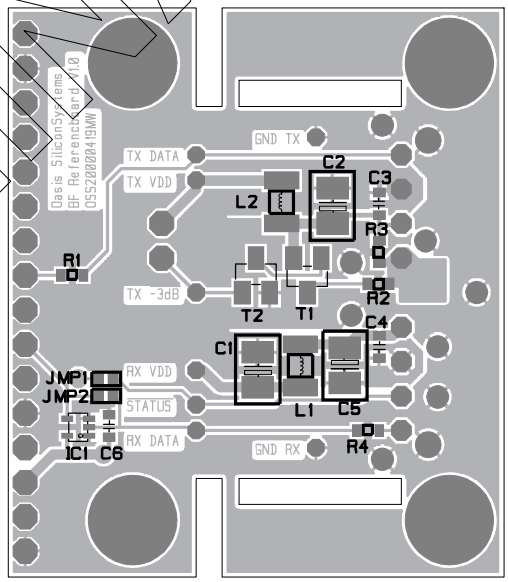
Top Layer with 180° version of the pigtail:



Bottom Layer (seen from the top side of the PCB):



Bottom Layer: Bottom side / positions



Other items:

- The shown circuit for the –3dB attenuation is just a proposal. Also any other circuit which can double the value of R_{ext} is permitted.

- **Due to the fact that the optical average level jumps if the power control signal (/-3dB) is toggled there can occur LOCK/coding – errors at the following device for a short time.** This is not very critical, since it does occur only in diagnosis mode. After a time of 10msec the device should lock again if the optical attenuation between the devices is not too high.

- The Rx and Tx signals can be measured by using standard probes (>1M/<10pF). However, if the signal quality is very bad and the LOCK signal of the MOST chip is flaky connecting a passive probe to the Rx signal can cause the MOST chip to lock better or worse to the signal. This is due to the capacitance of the analog probe which is usually in the range of 8..12pF and shifts the phase and PWD of the signal. In this case an active probe with a capacitance of less than 1pF is recommended.

- The reference test board which corresponds to the layout examples above is available at the Oasis Silicon System AG.

History of Design and Specification Status of MOST Transmitter:

Data Sheet Status	Bigfoot IC Revision	device color	comments, cause of change, important differences to last Status
Oct. 98	B	-	preliminary data sheet for 6 pin samples
May.99, Rev. D	C	-	preliminary data sheet for change from 6 pin to 4 pin package (change from package type SPF MOT 001 to SPF MOT 002)
Aug.99, Rev. E	C	red	p. 2: Operating Temperature Range -40 ..+60 °C, minimum output power @ 15 KOhm external resistor is 100 µW, p. 3: supply current, typ. 80 mA, eye diagram
24-Nov-99	D	green	review of data sheet: data sheet is target specification, first page gives information about sample status p. 1: fore word, difference of current revision to target spec. is shown in table: Operating Temperature Range -40 ..+75 °C, Typ. Supply Current 50 mA p. 2: storage temperature –40 °C minimum p. 3: influence of Rext; current consumption with DATAIN=0; eye diagram p. 6: application circuit; Design & Layout rules p. 7: layout examples p. 8: other items p. 9: history is added
03-July-00	E	blue	review of data sheet: data sheet corresponds to characterized values! p.1: Update block diagram Bigfoot Revision changed to E: Full Operating Temperature Range & Supply Current reduced; information that package type will change to CAI p.2: Soldering parameters changed according to JEDEC JESD22-B106-B Changed table of Characteristics LED into Optical Signal Characteristics. Changed Wavelength according to physical layer Specification. Added and updated values for average output power, optical rise/fall time, extinction ratio, pwd and jitter. p.3: Changed values for input voltage. Changed leakage current and added input impedance Changed current values just for ON- and OFF-state Update values in note 2 and note 3 Added values for power up/down in table AC char. p.4: Updated typical optical signal Added dependency of output power on external resistor p.6: Added device color: Blue p.7: Update Application Circuit p.8: Added point regarding good heat dissipation on PCB Changed section of Layout Example to the new reference board design of OSS (also on p.9) p.10: Changed last item: test board is available
21-July-00	E	blue	p. 1: Change of name to MOT 003 Change of package type from Sidelooker to CAI p. 3: Minimum low level input voltage added Maximum high level input voltage added p. 6: New Drawing mechanical design with CAI

Notes: