OV6645 SINGLE-CHIP CMOS CIF COLOR DIGITAL CAMERA

Description

The OV6645 (color) CMOS Image sensor is a single-chip video/imaging camera device designed to provide a high level of functionality in a single, small-footprint package. The device incorporates a 352 x 288 image array capable of operating at up to 60 frames per second. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the serial SCCB interface. The device can be programmed to provide image output in different 8-bit formats.

Features

- 101,376 pixels, 1/5" lens, CIF/QCIF format
- Progressive scan
- 8-bit Data output formats - YCrCb 4:2:2 ITU-656, GRB 4:2:2 & RGB Raw Data
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image Controls - brightness, contrast, gamma, saturation, sharpness, windowing, hue, etc.
- Internal & external synchronization
- Line exposure option
- 3.3-Volt operation, low power dissipation
  - < 20 mA active power at 60FPS
  - < 10 μA in power-down mode
- Built in Gamma correction (0.45/0.55/1.00)
- SCCB programmable:
  - Color saturation, brightness, hue, white balance, exposure time, gain, etc.

Ordering Information

Product	Package	Description
OV6645	**24 LCC** **0.400 in^2**	**COLOR, CIF, Digital, SCCB interface**

Applications

. Picture Phones
. Cell Phones
. Toys
. PC Multimedia
. PDAs

Key Specifications

Array Element(CIF) (QCIF)	352x288 (176x144)
Pixel Size	7.6μm x 7.6μm
Image Area	2.7mm x 2.18mm
Max Frames/Sec	Up to 60 FPS
Electronics Exposure	Up to 360:1 (at the selected frame rate)
Scan Mode	Progressive
Gamma Correction	0.45/0.55/1.0
Min. Illumination (3000K)	< 3lux @ f1.2
S/N Ratio	> 48 dB (AGC off, Gamma=1)
FPN	< 0.03% V_{PP}
Dark Current	< 1.3nA/cm^2
Dynamic Range	> 72 dB
Power Supply	3.0–3.6VDC
Power Requirements	< 20mA active < 10μA Standby
Package	24 pin LCC

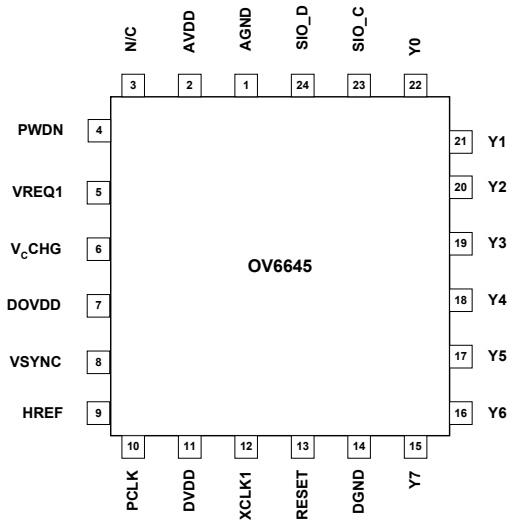

Figure 1. OV6645 Pin Diagram

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Pin Description

Table 1. Pin Description

Pin	Name	Pin Type	Function/Description
01	AGND	P	Analog ground
02	AVDD	P	Analog power supply (+3.3VDC), Bypass to ground with a 0.1μF capacitor
03	N/C	NC	Not connected internally
04	PWDN	Function (Default=0)	Enable Power Down, or sleep mode. All control register settings are maintained. "0" – Operating "1" – Powered Down
05	VREQ	V_{REF} (1.5V)	Array reference. Bypass to ground with a 0.1μF capacitor.
06	V_rCHG	V_{REF} (2.7V)	Internal voltage reference. Bypass to ground with a 1μF capacitor.
07	DOVDD	P	Power supply for digital output drive (3.3V)
08	VSYNC	O	Vertical sync output
09	HREF	O	HREF output (active video), used for horizontal sync.
10	PCLK	O	PCLK (Pixel Clock) output
11	DVDD	P	Digital power supply (+3.3VDC), Bypass to ground with a 0.1μF capacitor
12	XCLK1	I	Clock input
13	RESET	Function (Default=0)	Chip reset, active high. When asserted high, the control register settings are reset to the factory defaults.
14	DGND	P	Digital ground
15	Y7	O	Bit 7 of Y/UV video data output
16	Y6	O	Bit 6 of Y/UV video data output
17	Y5	O	Bit 5 of Y/UV video data output
18	Y4	O	Bit 4 of Y/UV video data output
19	Y3	O	Bit 3 of Y/UV video data output
20	Y2	O	Bit 2 of Y/UV video data output
21	Y1	O	Bit 1 of Y/UV video data output
22	Y0	O	Bit 0 of Y/UV video data output
23	SIO-C	I	SCCB serial control interface clock input.
24	SIO-D	I/O	SCCB serial control interface data input and output.

Legend: (I=Input), (O=Output), (I/O=Bi-directional), (P=Power)

Electrical and Mechanical Characteristics

Table 2. General Characteristics

Descriptions	Min	Max	Units
Operating temperature (guaranteed performance)	0	40	°C
Operating temperature (chip functional)	-10	70	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 3. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Min	Typ	Max	Units
Supply					
V_{DD1}	Supply voltage (DEVDD, ADVDD, AVDD, SVDD)	3.0	3.3	3.6	V
I_{DD1}	Supply current (@60 FPS frame rate and 3.3V digital I/O with 25pF plus 1TTL loading on 8-bit data bus)		20	25	mA
I_{DD2}	Supply current (V_{DD}=3V, @60 FPS frame rate without digital I/O loading)		15		mA
I_{DD3}	Standby supply current		5	10	µA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	PF
	Input pin impedance				
Digital Outputs (standard loading 25pF, 1.2KΩ to 3V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
	Output pin source	8		24	mA
	Output sink current	7		21	mA
SCCB Input					
V_{IL}	SIO-C and SIO-D (V_{DD2}=3V)	-0.5	0	1	V
V_{IH}	SIO-C and SIO-D (V_{DD2}=3V)	2.5	3	V_{DD}+0.5	V

Table 4. AC Characteristics (T_A=25°C, V_{DD}=3V)

Symbol	Descriptions	Min	Typ	Max	Units
ADC Parameters					
B	Analog bandwidth				MHz
Φ_{DIFF}					
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB

Table 5. Timing Characteristics

Symbol	Descriptions	Min	Typ	Max	Units
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1)	10	17.734	27	MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%

Symbol	Descriptions	Min	Typ	Max	Units
SCCB Timing (400Kbit/s)					
t_{BUF}	Bus free time between STOP and START	1.3			ms
$t_{HD:SAT}$	SIO-D change after START status	0.6			µs
t_{LOW}	SIO-D low period	1.3			µs
t_{HIGH}	SIO-D high period	0.6			µs
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:DAT}$	Data setup time	0.1			µs
$t_{SU:STP}$	Setup time for STOP status	0.6			µs
Digital Timing					
t_{PCLK}	PCLK cycle time 8-bit operation	56			ns
t_r, t_f	PCLK rise/fall time			15	ns
t_{PDD}	PCLK to data valid			15	ns
t_{PHD}	PCLK to HREF delay	5	10	20	ns

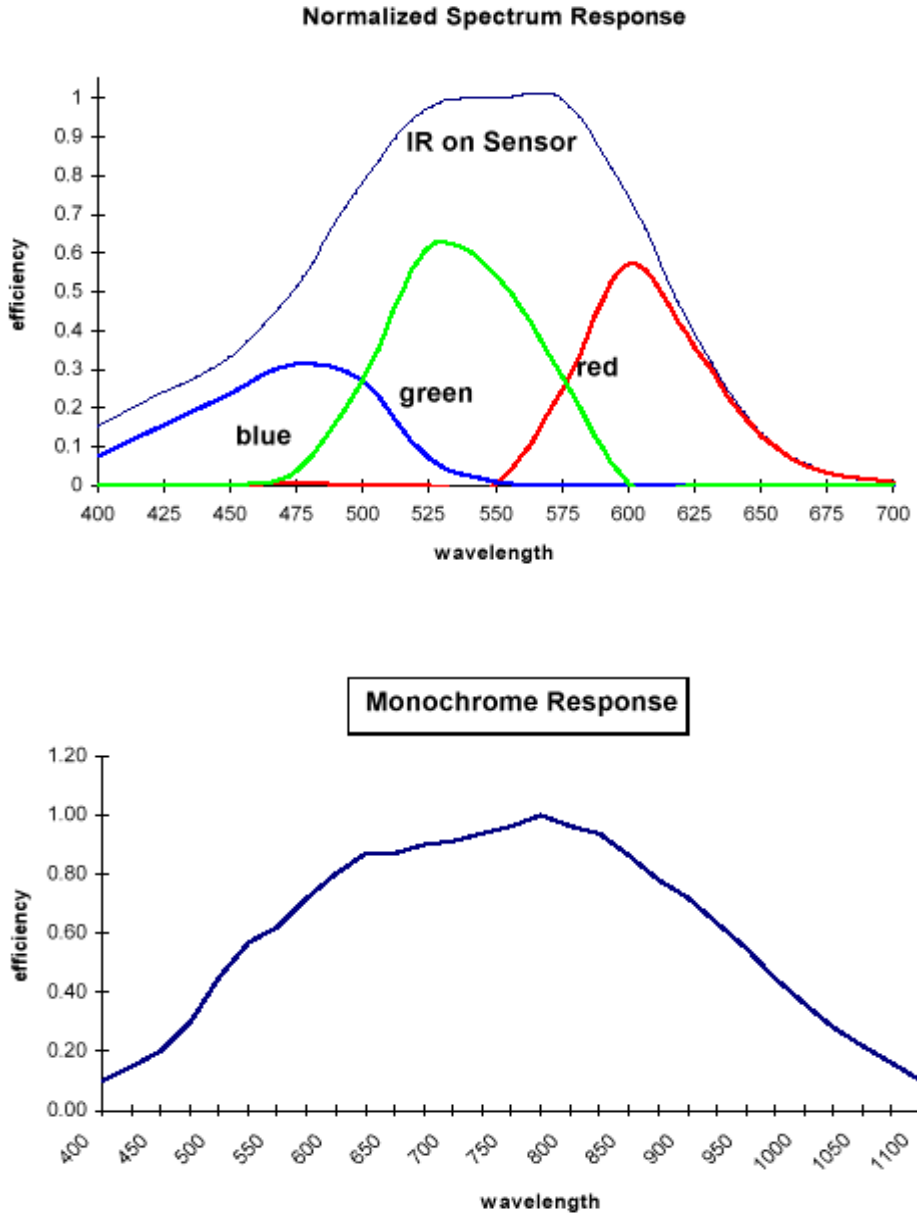


Figure 2. OV6645 Light Response

Function Description

Overview

Referring to Figure 3 below, the OV6645 sensor includes a 352 x 288 resolution image array, an analog signal processor, dual 8-bit A/D converters, analog video multiplexer, digital data formatter, video port, SCCB interface, registers, and digital controls that include timing block, exposure control, black level control, and white balance.

The OV6645 sensor is a 0.2" CMOS imaging device. The sensor contains approximately 101,376 pixels (352x288). Its design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme. The color filter of the sensor consists of a primary color RG/GB array arranged in line-alternating fashion.

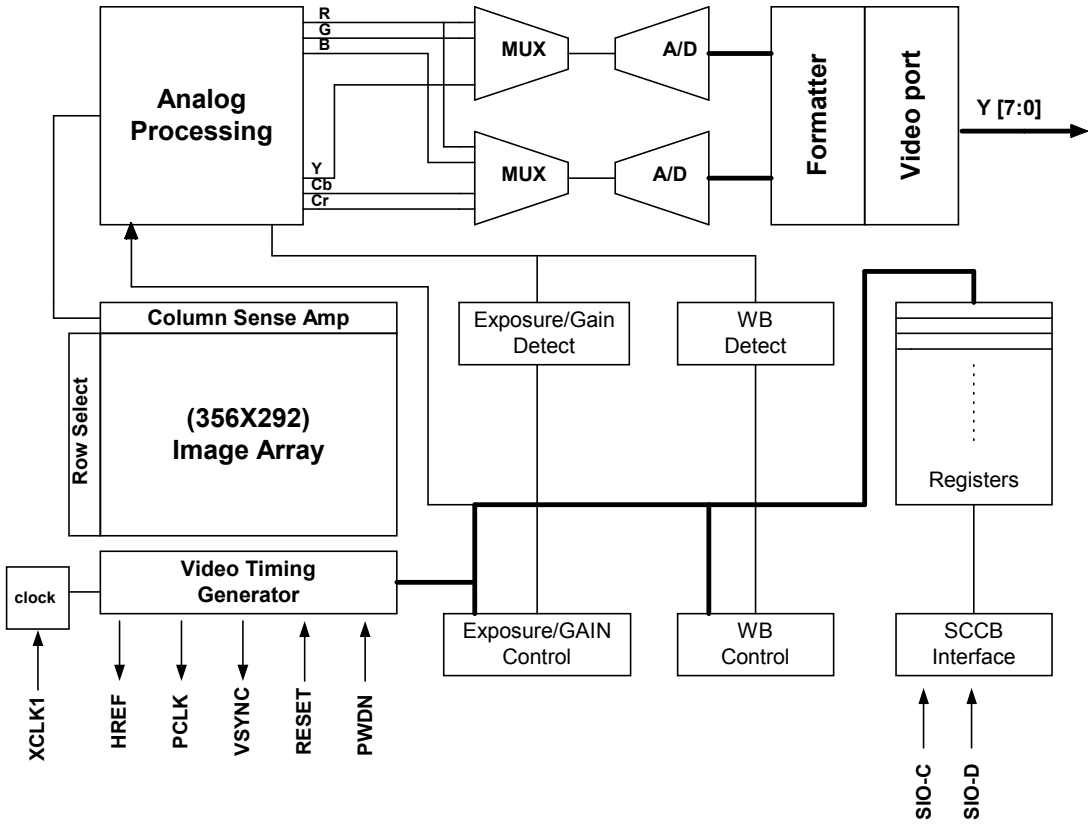


Figure 3. OV6645 CMOS Image Sensor Block Diagram

Analog Processor Circuits

Overview

The image is captured by the 352 x 288 pixel image array and routed to the analog processing section where the majority of signal processing occurs. This block contains the circuitry that performs color separation, color correction, automatic gain control (AGC), gamma correction, color balance, black level calibration, "knee" smoothing, aperture correction, controls for picture luminance and chrominance, and hue control for color. The analog video signals are based on the following formula:

Y = 0.59G + 0.31R + 0.11B
U = B – Y
V = R – Y
Where R,G,B are the equivalent color components in each pixel.

YCrCb format is also supported, based on the formula below:

Y = 0.59G + 0.31R + 0.11B
Cr = 0.713 (R – Y)
Cb = 0.564 (B – Y)

The YCrCb/RGB data signal from the analog processing section is fed to two on-chip 8-bit analog-to-digital (A/D) converters: one for the Y/G channel and one shared by the CrCb/BR channels. The converted data stream is further conditioned in the digital formatter. The processed signal is delivered to the digital video port through the video multiplexer which routes the user-selected 8-, or 4-bit video data to the correct output pins.

The on-chip 8-bit A/D operates at up to 9 MHz (approximately), and is fully synchronous to the pixel rate. Actual conversion rate is related to the frame rate. A/D black-level calibration circuitry ensures:

- The black level of Y/RGB is normalized to a value of 16
- The peak white level is limited to 240
- CrCb black level is 128
- CrCb Peak/bottom is 240/16
- RGB raw data output range is 16/240

(Note: Values 0 and 255 are reserved for sync flag)

Image Processing

The algorithm used for the electronic exposure control is based on the brightness of the full image. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the automatic exposure control (AEC) white/black ratio may be adjusted to suit the needs of the application.

Additional on-chip functions include:

- AGC that provides a gain boost of up to 24dB
- White balance control that enables setting of proper color temperature and can be programmed for automatic or manual operation.
- Separate saturation, brightness, hue, and sharpness adjustments allow for further fine-tuning of the picture quality and characteristics.

The OV6645 image sensor also provides control over the White Balance ratio for increasing/decreasing the image field Red/Blue component ratio. The sensor provides a default setting that may be sufficient for many applications.

Windowing

The windowing feature of the OV6645 image sensors allows user-definable window sizing as required by the application (See Figure 4). Window size setting (in pixels) ranges from 2 x 2 to 356 x 292, and can be positioned anywhere inside the 356 x 292 boundary. Note that modifying window size and/or position does not change frame or data rate. The OV6645 imager alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 352 x 288.

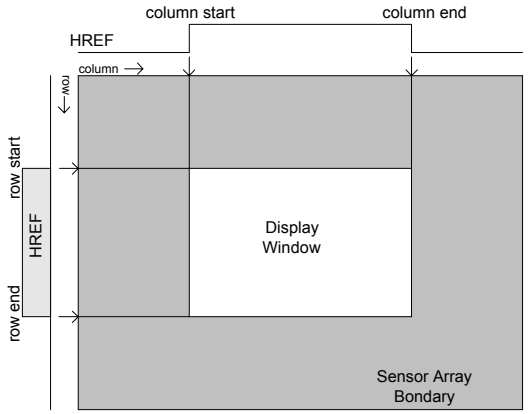


Figure 4. Windowing

QCIF Format

A QCIF mode is available for applications where higher resolution image capture is not required. Only half of the pixel rate is required when programmed in this mode. Default resolution is 176 x 144 pixels and can be programmed for other resolutions. Refer to Table 10. QCIF Digital Output Format (YUV beginning of line)

Video Output

The video output port of the OV6645 image sensors provides a number of output format/standard options to suit many different application requirements.

Table 6. Digital Output Format indicates the output formats available. These formats are user-programmable through the SCCB interface.

The OV6645 imager supports ITU-656 output formats in the following configurations:

8-bit data mode

- *(In this mode, video information is output in Cb Y Cr Y order using the one port only and running at twice the pixel rate. See* Table 7. 4:2:2 8-bit Format *below)*

4-bit nibble mode

- *(In the nibble mode, video output data appears at bits Y4-Y7. The clock rate for the output runs at twice the normal output speed when in B/W mode, and 4 times the normal pixel clock.)*

704 x 288 format

- *(When programmed in this mode, the pixel clock is doubled and the video output sequence is* $Y_0Y_0Y_1Y_1 \cdots$ *and* $U_0U_0V_0V_0 \cdots$. *See* Figure 5. Pixel Data Bus (YUV Output) *below.)*

The OV6645 imager provides VSYNC, HREF, PCLK, as standard output video timing signals**.**

The OV6645 imager can also be programmed to provide RGB data 8-bit, and 4-bit format. The output sequence is matched to the OV6645 color filter pattern (See Figure 6. Pixel Data Bus (RGB Output)). The output sequence is B G R G.

In RGB data ITU-656 modes, the OV6645 imager asserts SAV (Start of Active Video) and EAV (End of Active Video) to indicate the beginning and the ending of HREF window. As a result, SAV and EAV change with the active pixel window. The 8-bit RGB data is also accessible without SAV and EAV information.

Another useful format is RGB single-line RAW data format. It output data one line with each horizontal HREF, in the even line, the sequence is BGBG and odd line is GRGR, it exactly matches the Bayer pattern color filter.

The OV6645 imager offers flexibility in YUV output format. The device may be programmed as standard YUV 4:2:2. The device may also be configured to "swap" the U V sequence. When swapped, the 8-bit configuration becomes:

- V Y U Y···.

The third format available in the 8-bit configuration is the Y/UV sequence swap:

- Y U Y V···.

The MSB and LSB of Y/UV or RGB output can be reversed. Y7 is MSB and Y0 is LSB in the default setting. Y7 becomes LSB and Y0 becomes MSB in the reverse order configuration. Y2-Y6 are also reversed appropriately.

Table 6. Digital Output Format

Resolution	Pixel Clock	352 x 288	704 x 288	176 x 144
YUV	8-bit	Y	Y	Y
	ITU-656	Y	Y	Y
	Nibble	Y	Y	Y
RGB	8-bit	Y	Y	Y
	ITU-656[1]	Y	Y	Y
	Single-line	Y		Y
Y/UV swap	YUV	Y	Y	Y
	RGB	Y	Y	Y
U/V swap[2]	8-bit	Y	Y	Y
Single-line	8-bit	Y		
MSB/LSB swap		Y	Y	Y

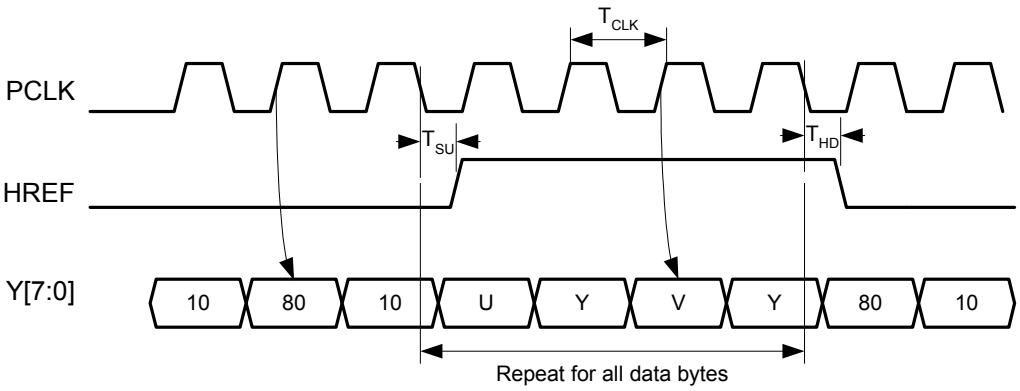
Notes:

("Y" indicates mode/combination is supported by OV6645)

1. Output is 8-bit in RGB ITU-656 format. SAV and EAV are inserted at the beginning and ending of HREF, which synchronize the acquisition of VSYNC and HSYNC. 8-bit data bus configuration (without VSYNC and CHSYNC) can provide timing and data in this format.
2. U/V swap means neighbor row B R output sequence swaps in RGB format. Refer to RGB raw data output format for further details.

Table 7. 4:2:2 8-bit Format

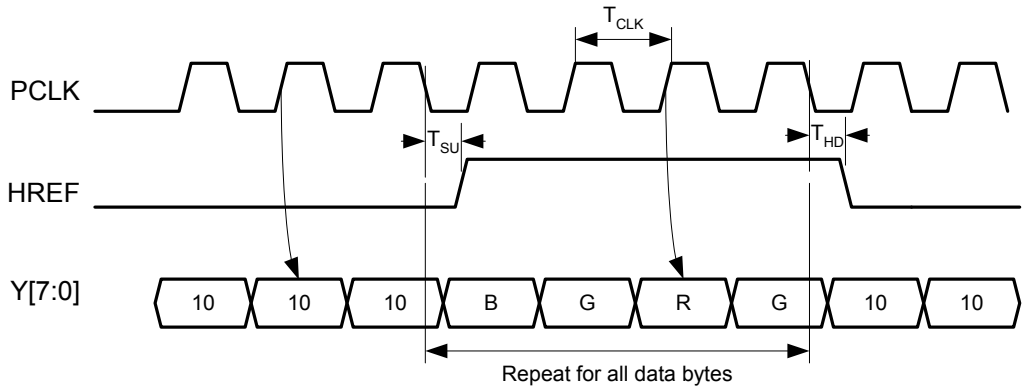
Data Bus	Pixel Byte Sequence							
Y7	U7	Y7	V7	Y7	U7	Y7	V7	
Y6	U6	Y6	V6	Y6	U6	Y6	V6	
Y5	U5	Y5	V5	Y5	U5	Y5	V5	
Y4	U4	Y4	V4	Y4	U4	Y4	V4	
Y3	U3	Y3	V3	Y3	U3	Y3	V3	
Y2	U2	Y2	V2	Y2	U2	Y2	V2	
Y1	U1	Y1	V1	Y1	U1	Y1	V1	
Y0	U0	Y0	V0	Y0	U0	Y0	V0	
Y Frame	0		1		2		3	
UV Frame	0 1				2 3			



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

Note: *T_{CLK} is pixel clock period.T_{CLK}=56ns for 8-bit output if the system clock is 17.73MHz. T_{SU} is the setup time of HREF. The maximum is 15ns. T_{HD} is the hold time of HREF. The maximum is 15ns.*

Figure 5. Pixel Data Bus (YUV Output)



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

Note: *T_{CLK} is pixel clock period. T_{CLK}=56ns for 8-bit output if the system clock is 17.73MHz. T_{SU} is the setup time of HREF. The maximum is 15ns. T_{HD} is the hold time of HREF. The maximum is 15ns.*

Figure 6. Pixel Data Bus (RGB Output)

The default Y/UV channel output port relation before MSB/LSB swap:

Table 8. Default Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The relation after MSB/LSB swap changes to:

Table 9. Swapped MSB/LSB Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Table 10. QCIF Digital Output Format (YUV beginning of line)

Pixel #	1	2	3	4	5	6	7	8
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
UV	U0, V0	U1, V1	U2, V2	U3, V3	U4, V4	U5, V5	U6, V6	U7, V7

- Y channel output U0Y0 V2Y2 U4Y4 V6 Y6 U8Y8 V10Y10 ···
- Half (176 pixels) data are outputted every line and only half line data (every other line, total 144 lines) in one frame.

Table 11. QCIF Digital Output Format (RGB raw data beginning of line)

Pixel #	1	2	3	4	5	6	7	8
Line 1	B0	G1	B2	G3	B4	G5	B6	G7
Line 2	G0	R1	G2	R3	G4	R5	G6	R7

Default RGB two line output mode:
- Y channel outputB0G1 G0 R1B4G5 G4 R5 B8G9G8 R9 ···
- Every line outputs half data (176 pixels) and all lines (144 lines) data in one frame will be output.

RGB Raw data single-line output mode:
- Y channel output B0 G1 B4 G5 B8 G9 ··· at even lines and G0R1G4R5G8R9··· at odd lines
- Every other 2 lines output (1,2,5,6,9,10···)

OV6645 provides raw data format. The following format is defined. The format is based on Bayer pattern color filter format.

Table 12. RGB Raw Data Format

R\C	1	2	3	4	···	353	354	355	356
1	$B_{1,1}$	$G_{1,2}$	$B_{1,3}$	$G_{1,4}$		$B_{1,353}$	$G_{1,354}$	$B_{1,355}$	$G_{1,356}$
2	$G_{2,1}$	$R_{2,2}$	$G_{2,3}$	$R_{2,4}$		$G_{2,353}$	$R_{2,354}$	$G_{2,355}$	$R_{2,356}$
3	$B_{3,1}$	$G_{3,2}$	$B_{3,3}$	$G_{3,4}$		$B_{3,353}$	$G_{3,354}$	$B_{3,355}$	$G_{3,356}$
4	$G_{4,1}$	$R_{4,2}$	$G_{4,3}$	$R_{4,4}$		$G_{4,353}$	$R_{4,354}$	$G_{4,355}$	$R_{4,356}$
289	$B_{289,1}$	$G_{289,2}$	$B_{289,3}$	$G_{289,4}$		$B_{289,353}$	$G_{289,354}$	$B_{289,355}$	$G_{289,356}$
290	$G_{290,1}$	$R_{290,2}$	$G_{290,3}$	$R_{290,4}$		$G_{290,353}$	$R_{290,354}$	$G_{290,355}$	$R_{290,356}$
291	$B_{291,1}$	$G_{291,2}$	$B_{291,3}$	$G_{291,4}$		$B_{291,353}$	$G_{291,354}$	$B_{291,355}$	$G_{291,356}$
292	$G_{292,1}$	$R_{292,2}$	$G_{292,3}$	$R_{292,4}$		$G_{292,353}$	$R_{292,354}$	$G_{292,355}$	$R_{292,356}$

Notes:

Single-line mode:

- 1st HREF Y channel output B_{11} G_{12} B_{13} G_{14} ···
- 2nd HREF Y channel output G_{21} R_{22} G_{23} R_{24} ···

8-bit Format (Total 292 HREFs):

- 1st HREF Y channel output unstable data.
- 2nd HREF Y channel output B_{11} G_{21} R_{22} G_{12} ···
- 3rd HREF Y channel output B_{31} G_{21} R_{22} G_{32} ···
- PCLK timing is doubled and PCLK rising edge latch data bus. Every line data output twice.

4-bit Nibble Mode Output Format:

- Uses higher 4 bits of Y port (Y[7:4]) as output port.
  - Supports YCrCb/RGB data,ITU-656 timing, Color/B&W.
  - Output sequence: High order 4 bits followed by lower order 4 bits
    $Y0_H$ $Y0_L$ $Y1_H$ $Y1_L$ ···
    $U0_H$ $U0_L$ $V0_H$ $V0_L$ ···
    Note: For B/W or single-line RGB raw data, the output data clock speed is doubled. In color mode, for nibble timing, the clock speed must be quadrupled.

Output sequence: $U0_H$ $U0_L$ $Y0_H$ $Y0_L$ $V0_H$ $V0_L$ $Y1_H$ $Y1_L$ ··

Reset

OV6645 includes a RESET pin (pin 13) that forces a complete hardware reset when it is pulled high (VCC). OV6645 clears all registers and resets to their default values when a hardware reset occurs. Reset can also be initiated through the SCCB interface.

Power-down Mode

Two methods are available to place OV6645 into power-down mode: hardware power-down and SCCB software power-down. All internal register settings remain unchanged when OV6645 is in the power-down mode.

To initiate hardware power-down, the PWDN pin (pin 4) must be tied to high (+3.3VDC). When this occurs, OV6645 internal device clock is halted and all internal counters are reset. The current draw is less than 10μA in this standby mode.

Executing a software power-down through the SCCB interface suspends internal circuit activity, but does not halt the device clock. The current requirements drop to less than 1mA in this mode.

Configure OV6645

The on-chip SCCB register programming capability provides a flexible and comprehensive method for configuring the OV6645. The SCCB interface provides access to all the programmable internal registers.

Register Set

The table below provides a list and description of available SCCB registers contained in the OV6645 image sensor. The device address for the OV6645 is C1 for write and C0 for read.

Table 13. SCCB Registers

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
00	GAIN	00	RW	AGC gain control GC[7:6] – Unimplemented. GC[5:0] – The current gain setting. *This register is updated automatically if AGC is enabled. The internal controller stores the optimal gain value in this register. The current value is stored in this register if AGC is not enabled.*
01	BLUE	80	RW	Blue gain control BLU[7:0] – blue channel gain balance value. "FFh" is highest and "00h" is lowest. *This register is updated automatically if AWB is enabled.*
02	RED	80	RW	Red gain control RED[7:0] – red channel balance value. "FFh" is highest and "00h" is lowest. *This register is updated automatically if AWB is enabled.*
03	SAT	80	RW	Color saturation control SAT[7:4] – Saturation adjustment. "F8h" is highest and "00h" is lowest. SAT[3:2] – YUV/YCrCB selection: "00" U = u, V = v "01" U = 0.938u, V = 0.838v "10" U = 0.563u, V = 0.714v "11" U = 0.5u, V = 0.877v SAT[1:0] – – Y channel delay selection: 0 ~ 3tp
04	HUE	10	RW	Color hue control HUE[7:6] – UV delay selection. "00" – no delay. "01" – 2tp delay with 3 points average. "10" – 4tp delay. "11" same as "01" . HUE[5] – Enable smart color HUE[4:0] – HUE control, range -30°~30°
05	ARL	A0	RW	AEC/AGC reference level ARL[7:5] – Voltage reference selection (Higher voltage = brighter final stable image) "000" = Lowest reference level "111" = Highest reference level ARL[4:0] – Reserved
06	BRT	80	RW	Brightness control BRT[7:0] – Brightness adjustment. "FFh" is highest and "00h" is lowest.
07	SHP	C6	RW	Sharpness control SHP[7:4] – Coring adjustment. Range: 0~80mV with step 5mV. SHP[3:0] – Strength adjustment. Range: 0~8× with step 0.5×.
08	OFC	00	RW	Dark current compensation OFC[7] – sign bit of offset. "0" positive offset and "1" negative offset. OFC[6:0] – add an offset before AGC to compensate the dark current.
09	CPP	08	RW	Color processing parameter control CPP[7:3] – Reserved CPP[2] – 1" aperture correction enable. Correction strength and threshold value will be decided by SHP[7:0]. CPP[1:0] – Reserved
0A	PID	66	R	Product ID number read only
0B	VER	40	R	Product version number, read only

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
0C	ABLU	20	RW	White balance background: Blue channel ABLU[7:6] – Reserved ABLU[5:0] - White balance blue ratio adjustment. [3F]=most blue, [00]=least blue
0D	ARED	20	RW	White balance background: Red channel ARED[7:6] – rsvd ARED[5:0] - White balance red ratio adjustment. [3F]=most red, [00]=least red
0E	COMR	0D	RW	Common control R COMR[7] – 3 dB gain boost COMR[6:4] – Reserved COMR[3:2] – Red channel pre-amplifier gain. 1~1.6x COMR[1:0] – Blue channel pre-amplifier gain 1~1.6x
0F	COMS	A8	RW	Common control S COMS[7:6] – Reserved COMS[5] – Luminance gamma function on/off COMS[4] – Bypass RGB matrix function COMS[3:0] – Reserved
10	AEC	9A	RW	Automatic exposure control AEC[7:0] - Set exposure time $T_{EX} = 2 \times T_{LINE} \times AEC[7:0]$
11	CLKRC	00	RW	Clock rate control CLKRC[7:6] – Sync output polarity selection “00” – HSYNC=Neg, CHSYNC=Neg, VSYNC=Pos “01” – HSYNC=Neg, CHSYNC=Neg, VSYNC=Neg “10” – HSYNC=Pos, CHSYNC=Neg, VSYNC=Pos “11” – HSYNC=Pos, CHSYNC=Pos, VSYNC=Pos CLKRC[5:0] – Clock pre-scaler CLK = (MAIN_CLOCK / ((CLKRC[5:0] + 1) × 2)) / n Where n=1 if register [3E], COMO<7> is set to “1” and n=2 otherwise.
12	COMA	24	RW	Common control A COMA[7] – SRST, “1” initiates soft reset. All registers are set to default values and chip is reset to known state and resumes normal operation. This bit is automatically cleared after reset. COMA[6] – MIRR, “1” selects mirror image COMA[5] – AGCEN, “1” enables AGC, COMA[4] – Digital output format, “1” selects 8-bit: Y U Y V Y U Y V. “0” selects 8-bit UYVYUYVY COMA[3] – Select video data output: “1” - select RGB, “0” - select YCrCb COMA[2] – Auto white balance “1” - Enable AWB, “0” - Disable AWB COMA[1] – Color bar test pattern: “1” - Enable color bar test pattern COMA[0] – Reserved
13	COMB	01	RW	Common control B COMB[7] – Enable TV timing. At this mode, analog luminance output can drove TV. COMB[6] – Enable nibble mode. COMB[5] – Reserved. COMB[4] – “1” - enable digital output in ITU-656 format COMB[3] – CHSYNC output. “1” - horizontal sync, “0” - composite sync COMB[2] – “1” – Tri-state Y and UV busses. “0” - enable both busses COMB[1] – Reserved COMB[0] – “1” - Enable auto adjust mode.

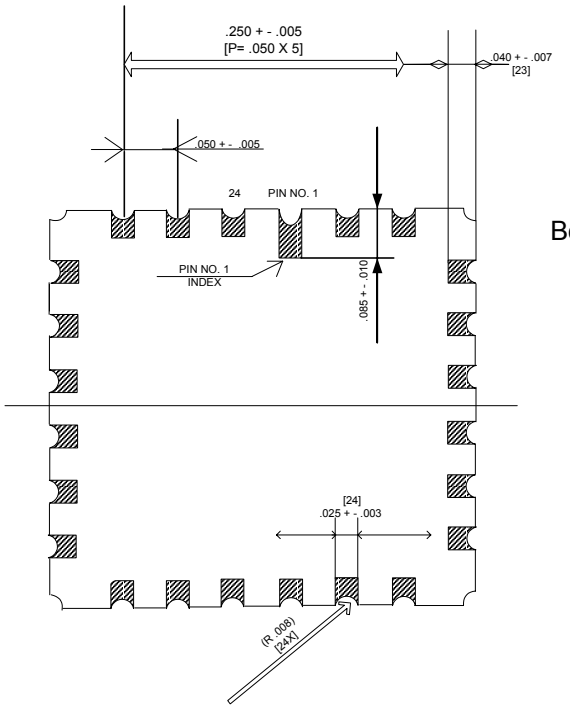
Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
14	COMC	00	RW	Common control C COMC[7] – reserved COMC[6] – "1" Enable one frame drop when AEC change to keep data valid when Banding filter mode enable. COMC[5] – QCIF digital output format selection. 1 - 176x144; 0 - 352x288. COMC[4] – Field/Frame vertical sync output in VSYNC port selection: 1 - frame sync, only ODD field vertical sync; 0 - field vertical sync, effect in Interlaced mode COMC[3] – HREF polarity selection: 0 - HREF positive effective, 1 - HREF negative. COMC[2] – gamma selection: 1 - RGB Gamma on ; 0 - RGB gamma is 1. COMC[1:0] – Select the maximum AGC. "00" maximum gain=6dB, step 1/16 "01" maximum gain=12dB, step 1/16 "10" maximum gain=6dB, step 1/16 "11" maximum gain=18dB, step 1/8reserved
15	COMD	01	RW	Common Control D COMD[7] – Optical black output enable. "1" HREF has extra line at the beginning of the frame to output black signal. Effective only COMD[5] high COMD[6] – PCLK polarity selection. "0" - OV6645 output data at PCLK falling edge and data bus will be stable at PCLK rising edge; "1" - rising edge output data and stable at PCLK falling edge. This bit is disable and should use PCLK rising edge latch data bus in ITU-656 format (COMB[4]=1). COMD[5] – Enable optical black function COMD[4] – Enable BLC with optical black line COMD[3:1] – Reserved. COMD[0] – U V digital output sequence exchange control. 1 - U Y V Y ··· for 8-bit; 0 -V Y U Y ··· for 8-bit.
16	FSD	03	RW	Field slot division FSD[7:2] – Field interval selection. It has functional in EVEN and ODD mode defined by FSD[1:0]. It is disabled in OFF and FRAME mode. The purpose of FSD[7:2] is to divide the video signal into programmed number of time slots, and allows HREF to be active only one field in every FSD[7:2] fields. It does not affect the video data or pixel rate. FSD[7:2] disables digital data output, there is only black reference level at the output. FSD[7:2]=1 outputs every field. FSD[7:2]=2 outputs one field and disables one field, etc. FSD[1:0] – field mode selection. Each frame consists of two fields: Odd and Even, FSD[1:0] define the assertion of HREF in relation to the two fields. "00" – OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13) "01" – ODD mode; HREF is asserted in odd field only. "10" – EVEN mode; HREF is asserted in even field only. "11" – FRAME mode; HREF is asserted in both odd field and even field. FSD[7:2] disabled.
17	HREFST	38	RW	Horizontal HREF start HS[7:0] – selects the starting point of HREF window, each LSB represents two pixels for CIF resolution mode, one pixels for QCIF resolution mode, this value is set based on an internal column counter, the default value corresponds to 352 horizontal window. Maximum window size is 356. See window description below. HS[7:0] programmable range is [38] - [EB], and should less than HE[7:0]. HS[7:0] should be programmable to value larger than or equal to [38]. Value larger than [EC] is invalid. See window description below.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
18	HREFEND	EA	RW	Horizontal HREF end HE[7:0] – selects the ending point of HREF window, each LSB represents two pixels for full resolution and one pixels for QCIF resolution, this value is set based on an internal column counter, the default value corresponds to the last available pixel. The HE[7:0] programmable range is [39] - [EC]. HE[7:0] should be larger than HS[7:0] and less than or equal to [EC]. Value larger than [EC] is invalid. See window description below.
19	VSTRT	03	RW	Vertical line start VS[7:0] – selects the starting row of vertical window, in full resolution mode, each LSB represents 1 scan line in one frame. See window description below. Min. is [03], max. is [93] and should less than VE[7:0].
1A	VEND	92	RW	Vertical line end VE[7:0] – selects the ending row of vertical window, in full resolution mode, each LSB represents 1 scan line in one frame, see window description below. Min. is [04], max. is [94] and should larger than VS[7:0].
1B	PSHFT	00	RW	Pixel shift PS[7:0] – to provide a way to fine tune the output timing of the pixel data relative to that of HREF, it physically shifts the video data output time late in unit of pixel clock as shown in the figure below. This function is different from changing the size of the window as defined by HS[7:0] and HE[7:0] in registers 17 and 18. Higher than default number delay the pixel output relative to HREF. The highest number is “FF” and the maximum shift number is delay 256 pixels.
1C	MIDH	7F	R	Manufacture ID byte: High MIDH[7:0] – read only, always returns “7F” as manufacturer’s ID no.
1D	MIDL	A2	R	Manufacture ID byte: Low MIDL[7:0] – read only, always returns “A2” as manufacturer’s ID no.
1E	HSST	0F	RW	Horizontal sync start position HSST[7:0] – lower 8 bit of horizontal sync starting position, combined with register bit of COMI[4], total 9 bit control. range: [00] -- [FF]. HSEND[8:0] must be less than HSST[8:0]
1F	HSEND	3C	RW	Horizontal sync end position HEND[7:0] – lower 8 bit of horizontal sync ending position, combined with register bit of COMI[3], total 9 bit control. range: [00] - [FF]. HSEND[8:0] must be larger than HSST[8:0]
20	COME	00	RW	Common control E COME[7] – HREF pixel number selection. “1” - HREF include 704 PCLK, every data output twice. COME[6] – AWB value in Reg<1> and Reg<2> can be updated by manual in auto mode. COME[5] – Central 1/4 image area rather whole image used to calculate AWB. “0” uses whole image area to calculate AWB. COME[4] – Digital output driver capability increase selection: “1” Double digital output driver current; “0” low output driver current status. Independent control with COME[0]. COME[3] – Enable system reset when write Reg<11>. COME[2:1] – AWB fast/slow mode selection. “11” - AWB is the fastest mode, that is register [01] and [02] is changed every field. “10” AWB change every 4 fields. “00” AWB change every 16 fields, is the slowest mode. COME[0] – Digital output driver capability increase selection: “1” Double digital output driver current; “0” low output driver current status.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
21	YOFF	80	RW	Y channel offset adjustment YOFF[7] – Offset adjustment direction 0 - Add Y[6:0]; 1 -Subtract Y[6:0]. YOFF[6:0] –Y channel digital output offset adjustment. Range: +127 ~ -127. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through SCCB has no effect. COMG[2]=1, Y channel offset adjustment will use the stored value which can be changed through SCCB. This register has no effect to A/D output data if COMF[1]=0. If output RGB raw data, this register will adjust R/G/B data.
22	UOFF	80	RW	U Channel offset adjustment UOFF[7] – Offset adjustment direction: 0 - Add U[6:0]; 1 - Subtract U[6:0]. UOFF[6:0] – U channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through SCCB has no effect. COMG[2]=1, U channel offset adjustment will use the stored value which can be changed through SCCB. This register has no effect to A/D output data if COMF[1]=1. If output RGB raw data, this register will adjust R/G/B data.
23	CLKC	04	RW	Oscillator circuit control CLKC[7:6] – Select different crystal circuit power level (“11” = minimum). CLKC[5] – Enable smart banding filter mode. It means banding filter limited exposure time will out of limited when light is too strong. CLKC[4] – AEC/AGC change mode selection CLKC[3] – AEC/AGC change mode selection CLKC[2] – AEC/AGC change fastest mode CLKC[1] – AEC/AGC change fast mode CLKC[0] – AEC/AGC change slowest mode
24	AEW	33	RW	Automatic exposure control: Bright pixel ratio adjustment AEW[7:0] – Used as calculate bright pixel ratio. OV6645 AEC algorithm is count whole field bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is same as the ratio defined by register [25] and [26], image stable. This register is used to define bright pixel ratio, default is 25%, each LSB represent step: 0.5% Change range is: [01] ~ [CA]; Increase AEW[7:0] will increase bright pixel ratio. For same light condition, the image brightness will increase if AEW[7:0] increase. ***Note:*** *AEW[7:0] must combine with register [26] AEB[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] > [CA].*
25	AEB	97	RW	Automatic Exposure Control: Black pixel ratio adjustment AEB[7:0] – used as calculate black pixel ratio. OV6645 AEC algorithm is count whole field/ frame bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is same as the ratio defined by register [25] and [26], image stable. This register is used to define black pixel ratio, default is 80%, each LSB represent step: 0.5%; Change range is: [01] ~ [CA]; Increase AEB[7:0] will increase black pixel ratio. For same light condition, the image brightness will decrease if AEB[7:0] increase. ***Note:*** *AEB[7:0] must e combined with register [25] AEW[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] > [CA].*

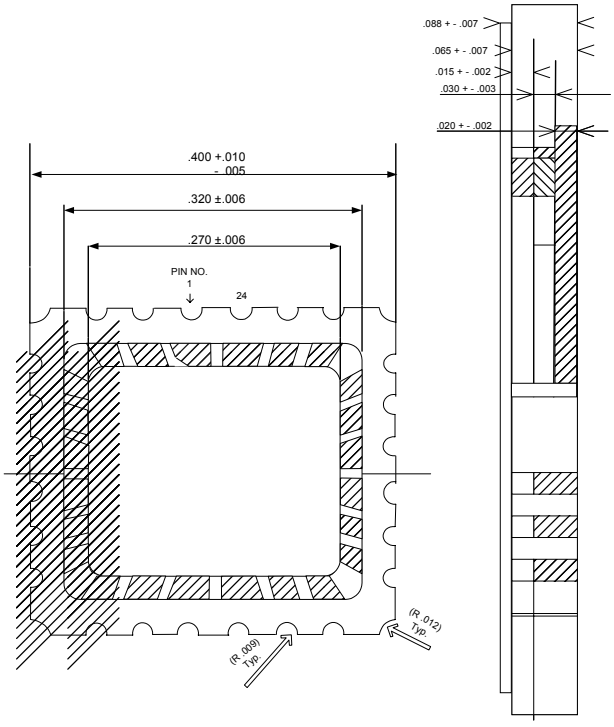
Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
26	COMF	B0	RW	Common control F COMF[7] – Input main clock divided by 2 or 4 selection. “1” -- 2; “0” – 4 COMF[6] – Enable Minimum exposure time is 4 line. Default is 1 line COMF[5] – Reserved. COMF[4] – PCLK output timing selection. “1” - PCLK valid only when HREF is high; “0” - PCLK is free running. COMF[3] – UV offset difference. “1” use separate offsets for U and V; “0” use one offset for both U and V. COMF[2] – Digital data MSB/LSB swap. “1” LSB→bit7, MSB→bit0; “0” normal. COMF[1] – “1” digital offset adjustment enable. “0” disable. COMF[0] – “1” Output first 4 line black level before valid data output. HREF number will increase 4 relatively. “0” no black level output.
27	COMG	A0	RW	Common control G COMG[7:5] – reserved COMG[4] – Soft chip power down enable, can be waked up by disable this bit COMG[3] – Tri-state all control signal output (VSYNC, HREF, PCLK). COMG[2] – “1” digital offset adjustment manually mode enable. Digital data will be add/subtract a value defined by register [21] and [22], the contents are programmed through SCCB. “0” - digital data will be added/subtract a value defined by register [21] and [22], which are updated by internal circuit. COMG[1] – Digital output full range selection. OV6645 default output data range is [10] - [F0]. The output range changes to [01] - [FE] with signal overshoot and undershoot level if COMG[1]=1. COMG[0] – reserved.
28	COMH	01	RW	Common control H COMH[7] – “1” selects one-line RGB raw data output format, “0” selects normal two-line RGB raw data output. COMH[6:5] – Reserved COMH[4] – Freeze AEC/AGC value, effective only at COMB[0]=1. “1” - register [00] and [10] will not be updated and hold latest value. “0” - AEC/AGC normal working status. COMH[3] – AGC disable. “1” - when COMB[0]=1 and COMA[5]=1, internal circuit will not update register [00], register [00] will kept latest updated value before COMH[3]=1. “0” - when COMB0=1 and COMA[5]=1, register [00] will be updated by internal algorithm. COMH[2:0] – Reserved.
29	COMI	00	RW	Common control I COMI[7] – AEC disable. “1” If COMB[0]=1, AEC stop and register [10] value will be held at last AEC value and not be updated by internal circuit. “0” - if COMB[0]=1, register [10] value will be updated by internal circuit COMI[6] – “1” select CHSYNC output from HREF port. “0” normal COMI[5] – reserved COMI[4] – Central 1/4 image area rather whole image used to calculate AEC/AGC. “0” use whole image area to calculate AEC/AGC. COMI[3] – Highest 1 bit of horizontal sync starting position, combined with register [1E] COMI[2] – Highest 1 bit of horizontal sync ending position, combined with register [1F] COMI[1:0] – Version flag. For version A, value is [00], these two bits are read only.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
2A	COMJ	80	RW	Common control J OOMJ7] – Vertical sync only with valid data when "1", otherwise always output VSYNC. COMJ[6] – reserved COMJ[5] – Highest 1bit of frame rate adjust control byte. See explanation below. COMJ[4] – Tri-state Y port output when in power down mode. COMJ[3] – Y channel brightness adjustment enable. When COMF[2]=1 active. COMJ[2] – "1" update white balance update only if AGC/AEC is stable. "0" update white balance independent with AEC/AGC. COMJ[1] – Reserved. COMJ[0] – Banding filter on.
2B	FRARL	5E	RW	Frame rate adjust low FRARL[7:0] – Lowest 8 bit of frame rate adjust control byte. Frame rate adjustment resolution is 0.21%. Control byte is 10 bit. Every LSB equal decrease frame rate 0.21%. Range is 0.21% - 109%. IF frame rate adjustment enable, COME[7] must set to "0".
2C	Rsvd 2C	88	RW	Reserved
2D	Rsvd 2D	B6	RW	Reserved
2E	VCOFF	80	RW	V channel offset adjustment VCOFF[7] – Offset adjustment direction: "0" = Add V[6:0]; "1" = Subtract V[6:0]. VCOFF[6:0] – V channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write to this register through SCCB has no effect. If COMG[2] =1, V channel offset adjustment will use the stored value which can be changed through SCCB. If COMF[1] =1, this register has no effect to digital output data. If output RGB raw data, this register will adjust R/G/B data.
2F –33	Rsvd 2F-33	××	RW	Reserved
34	RGAM	8F	RW	RGB gamma control RGAM[7:6] Gamma curve saturation level selection for luminance. RGAM[5:4] Gamma curve turning point selection for luminance. RGAM[3:0] Different gamma curve selection.
35	YGAM	8F	RW	Luminance gamma control YGAM[7:6] Gamma curve saturation level selection for luminance. YGAM[5:4] Gamma curve turning point selection for luminance. YGAM[3:0] Different gamma curve selection.



Bottom View

Top View



Note:
Die thickness=0.0275

Figure 7. OV6645 Package Diagram

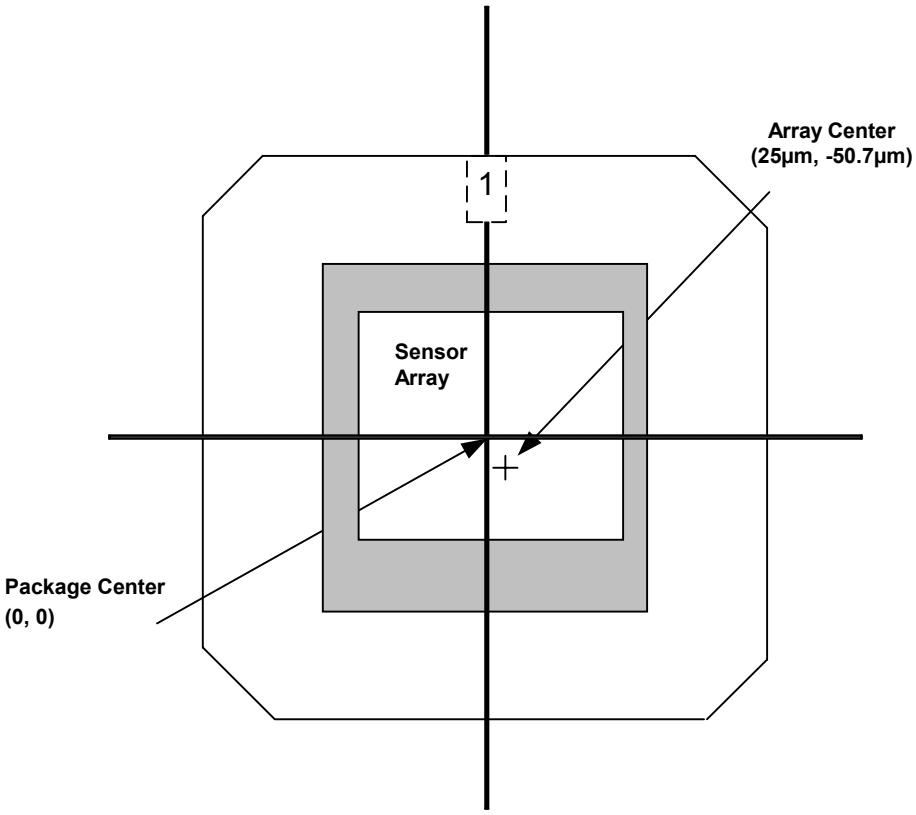


Figure 8. OV6645 Sensor array center location

Note: *Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 down.*