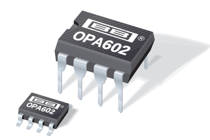
OPA602



SBOS155A – AUGUST 1987 – REVISED OCTOBER 2002

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- **WIDE BANDWIDTH: 6.5MHz**
- **HIGH SLEW RATE: 35V/µs**
- **LOW OFFSET: ±250µV max**
- **LOW BIAS CURRENT: ±1pA max**
- **FAST SETTLING TIME: 1µs to 0.01%**
- **UNITY-GAIN STABLE**

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **OPTOELECTRONICS**
- **SONAR, ULTRASOUND**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **MEDICAL EQUIPMENT**
- **DATA CONVERSION**

DESCRIPTION

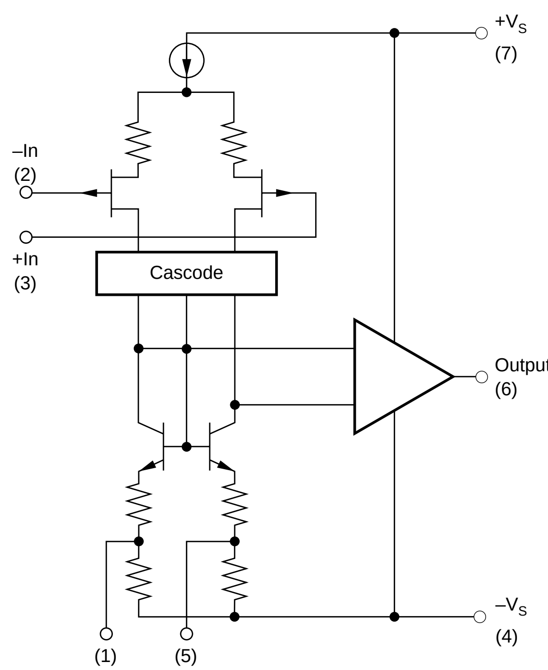
The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic ***Difet*** (dielectrically isolated FET) construction provides an unusual combination of high-speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. ***Difet*** construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.

Difet® Burr-Brown Corp.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[(1)]

Supply Voltage	$\pm 18V_{DC}$
Internal Power Dissipation ($T_J \leq +175°C$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
P and U Packages	–40°C to +125°C
Operating Temperature Range	
P and U Packages	–25°C to + 85°C
Lead Temperature	
U Package, SO (3s)	+260°C
Output Short-Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

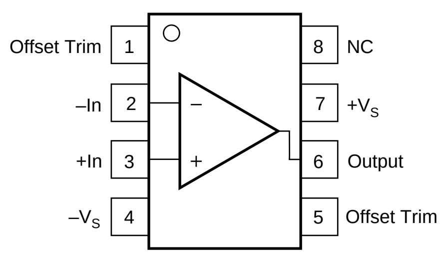
PACKAGE/ORDERING INFORMATION

PRODUCT	OFFSET VOLTAGE MAX (μV) AT 25°C	PACKAGE-LEAD	PACKAGE DESIGNATOR[(1)]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA602AP	±2000	DIP-8	P	–25°C to +85°C	602AP	602AP	Tubes, 50
OPA602BP	±1000	"	"	"	602BP	602BP	Tubes, 50
OPA602AU	±3000	SO-8	D	–25°C to +85°C	602AU	602AU	Tubes, 100

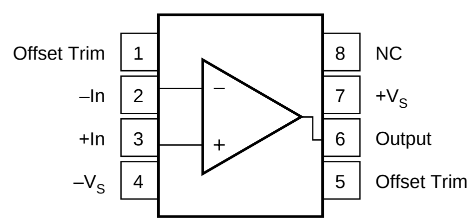
NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS

Top View **DIP, SO**



DIP-8



SO-8

NC = No Connection

ELECTRICAL CHARACTERISTICS

At $V_S = \pm15V_{DC}$ and $T_A = +25°C$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA602BP MIN	OPA602BP TYP	OPA602BP MAX	OPA602AP, AU MIN	OPA602AP, AU TYP	OPA602AP, AU MAX	UNITS
INPUT NOISE								
Voltage:								
f_O = 10Hz			23			✻		nV/√Hz
f_O = 100Hz			19			✻		nV/√Hz
f_O = 1kHz			13			✻		nV/√Hz
f_O = 10kHz			12			✻		nV/√Hz
f_B = 10Hz to 10kHz			1.4			✻		µVrms
f_B = 0.1Hz to 10Hz			0.95			✻		µVp-p
Current:								
f_B = 0.1Hz to 10Hz			12			✻		fAp-p
f_O = 0.1Hz to 20kHz			0.6			✻		fA/√Hz
OFFSET VOLTAGE								
Input Offset Voltage:								
P Package			0.5	1		1	2	mV
U Package						1	3	mV
Over Specified Temperature								
P, U Packages			±0.75	±1.5		±1.5		mV
Average Drift[(1)]	$T_A = T_{MIN}$ to T_{MAX}		±3	±5		✻	±15	µV/°C
Supply Rejection	$\pm V_S$ = 12V to 18V	80	100		70	✻		dB
BIAS CURRENT								
Input Bias Current	$V_{CM} = 0V_{DC}$		±1	±2		±2	±10	pA
Over Specified Temperature			±20	±200		±20	±500	pA
OFFSET CURRENT								
Input Offset Current	$V_{CM} = 0V_{DC}$		0.5	2		1	10	pA
Over Specified Temperature			20	200		20	500	pA
INPUT IMPEDANCE								
Differential			10^{13} || 1			✻		Ω || pF
Common-Mode			10^{14} || 3			✻		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±10.2	+13, –11		✻	✻		V
Common-Mode Rejection	$V_{IN} = \pm10V_{DC}$	88	100		75	✻		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 1k\Omega$	88	100		75	✻		dB
FREQUENCY RESPONSE								
Gain Bandwidth	Gain = 100	4	6.5		3.5	✻		MHz
Full-Power Response	20Vp-p, $R_L = 1k\Omega$		570			✻		kHz
Slew Rate	$V_O = \pm10V$, $R_L = 1k\Omega$	24	35		20	✻		V/µs
Settling Time:								
0.1%	Gain = –1, $R_L = 1k\Omega$		0.6			✻		µs
0.01%	C_L = 500pF, 10V Step		1.0					µs
RATED OUTPUT								
Voltage Output	$R_L = 1k\Omega$	±11.5	+12.9, –13.8		±11	✻		V
Current Output	$V_O = \pm10V_{DC}$	±15	±20		✻	✻		mA
Output Resistance	1MHz, Open Loop		80			✻		Ω
Load Capacitance Stability	Gain = +1		1500			✻		pF
Short-Circuit Current		±30	±50		±25	✻		mA
POWER SUPPLY								
Rated Voltage			±15			✻		V_{DC}
Voltage Range, Derated Performance		±5		±18	✻		✻	V_{DC}
Current, Quiescent	I_O = 0mADC		3	4		✻	✻	mA
Over Specified Temperature			3.5	4.5		✻	✻	mA
TEMPERATURE RANGE								
Specification	Ambient Temperature	–25		+85	✻		✻	°C
Operating:								
P, U Packages		–25		+85	✻		✻	°C
Storage:								
P, U Packages		–40		+125	✻		✻	°C
θ_{JA}		200			✻		°C/W	

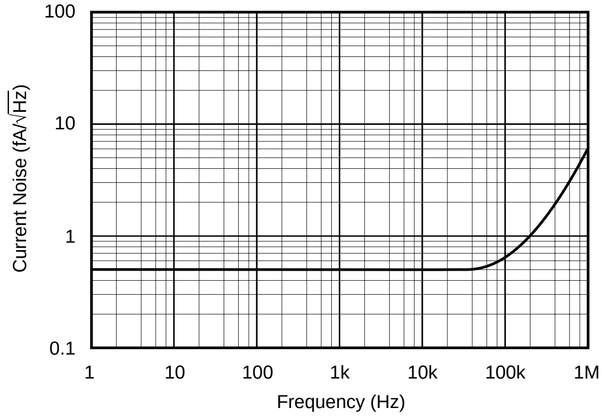
✻ Same specifications as OPA602BP.

NOTE: (1) OPA602AP, AU ensured by design with a 99% confidence level.

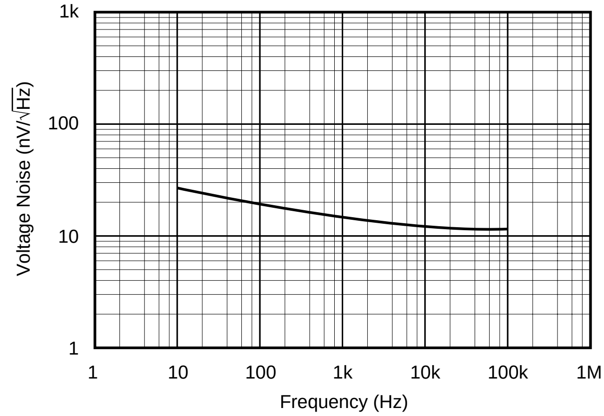
TYPICAL CHARACTERISTICS

At $T_A = +25°C$ and $V_S = \pm15V_{DC}$, unless otherwise noted.

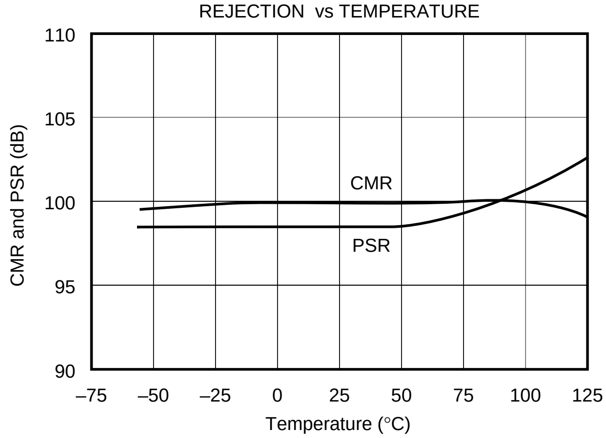
INPUT CURRENT NOISE SPECTRAL DENSITY



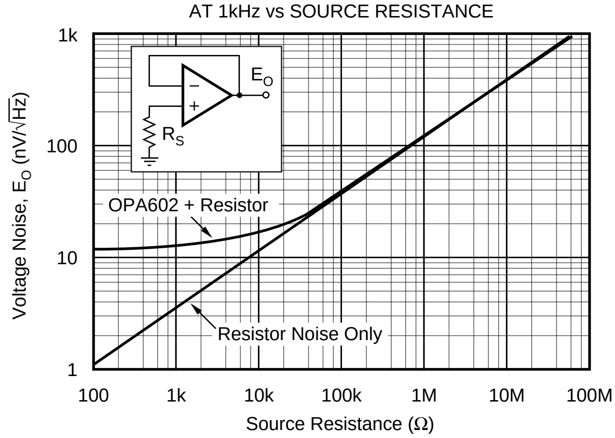
INPUT VOLTAGE NOISE SPECTRAL DENSITY



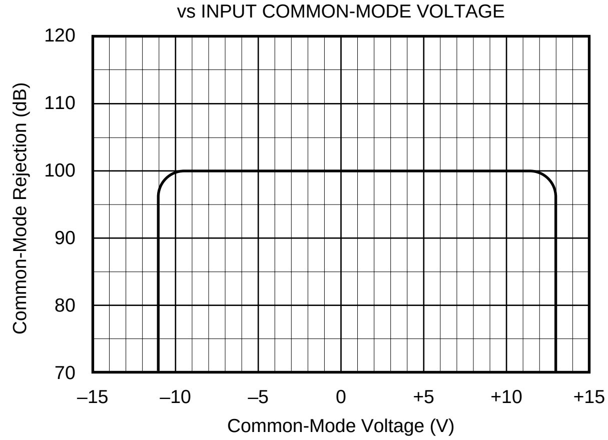
POWER-SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



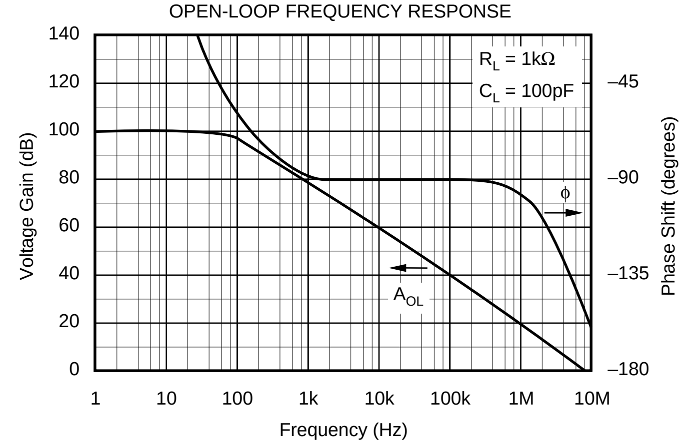
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE

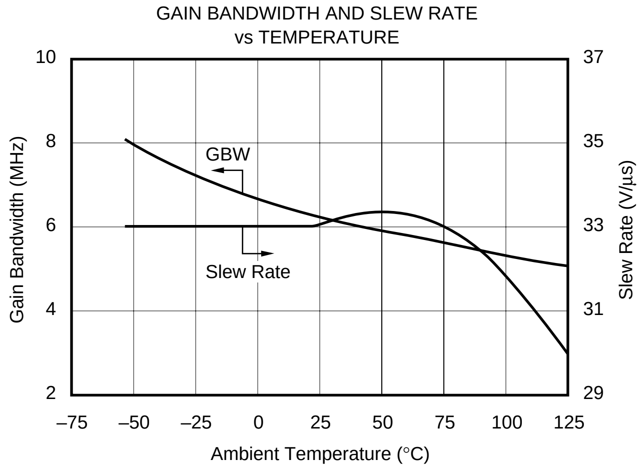


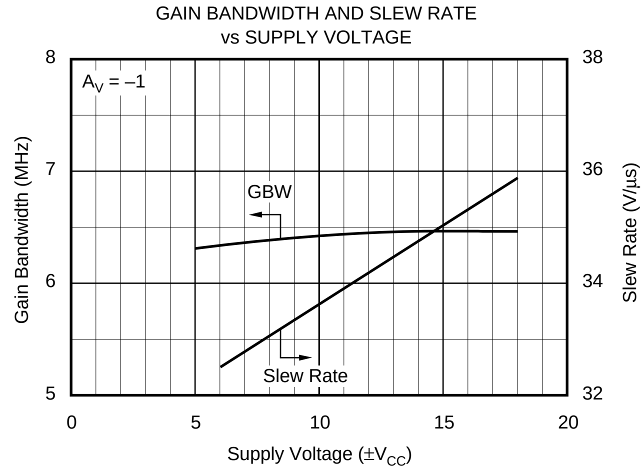
OPEN-LOOP FREQUENCY RESPONSE

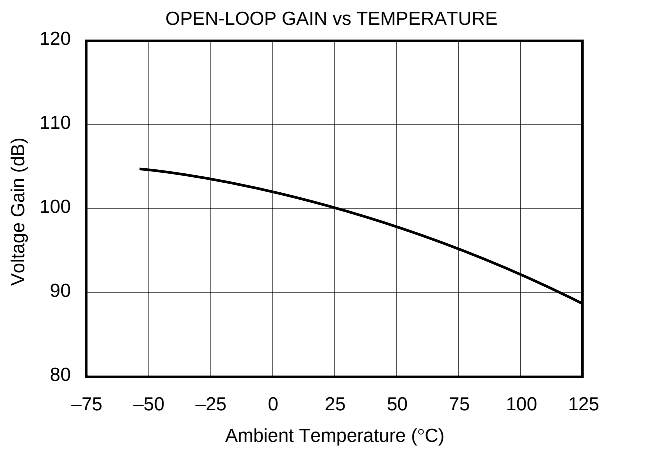


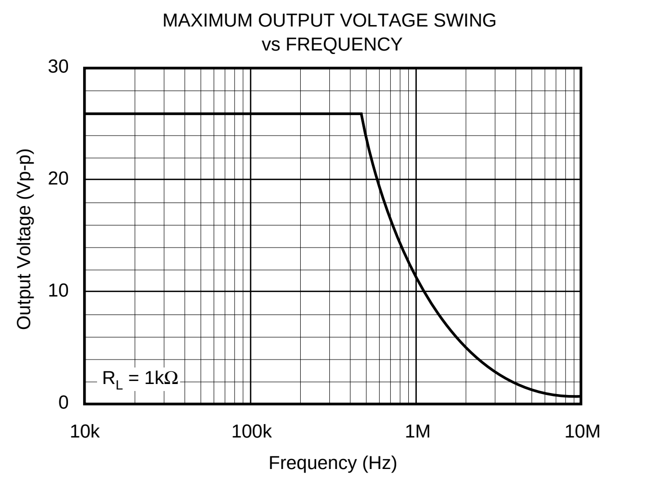
TYPICAL CHARACTERISTICS (Cont.)

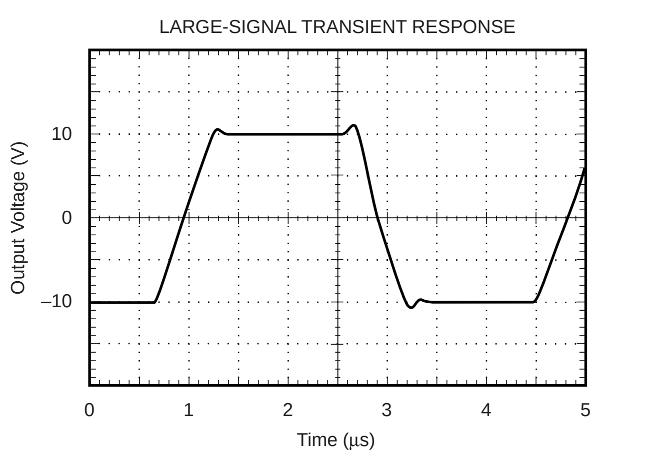
At T_A = +25°C and V_S = ±15V_{DC}, unless otherwise noted.

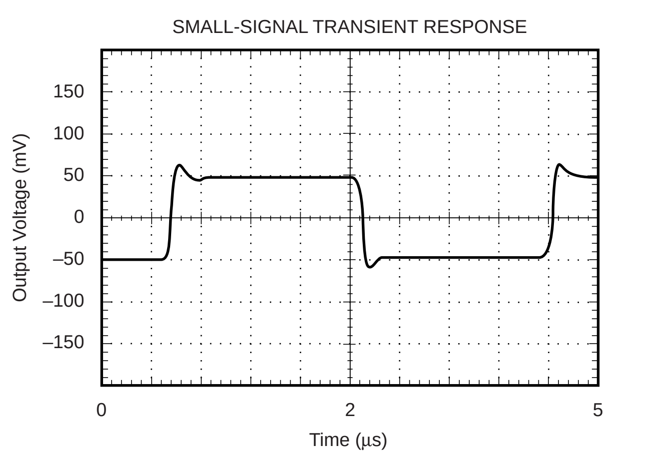








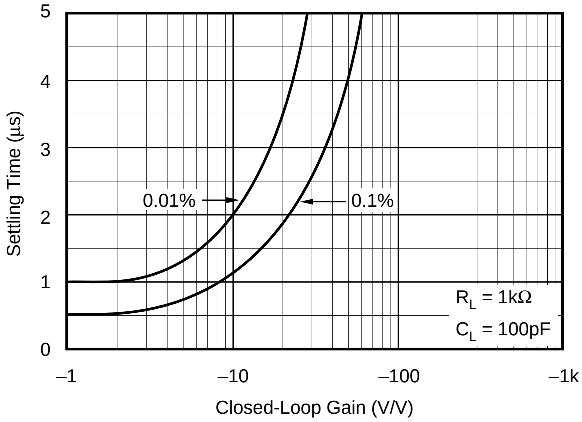




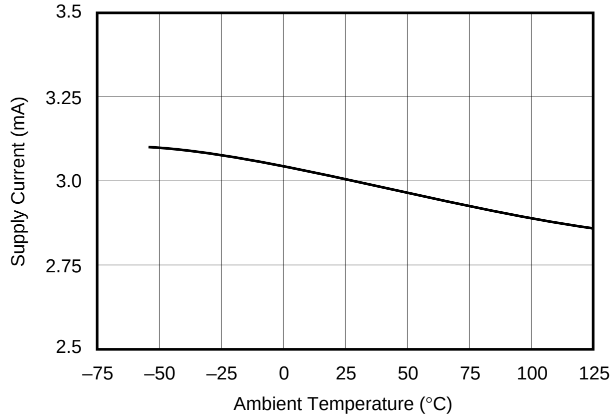
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25°C$ and $V_S = ±15V_{DC}$, unless otherwise noted.

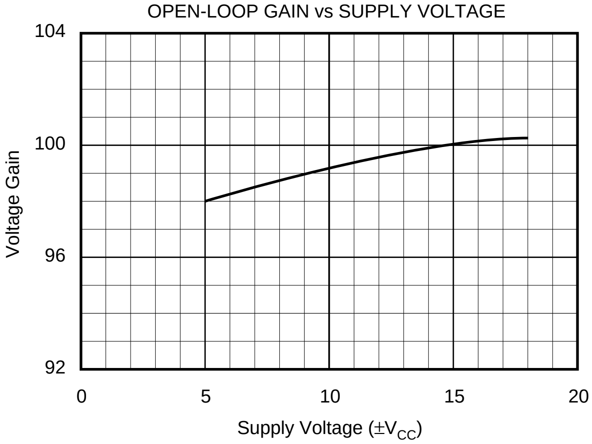
SETTLING TIME vs CLOSED-LOOP GAIN



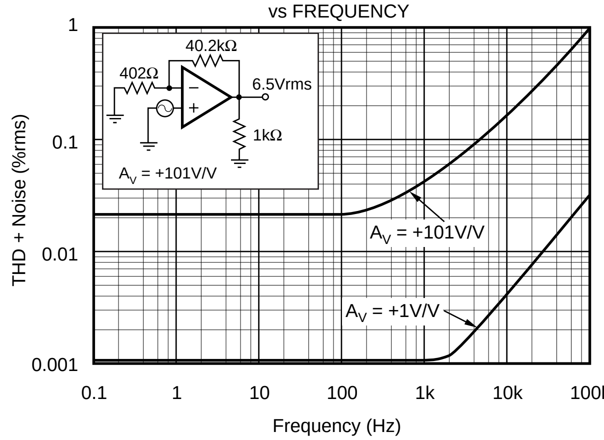
SUPPLY CURRENT vs TEMPERATURE



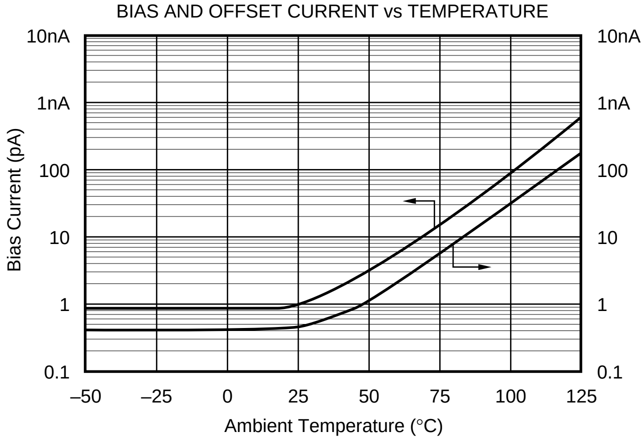
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



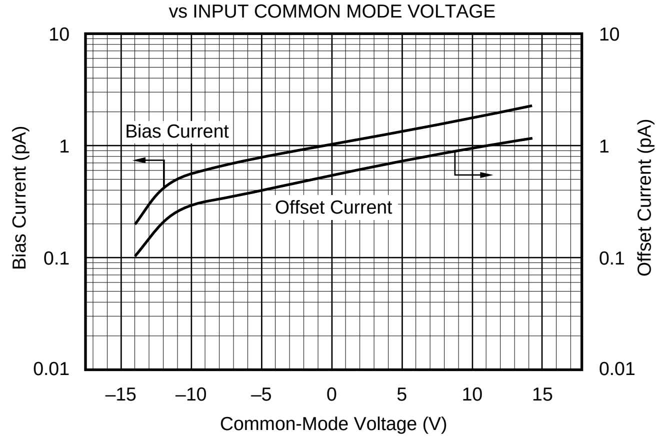
TOTAL HARMONIC DISTORTION vs FREQUENCY



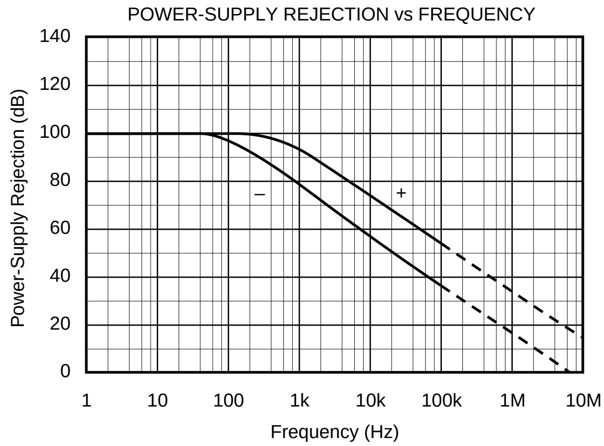
BIAS AND OFFSET CURRENT vs TEMPERATURE

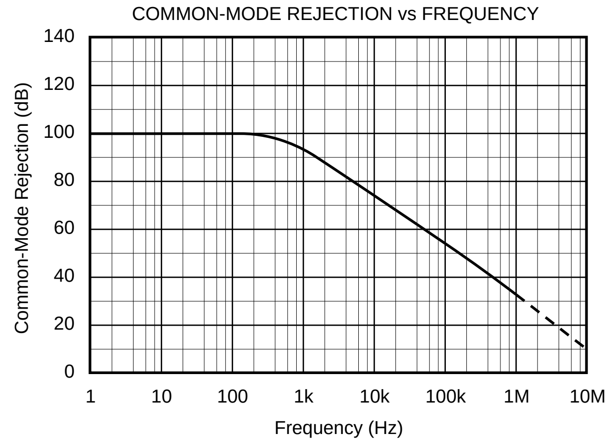


BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



At $T_A = +25°C$ and $V_S = ±15V_{DC}$, unless otherwise noted.





APPLICATIONS INFORMATION

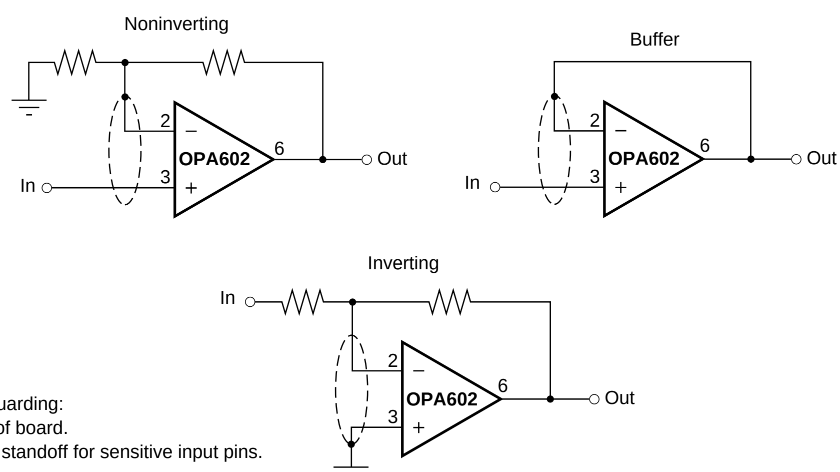
Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high-speed amplifiers. However, as with any high-speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the inverting input pin.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional 1.0µF tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board "guard" pattern, as shown in Figure 1, is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low-impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at +85°C.

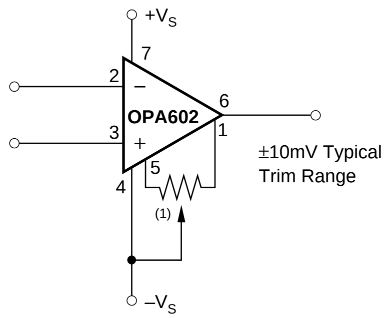


Board Layout for Input Guarding:
Guard top and bottom of board.
Alternate—use Teflon® standoff for sensitive input pins.

Teflon® E.I. Du Pont de Nemours & Co.

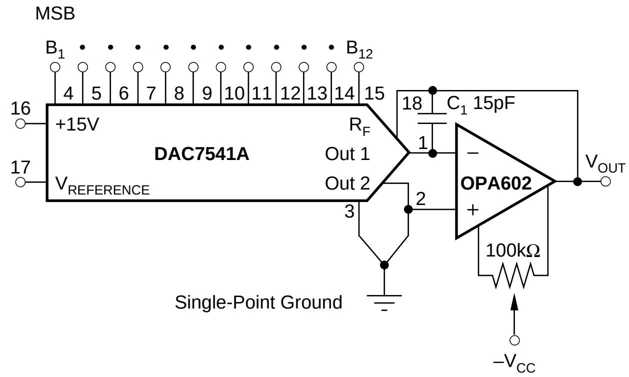
FIGURE 1. Connection of Input Guard.

APPLICATION CIRCUITS



NOTE: (1) 10kΩ to 1MΩ trim potentiometer (100kΩ recommended).

FIGURE 2. Offset Voltage Trim.



$$V_{OUT} = -V_{REF}\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \cdots + \frac{B_{12}}{4096}\right)$$

$$-10V \le V_{REF} \le +10V$$

$$0 \le V_{OUT} \le -\frac{4095}{4096} V_{REF}$$

Where: $B_N = 1$ if the B_N digital input is high.
$B_N = 0$ if the B_N digital input is low.

FIGURE 3. Voltage Output Digital-to-Analog Converter.

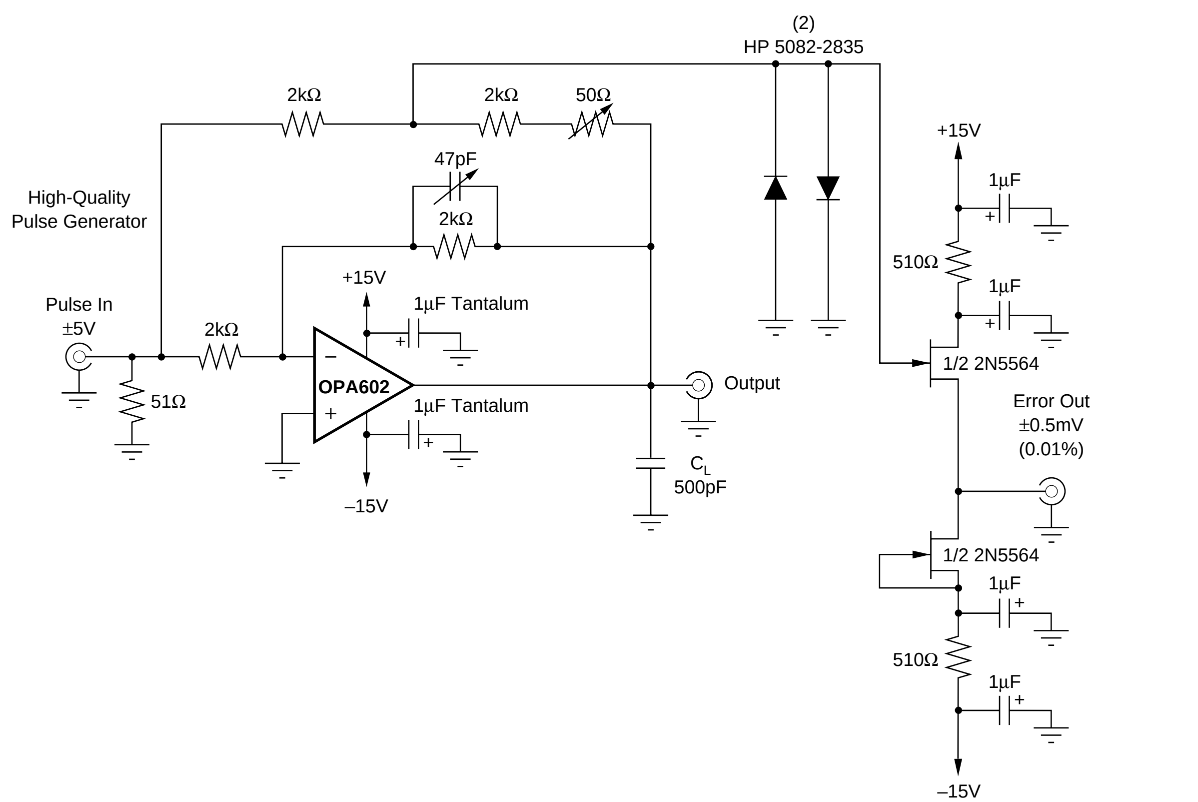
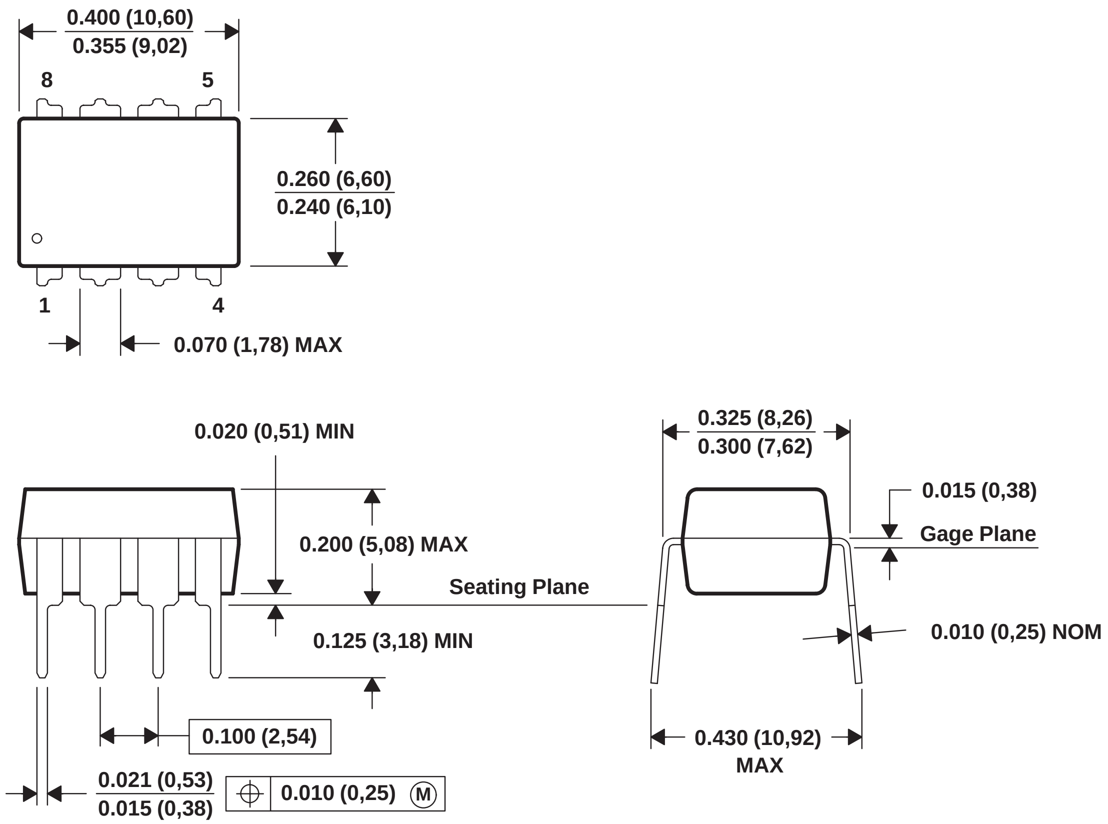


FIGURE 4. Settling Time and Slew Rate Test Circuit.

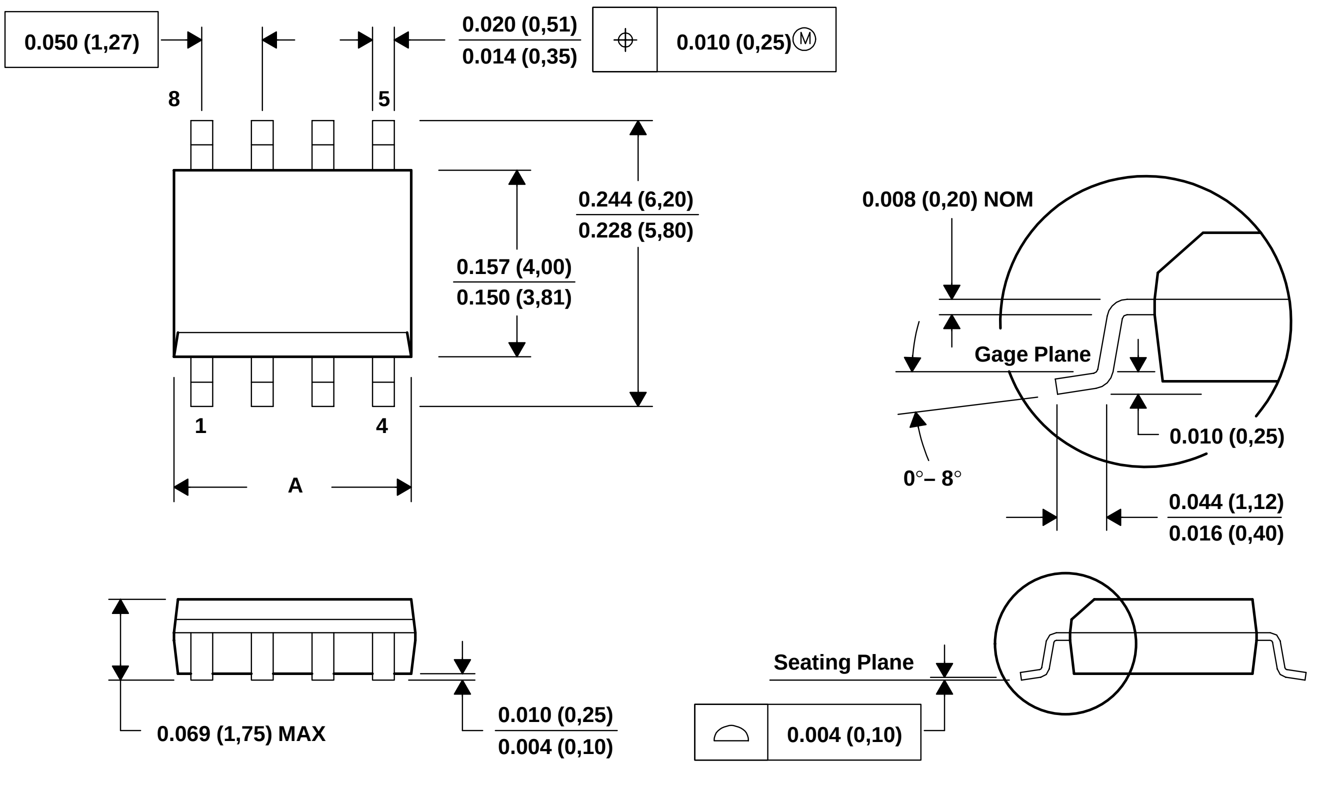
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

IMPORTANT NOTICE

Mailing Address:

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Dallas, Texas 75265