



SBOS155A - AUGUST 1987 - REVISED OCTOBER 2002

High-Speed Precision Difet® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±250µV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING TIME: 1µs to 0.01%
- UNITY-GAIN STABLE

DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high-speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a $1k\Omega$ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

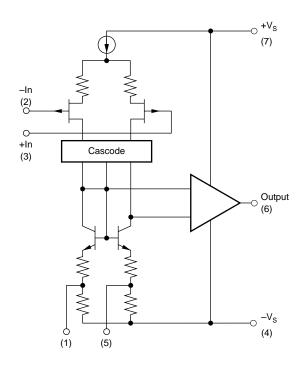
Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.

Difet® Burr-Brown Corp.

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V _{DC}
Internal Power Dissipation (T _J ≤ +175°C)	
Differential Input Voltage	Total V _S
Input Voltage Range	±V _S
Storage Temperature Range	
P and U Packages40	0°C to +125°C
Operating Temperature Range	
P and U Packages2	5°C to + 85°C
Lead Temperature	
U Package, SO (3s)	+260°C
Output Short-Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE/ORDERING INFORMATION



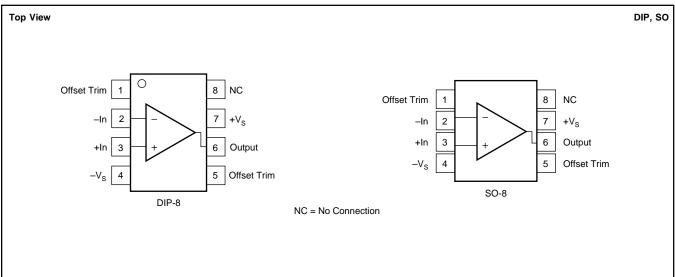
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	OFFSET VOLTAGE MAX (μV) AT 25°C	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA602AP	±2000	DIP-8	Р	–25°C to +85°C	602AP	602AP	Tubes, 50
OPA602BP	±1000	"	"	"	602BP	602BP	Tubes, 50
OPA602AU	±3000	SO-8	D	–25°C to +85°C	602AU	602AU	Tubes, 100

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS

At $V_S = \pm 15 V_{DC}$ and $T_A = +25^{\circ}C$, unless otherwise noted.

INPUT NOISE Voltage: $f_{O} = 10HZ$ $f_{O} = 100HZ$ $f_{O} = 100HZ$ $f_{O} = 100HZ$ $f_{O} = 100HZ$ $f_{O} = 100HZ$ $f_{O} = 100HZ$ $f_{B} = 0.10HZ$ to 100HZ Current: $f_{B} = 0.1HZ$ to 10HZ Current: $f_{B} = 0.1HZ$ to 10HZ $f_{O} = 0.1HZ$ to 200HZOFFSET VOLTAGE Input Offset Voltage: P Package U Package Over Specified Temperature P, U Packages Average Driff(1) $T_{A} =$ $\pm V_{S} =$ BIAS CURRENT Input Bias Current Over Specified TemperatureV V Over Specified TemperatureOFFSET CURRENT Input Offset Current Over Specified TemperatureV V Over Specified TemperatureOFFSET CURRENT Input Offset Current Over Specified TemperatureV V Over Specified TemperatureOFFSET CURRENT Input Offset Current Over Specified TemperatureV V Over Specified TemperatureOPEN-LOOP GAIN, DC Open-Loop Voltage GainO OPEN-LOOP GAIN, DC OPEN-LOOP Kain, DC Open-Loop Voltage GainO OV V O = ± Settling Time:	T _{MIN} to T _{MAX} = 12V to 18V $_{CM} = 0V_{DC}$ $_{CM} = 0V_{DC}$	MIN 80	TYP 23 19 13 12 1.4 0.95 12 0.6 0.5 ±0.75 ±3 100 ±1 ±20 0.5 20	MAX 1 ±1.5 ±5 ±2 ±200	MIN 70	TYP * * * * * * * * * * * * * * * * * * *	MAX 2 3 ±15 ±10	UNITS nV/√Hz nV/√Hz nV/√Hz nV/√Hz μVrms μVp-p fAp-p fA/√Hz mV mV mV mV pA
Voltage: $f_{O} = 10Hz$ $f_{O} = 10Hz$ $f_{O} = 10Hz$ $f_{O} = 10Hz$ $f_{O} = 10Hz$ $f_{O} = 10Hz$ $f_{B} = 0.1Hz$ to 10Hz $f_{B} = 0.1Hz$ to 10Hz $f_{B} = 0.1Hz$ to 10Hz $f_{O} = 0.1Hz$ to 20KHzOFFSET VOLTAGE Input Offset Voltage: P Package U Package Over Specified Temperature P, U Packages Average Drift ⁽¹⁾ Average Drift ⁽¹⁾ TA = Supply RejectionBIAS CURRENT Input Bias Current OVer Specified TemperatureV V V OOFFSET CURRENT Input Offset Current Over Specified TemperatureV V V OOUT IMPEDANCE Differential Common-ModeImput Range Common-Mode NodeINPUT VOLTAGE RANGE Common-Mode RejectionO V V V OFREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Settling Time:G C C D C O C D C O C Slew Rate Settling Time:	= 12V to 18V $_{CM} = 0V_{DC}$	80	$ \begin{array}{c} 19\\ 13\\ 12\\ 1.4\\ 0.95\\ 12\\ 0.6\\ \end{array} $ $ \begin{array}{c} 0.5\\ \pm 0.75\\ \pm 3\\ 100\\ \end{array} $ $ \begin{array}{c} \pm 1\\ \pm 20\\ \end{array} $ $ \begin{array}{c} 0.5\\ \end{array} $	±1.5 ±5 ±2	70	* * * * 1 1 ±1.5 * *	3 ±15	nV/\ <u>Hz</u> nV/\ <u>Hz</u> nV/\ <u>Hz</u> μVms μVp-p fAp-p fA/\ <u>Hz</u> mV mV mV μV/°C dB
$f_o = 10Hz$ $f_o = 100Hz$ $f_o = 100Hz$ $f_o = 10Hz$ $f_o = 10Hz$ $10Hz$ $f_o = 10Hz$ $10Hz$ $f_B = 0.1Hz$ $10Hz$ Current: $f_B = 0.1Hz$ $f_B = 0.1Hz$ $10Hz$ $f_o = 0.1Hz$ $10Hz$ $f_o = 0.1Hz$ $20KHz$ OFFSET VOLTAGEInput Offset Voltage:P PackageU PackageU Package $\pm V_S$ Over Specified Temperature $\pm V_S$ P Dackage $\pm V_S$ Over Specified Temperature ∇V_0 Differential $Common-Mode$ Common-Mode M INPUT VOLTAGE RANGE $\nabla Pen-Loop$ GAIN, DCOpen-Loop Voltage Gain M FREQUENCY RESPONSE $Gain Bandwidth$ Gain Bandwidth GG Slew Rate $\nabla_0 = \pm$ Settling Time: $\nabla_0 = \pm$	= 12V to 18V $_{CM} = 0V_{DC}$	80	$ \begin{array}{c} 19\\ 13\\ 12\\ 1.4\\ 0.95\\ 12\\ 0.6\\ \end{array} $ $ \begin{array}{c} 0.5\\ \pm 0.75\\ \pm 3\\ 100\\ \end{array} $ $ \begin{array}{c} \pm 1\\ \pm 20\\ \end{array} $ $ \begin{array}{c} 0.5\\ \end{array} $	±1.5 ±5 ±2	70	* * * * 1 1 ±1.5 * *	3 ±15	nV/\ <u>Hz</u> nV/\ <u>Hz</u> nV/\ <u>Hz</u> μVms μVp-p fAp-p fA/\ <u>Hz</u> mV mV mV μV/°C dB
$f_o = 100Hz$ $f_o = 10Hz$ $f_o = 10Hz$ $f_o = 10Hz$ $f_o = 10Hz$ $t_o = 10Hz$ $f_B = 0.1Hz$ $t_o = 10Hz$ Current: $f_B = 0.1Hz$ $f_B = 0.1Hz$ $t_o = 10Hz$ $f_o = 0.1Hz$ $t_o = 20Hz$ OFFSET VOLTAGEInput Offset Voltage:P PackageU PackageOver Specified Temperature $+V_S$ P, U Packages $\pm V_S$ Average Drift ⁽¹⁾ $T_A =$ Supply Rejection $\pm V_S$ INPUT Bias CurrentOver Specified TemperatureOver Specified Temperature V_0 Over Specified Temperature V_0 Over Specified Temperature V_0 Input Offset Current V_0 Over Specified Temperature V_0 Differential $Common-Mode$ Common-Mode $Mneg$ Open-Loop Voltage Gain M FREQUENCY RESPONSE $Gain Bandwidth$ Gain Bandwidth G Full-Power Response $20Vp$ Slew Rate $V_0 = \pm$ Settling Time: $V_0 = \pm$	= 12V to 18V $_{CM} = 0V_{DC}$	80	$ \begin{array}{c} 19\\ 13\\ 12\\ 1.4\\ 0.95\\ 12\\ 0.6\\ \end{array} $ $ \begin{array}{c} 0.5\\ \pm 0.75\\ \pm 3\\ 100\\ \end{array} $ $ \begin{array}{c} \pm 1\\ \pm 20\\ \end{array} $ $ \begin{array}{c} 0.5\\ \end{array} $	±1.5 ±5 ±2	70	* * * * 1 1 ±1.5 * *	3 ±15	nV/\ <u>Hz</u> nV/\ <u>Hz</u> nV/\ <u>Hz</u> μVms μVp-p fAp-p fA/\ <u>Hz</u> mV mV mV μV/°C dB
$f_{O} = 1$ kHz $f_{O} = 10$ kHz $f_{O} = 10$ kHz $f_{B} = 10$ Hz to 10kHz $f_{B} = 0.1$ Hz to 10HzCurrent: $f_{B} = 0.1$ Hz to 10Hz $f_{O} = 0.1$ Hz to 20kHzOFFSET VOLTAGEInput Offset Voltage:P PackageU PackageOver Specified Temperature P, U PackagesAverage Drift ⁽¹⁾ $T_{A} =$ Supply Rejection $\pm V_{S} =$ BIAS CURRENTInput Bias Current V_{O} Over Specified Temperature V_{O} OFFSET CURRENTInput Offset Current V_{O} Over Specified Temperature V_{O} INPUT IMPEDANCEDifferentialCommon-ModeCommon-ModeInput Voltage RangeCommon-Mode Rejection V_{O} PREQUENCY RESPONSEGain BandwidthGFREQUENCY RESPONSE20V/PSlew Rate $V_{O} = \pm$ Settling Time: $V_{O} = \pm$	= 12V to 18V $_{CM} = 0V_{DC}$	80	$ \begin{array}{c} 13\\12\\1.4\\0.95\\12\\0.6\\\\ \end{array} $ $ \begin{array}{c} 0.5\\\pm 0.75\\\pm 3\\100\\\\\\\pm 1\\\pm 20\\\\0.5\\\end{array} $	±1.5 ±5 ±2	70	* * * * 1 1 ±1.5 * *	3 ±15	nV/\ <u>Hz</u> nV/\ <u>Hz</u> μVms μVp-p fAp- <u>p</u> fA/\/ <u>Hz</u> mV mV mV μV/°C dB
$f_o = 10kHz$ $f_B = 10Hz$ to $10kHz$ $f_B = 10Hz$ to $10Hz$ $f_B = 0.1Hz$ to $10Hz$ $f_B = 0.1Hz$ to $10Hz$ $Current:$ $f_0 = 0.1Hz$ to $20kHz$ OFFSET VOLTAGEInput Offset Voltage: P Package U PackageOVer Specified Temperature P, U Packages $T_A =$ Supply Rejection $\pm V_S$:BIAS CURRENTInput Bias Current Over Specified TemperatureOFFSET CURRENT Input Offset Current Over Specified Temperature V_0 OFFSET CURRENT Input Offset Current Over Specified Temperature V_0 INPUT IMPEDANCE Differential Common-ModeINPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode RejectionOFEN-LOOP GAIN, DC Open-Loop Voltage GainOFREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Settling Time: $20Vp$	= 12V to 18V $_{CM} = 0V_{DC}$	80	$ \begin{array}{c} 12\\ 1.4\\ 0.95\\ 12\\ 0.6\\ \end{array} $ $ \begin{array}{c} 0.5\\ \pm 0.75\\ \pm 3\\ 100\\ \end{array} $ $ \begin{array}{c} \pm 1\\ \pm 20\\ \end{array} $ $ \begin{array}{c} 0.5\\ \end{array} $	±1.5 ±5 ±2	70	* * * 1 1 ±1.5 * *	3 ±15	nV/√Hz μVrms μVp-p fAp <u>-p</u> fA/√Hz mV mV mV μV/°C dB
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$f_B = 0.1Hz$ to 10HzCurrent: $f_B = 0.1Hz$ to 10Hz $f_O = 0.1Hz$ to 20kHzOFFSET VOLTAGEInput Offset Voltage:P PackageU PackageOver Specified TemperatureP, U PackagesAverage Drift ⁽¹⁾ TA =Supply Rejection $\pm V_S$:BIAS CURRENTInput Bias CurrentOver Specified TemperatureOFFSET CURRENTInput Offset CurrentOver Specified TemperatureOVer Specified TemperatureDifferentialCommon-ModeINPUT VOLTAGE RANGECommon-Mode Input RangeCommon-Mode RejectionOPEN-LOOP GAIN, DCOpen-Loop Voltage GainFREQUENCY RESPONSEGain BandwidthGain BandwidthGuest RateVo = ±Settling Time:	= 12V to 18V $_{CM} = 0V_{DC}$	80	$\begin{array}{c} 0.95 \\ 12 \\ 0.6 \\ \end{array}$ $\begin{array}{c} 0.5 \\ \pm 0.75 \\ \pm 3 \\ 100 \\ \end{array}$ $\begin{array}{c} \pm 1 \\ \pm 20 \\ \end{array}$ $0.5 \\ \end{array}$	±1.5 ±5 ±2	70	* * 1 1 ±1.5 *	3 ±15	μVp-p fAp <u>-p</u> fA/√Hz mV mV mV μV/°C dB
Current: $f_B = 0.1Hz$ to 10Hz $f_O = 0.1Hz$ to 20kHz OFFSET VOLTAGE Input Offset Voltage: P Package U Package Over Specified Temperature P, U Packages Average Drift ⁽¹⁾ TA = Supply Rejection HAS CURRENT Input Bias Current Over Specified Temperature OFFSET CURRENT Input Offset Current Over Specified Temperature OVer Specified Temperature Input Offset Current Over Specified Temperature INPUT IMPEDANCE Differential Common-Mode INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection OPEN-LOOP GAIN, DC Open-Loop Voltage Gain FREQUENCY RESPONSE Gain Bandwidth Full-Power Response Settling Time:	= 12V to 18V $_{CM} = 0V_{DC}$	80	$ \begin{array}{c} 12\\ 0.6\\ \\ 0.5\\ \pm 0.75\\ \pm 3\\ 100\\ \\ \pm 1\\ \pm 20\\ \\ 0.5\\ \end{array} $	±1.5 ±5 ±2	70	* 1 1 ±1.5 *	3 ±15	fAp <u>-p</u> fA/√Hz mV mV μV/°C dB
$f_B = 0.1Hz$ to 10Hz $f_O = 0.1Hz$ to 20kHz OFFSET VOLTAGE Input Offset Voltage: P Package U Package U Package Over Specified Temperature P, U Packages Average Drift ⁽¹⁾ $T_A =$ Supply Rejection $\pm V_S$ st BIAS CURRENT Input Bias Current Input Offset Current Votometric Over Specified Temperature Votometric OFFSET CURRENT Input Offset Current Input IMPEDANCE Differential Common-Mode Common-Mode INPUT VOLTAGE RANGE Common-Mode Rejection OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Gain Bandwidth G FREQUENCY RESPONSE Gain Bandwidth Gain Bandwidth G Slew Rate Vo = ± Settling Time: Vo = ±	= 12V to 18V $_{CM} = 0V_{DC}$	80	0.6 0.5 ±0.75 ±3 100 ±1 ±20 0.5	±1.5 ±5 ±2	70	* 1 ±1.5 *	3 ±15	fA/√Hz mV mV μV/°C dB
$f_0 = 0.1Hz$ to 20kHzOFFSET VOLTAGE Input Offset Voltage: P Package U Package Over Specified Temperature P, U Packages Average Drift ⁽¹⁾ $T_A =$ $\pm V_S$ =Supply Rejection $\pm V_S$ =BIAS CURRENT Input Bias Current Over Specified TemperatureV V OVER OVER Specified TemperatureOFFSET CURRENT Input Offset Current Over Specified TemperatureV V OVER OVER Specified TemperatureINPUT IMPEDANCE Differential Common-ModeInput Sange Common-ModeINPUT VOLTAGE RANGE Common-Mode RejectionO V V V OPEN-LOOP GAIN, DC Open-Loop Voltage GainFREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Settling Time:Q V O = ±	= 12V to 18V $_{CM} = 0V_{DC}$	80	0.6 0.5 ±0.75 ±3 100 ±1 ±20 0.5	±1.5 ±5 ±2	70	* 1 ±1.5 *	3 ±15	fA/√Hz mV mV μV/°C dB
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U PackageOver Specified TemperatureP, U PackagesAverage Drift(1)Supply Rejection $\pm V_S$ =BIAS CURRENTInput Bias CurrentOver Specified TemperatureOFFSET CURRENTInput Offset CurrentOver Specified TemperatureOver Specified TemperatureINPUT IMPEDANCEDifferentialCommon-ModeINPUT VOLTAGE RANGECommon-Mode Input RangeCommon-Mode RejectionOPEN-LOOP GAIN, DCOpen-Loop Voltage GainFREQUENCY RESPONSEGain BandwidthGull-Power ResponseSlew RateVo = ±Settling Time:	= 12V to 18V $_{CM} = 0V_{DC}$	80	±0.75 ±3 100 ±1 ±20 0.5	±1.5 ±5 ±2	70	1 ±1.5 * *	3 ±15	mV mV μV/°C dB
Over Specified Temperature P, U Packages Average Drift(1) $T_A =$ $\pm V_S =$ Supply Rejection $\pm V_S =$ BIAS CURRENT Input Bias Current Over Specified TemperatureV V Over Specified TemperatureOFFSET CURRENT Input Offset Current Over Specified TemperatureV V V Over Specified TemperatureINPUT IMPEDANCE Differential Common-ModeV V Over Specified TemperatureINPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode RejectionV V V V V V OPEN-LOOP GAIN, DC Open-Loop Voltage GainFREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Settling Time:20Vp V V O = ±	= 12V to 18V $_{CM} = 0V_{DC}$	80	±3 100 ±1 ±20 0.5	±5 	70	±1.5 * *	±15	mV µV/°C dB
P, U Packages $T_A =$ Average Drift ⁽¹⁾ $T_A =$ Supply Rejection $\pm V_S$ BIAS CURRENT V Input Bias Current V Over Specified Temperature V OFFSET CURRENT V Input Offset Current V Over Specified Temperature V Differential Common-Mode Common-Mode InPUT VOLTAGE RANGE Common-Mode Input Range V Common-Mode Rejection V OPEN-LOOP GAIN, DC Open-Loop Voltage Gain FREQUENCY RESPONSE Gain Bandwidth Gain Bandwidth G Slew Rate V _O = ± Settling Time: V	= 12V to 18V $_{CM} = 0V_{DC}$	80	±3 100 ±1 ±20 0.5	±5 	70	* *		μV/°C dB
Average Drift ⁽¹⁾ $T_A =$ Supply Rejection $\pm V_S =$ BIAS CURRENT Input Bias Current Input Bias Current V_G OVer Specified Temperature V_G OFFSET CURRENT Input Offset Current Input Offset Current V_G Over Specified Temperature V_G INPUT IMPEDANCE Differential Common-Mode Common-Mode INPUT VOLTAGE RANGE Open-Loop GAIN, DC Open-Loop Voltage Gain Input FREQUENCY RESPONSE Gain Bandwidth G Full-Power Response 20Vp Slew Rate $V_O = \pm$	= 12V to 18V $_{CM} = 0V_{DC}$	80	±3 100 ±1 ±20 0.5	±5 	70	* *		μV/°C dB
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Common-Mode INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection OPEN-LOOP GAIN, DC Open-Loop Voltage Gain FREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Vo = ±								
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection OPEN-LOOP GAIN, DC Open-Loop Voltage Gain FREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Settling Time:		1	10 ¹³ 1			*		Ω pF
Common-Mode Input Range V Common-Mode Rejection V OPEN-LOOP GAIN, DC V Open-Loop Voltage Gain I FREQUENCY RESPONSE G Gain Bandwidth G Full-Power Response 20Vp Slew Rate Vo = ± Settling Time: V			10 ¹⁴ 3			*		Ω pF
Common-Mode Rejection N OPEN-LOOP GAIN, DC Open-Loop Voltage Gain FREQUENCY RESPONSE Gain Bandwidth Gain Bandwidth Gain Sandwidth Full-Power Response 20Vp Slew Rate Vo = ± Settling Time: Vo = ±								
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain FREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Vo = ± Settling Time:		±10.2	+13, -11		*	*		V
Open-Loop Voltage Gain I FREQUENCY RESPONSE G Gain Bandwidth G Full-Power Response 20Vp Slew Rate Vo = ± Settling Time: Vo = ±	$V_{IN} = \pm 10 V_{DC}$	88	100		75	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full-Power Response Slew Rate Vo = ± Settling Time:								
	$R_L \ge 1k\Omega$	88	100		75	*		dB
Full-Power Response 20Vp Slew Rate V _O = ± Settling Time:								
Slew Rate V _O = ± Settling Time:	iain = 100	4	6.5		3.5	*		MHz
Settling Time:	p-p, $R_L = 1k\Omega$		570			*		kHz
	10V, $R_L = 1k\Omega$	24	35		20	*		V/µs
								1
	= –1, R _L = 1kΩ		0.6			*		μs
0.01% C _L = 50	00pF, 10V Step		1.0					μs
RATED OUTPUT								
Voltage Output	$R_{L} = 1k\Omega$	±11.5	+12.9, -13.8		±11	*		V
Current Output	101/	±15	-13.8 ±20		*	N.		
	_o = ±10V _{DC} z, Open Loop	±15			*	*		mA
			80			*		Ω
· · · · ·	Gain = +1	100	1500		105	*		pF
Short-Circuit Current		±30	±50		±25	*		mA
POWER SUPPLY								V
Rated Voltage			±15			*		V _{DC}
Voltage Range, Derated Performance	0	±5		±18	*		*	V _{DC}
Current, Quiescent I _O Over Specified Temperature	= 0mADC	1	3 3.5	4 4.5		* *	* *	mA mA
			0.0	т.J			~	
TEMPERATURE RANGE Specification Ambien		-25		+85	*		*	°C
Operating:	t Temperature	-20		100	~		r i	Ŭ
P, U Packages	nt Temperature	1			*		*	°C
Storage:	nt Temperature	_25		+85 1	~			
P, U Packages	nt Temperature	-25		+85				1
θ_{JA}	nt Temperature	-25 -40		+85 +125	*		*	°C

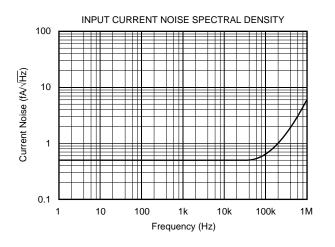
* Same specifications as OPA602BP.

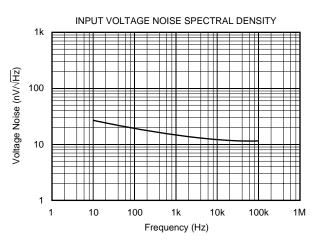
NOTE: (1) OPA602AP, AU ensured by design with a 99% confidence level.



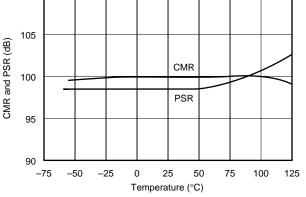
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = $\pm 15 V_{DC},$ unless otherwise noted.





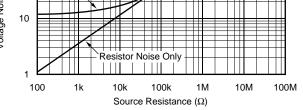
POWER-SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE

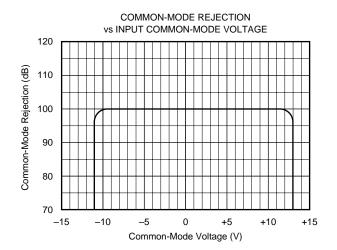


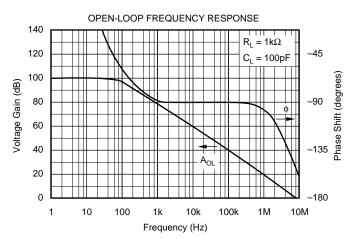
110

AT 1kHz vs SOURCE RESISTANCE

TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY



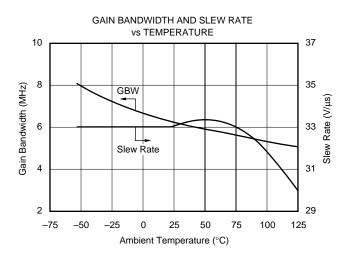


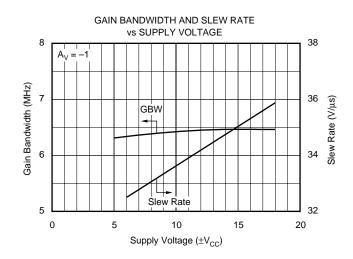


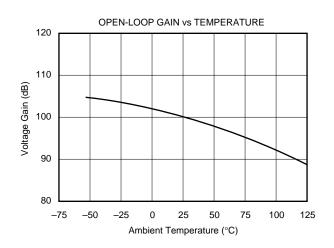


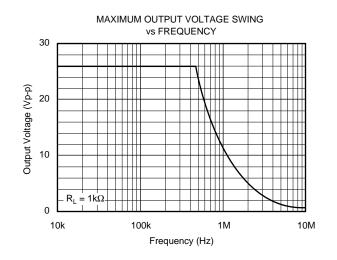
TYPICAL CHARACTERISTICS (Cont.)

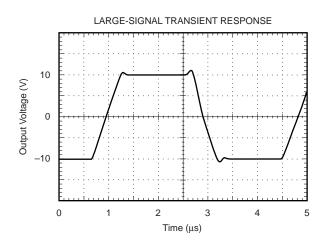
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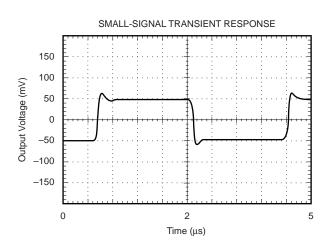










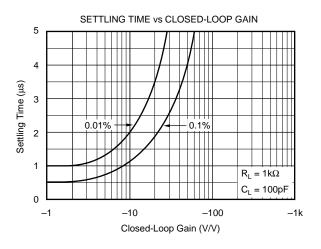


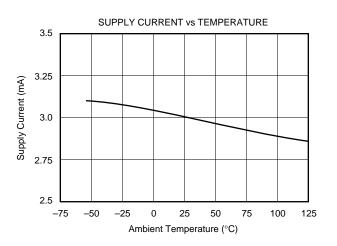


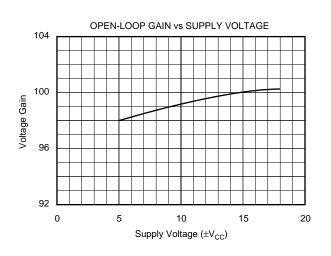


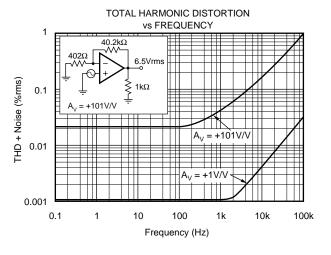
TYPICAL CHARACTERISTICS (Cont.)

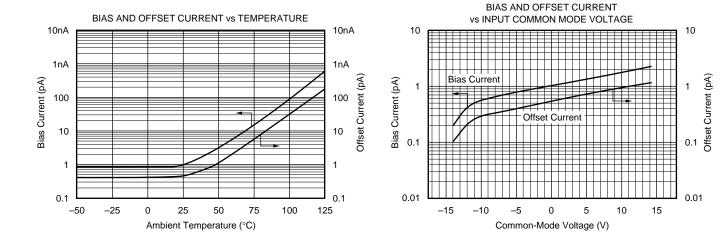
At T_A = +25°C and V_S = ±15 V_{DC} , unless otherwise noted.









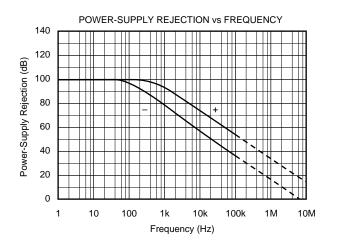


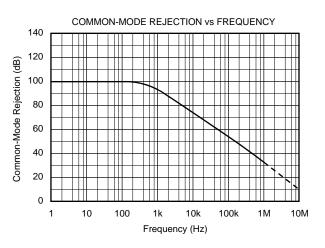




TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C and V_S = $\pm 15 V_{DC},$ unless otherwise noted.





APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high-speed amplifiers. However, as with any high-speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance especially at the inverting input pin.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases $0.1\mu F$ ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional $1.0\mu F$ tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board "guard" pattern, as shown in Figure 1, is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low-impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at +85°C.

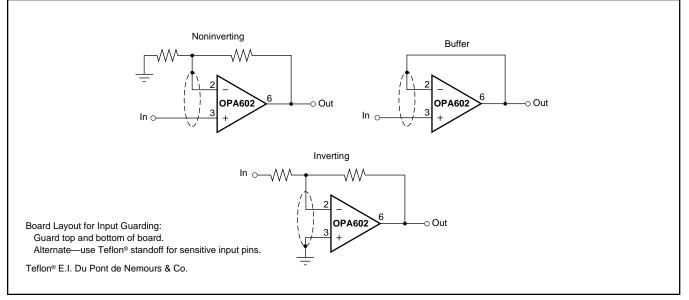
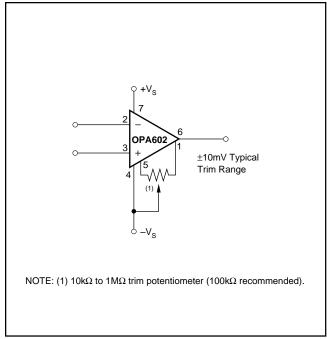


FIGURE 1. Connection of Input Guard.





APPLICATION CIRCUITS



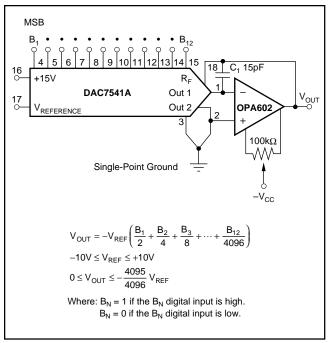


FIGURE 2. Offset Voltage Trim.

FIGURE 3. Voltage Output Digital-to-Analog Converter.

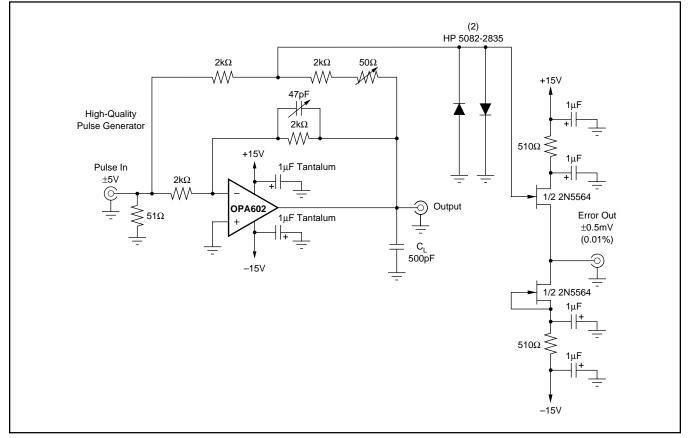
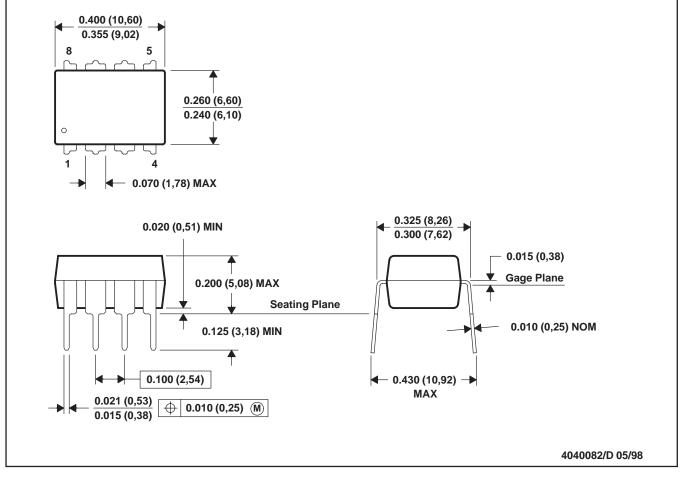


FIGURE 4. Settling Time and Slew Rate Test Circuit.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

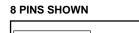


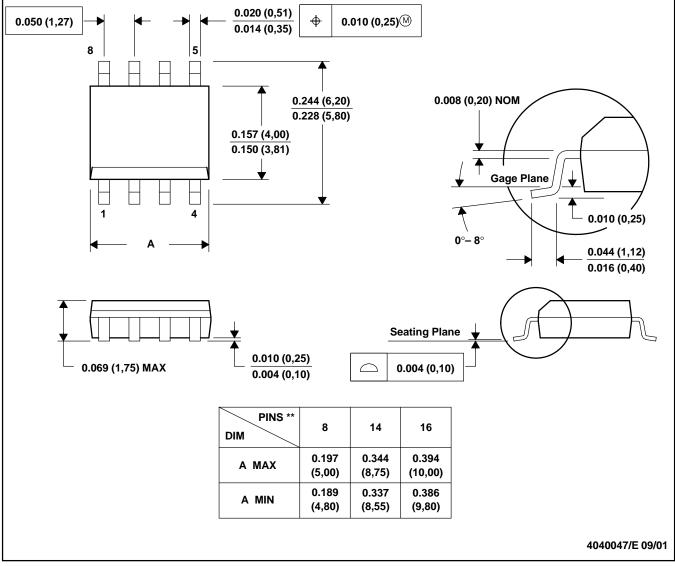
- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001



D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE





- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012



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