ORCA® ORSO82G5 1.0—1.35/2.0—2.7 Gbits/s SONET Octal Backplane Interface FPSC

Introduction

Agere Systems Inc. has developed a next-generation FPSC intended for high-speed serial SONET backplane data transmission. Built on the Series 4 reconfigurable embedded system-on-chips (SoC) architecture, the ORSO82G5 is made up of backplane transceivers containing eight channels, each operating at up to 2.7 Gbits/s data rate, with a full-duplex synchronous interface with built-in clock and data recovery (CDR), along with up to 400k usable FPGA system gates. The CDR circuitry is a macrocell available from Agere's Smart Silicon macro library, and has already been implemented in numerous applications including ASICs, standard products, and FPSCs to create interfaces for SONET/SDH, STS-48/STM-16, and STS-192/STM-64 applications. Additionally the ORSO82G5 also includes optional cell creation and extraction capabilities across either all eight links or four independent pairs of links.

With the addition of protocol and access logic such as protocol-independent framers, asynchronous transfer mode (ATM) framers, packet-over-SONET (POS) interfaces, and framers for HDLC for Internet protocol (IP), designers can build a configurable interface retaining proven backplane driver/receiver technology. Designers can also use the device to drive high-speed data transfer across SONET/SDH based buses. The ORSO82G5 can also be used to provide a full 10 Gbits/s backplane data connection with protection between a line card/redundant line card and switch fabric/redundant switch fabric. The FPGA portion can be used for implementing 2.5G or 10G CSIX switch fabric interfaces or interfaces to Agere's PI family of switch fabric devices.

The ORSO82G5 offers a clockless high-speed interface for interdevice communication on a board or across a backplane. The built-in clock recovery of the ORSO82G5 allows for higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will benefit from the backplane transceiver as a network termination device. The ORSO82G5 supports SONET data scrambling/descrambling, streamlined SONET framing which is optional, transport overhead handling, cell creation and extraction, idle cell insertion/deletion plus the programmable logic to terminate the network into proprietary systems. For non-SONET applications, all SONET functionality is hidden from the user and no prior networking knowledge is required.

Table 1. ORCA ORSO82G5 Family—Available FPGA Logic

Device	PFU Rows	PFU Columns	Total PFUs	User I/O	LUTs	EBR Blocks	EBR Bits (k)	Usable† Gates (k)
ORSO82G5	36	36	1296	372/432*	10,368	12	111	380—800

* 372 user I/Os out of a total of 432 user I/Os are bonded in the 680 PBGAM package.

† The embedded core and interface are not included in the above gate counts. The usable gate counts range from a logic-only gate count to a gate count assuming that 20% of the PFUs/SLICs are being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit, plus each block has an additional 25k gates. 7k gates are used for each PLL and 50k gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate count calculations.

Embedded Function Features

- High-speed SERDES programmable serial data rates of 1.0 Gbits/s to 2.7 Gbits/s.
- Asynchronous operation per receive channel (separate PLL per channel).
- Transmit pre-emphasis (programmable) for improved receive data eye opening.
- Receiver energy detector to determine if a link is active.
- Provides a 10 Gbits/s backplane interface to switch fabric with protection. Also supports port cards at rates between 1.0 Gbits/s and 2.7 Gbits/s.
- Allows wide range of applications for SONET network termination, as well as generic data moving for high-speed backplane data transfer.
- No knowledge of SONET/SDH needed in generic applications. Simply supply data (125 MHz—168.75 MHz clock) and optionally a frame pulse.
- High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- Eight-channel HSI function provides 2.7 Gbits/s serial user data interface per channel for a total chip bandwidth of >20 Gbits/s (full duplex).
- SERDES has low-power CML buffers. Support for 1.5 V/1.8 V I/Os and interfaces to LVDS and LVPECL I/Os through external resister networks.
- Powerdown option of SERDES HSI receiver/transmitter on a per-channel basis.
- Ability to mix half-rate and full-rate between the channels with the same reference clock.
- Ability to configure each quad SERDES block independently with its own reference clock.
- STS-48 framing in SONET mode. OC-192 framing in quad OC-48 (four channels) also supported.
- Programmable enable of SONET scrambler/descrambler.
- Ability to bypass all functions to send and receive raw data to/from the SERDES interface (user must guarantee needed one's density for proper SERDES operation).
- Insertion and checking of link assignment values to facilitate interconnection and debugging of backplanes.
- Optional AIS-L (alarm indication signal) insertion during loss-of-frame. Optional RDI-L (remote defect indicator) insertion for maintenance capabilities.
- SONET FI link I/O insertion on transmit (microprocessor programmed) and extraction to a status register on receive.
- SPE signal marks payload bytes when cell processing is not used. Optional ability to perform simple pointer byte processing for increment and decrement also included.
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Ability to select half-rate or full-rate for each channel individually.
- Frame alignment across multiple ORSO82G5 devices for work/protect switching at STS-768/STM-256 and above rates.
- In-band management and configuration through transport overhead extraction/insertion.
- Supports transparent mode where all internally generated SONET overhead bytes can be overridden by user-generated overhead bytes from FPGA.
- Optional A1/A2 corruption, B1 byte corruption and K2 byte corruption, to facilitate system testing.
- Built-in boundary scan (*IEEE* ® 1149.1 and 1149.2 JTAG), including the SERDES interface.
- FIFOs align incoming data across all eight channels (all eight channels, two groups of four channels, or four groups of two channels). Optional ability to bypass alignment FIFOs for asynchronous operation between channels. (Each channel includes its own clock and frame pulse.)
- Cell processing blocks (X8 or X2) included to provide glueless interface to Agere's Pi-40 fabric devices and 10 Gbits/s network processor. Cell processing includes cell creation, cell extraction, idle cell insertion, and idle cell deletion asynchronous from line rates. This logic can also be used when both ends of a link are ORSO82G5 devices for generic cell-based backplanes. This logic is by-passable when not being used.
- Addition of two 4K x 36 dual-port RAMs with access to the programmable logic.
- Pinout compatible to the *ORCA* ORT82G5 8B/10B backplane driver FPSC in the 680 PBGAM package.

Intellectual Property Features

Programmable logic provides a variety of interface functions, including the following Agere's IP core functions:

- Backplane drivers:
  - — Pi-BridgeNP48S: Provides two OC-48 full-duplex serial backplane interfaces for Agere's *Payload-Plus*™ network processor chipset to Agere's Pi-40 switch fabric.
  - — Pi-BridgeAPC: Provides four full-duplex serial backplane interfaces for Agere's *ATLANTA* ATM port controller (APC) to Agere's Pi-40 switch fabric.
- Very short reach (VSR) optical interface.
  - — Flexible interface to VSR-3 (4-fiber, 850 nm optics) optical modules.

Programmable Features

- High-performance programmable logic:
  - — 0.16 µm 7-level metal technology.
  - — Internal performance of >250 MHz.
  - — Over 400k usable system gates.
  - — Meets multiple I/O interface standards.
  - — 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - — LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - — Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - — Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - — Two slew rates supported (fast and slew-limited).
  - — Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
  - — Off-chip clock drive capability.
  - — Two-input function generator in output path.
- New programmable high-speed I/O:
  - — Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - — Double-ended: LVDS, bused-LVDS, and LVPECL.
- New capability to (de)multiplex I/O signals:
  - — New DDR on both input and output at rates up to 350 MHz (700 MHz effective rate).
  - — New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-quad programmable function unit (PFU):
  - — Eight 16-bit look-up tables (LUTs) per PFU.
  - — Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - — New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - — New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - — 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - — Flexible fast access to PFU inputs from routing.
  - — Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and non-buffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and *PAL*™-like and-or-invert (AOI) in each programmable logic cell.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provides optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz. Multiplication of input frequency of up to 64x and division of input frequency down to 1/64x possible.

Programmable Features (continued)

- New 200 MHz embedded quad-port RAM blocks, two read ports, two write ports, and 2 sets of byte lane enables. Each embedded RAM block can be configured as:
  - — One—512 x 18 (quad-port, two read/two write) with optional built in arbitration.
  - — One—256 x 36 (dual-port, one read/one write).
  - — One—1k x 9 (dual-port, one read/one write).
  - — Two—512 x 9 (dual-port, one read/one write for each).
  - — Two RAMs with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - — Supports joining of RAM blocks.
  - — Two 16 x 8-bit content addressable memory (CAM) support.
  - — FIFO 512 x 18, 256 x 36, 1k x 9, or dual 512 x 9 (synchronous or asynchronous).
  - — Constant multiply (8 x 16 or 16 x 8).
  - — Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard-cell blocks with 66 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - — Full boundary scan (*IEEE* 1149.1 and Draft 1149.2 JTAG).
  - — Programming and readback through boundary-scan port compliant to *IEEE* Draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC*®/PowerQUICC 860 and *PowerPC* II MPC8260 high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA*™ specification 2.0 AHB system bus (*ARM* ® processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard cell blocks.
- Variable-size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to six high-speed clocks on each edge of the device for improved setup/hold and clock to out performance.
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced-speed internal logic.
- *ORCA Foundry* development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets universal test and operations PHY interface for ATM (UTOPIA) Levels 1, 2, and 3; as well as POS-PHY3. Also meets proposed specifications for UTOPIA Level 4 for and POS-PHY3 (2.5 Gbits/s) and POS-PHY4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.

Overview

The ORSO82G5 backplane transceiver FPSC has eight serializer/deserializer (SERDES) channels, each operating at up to 2.7 Gbits/s with a full-duplex synchronous interface with built-in clock/data recovery (CDR). The CDR interface provides a physical medium for high-speed serial transfer between system devices. Devices can be on the same PC-board, on separate boards connected across a backplane, or connected by cables. The other major function of the SERDES is to serialize the incoming serial data into a separate 8-bit bus.

The other major blocks in the embedded core of the ORSO82G5 include the SONET Rx block, SONET Tx block, the input port controller (IPC), and the output port controller (OPC). A block diagram of the ORSO82G5 is shown in Figure 1.

SONET Tx Block

The major functions of the SONET Tx block are: the creation of the SONET frame, insertion of the data from the OPC or FPGA logic into the synchronous payload envelope (SPE), and either creation of the transport overhead or insertion of the transport overhead from the FPGA logic. This block also optionally scrambles the data to ensure a proper density for the SERDES.

SONET Rx Block

The SONET Rx block optionally descrambles and then frames the incoming SONET frames, extracts the overhead and processes a limited number of bytes (such as BIP-8, K2). The resulting SPE is then forwarded to the IPC or FPGA logic for further processing.

IPC

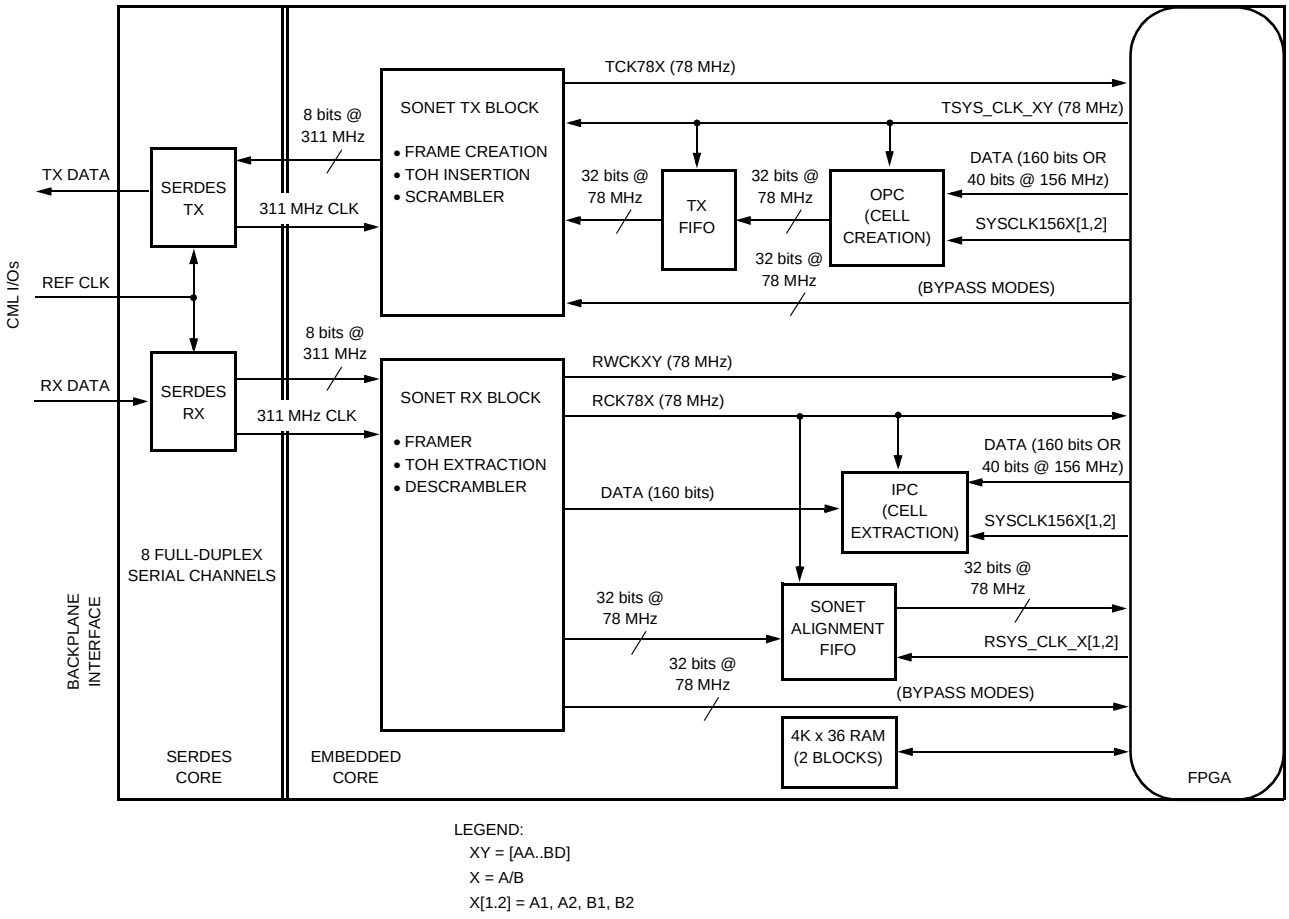
The IPC (input port controller) is used to direct cell traffic in the receive direction. Cells are typically distributed across several SERDES links. One of the main functions of the input port controller is to extract cells from different links and regroup them. The IPC can service link bundles of 8 or 2. The essential functions of the input port controller are:

- Determines when cell data can be read from the Rx FIFOs of the individual SERDES links and ensures group bundles are properly aligned.
- Schedules these reads from the Rx FIFOs of the links. Cells are read one at a time in a round-robin fashion from the active links.
- Parses the cell data into payload data and detects cells which have errors (BIP errors or sequence errors).

OPC

The (OPC) output port controller stripes the cell payload across several links in the transmit direction. It schedules, manages and preforms writes of cell data into the Tx FIFOs of the individual SERDES links. The OPC can service link bundles of 8 or 2.

Block Diagrams



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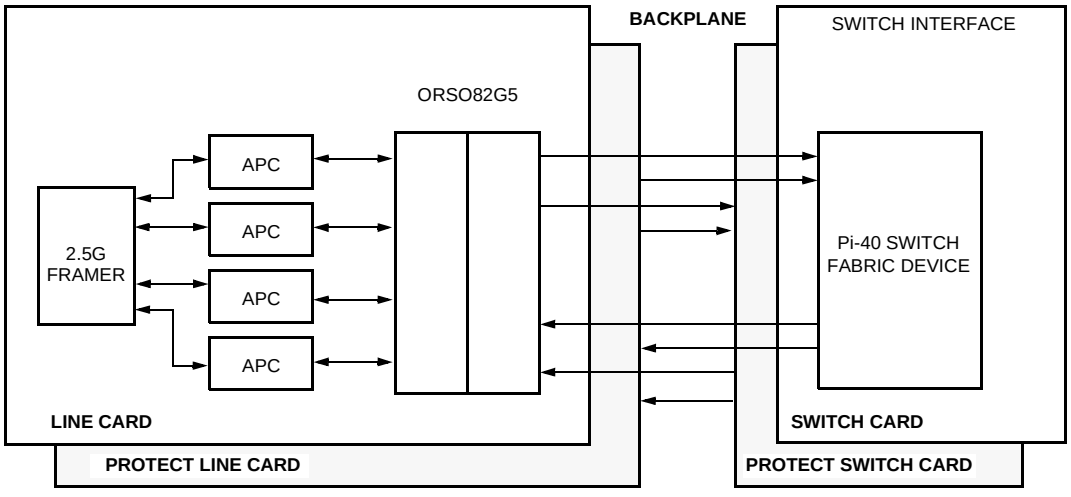
Note: All data bit widths are per channel except the 160-bit interfaces to the IPC and OPC.

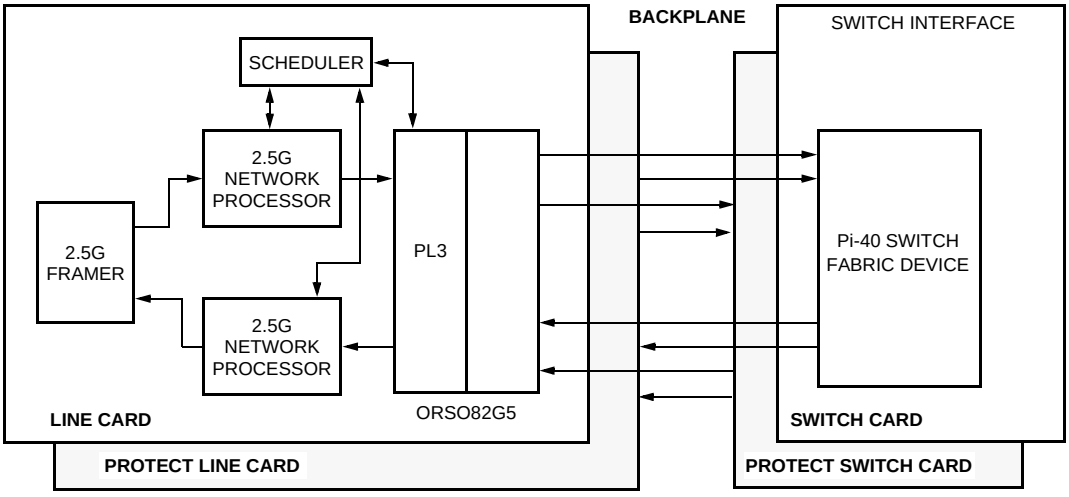
Figure 1. ORSO82G5 Block Diagram



2505(F)

Figure 2. 2.5 Gbits/s Application with (Quad ATM Port Controller) Protection

Block Diagrams (continued)



2506(F)

Figure 3. 2.5 Gbits/s Application (Network Processor) with Protection

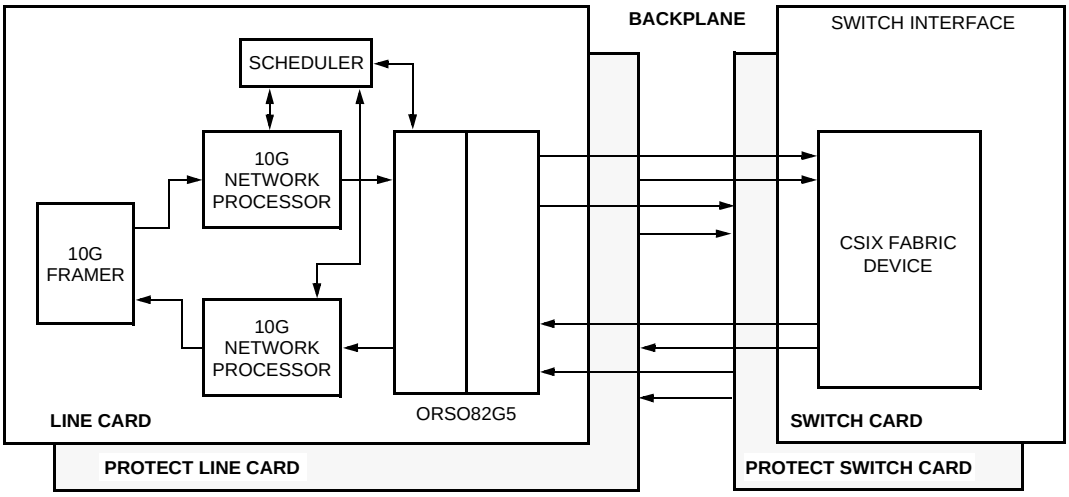


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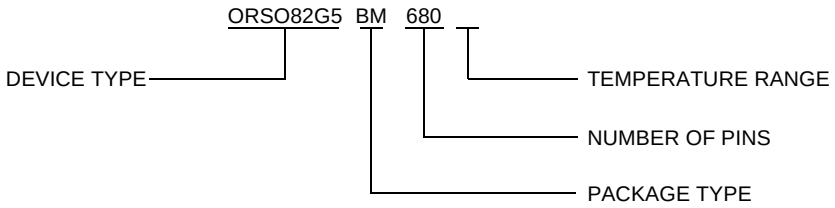
Figure 4. 10 Gbits/s Application (Network Processor) with Protection

Ordering Information



5-6435.r(F)

Table 2. Device Options

Device	Parameter	Value
ORSO82G5	Voltage	1.5 V core 3.3 V/2.5 V/1.8 V/1.5 V I/O
	Package	680-pin PBGAM

Table 3. Temperature Options

Symbol	Description	Temperature
(Blank)	Industrial	–40 °C to +85 °C

Table 4. Package Type Options

Symbol	Description
BM	Plastic Ball Grid Array, Multilayer

Table 5. Package Matrix (Speed Grade)

Devices	680-Pin PBGAM (BM680)
ORSO82G5	–1, –2, –3

Software Ordering Information

Implementing a design in an ORSO82G5 requires the *ORCA Foundry* Development System and an ORSO82G5 FPSC Design Kit. For ordering information, please visit:

http://www.agere.com/netcom/ipkits

Notes:

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