

OPA130
OPA2130
OPA4130

Low Power, Precision FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

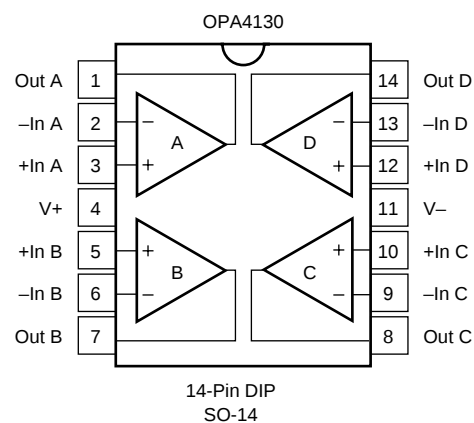
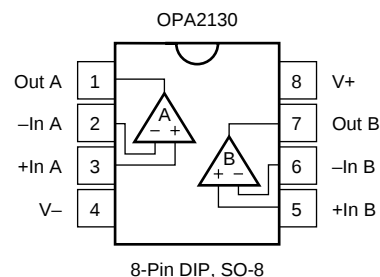
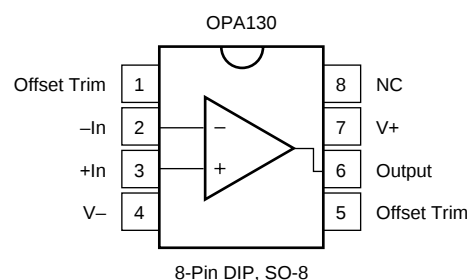
- **LOW QUIESCENT CURRENT:** 530 μ A/amp
- **LOW OFFSET VOLTAGE:** 1mV max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH CMRR:** 90dB min
- **FET INPUT:** $I_B = 20$ pA max
- **EXCELLENT BANDWIDTH:** 1MHz
- **WIDE SUPPLY RANGE:** ± 2.25 to ± 18 V
- **SINGLE, DUAL, AND QUAD VERSIONS**

DESCRIPTION

The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for -40°C to $+85^{\circ}\text{C}$ operation.



SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITION	OPA130PA, UA OPA2130PA, UA OPA4130PA, UA			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature ⁽¹⁾ vs Power Supply Channel Separation (dual and quad)	Operating Temperature Range $V_S = \pm 2.25\text{V to } \pm 18\text{V}$		± 0.2 ± 2 2 0.3	± 1 ± 10 20	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V/V}$ $\mu\text{V/V}$
INPUT BIAS CURRENT ⁽²⁾ Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		+5 See Typical Curve ± 2	± 10 ± 20	pA pA
NOISE Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			30 18 16 16 4		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range, Positive Negative Common-Mode Rejection	$V_{CM} = -13\text{V to } +13\text{V}$	(V+)-2 (V-)+2 90	(V+)-1.5 (V-)+1.2 105		V V dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = -13\text{V to } +13\text{V}$		$10^{13} \parallel 1$ $10^{13} \parallel 3$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-loop Voltage Gain	$V_O = -13.8\text{V to } +13\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = -13\text{V to } +12\text{V}$	120 120	135 135		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	$G = 1$, 10V Step, $C_L = 100\text{pF}$ $G = 1$, 10V Step, $C_L = 100\text{pF}$ $G = 1$, $V_{IN} = \pm 15\text{V}$ 1kHz, $G = 1$, $V_O = 3.5\text{Vrms}$		1 2 5.5 7 2 0.0003		MHz V/ μs μs μs μs %
OUTPUT Voltage Output, Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation)	$R_L = 2\text{k}\Omega$ $R_L = 2\text{k}\Omega$	(V+)-2 (V-)+1.2 (V+)-3 (V-)+2	(V+)-1.5 (V-)+1 (V+)-2.5 (V-)+1.5 ± 18 10		V V V V mA nF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	± 2.25	± 15 ± 530	± 18 ± 650	V V μA
TEMPERATURE RANGE Operating Range Storage Thermal Resistance, θ_{JA} 8-Pin DIP SO-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount		-40 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$

NOTES: (1) Guaranteed by wafer test. (2) High-speed test at $T_J = 25^\circ\text{C}$.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit ⁽¹⁾	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
Single			
OPA130PA	8-Pin Plastic DIP	006	–40°C to +85°C
OPA130UA	SO-8 Surface-Mount	182	–40°C to +85°C
Dual			
OPA2130PA	8-Pin Plastic DIP	006	–40°C to +85°C
OPA2130UA	SO-8 Surface-Mount	182	–40°C to +85°C
Quad			
OPA4130PA	14-Pin Plastic DIP	010	–40°C to +85°C
OPA4130UA	SO-14 Surface-Mount	235	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



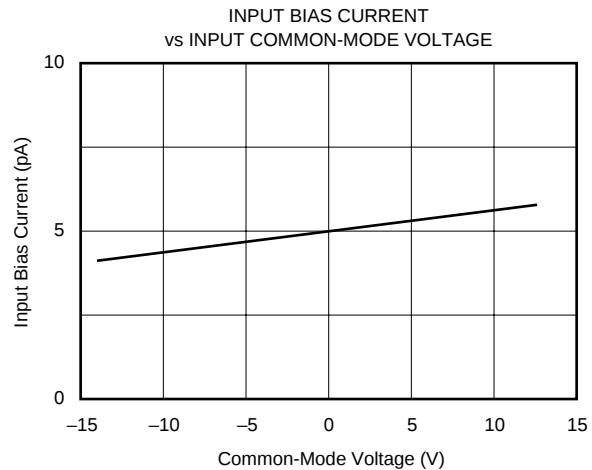
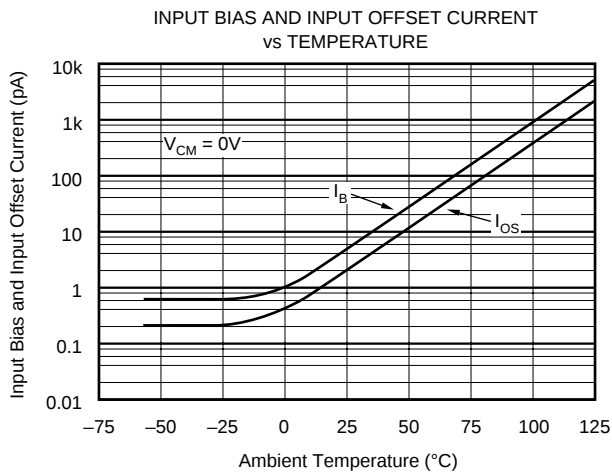
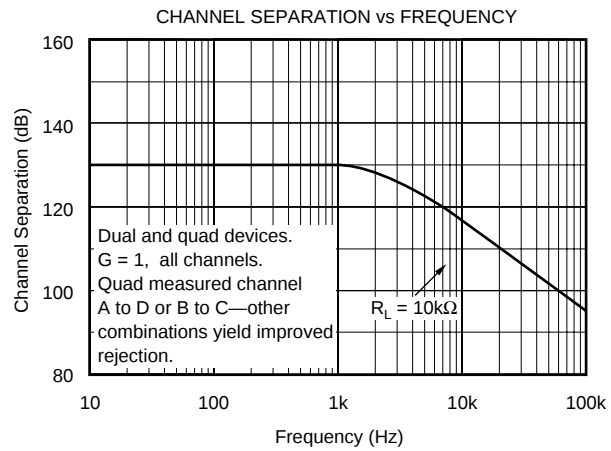
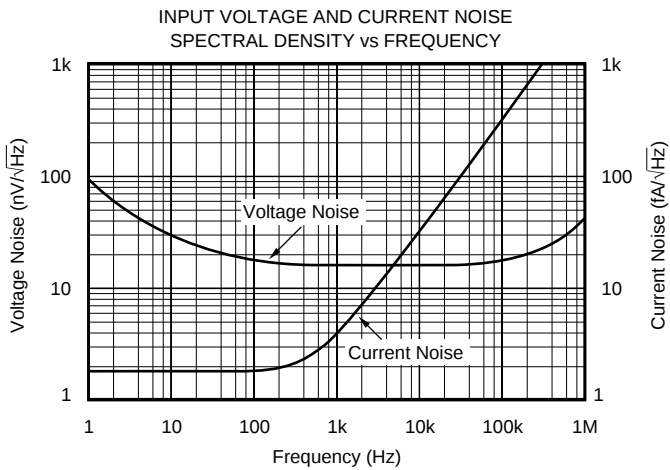
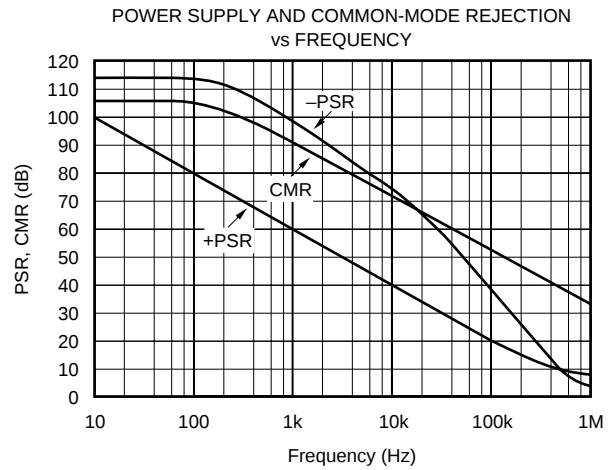
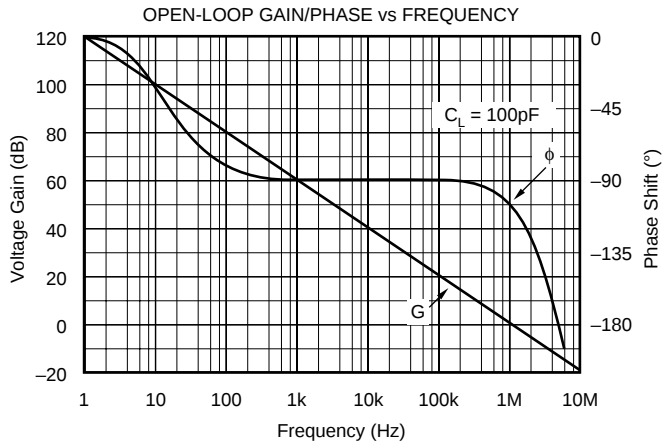
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

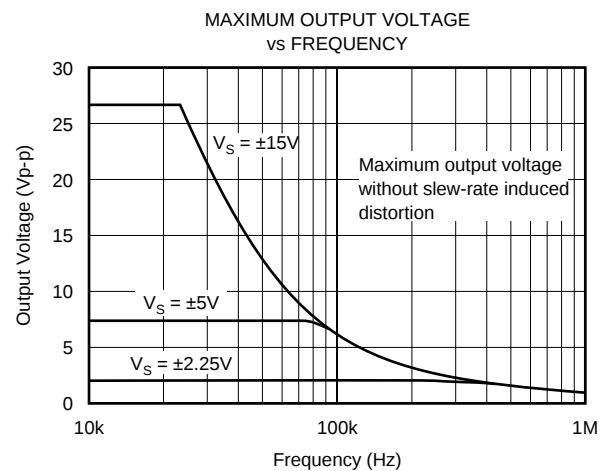
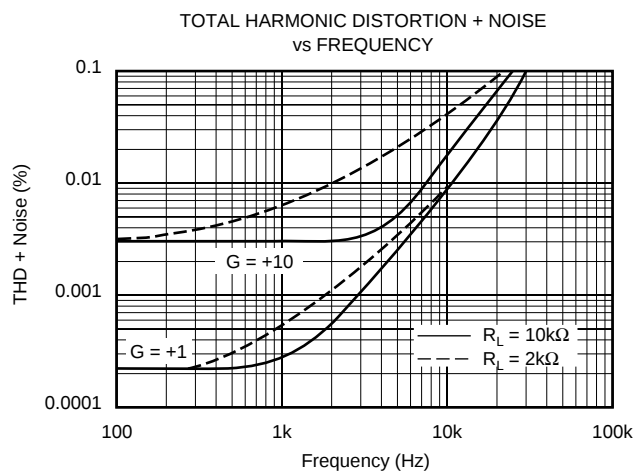
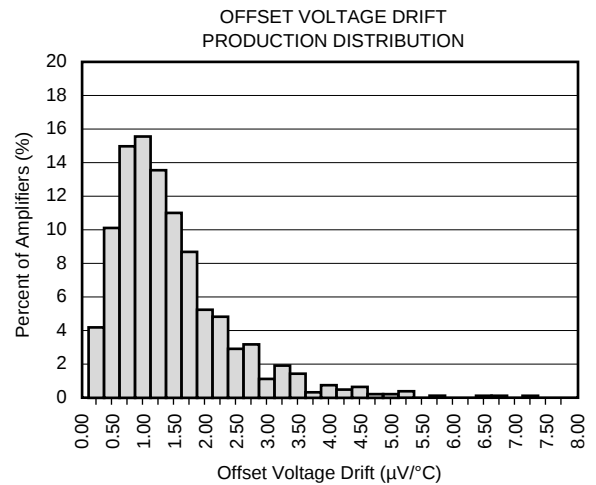
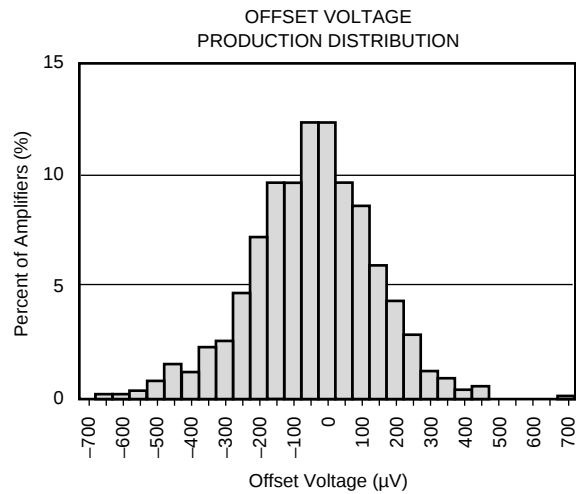
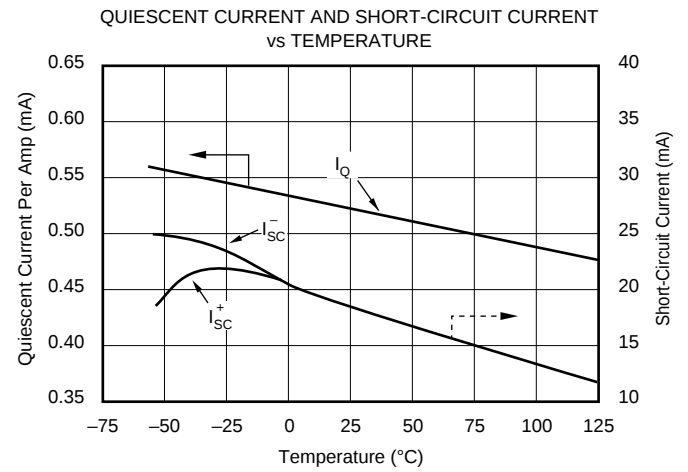
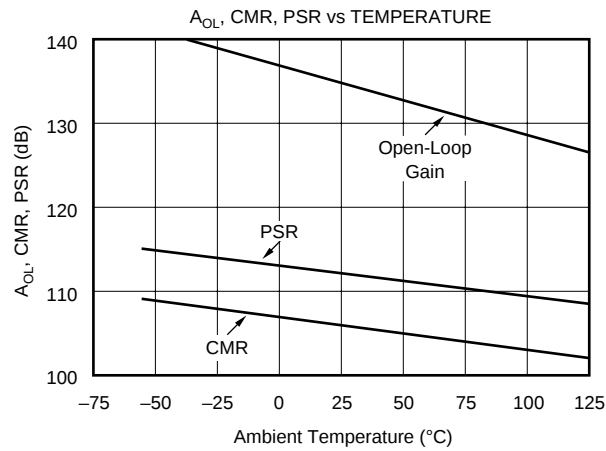
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

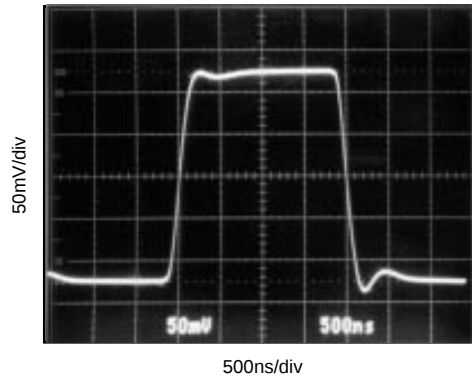
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.



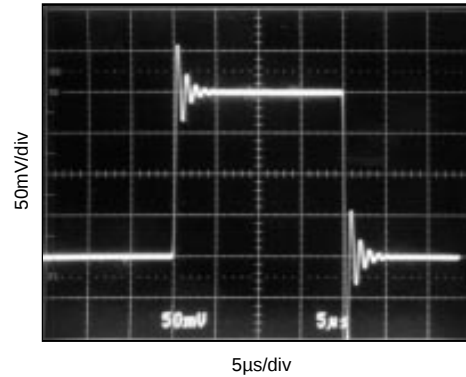
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.

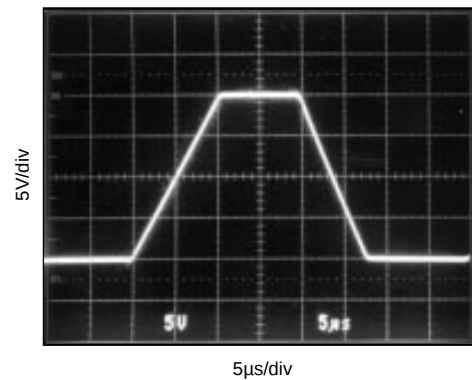
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$



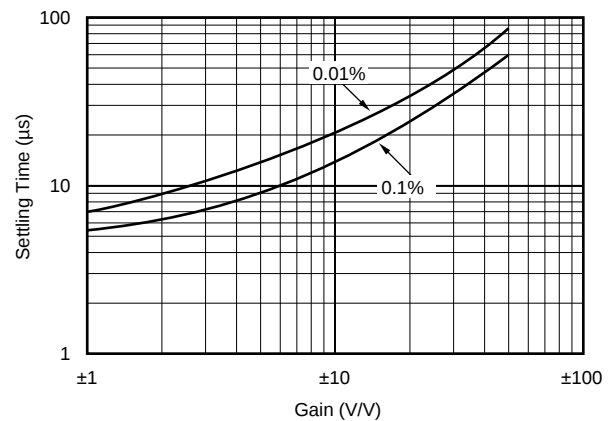
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 1000\text{pF}$



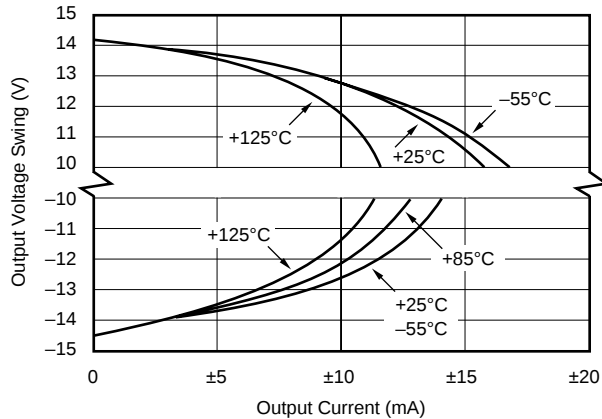
LARGE-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$



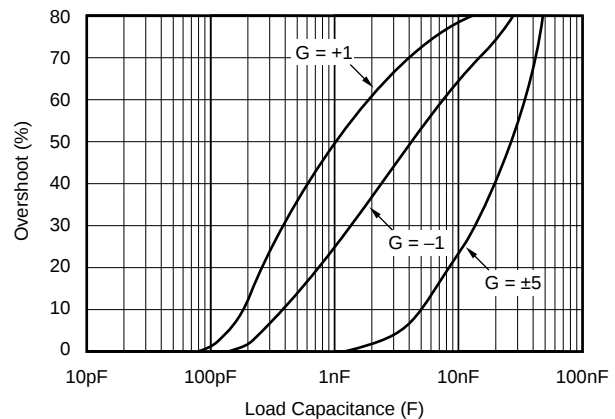
SETTLING TIME vs GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from $\pm 2.25\text{V}$ to $\pm 18\text{V}$ with excellent performance. Although specifications are production tested with $\pm 15\text{V}$ supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

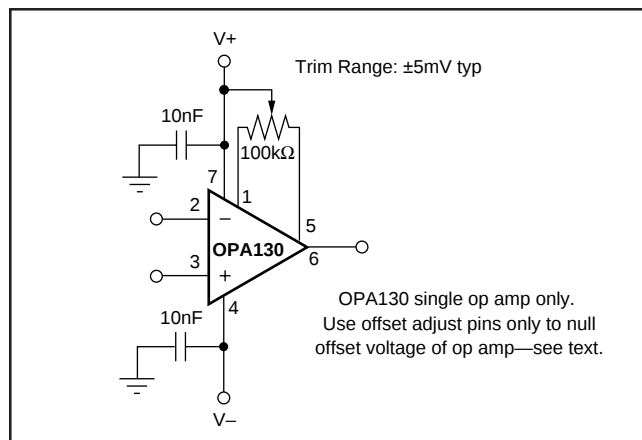


FIGURE 1. OPA130 Offset Voltage Trim Circuit.

INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical performance curve “Input Bias Current vs Temperature.”

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA130. See the typical performance curve “Input Bias Current vs Common-Mode Voltage.”

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.