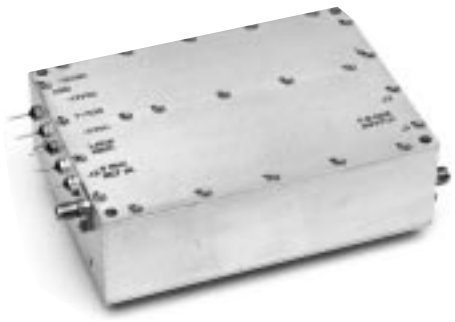
SPECIAL FEATURES

- Low Noise: - 138 dBc/Hz @ 100 kHz offset
- Dual Loop Design
- Suitable for Low Cost, High Volume Applications



This PLDRO uses two phase lock loops for good phase noise performance. The 6.6 GHz DRO, which drives the far-out noise levels, is phase locked to an internal 110 MHz PLXO, which drives the moderately close-in noise; close-in noise is a function of the phased locked PLXO and input 5 MHz reference.

The stand alone dual output DRO consumes only 1 W, nominal, while the complete phase locked assembly uses about 3 W. The circuitry is suitable for operation over the 3 to 7 GHz frequency range, and single output versions are available in smaller package styles.

ELECTRICAL SPECIFICATIONS

Operating Frequency:	6.6 GHz
Input Reference Signal:	5 MHz @ + 2 dBm ± 3 dB
Output Power:	+ 10 dBm ± 2 dB

SSB Phase Noise (dBc/Hz, typical):

offset	Free-Running	Phase Locked
10 Hz	- 27	- 43
100 Hz	- 60	- 55
1 kHz	- 95	- 84
10 kHz	- 118	- 114
100 kHz	- 138	- 122

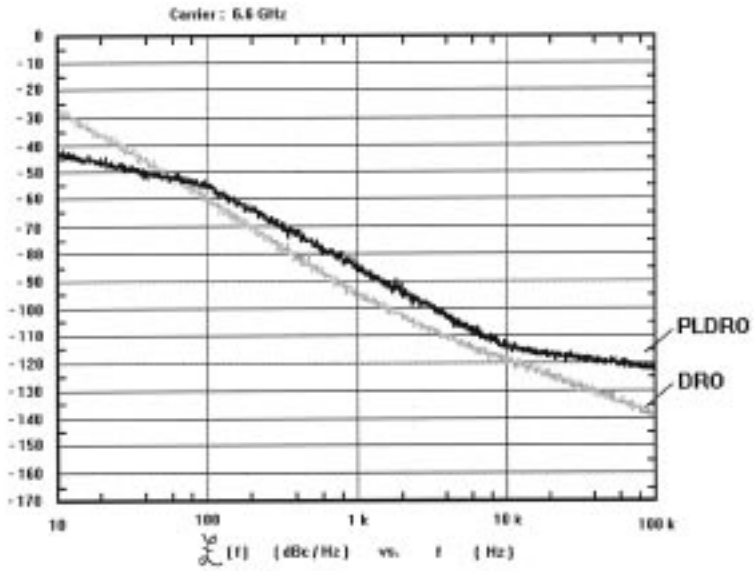
Spurious:	- 75 dBc, maximum
Harmonics:	- 25 dBc, maximum
VSWR:	1.25:1
BITE Scheme:	Phase Lock Indication, TTL "1" = locked condition
DC Power:	+ 12 V ± 1.5 % @ 160 mA, nominal + 5 V ± 1.5 % @ 15 mA, nominal - 12 V ± 1.5 % @ 85 mA, nominal
Power Consumption:	3.1 W, nominal

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature:	0 to + 70 °C, baseplate

MECHANICAL SPECIFICATIONS

Size: (excluding connectors)	0.91 x 0.91 x 0.27 inches 23 x 23 x 7 mm
Weight:	0.17 oz (4.7 g), approximate



Note 1: Unit does not have temperature compensation or heater circuitry.
Specifications subject to change without notice.