



## Features

- 667 Mb/s port data bandwidth, >85Gb/s aggregate bandwidth
- Low power CMOS, 2.5V and 3.3V power supply
- SRAM-based, in-system programmable
- LVDS I/O (OCX256L) and LVPECL I/O (OCX256P) versions
- 256 configurable I/O ports
  - 128 dedicated differential input ports
  - 128 dedicated differential output ports
  - LVTTTL control interface
  - Output Enable control for all outputs
- Non-blocking switch matrix
  - Patented ActiveArray™ matrix for superior performance
  - Double-buffered configuration RAM cells for simultaneous global updates
  - ImpliedDisconnect™ function for single cycle disconnect/connect
- Full Broadcast and multicast capability
  - One-to-One and One-to-Many connections
  - Special broadcast mode routes one input to all outputs at maximum data rate
- Registered and flow-through data modes
  - 333 MHz synchronous mode
  - 667 Mb/s asynchronous mode
  - Low jitter and signal skew
  - Low duty cycle distortion
- RapidConfigure™ parallel interface for configuration and readback
- JTAG serial interface for configuration and Boundary Scan testing
- 792 TBGA package with 1.00mm ball spacing
- Integrated Termination Resistors

## Description

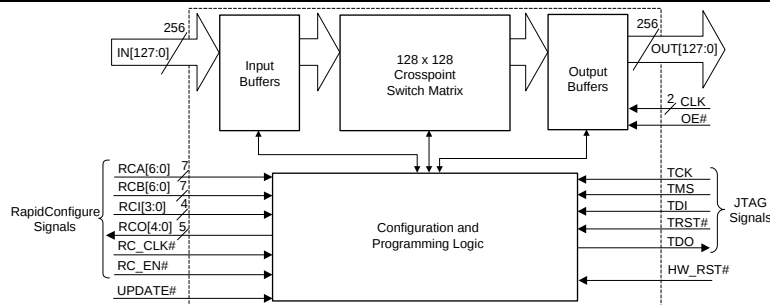
The OCX256 SRAM-based devices are non-blocking 128 X 128 digital crosspoint switches and are available in LVDS (Low Voltage Differential Signaling) and LVPECL (Low Voltage PECL) versions. Both devices are capable of data rates of 667 Megabits per second per port. The I/O ports are fixed as either input or output ports. The input ports support flow-through mode only. The output ports are individually programmable to operate in either flow-through (asynchronous) or registered (synchronous) mode. Each output register may be clocked by a global clock or a next neighbor clock source.

The patented ActiveArray provides greater density, superior performance, and greater flexibility compared to a traditional  $n:1$  multiplexer architecture. The OCX™ devices support various operating modes covering one input to one output at a time as well as one input to many outputs, plus a special broadcast mode to program one input to all outputs while maintaining maximum data rates. In all modes data integrity and connections are maintained on all unchanged data paths.

The RapidConfigure parallel interface allows fast configuration of both the Output Buffers and the switch matrix. Readback is supported for device test and verification purposes. The OCX256 also supports the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The JTAG interface can also be used to download configuration data to the device and readback data. A functional block diagram of the OCX256 is shown in Figure 1.

## Applications

- SONET/SDH and DWDM
- Digital Cross-Connects
- System Backplanes and Interconnects
- High Speed Test Equipment
- ATM Switch Cores
- Video Switching



**Figure 1 OCX256 Functional Block Diagram**



*(This page intentionally left blank)*



## Contents

|                                                       |           |
|-------------------------------------------------------|-----------|
| <b>1. Introduction .....</b>                          | <b>7</b>  |
| 1.1 Input and Output Buffers .....                    | 8         |
| 1.1.1 Input and Output Port Function Mode .....       | 8         |
| 1.1.2 Broadcast Mode .....                            | 9         |
| 1.2 Output Buffer Configuration .....                 | 9         |
| 1.2.1 Output Control Signals.....                     | 9         |
| 1.2.2 Neighboring Output Port as a Clock Source ..... | 9         |
| 1.3 RapidConfigure Interface .....                    | 11        |
| 1.3.1 RapidConfigure Programming Instructions.....    | 11        |
| 1.4 JTAG Configuration Controller.....                | 14        |
| 1.4.1 JTAG Interface.....                             | 14        |
| 1.4.2 Output Port Configuration .....                 | 14        |
| 1.4.3 Switch Matrix Configuration .....               | 14        |
| 1.4.4 Mode Control Register Configuration.....        | 14        |
| 1.4.5 JTAG Architecture and Shift Registers .....     | 15        |
| 1.4.6 JTAG State Machine .....                        | 16        |
| 1.4.7 JTAG Input Format .....                         | 16        |
| 1.4.8 JTAG Instructions .....                         | 17        |
| 1.5 ImpliedDisconnect .....                           | 19        |
| 1.6 Device Reset Options .....                        | 20        |
| <b>2. Pin Description .....</b>                       | <b>21</b> |
| <b>3. Differential I/O Standards .....</b>            | <b>22</b> |
| 3.1 LVDS .....                                        | 22        |
| 3.2 LVPECL .....                                      | 23        |
| <b>4. Electrical Specifications .....</b>             | <b>24</b> |
| 4.1 Absolute Maximum Ratings .....                    | 24        |
| 4.2 Recommended Operating Conditions .....            | 24        |
| 4.3 Pin Capacitance .....                             | 24        |
| 4.4 DC Electrical Specifications .....                | 25        |



|           |                                                              |           |
|-----------|--------------------------------------------------------------|-----------|
| 4.5       | AC Electrical Specifications.....                            | 26        |
| 4.6       | Timing Diagrams.....                                         | 27        |
| <b>5.</b> | <b>Package and Pinout .....</b>                              | <b>31</b> |
| 5.1       | Package Pinout .....                                         | 31        |
| 5.2       | Pinout by Ball Sequence.....                                 | 32        |
| 5.3       | Pinout by Ball Name .....                                    | 36        |
| 5.4       | Package Dimensions.....                                      | 40        |
| 5.5       | Package Thermal Characteristics.....                         | 42        |
| <b>6.</b> | <b>Power Consumption .....</b>                               | <b>43</b> |
| 6.1       | Power for OCX256L (LVDS) .....                               | 43        |
| 6.2       | Power for OCX256P (LVPECL) .....                             | 44        |
| <b>7.</b> | <b>Component Availability and Ordering Information .....</b> | <b>45</b> |
| <b>8.</b> | <b>Glossary.....</b>                                         | <b>45</b> |
| <b>9.</b> | <b>Product Status Definition .....</b>                       | <b>47</b> |



## Figures

|           |                                                             |    |
|-----------|-------------------------------------------------------------|----|
| Figure 1  | OCX256 Functional Block Diagram .....                       | 1  |
| Figure 2  | OCX256 Switch Matrix .....                                  | 7  |
| Figure 3  | Input and Output Buffer Configuration .....                 | 8  |
| Figure 4  | Next Neighbor Clock Block Diagram .....                     | 10 |
| Figure 5  | OCX256 JTAG Architecture .....                              | 15 |
| Figure 6  | OCX256 JTAG State Machine .....                             | 16 |
| Figure 7  | OCX256L LVDS Signal Circuit.....                            | 22 |
| Figure 8  | OCX256P LVPECL Signal Circuit .....                         | 23 |
| Figure 9  | Registered Output Mode Timing .....                         | 27 |
| Figure 10 | Flow-Through Mode Timing .....                              | 27 |
| Figure 11 | Output Enable Timing .....                                  | 27 |
| Figure 12 | Duty Cycle Distortion.....                                  | 28 |
| Figure 13 | RapidConfigure Write Cycle .....                            | 28 |
| Figure 14 | RapidConfigure Read Cycle .....                             | 29 |
| Figure 15 | JTAG Timing.....                                            | 29 |
| Figure 16 | Typical Performance at 667 Mb/s with PRBS Data .....        | 30 |
| Figure 17 | OCX256 Package Pinout .....                                 | 31 |
| Figure 18 | OCX256 Package—Bottom View .....                            | 40 |
| Figure 19 | OCX256 Package—Top and Side Views .....                     | 41 |
| Figure 20 | Power Consumption Diagram for the OCX256L using LVDS .....  | 43 |
| Figure 21 | Power Consumption Diagram for the OCX256P using LVPECL..... | 44 |



## Tables

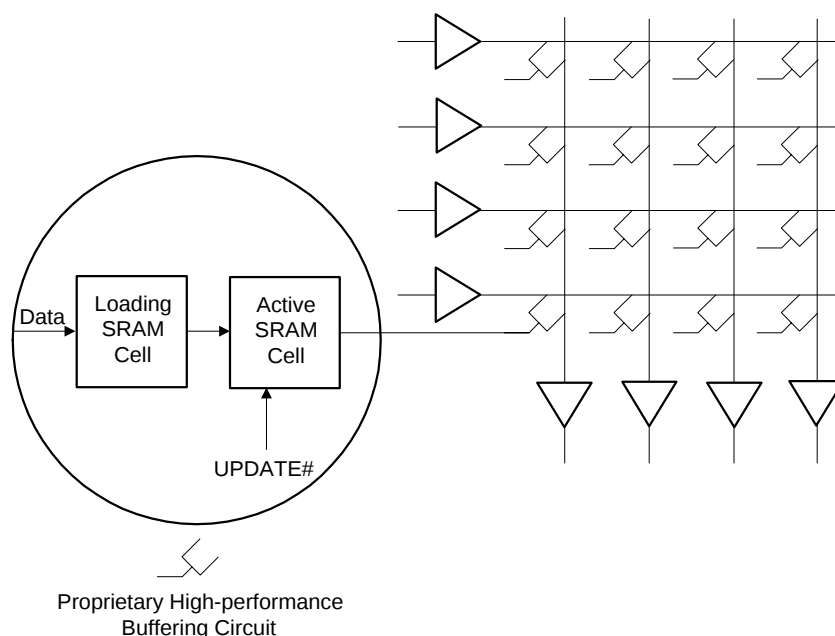
|          |                                                                            |    |
|----------|----------------------------------------------------------------------------|----|
| Table 1  | Summary for Programmable I/O Attributes for OCX256.....                    | 8  |
| Table 2  | Next Neighbor Outputs.....                                                 | 10 |
| Table 3  | RapidConfigure Programming Instructions .....                              | 11 |
| Table 4  | RCO[4:0] Readback Pin Assignment.....                                      | 13 |
| Table 5  | Programming an Output Buffer using RapidConfigure .....                    | 13 |
| Table 6  | Mode Control Register .....                                                | 14 |
| Table 7  | JTAG Input Format .....                                                    | 16 |
| Table 8  | JTAG Instructions .....                                                    | 17 |
| Table 9  | Programming an Output using JTAG.....                                      | 19 |
| Table 10 | Number of JTAG Cycles and Configuration Time .....                         | 19 |
| Table 11 | Device Reset Options .....                                                 | 20 |
| Table 12 | OCX256 Pin Description.....                                                | 21 |
| Table 13 | Absolute Maximum Ratings.....                                              | 24 |
| Table 14 | Recommended Operating Conditions.....                                      | 24 |
| Table 15 | Pin Capacitance .....                                                      | 24 |
| Table 16 | LVTTL DC Electrical Specifications.....                                    | 25 |
| Table 17 | OCX256L (LVDS) DC Electrical Specifications ( $V_{DD,PAD} = 2.5V$ ) .....  | 25 |
| Table 18 | OCX256P (LVPECL) DC Electrical Specifications ( $V_{DD,PAD} = 3.3V$ )..... | 25 |
| Table 19 | AC Electrical Specifications.....                                          | 26 |
| Table 20 | OCX256 Pinout By Ball Sequence.....                                        | 32 |
| Table 21 | OCX256 Pinout By Ball Name .....                                           | 36 |
| Table 22 | Package Thermal Coefficients.....                                          | 42 |



## 1. Introduction

The OCX256 is a differential crosspoint-switching device. The main functional block of the device is a Switch Matrix as shown in Figure 1. The Switch Matrix is a x-y structure supporting an input-to-output data flow. Figure 2 shows a conceptual view of the switch matrix with inputs connected to the horizontal trace and outputs to the vertical trace. Connections between vertical and horizontal lines are implemented with a proprietary high-performance buffering circuit. Signal path delays through the Switch Matrix are very well balanced, resulting in predictable and uniform pin-to-pin delays.

**Note** – For the purpose of clarity, the logic diagrams within this data sheet are conceptual representations only and do not show actual circuit implementation.



**Figure 2** OCX256 Switch Matrix

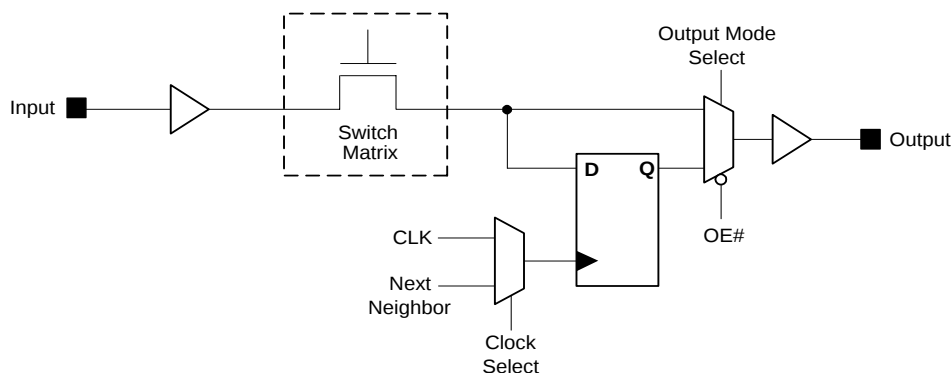
The Active SRAM cells are responsible for establishing connections in the switch matrix by turning on the interconnect circuit, while the Loading SRAM cell can be used to store a second configuration that can be transferred to the Active SRAM cell at a later time. The two SRAM cells are arranged so that a double buffered scheme can be employed. Through the use of an internal signal (generated automatically during a programming cycle) it is possible to store a second configuration map in the Loading SRAM while the Active SRAM maintains its present connection status. When the UPDATE# signal is asserted low (# denotes active low), the contents of the Loading SRAM cell are transferred to the Active SRAM cell and the switch matrix connection is either made or broken.

The UPDATE# signal can be used to control when the switch matrix is reconfigured. For instance, as long as the UPDATE# signal is de-asserted (held high), the Loading SRAM cells for the entire switch matrix could be changed without affecting the current configuration of the switch. When the UPDATE# signal is asserted low, the entire switch matrix would be reconfigured simultaneously. If the UPDATE# signal is asserted continuously, all crosspoint programming commands (generated by RapidConfigure or JTAG programming cycles) will take effect immediately, since the Loading SRAM cell's contents will be transferred directly to the Active SRAM cell.



## 1.1 Input and Output Buffers

All of the input buffers are differential inputs with flow-through mode. The output buffers are programmable for either flow-through or registered mode. Figure 3 shows the basic block diagram of the input and output blocks with the sources for the output control signals (OE# and CLK). The control signals are explained in more details in the following sections.



**Figure 3 Input and Output Buffer Configuration**

### 1.1.1 Input and Output Port Function Mode

The following legend describes the various modes of the Input and Output Ports and the specification used by the OCXPro™ Software.

Legend:

**Ax**—Switch Matrix Signal

**Px**—Port Signal

**OE#**—Output Enable (# means “Active Low”)

**CLK**—Clock

**Table 1 Summary for Programmable I/O Attributes for OCX256**

| Symbol | I/O Port Function                                                                                                                                                                                                                           | Mnemonic  |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
|        | <b>Input</b> – The external signal is buffered from the Input Port pin to the corresponding Switch Matrix line.                                                                                                                             | <b>IN</b> |
|        | <b>Output</b> – The internal signal is buffered from the corresponding Switch Matrix line to the Output Port pin. In this mode an optional output enable (OE#) can be selected. The default state is logic high with enable set to ON.      | <b>OP</b> |
|        | <b>Registered Output</b> – The internal signal on the Switch Matrix line is registered by an edge-triggered register within the Output Port. A clock source is required in this mode. An output enable (OE#) is available but not required. | <b>RO</b> |
|        | <b>No Connect</b> – In this mode, the output Port pin is isolated from the Switch Matrix.                                                                                                                                                   | <b>NC</b> |



## 1.1.2 Broadcast Mode

The OCX256 has a special Broadcast Mode which connects any input to all outputs without performance degradation. The input is selected using RapidConfigure or JTAG and disconnects all other inputs. The Global Update pin (UPDATE#) must be held high during Broadcast Mode. Asserting the UPDATE# pin returns the array to the previous program condition.

## 1.2 Output Buffer Configuration

Every output port of the OCX256 can be configured as either a flow-through or registered output. In registered mode there are two clock sources that are available:

- Global Clock
- Next Neighbor

Additionally, there are output control signals.

### 1.2.1 Output Control Signals

Every output port of the OCX has a global Output Enable signal (OE#). All output buffers have output enables that have programmable polarity and are individually configurable.

Additionally each output can be permanently enabled (always ON) or disabled (always OFF) which is useful for applications which need to tri-state outputs (for example when using multiple chips in expansion mode) or for power saving in designs that do not need to use all the outputs available.

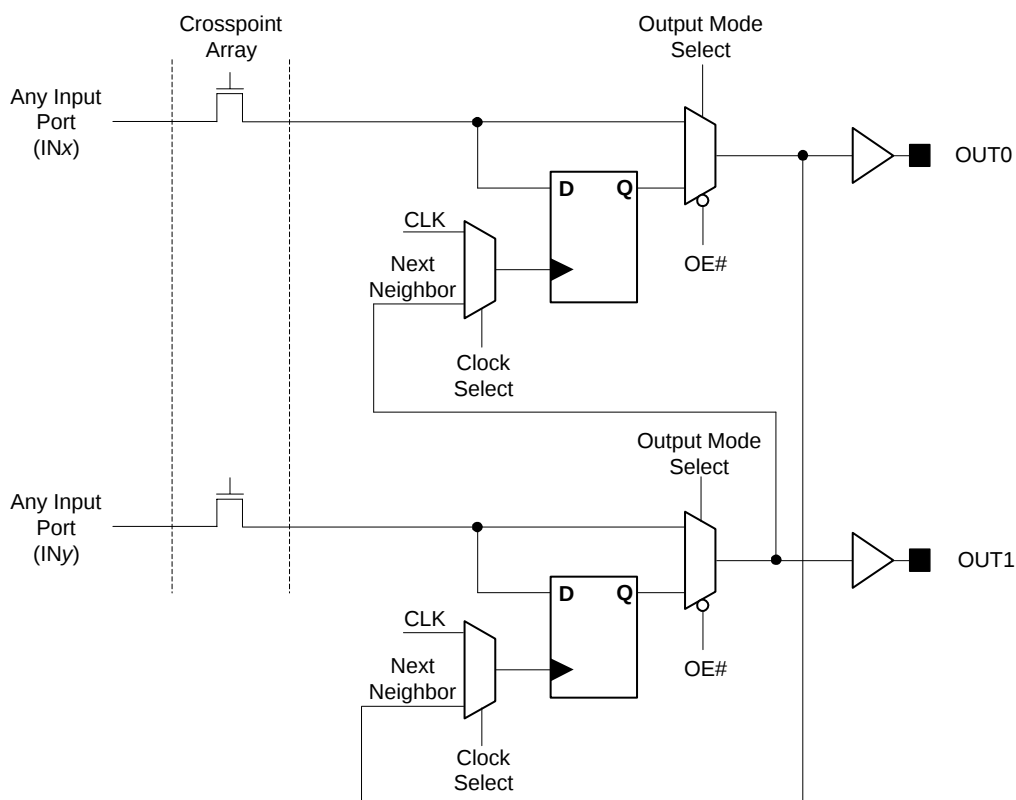
Two control bits are used to control the function of the output enable function as described in Table 5.

### 1.2.2 Neighboring Output Port as a Clock Source

A physically adjacent port can be used as a clock source for an output port configured in registered mode. These outputs are grouped in pairs such that the signal being switched through OUT0 can be used to clock the signal being switched through OUT1, and vice versa. Any single clock or data input signal can be used to clock any other input signal provided they are switched to an appropriate output pair (see Table 2). Figure 4 shows the implementation of next neighbor output port clocking in the OCX256 switch.

For example, IN<sub>x</sub> is used for data input while IN<sub>y</sub> is used for the corresponding clock. IN<sub>x</sub> is connected to OUT0 via the crosspoint array while IN<sub>y</sub> is connected to OUT1 via the crosspoint array. OUT0 is configured in registered output (RO) mode with OUT1 as its next neighbor clock selection. OUT1 will output the clock signal as well as clock the data in OUT0. Adjacent port selection is required for next neighbor clocking in the registered output mode.

This feature is useful in many applications where different types of data switching through the crosspoint array have various associated clocks. To match the delays in the data and corresponding clocks, it is common practice to pass the clocks through the switch along with the data.



**Figure 4** Next Neighbor Clock Block Diagram

The advantages of next neighbor clocking are:

1. Using next neighbor clocking in the registered output (RO) mode helps reduce the skew in outgoing data.
2. For a design with a large number of outputs switching simultaneously, next neighbor clocking mode is useful to stagger outputs for reduced board noise caused by simultaneous switching outputs.

**Note** – Selecting the next neighbor clock for both outputs at the same time is not recommended. Only one output in the pair at a time can be clocked by its next neighbor.

**Table 2** Next Neighbor Outputs

| Pairing Sequence for Neighboring Outputs |     |     |     |     |     |      |         |         |  |
|------------------------------------------|-----|-----|-----|-----|-----|------|---------|---------|--|
| Output Next Neighbor Pairs               | 0,1 | 2,3 | 4,5 | 6,7 | 8,9 | ▶▶▶▶ | 124,125 | 126,127 |  |

Only OUT1 can neighbor with OUT0, OUT3 with OUT2, etc. OUT2 cannot neighbor with OUT1, or OUT4 with OUT3, etc.



### 1.3 RapidConfigure Interface

RapidConfigure (RC) is a 25 signal parallel interface that is used to program the OCX256 device. The 25 pins are allocated as follows:

RCA[6:0] = RapidConfigure Address A. RCA are input pins.

RCB[6:0] = RapidConfigure Address B. RCB are input pins.

RCI[3:0] = RapidConfigure Instruction Bits

RCO[4:0] = RapidConfigure Readback. RCO are output pins.

RC\_CLK# = RapidConfigure Clock

RC\_EN# = RapidConfigure Cycle Enable (state is sensed on negative edge of clock)

#### 1.3.1 RapidConfigure Programming Instructions

The RC interface supports both write and read types of operations:

1. Write Operations (reset crosspoint and Input or Output Buffer (IOB), configure an Output Buffer, connect/disconnect crosspoint)
2. Read Operations (Output Buffer and crosspoint configuration read).

**Table 3 RapidConfigure Programming Instructions**

| RCI[3:0]       | RCA[6:0]            | RCB[6:0]           | RCO[4:0] | Instruction                               | Description                                                                                                                                                                                                                                                  |
|----------------|---------------------|--------------------|----------|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0000           |                     |                    |          | Reserved                                  |                                                                                                                                                                                                                                                              |
| 0001           |                     |                    |          | Reserved                                  |                                                                                                                                                                                                                                                              |
| 0010           | X                   | X                  |          | Reset Crosspoint Array                    | Reset, along with an Update operation (UPDATE# pin or Update command), resets the entire crosspoint array to no connect. All Output Buffers remain unchanged by this operation.                                                                              |
| 0011           | X                   | Input Port Address |          | Set Array to Broadcast mode               | Connects the input selected by RCB[6:0] to all output ports and disconnects all other inputs. The Global Update (UPDATE#) pin must be held high during Broadcast mode. Activating the Global Update pin returns the array to the previous program condition. |
| 0100           | Output Port Address | Data               |          | Configure an Output Buffer                | Program an Output Buffer specified by RCA[6:0].<br>See Table 5 for RCB[6:0] bit assignment and buffer functionality.                                                                                                                                         |
| 0101           |                     |                    |          | Readback Crosspoint, Output Buffer status | This is a two-cycle instruction.                                                                                                                                                                                                                             |
| <u>Cycle 1</u> | Output Port Address | Input Port Address | X        |                                           | Specify the crosspoint connect status at output location specified by RCA[6:0] to the input location specified by RCB[6:0].                                                                                                                                  |



**Table 3 RapidConfigure Programming Instructions (Continued)**

| RCI[3:0]       | RCA[6:0]            | RCB[6:0]           | RCO[4:0]    | Instruction                        | Description                                                                                                                                                                                                                                                                     |
|----------------|---------------------|--------------------|-------------|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <u>Cycle 2</u> | X                   | X                  | Output Data |                                    | Readback (using RCO[4:0]) the status of the output buffer specified in Cycle 1 by RCA[6:0], the output buffer specified in Cycle 1 by RCO[4:0] and the crosspoint connect status.<br><br>See Table 4 for RCO[4:0] readback pin assignment.                                      |
| 0110           | X                   | X                  |             | Update                             | Program the Global Update function without the use of the UPDATE# pin.                                                                                                                                                                                                          |
| 0111           | X                   | Input Port Address |             | Disconnect Input                   | Disconnect the crosspoint cells of the output row location specified by RCA[6:0].                                                                                                                                                                                               |
| 1000           | Output Port Address | Input Port Address |             | Disconnect Input and Output        | Disconnect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the source input address or to the same output address remain the same as before.                                           |
| 1001           | Output Port Address | Input Port Address |             | Connect, with ImpliedDisconnect    | Connect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the same input address or to the same output address are set to no connect (NC).                                               |
| 1010           | Output Port Address | Input Port Address |             | Connect, without ImpliedDisconnect | Connect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections to the same output address are set to no connect while all other connections from the same input address remain the same as before. |
| 1011           |                     |                    |             | Reserved                           |                                                                                                                                                                                                                                                                                 |
| 1100           |                     |                    |             | Reserved                           |                                                                                                                                                                                                                                                                                 |
| 1101           | X                   | X                  |             | Reset All                          | Reset the switch matrix to no connects (NC). Update is forced internally. Sets the Output Buffer to Flow-through mode with Output Enabled.                                                                                                                                      |
| 1110           |                     |                    |             | Reserved                           |                                                                                                                                                                                                                                                                                 |
| 1111           |                     |                    |             | Reserved                           |                                                                                                                                                                                                                                                                                 |

**Note – X = Don't care.**



**Table 4 RCO[4:0] Readback Pin Assignment**

| RCO[4:0]                           | Readback Location | Signal/Function                                                                                                                                                                              |
|------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| O4                                 | Crosspoint        | <b>Connection Status:</b><br>0 = No connection (NC) — (default state at reset)<br>1 = Connected                                                                                              |
| O3                                 | Output Buffer     | <b>Clock Select:</b><br>0 = Global Clock — (default state at reset)<br>1 = Next Neighbor                                                                                                     |
| O2                                 | Output Buffer     | <b>Output Mode:</b><br>0 = Flow-through (OP) — (default state at reset)<br>1 = Registered (RO)                                                                                               |
| O1, O0<br>0,0<br>0,1<br>1,0<br>1,1 | Output Buffer     | <b>Output Enable:</b><br>Output enabled (ON) – this is the default state at reset<br>Output disabled (OFF)<br>Output controlled by OE (active high)<br>Output controlled by OE# (active low) |

**Table 5 Programming an Output Buffer using RapidConfigure**

| RCB[6:0]                           | Signal/Function                                                                                                                                                                              |
|------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B6, B5, B4                         | Don't care                                                                                                                                                                                   |
| B3                                 | <b>Clock Select:</b><br>0 = Global Clock<br>1 = Next Neighbor                                                                                                                                |
| B2                                 | <b>Output Mode:</b><br>0 = Flow-through (OP)<br>1 = Registered (RO)                                                                                                                          |
| B1, B0<br>0,0<br>0,1<br>1,0<br>1,1 | <b>Output Enable:</b><br>Output enabled (ON) – this is the default state at reset<br>Output disabled (OFF)<br>Output controlled by OE (active high)<br>Output controlled by OE# (active low) |



## 1.4 JTAG Configuration Controller

The Output port attributes and the Switch Matrix connections can be programmed using the JTAG serial bus. The RapidConfigure Interface can be enabled or disabled using the JTAG serial bus.

The JTAG-based serial mode is always available for configuration regardless of whether the RapidConfigure mode is enabled or disabled. However, proper care must be taken when switching between JTAG and RapidConfigure for configuring the devices. Before attempting to change Switch Matrix connections or output port configuration through JTAG, the user must first ensure that the RapidConfigure mode is disabled by using JTAG serial mode to set the RCE bit to zero in the Mode Control Register.

### 1.4.1 JTAG Interface

The dedicated JTAG TAP interface is designed in compliance with the IEEE-1149.1. The standard interface has five pins: Test Data Out (TDO), Test Mode Select (TMS), Test Data In (TDI), Test Reset (TRST#), and Test Clock (TCK), which allow Boundary Scan Testing as well as device configuration and verification. The I-Cube supplied software will automatically generate the necessary bitstream from a higher-level textual description of the required configuration. Data on the TDI and TMS pins are clocked into the device on the rising edge of the TCK signal, while the valid data appears on the TDO pin after the falling edge of TCK. For more detailed information on JTAG programming, refer to the *OCX Family Register Programming Manual*.

### 1.4.2 Output Port Configuration

Output port configuration is accomplished by loading the appropriate bitstream into the programming registers present at each Output port. The JTAG serial bus is used to load configuration data into the Output port programming registers, one Output port at a time.

### 1.4.3 Switch Matrix Configuration

The contents of the SRAM cells controlling Switch Matrix connection can be modified using the JTAG. This is accomplished by loading the configuration data, one word at a time, into the SRAM cells in the Switch Matrix.

### 1.4.4 Mode Control Register Configuration

The OCX256 contains a single bit Mode Control Register used to store user flags for RapidConfigure Enable (RCE). These are required for proper functioning of the device. The contents of this register can be changed using the JTAG interface and a special JTAG instruction.

**Table 6 Mode Control Register**

| RCE | Mode                                    |
|-----|-----------------------------------------|
| 0   | RapidConfigure interface disabled (OFF) |
| 1   | RapidConfigure interface enabled (ON)   |



## 1.4.5 JTAG Architecture and Shift Registers

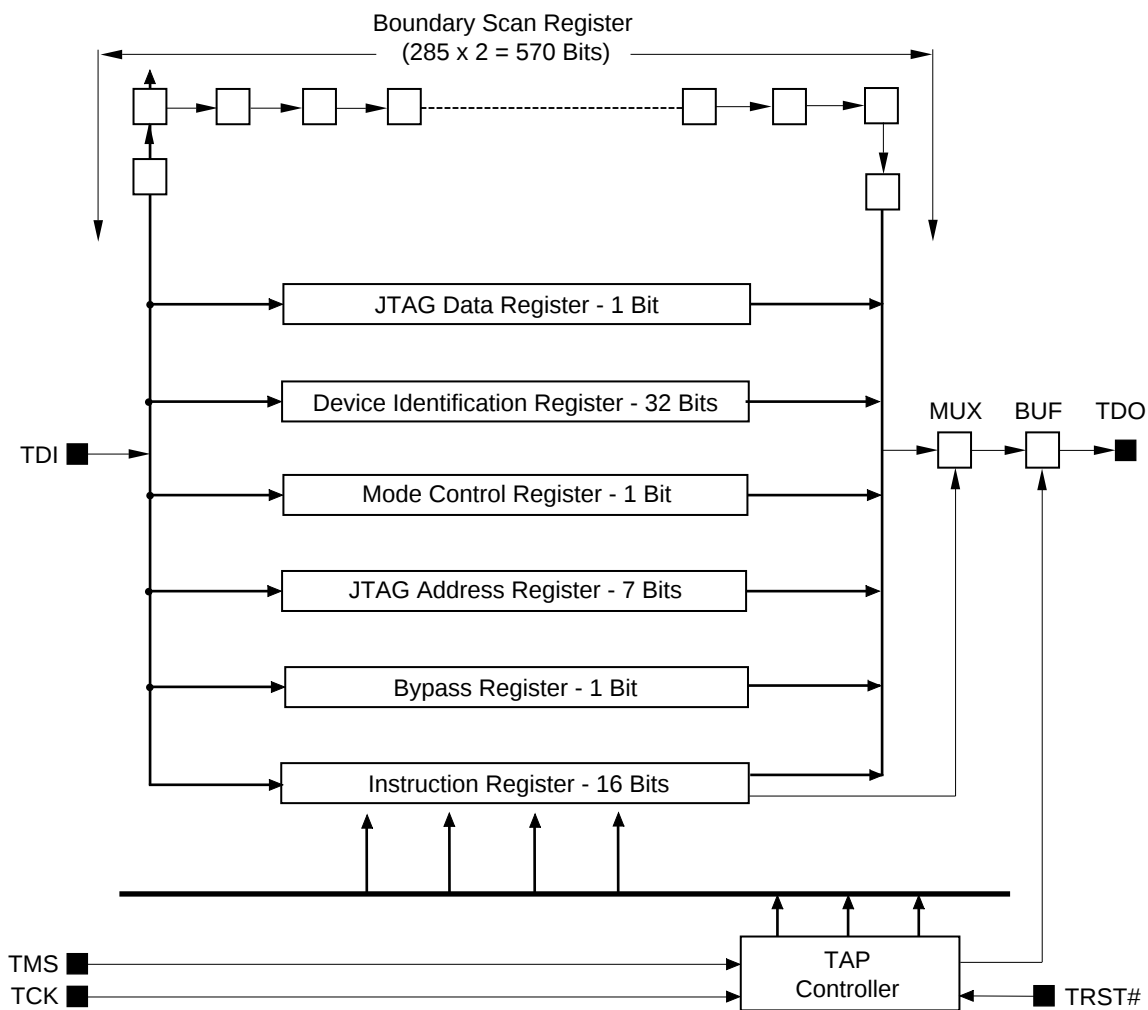


Figure 5 OCX256 JTAG Architecture



### 1.4.6 JTAG State Machine

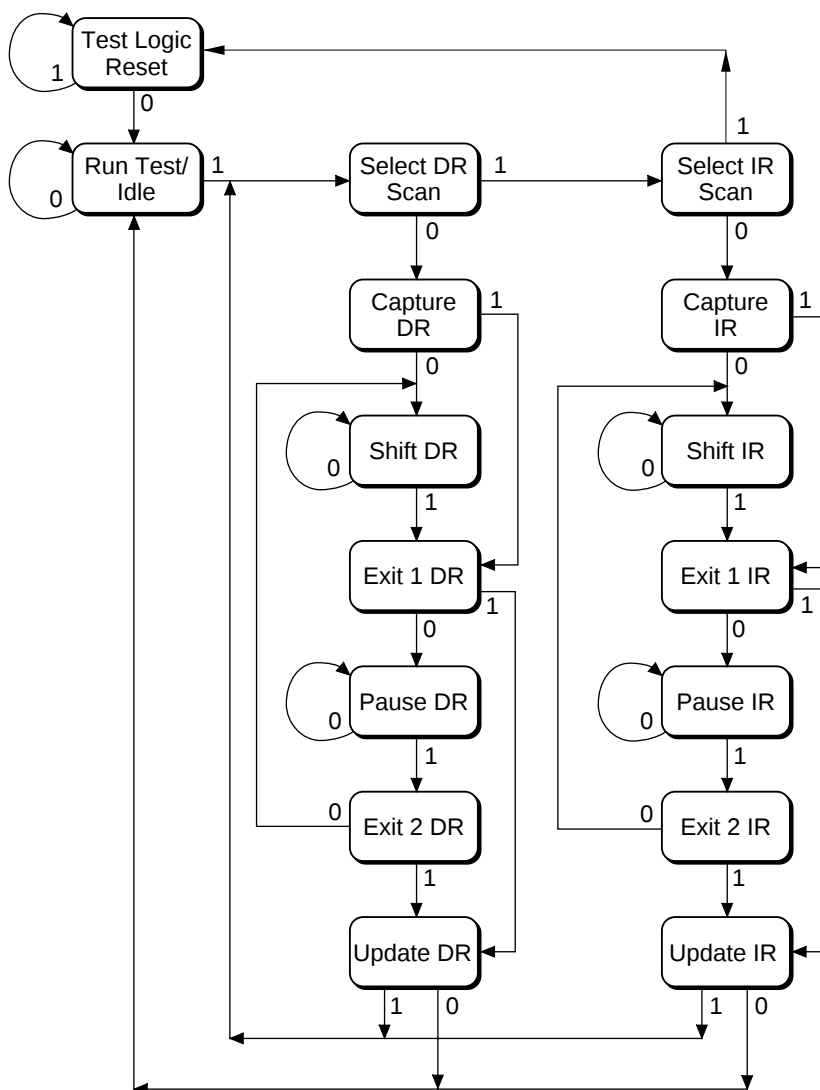


Figure 6 OCX256 JTAG State Machine

### 1.4.7 JTAG Input Format

Table 7 JTAG Input Format

|            | Instruction |    |    |    | Data |    |    |    |    | Address A |    |    |    |    |    |    |
|------------|-------------|----|----|----|------|----|----|----|----|-----------|----|----|----|----|----|----|
| Bit Number | 15          | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7  | 6         | 5  | 4  | 3  | 2  | 1  | 0  |
| Bit Name   | I3          | I2 | I1 | I0 | BB   | BA | B9 | B8 | B7 | A6        | A5 | A4 | A3 | A2 | A1 | A0 |



## 1.4.8 JTAG Instructions

**Table 8 JTAG Instructions**

| I [3:0] | BB | BA           | B9        | B8 | B7 | A6-A0                 | Instruction                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|----|--------------|-----------|----|----|-----------------------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 0 0 0 | X  | X            | X         | X  | X  | X                     | Sample/EXTEST                | Places the device in scan mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 0 0 0 1 | X  | X            | X         | X  | X  | X                     | Sample/EXTEST                | Places the device in scan mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 0 0 1 0 | X  | X            | X         | X  | X  | X                     | Reset the Crosspoint Array   | Resets the entire Crosspoint Array to no-connect. All other Output Buffer configurations are unchanged by this operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0 0 1 1 | X  | X            | X         | X  | X  | X                     | Set Array for Broadcast mode | Use the JTAG Address Register as the Input address to be the broadcast input Connects the selected Input to all Output cells and disconnects all other Inputs. Activating the Global Update JTAG instruction returns the Crosspoint array from the Broadcast mode to the previous programed state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 0 1 0 0 | X  | Clock Select | Data Mode | OE | OE | Output Buffer Address | Program a Buffer             | Programs the Output Buffer address specified in the JTAG instruction (A6-A0). The configuration data is also specified in the JTAG instruction bits BA-B7. See Table 9 for bit assignment of the Buffer functionality.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0 1 0 1 | X  | X            | X         | X  | X  | Output Address/Buffer | Configuration readback       | <p>Readback the connectivity of the Crosspoint cell with the Input location specified in the JTAG Address Register and the Output location specified JTAG instruction (A0-A6). It also returns the configuration of the Output Buffer addressed in the JTAG instruction (A0-A6).</p> <p>The readback data is shifted out of TDO in the following sequence:</p> <ol style="list-style-type: none"> <li>1. Crosspoint Connect (1=connected, 0=no connection)</li> <li>2. Output Enable—B7 (see Table 9)</li> <li>3. Output Enable—B8 (see Table 9)</li> <li>4. Output Data Source—B9 (0=Flow-through, 1=registered)</li> <li>5. Output Clock Select—BA (0=Global Clock, 1=Next Neighbor)</li> <li>6. State of Broadcast bit</li> <li>7. State of the RCE bit</li> </ol> <p>NOTE: This instruction does not increment the JTAG Address Register. This instruction also requires two DR cycles</p> |
| 0 1 1 0 | X  | X            | X         | X  | X  | X                     | Update the Crosspoint Array  | Update the programmed connection from the Loading SRAM to the Active SRAM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 0 1 1 1 | X  | X            | X         | X  | X  | X                     | Disconnect Input cell        | Disconnect the Crosspoint connections from the Input address specified in the JTAG Address Register.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |



**Table 8 JTAG Instructions (Continued)**

| I [3:0] | BB | BA | B9 | B8 | B7 | A6-A0          | Instruction                              | Description                                                                                                                                                                                                                                                                                                                                                  |
|---------|----|----|----|----|----|----------------|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 0 0 0 | X  | X  | X  | X  | X  | Output Address | Disconnect Input and Output              | Disconnect the Crosspoint cell at the Input location specified at the JTAG Address Register and the Output location specified in the Disconnect JTAG instruction (A6-A0).<br>All other connections from the same input address or to the same output address remain the same.                                                                                |
| 1 0 0 1 | X  | X  | X  | X  | X  | Output Address | Connect with ImpliedDisconnect           | Connects the Crosspoint cell at the Input location specified on the JTAG Address Register and the output location specified in the Connect JTAG instruction (A6-A0).<br>All other connections from the same Input address or the same Output address are set to no-connects.<br>NOTE: This instruction increments the JTAG Address Register (Input address). |
| 1 0 1 0 | X  | X  | X  | X  | X  | Output Address | Connect—no ImpliedDisconnect             | Connects the Crosspoint cell at the Input address specified in the JTAG Address Register and the Output address specified in the Connect JTAG instruction (A6-A0).<br>All connections to the same output address are set to “no connect” while all other connections from the same input remain the same as before.                                          |
| 1 0 1 1 | X  | X  | X  | X  | X  | Input Address  | Set the JTAG Address Register            | Sets the 7-bit JTAG Address Register with the 7-bit address (A6-A0) of the JTAG Instruction Register. The 7-bit address of the JTAG Address Register becomes the Input port address for Crosspoint Access.                                                                                                                                                   |
| 1 1 0 0 | X  | X  | X  | X  | X  | X              | Device ID out                            | Serialize the device ID and revision history out to TDO. ID for the OCX256 is <b>0x0000C89F</b>                                                                                                                                                                                                                                                              |
| 1 1 0 1 | X  | X  | X  | X  | X  | X              | Reset Output Buffer and Crosspoint Array | Resets the Crosspoint Array to no-connects. Sets the Output buffer to Flow-through mode with Output Enabled. The device ID is serialized to TDO.                                                                                                                                                                                                             |
| 1 1 1 0 | X  | X  | X  | X  | X  | X              | Set RCE Bit                              | Sets the RCE bit of the Mode Control Register with the JTAG instruction bit A0.<br>To turn ON the RCE bit, encode bit A0 to 1.<br>To turn OFF the RCE bit, encode bit A0 to 0.                                                                                                                                                                               |
| 1 1 1 1 | X  | X  | X  | X  | X  | X              | Bypass                                   | Places device in a mode to pass TDI data to TDO with one clock delay. Used for programming and testing devices through serial connected JTAG controls.                                                                                                                                                                                                       |



**Table 9 Programming an Output using JTAG**

| BA, B9, B8, B7                     | Signal/Function                                                                                                                                                                              |
|------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BA                                 | <b>Clock Select:</b><br>0 = Global Clock<br>1 = Next Neighbor                                                                                                                                |
| B9                                 | <b>Output Mode:</b><br>0 = Flow-through (OP)<br>1 = Registered (RO)                                                                                                                          |
| B8, B7<br>0,0<br>0,1<br>1,0<br>1,1 | <b>Output Enable:</b><br>Output enabled (ON) – this is the default state at reset<br>Output disabled (OFF)<br>Output controlled by OE (active high)<br>Output controlled by OE# (active low) |

**Table 10 Number of JTAG Cycles and Configuration Time**

| Operation                                                                            | OCX256      |
|--------------------------------------------------------------------------------------|-------------|
|                                                                                      | JTAG Cycles |
| JTAG Reset Sequence (TMS = “11111”)                                                  | 7           |
| Enable or Disable RapidConfigure                                                     | 28          |
| Change attributes of ONE Output Port                                                 | 28          |
| Change attributes of ALL Output Ports                                                | 3,584       |
| Reset JTAG Controller + Reset ALL Output Ports + Clear ALL SRAM cells                | 35          |
| Connect or disconnect two Ports                                                      | 56          |
| Configure Entire Switch Matrix                                                       | 462,336     |
| Completely Configure the Device (All Output Ports and All Switch Matrix Connections) | 456,920     |

## 1.5 ImpliedDisconnect

ImpliedDisconnect is a feature that provides the ability to make fast switch connection changes. When using the instruction “Connect, without ImpliedDisconnect” all other connections to the specified output are set to “no connect”. However, the specified input remains connected to any output that it was connected to before.

When using the instruction “Connect, with ImpliedDisconnect” all connections from the specified input and to the specified output are set to “no connect”.

Thus, a connection change, i.e. breaking an existing connection and then making a new one, can be accomplished in one RapidConfigure cycle.



## 1.6 Device Reset Options

The power-on reset, RapidConfigure reset, hardware reset, and JTAG reset functions will program the output buffers to flow-through mode (with Global Clock selected), and Output Enabled (ON). JTAG can be reset via the TRST# pin or by clocking five consecutive one to the TMS pin. The hardware reset pin can be done accomplished through the HW\_RST# pin (active low). RC reset can be accomplished by applying the RC instruction 1101 to the RCI[3:0] pins.

**Table 11 Device Reset Options**

| Programming Interface       | Reset Method                                 | Output Ports | Switch Matrix | RCE Mode Control  | JTAG TAP         |
|-----------------------------|----------------------------------------------|--------------|---------------|-------------------|------------------|
| <b>Hardware Reset</b>       | Power-on Reset                               | OP           | NC            | 1<br>(RC Enabled) | TLR <sup>1</sup> |
|                             | HW_RST# (low pulse)                          | OP           | NC            | 1<br>(RC Enabled) | TLR              |
| <b>JTAG Reset</b>           | 1. Low Pulse on TRST#                        | Unchanged    | Unchanged     | Unchanged         | TLR              |
|                             | 2. TMS high for 5 TCLK cycles                | Unchanged    | Unchanged     | Unchanged         | TLR              |
|                             | 3. Device Reset (instruction 1101)           | OP           | NC            | 1<br>(RC Enabled) | TLR              |
|                             | 4. Reset Crosspoint Array (instruction 0010) | Unchanged    | NC            | Unchanged         | Unchanged        |
| <b>RapidConfigure Reset</b> | 1. Device reset (instruction 1101)           | OP           | NC            | 1<br>(RC Enabled) | Unchanged        |
|                             | 2. Reset Crosspoint Array (instruction 0010) | Unchanged    | NC            | Unchanged         | Unchanged        |

1. TLR = Test Logic Reset state.



## 2. Pin Description

Table 12 OCX256 Pin Description

| Pin Name                              | # of Pins | Type               | Description                                                      |
|---------------------------------------|-----------|--------------------|------------------------------------------------------------------|
| INPP[127:0]                           | 128       | Input              | Non-inverting differential input signals                         |
| INN[127:0]                            | 128       | Input              | Inverting differential input signals                             |
| OUTP[127:0]                           | 128       | Output             | Non-inverting differential input signals                         |
| OUTN[127:0]                           | 128       | Output             | Inverting differential input signals                             |
| CLKP                                  | 1         | Input              | Non-inverting differential Global Clock                          |
| CLKN                                  | 1         | Input              | Inverting differential Global Clock                              |
| OE#                                   | 1         | Input              | Global Output Enable                                             |
| HW_RST#                               | 1         | Input              | Hardware Reset                                                   |
| UPDATE#                               | 1         | Input              | Global Update                                                    |
| <b>RC Pins</b>                        |           |                    |                                                                  |
| RCA[6:0]                              | 7         | Input              | RapidConfigure Address A                                         |
| RCB[6:0]                              | 7         | Input              | RapidConfigure Address B                                         |
| RCO[4:0]                              | 5         | Output             | RapidConfigure Readback                                          |
| RCI[3:0]                              | 4         | Input              | RapidConfigure Instruction Bits                                  |
| RC_CLK#                               | 1         | Input              | RapidConfigure Clock                                             |
| RC_EN#                                | 1         | Input              | RapidConfigure Cycle Enable                                      |
| <b>JTAG Pins</b>                      |           |                    |                                                                  |
| TCK                                   | 1         | Input              | JTAG Test Clock                                                  |
| TMS                                   | 1         | Input              | JTAG Test Mode Select                                            |
| TDI                                   | 1         | Input              | JTAG Test Data In                                                |
| TRST#                                 | 1         | Input              | JTAG Test Reset                                                  |
| TDO                                   | 1         | Output             | JTAG Test Data Out                                               |
| <b>Power and Ground Pins</b>          |           |                    |                                                                  |
| V <sub>DD</sub> -CORE                 | 100       | 2.5V Power         | Core Voltage                                                     |
| V <sub>DD</sub> -PAD <sup>(2)</sup>   | 15        | 2.5V or 3.3V Power | Differential Output Buffer Voltage                               |
| V <sub>DD</sub> -IN <sup>(1, 3)</sup> | 16        | 3.3V Power         | LVTTL Control pins Voltage and Differential Input Buffer Voltage |
| V <sub>SS</sub>                       | 111       | Ground             | Ground                                                           |

### NOTES:

1. Dedicated differential input buffers can receive both LVDS and LVPECL voltage levels using 3.3V supply.
2. V<sub>DD</sub>-PAD is 2.5V for OCX256L or 3.3V for OCX256P.
3. The LVTTL control, JTAG pins, and differential input ports are 3.3V—they are not 5V tolerant.
4. The differential output pins powered from 2.5V are 3.3V tolerant.



### 3. Differential I/O Standards

The OCX256 supports the two most popular differential signaling standards: Low Voltage Differential Signaling (LVDS) and Low Voltage Positive Emitter Coupled Logic (LVPECL).

LVDS is typically used in communication systems as high speed, low noise point-to-point links. The OCX256 conforms to the ANSI/TIA/EIA-644 standard covering electrical specifications for output drivers and receiver inputs.

LVPECL is commonly used in video switching applications or those designs requiring transmission of high-speed clock signals.

#### 3.1 LVDS

LVDS is a differential signaling standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage or a board termination voltage is not required. LVDS requires the use of two pins per input or output. The OCX256L supports LVDS signalling. Integrated Output Attenuator resistors produce the required LVDS Output swing while providing a 100 ohm output impedance to minimize return reflections.

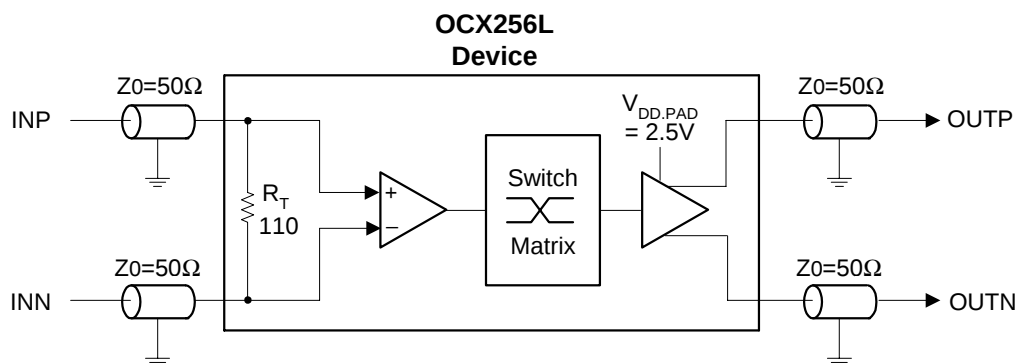


Figure 7 OCX256L LVDS Signal Circuit



## 3.2 LVPECL

LVPECL is another differential signaling standard that specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage or a board termination voltage is not required. The OCX256P supports LVPECL signalling. Integrated Output Attenuator resistors produce the required LVPECL Output swing while providing a 100 ohm output impedance to minimize return reflections.

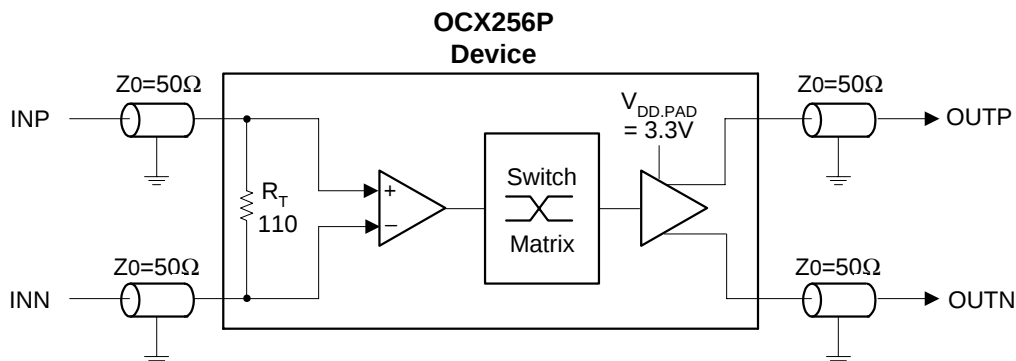


Figure 8 OCX256P LVPECL Signal Circuit



## 4. Electrical Specifications

### 4.1 Absolute Maximum Ratings

Table 13 Absolute Maximum Ratings<sup>1</sup>

| Symbol             | Parameter                             | Limits                      | Units |
|--------------------|---------------------------------------|-----------------------------|-------|
| $V_{DD,CORE}$      | Supply Voltage (core)                 | -0.3 to +3.0                | V     |
| $V_{DD,IN}$        | Supply Voltage (inputs)               | -0.3 to +3.6                | V     |
| $V_{DD,PAD}$       | Supply Voltage (differential outputs) | -0.3 to +3.6                | V     |
| $V_{IN}^{(2)}$     | Input Voltage                         | -0.3 to +3.6 <sup>(3)</sup> | V     |
| $T_J$              | Junction Temperature                  | +150                        | °C    |
| $T_{STG}$          | Storage Temperature                   | -65 to +150                 | °C    |
| $P_{MAX}$          | Maximum Power Dissipation             | 8.6                         | W     |
| ESD <sup>(6)</sup> | Electrostatic Discharge               | 2000                        | V     |

### 4.2 Recommended Operating Conditions

Table 14 Recommended Operating Conditions

| Symbol             | Parameter                                                              | Limits                          | Units |
|--------------------|------------------------------------------------------------------------|---------------------------------|-------|
| $V_{DD,CORE}$      | Supply Voltage (core)                                                  | +2.375 to +2.625                | V     |
| $V_{DD,PAD}^{(4)}$ | Supply Voltage (differential output buffers)                           | 3.3V $\pm$ 10% or 2.5V $\pm$ 5% | V     |
| $V_{DD,IN}$        | Supply Voltage (inputs)                                                | +3.0 to +3.6                    | V     |
| $T_A$              | Operating Temperature: Commercial<br>Operating Temperature: Industrial | 0 to +70<br>-40 to +85          | °C    |

### 4.3 Pin Capacitance

Table 15 Pin Capacitance<sup>5</sup>

| Symbol    | Parameter              | Max | Units |
|-----------|------------------------|-----|-------|
| $C_{PIN}$ | Signal Pin Capacitance | 10  | pF    |

1. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. A maximum undershoot of 2V for a maximum duration of 20 ns is acceptable. Overshoot to 3.6V is acceptable.
3. All inputs are 3.3V tolerant with the  $V_{DD}$  pin at 2.5V or 3.3V.
4. Note that min and max values for  $V_{DD}$  for differential outputs are I/O Standard dependent.
5. Capacitance measured at 25°C. Sample tested only.
6. Measured using Human Body Model.



#### 4.4 DC Electrical Specifications

( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD,IN} = 3.3\text{V} \pm 10\%$ ,  $V_{DD,CORE} = 2.5\text{V} \pm 5\%$ )

**Table 16 LVTTTL DC Electrical Specifications**

| Symbol                   | Parameter                                        | Conditions                                            | Min  | Max                | Units         |
|--------------------------|--------------------------------------------------|-------------------------------------------------------|------|--------------------|---------------|
| $V_{IH}$                 | High-level Input                                 | Ports are 3.3V tolerant                               | 2.0  | 3.6                | V             |
| $V_{IL}$                 | Low-level Input                                  | Ports are 3.3V tolerant                               | -0.3 | 0.8                | V             |
| $V_{OH}$                 | High-level Output                                | $V_{DD,PAD} = \text{Min}$<br>$I_{OH} = -4\text{mA}$   | 2.4  | $V_{DD,PAD} + 0.3$ | V             |
| $V_{OL}$                 | Low-level Output                                 | $V_{DD,PAD} = \text{Min}$<br>$I_{OL} = 8\text{mA}$    |      | 0.4                | V             |
| $IL_{IH}, IL_{IL}^{(1)}$ | Input Pin Leakage Current <sup>(2)</sup>         | $V_{DD,IN} = \text{Max}$<br>$0.0 < I_n < V_{DD,PAD}$  |      | +5<br>-50          | $\mu\text{A}$ |
| $IL_{OZ}$                | Tristate Leakage Output OFF State <sup>(2)</sup> | $V_{DD,PAD} = \text{Max}$<br>$0.0 < I_n < V_{DD,PAD}$ |      | +5<br>-5           | $\mu\text{A}$ |
| <b>Power</b>             |                                                  |                                                       |      |                    |               |
| $P_{DDQ}^{(3)}$          | Quiescent Power                                  | All $V_{DD} = \text{Max}$                             |      | 0.7                | W             |

**Table 17 OCX256L (LVDS) DC Electrical Specifications ( $V_{DD,PAD} = 2.5\text{V}$ )**

| DC Parameter                               | Min       | Typ       | Max       | Units    |
|--------------------------------------------|-----------|-----------|-----------|----------|
| Output High Voltage for OUTP and OUTN      |           |           | 1.6       | V        |
| Output Low Voltage for OUTP and OUTN       | 0.90      |           |           | V        |
| Differential Output Voltage <sup>(4)</sup> | $\pm 250$ | $\pm 350$ | $\pm 450$ | mV       |
| Output Common-Mode Voltage                 | 1.125     | 1.25      | 1.375     | V        |
| Differential Input Voltage                 | $\pm 100$ | $\pm 350$ |           | mV       |
| Input Common-Mode Voltage                  | 0.25      | 1.25      | 2.25      | V        |
| $Z_{IN}$ — Termination Impedance           | 88        |           | 132       | $\Omega$ |

1. All LVTTTL input pins have pull-up resistors.
2. Input leakage only valid when both positive and negative inputs/outputs area equal (i.e. both high or both low)
3. See section 6 for dynamic power consumption calculation.
4. Maximum capacitive load is 12 pF.

**Table 18 OCX256P (LVPECL) DC Electrical Specifications ( $V_{DD,PAD} = 3.3\text{V}$ )**

| Symbol          | DC Parameters               | Min                    | Max                    | Units    |
|-----------------|-----------------------------|------------------------|------------------------|----------|
| $V_{IN\_DIFF}$  | Input Differential Voltage  | $\pm 100$              |                        | mV       |
| $V_{IN\_COM}$   | Input Common Mode Voltage   | 0.25                   | 2.25                   | V        |
| $V_{OUT\_DIFF}$ | Output Differential Voltage | $\pm 350$              | $\pm 650$              | mV       |
| $V_{OUT\_COM}$  | Output Common Mode Voltage  | $\frac{V_{DD,PAD}}{2}$ | $\frac{V_{DD,PAD}}{2}$ | V        |
| $Z_{IN}$        | Termination Impedance       | 80                     | 120                    | $\Omega$ |

The  $V_{OH}$  levels are 200mV below LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The above table summarizes the DC output specifications of LVPECL.



## 4.5 AC Electrical Specifications

( $V_{DD-IN} = 3.3V \pm 10\%$ ,  $V_{DD-CORE} = 2.5V \pm 5\%$ )

**Table 19 AC Electrical Specifications**

| Symbol                           | Parameter                                                | 0°C to 70°C |     | -40°C to +85°C |     | Units |
|----------------------------------|----------------------------------------------------------|-------------|-----|----------------|-----|-------|
|                                  |                                                          | Min         | Max | Min            | Max |       |
| $R_{DATA}$                       | NRZ Data Rate <sup>(1)</sup>                             |             | 667 |                | 667 | Mb/s  |
| $F_{RO}$                         | Registered Output Clock Frequency <sup>(1)</sup>         |             | 333 |                | 333 | MHz   |
| $t_{W\_RO}$                      | Registered Clock Pulse Width, High or Low <sup>(1)</sup> | 2           |     | 2              |     | ns    |
| $t_{S\_RO}$                      | Registered Output Setup Time to Clock                    | 4           |     | 4              |     | ns    |
| $t_{H\_RO}$                      | Registered Output Clock to Hold Data                     | 0           |     | 0              |     | ns    |
| $t_{CO\_RO}$                     | Registered Output Clock to Data Out Valid                |             | 2.5 |                | 2.5 | ns    |
| $t_{PHL}$ , $t_{PLH}$            | One Way Signal Propagation Delay, Fanout = 1             |             | 5.5 |                | 6.5 | ns    |
| $t_{W+}$                         | Input Flow-through Positive Pulse Width                  | 1.5         |     | 1.5            |     | ns    |
| $t_{W-}$                         | Input Flow-through Negative Pulse Width                  | 1.5         |     | 1.5            |     | ns    |
| $t_{DCD+}$ , $t_{DCD-}$          | Duty Cycle Distortion                                    |             | 0.5 |                | 0.6 | ns    |
| $t_{JITTER}$                     | Output Jitter                                            |             | 0.5 |                | 0.5 | ns    |
| $t_{SK}$                         | Skew between Output Ports <sup>(1)</sup>                 |             | 0.5 |                | 0.6 | ns    |
| $t_{PHZ\_OT}$ ,<br>$t_{PLZ\_OT}$ | Output Enable to Valid Data                              |             | 3   |                | 3   | ns    |
| $t_{PZH\_OT}$ ,<br>$t_{PZL\_OT}$ | Output Enable to High Z State                            |             | 3   |                | 3   | ns    |
| $t_{RC}$                         | RapidConfigure Clock Period                              | 12          |     | 12             |     | ns    |
| $t_{W+\_RC}$ ,<br>$t_{W-\_RC}$   | RapidConfigure Clock Pulse Width                         | 5           |     | 5              |     | ns    |
| $t_{S\_RC}$                      | RapidConfigure Address Setup to RC_CLK#                  | 3           |     | 4              |     | ns    |
| $t_{H\_RC}$                      | RapidConfigure Address and Enable Hold Time to RC_CLK#   | 3           |     | 4              |     | ns    |
| $t_{P\_UD}$                      | Update of Crosspoint to Data Out                         |             | 10  |                | 10  | ns    |
| $f_{JTAG}$                       | JTAG Clock Frequency (TCK)                               |             | 20  |                | 20  | MHz   |
| $t_{W\_JTAG}$                    | JTAG Clock Pulse Width (TCK) @ 20MHz cycle               | 20          | 30  | 20             | 30  | ns    |
| $t_{S\_JTAG}$                    | JTAG Setup Time                                          | 4           |     | 4              |     | ns    |
| $t_{H\_JTAG}$                    | JTAG Hold Time                                           | 0           |     | 0              |     | ns    |
| $t_{P\_JTAG}$                    | JTAG Clock to Output Data Valid (TDO)                    |             | 20  |                | 20  | ns    |

### NOTES:

1. These parameters are guaranteed but not tested in production.



## 4.6 Timing Diagrams

**Note** – For the purpose of clarity, the timing diagrams within this data sheet are conceptual representations only and do not show actual circuit implementation.

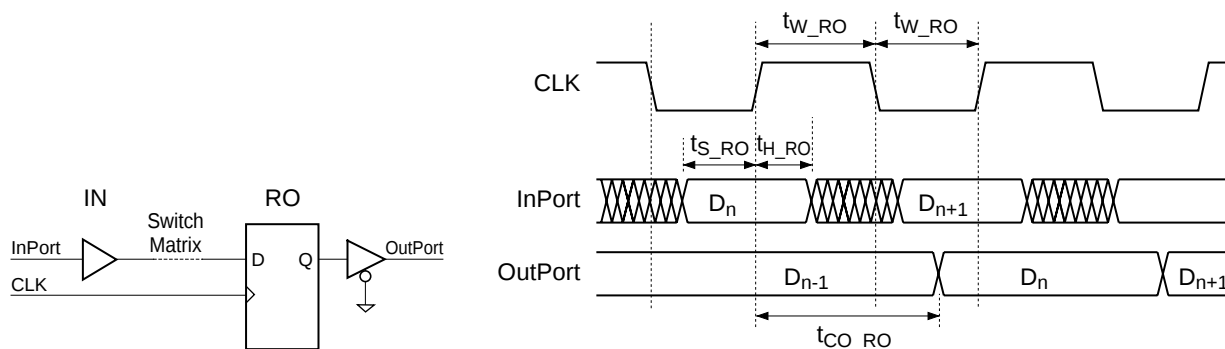


Figure 9 Registered Output Mode Timing

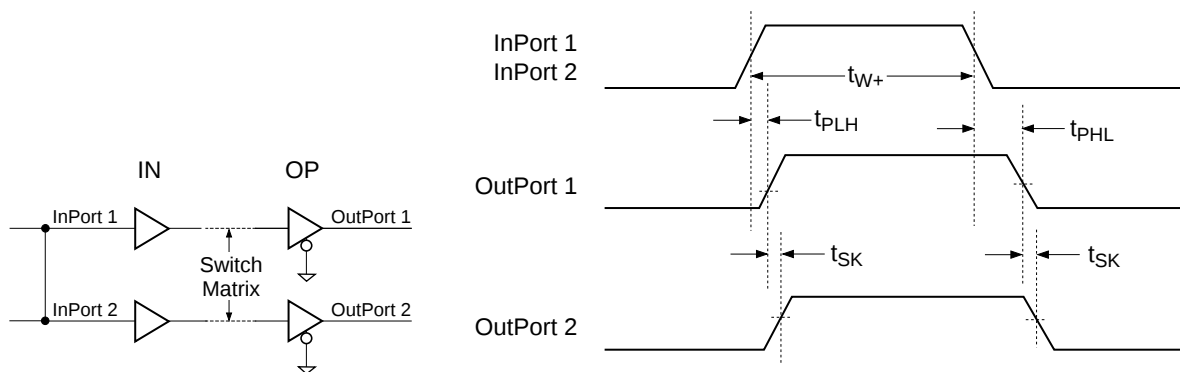


Figure 10 Flow-Through Mode Timing

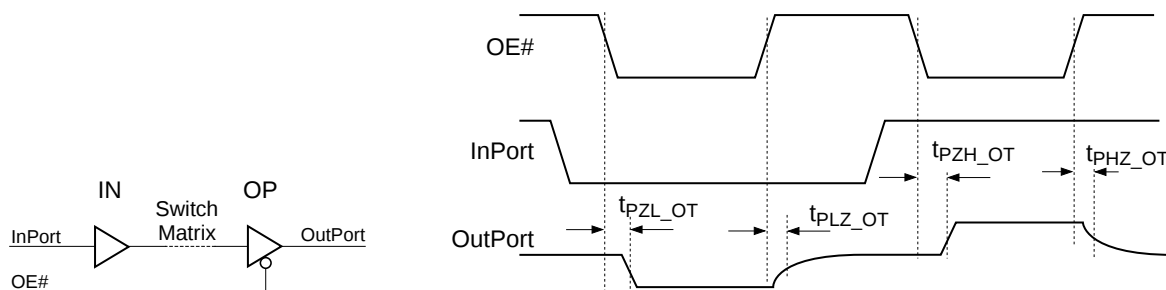
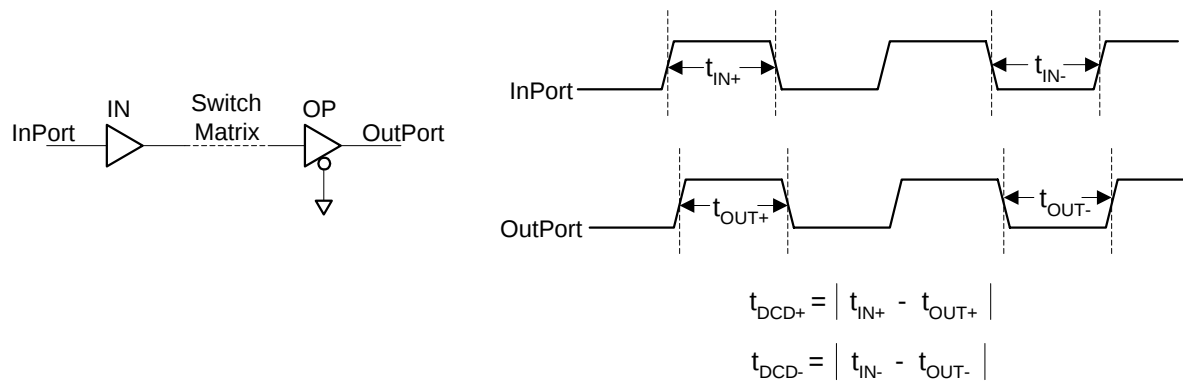
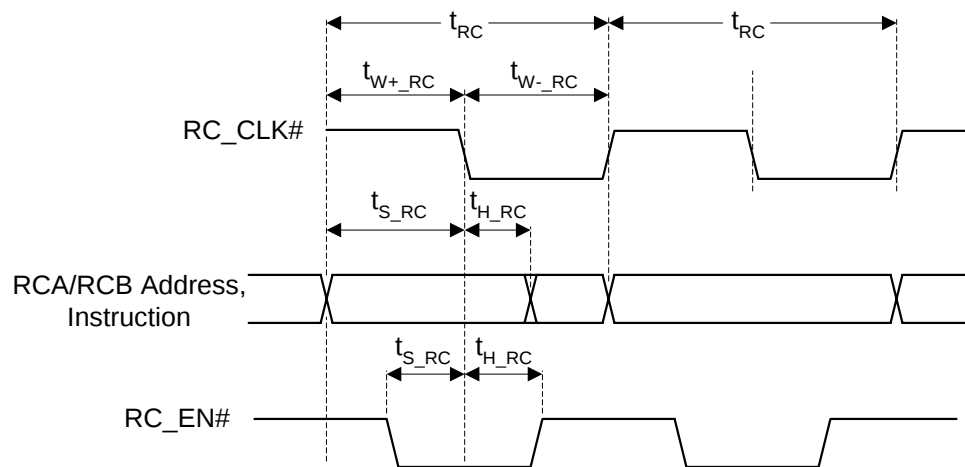


Figure 11 Output Enable Timing



**Figure 12 Duty Cycle Distortion**



**Figure 13 RapidConfigure Write Cycle**

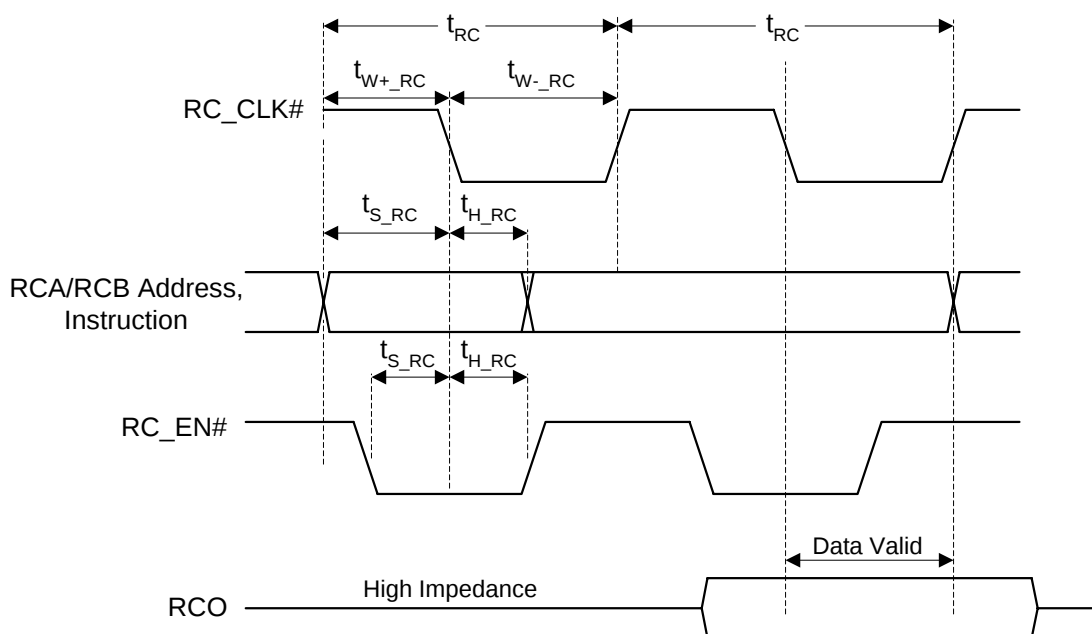


Figure 14 RapidConfigure Read Cycle

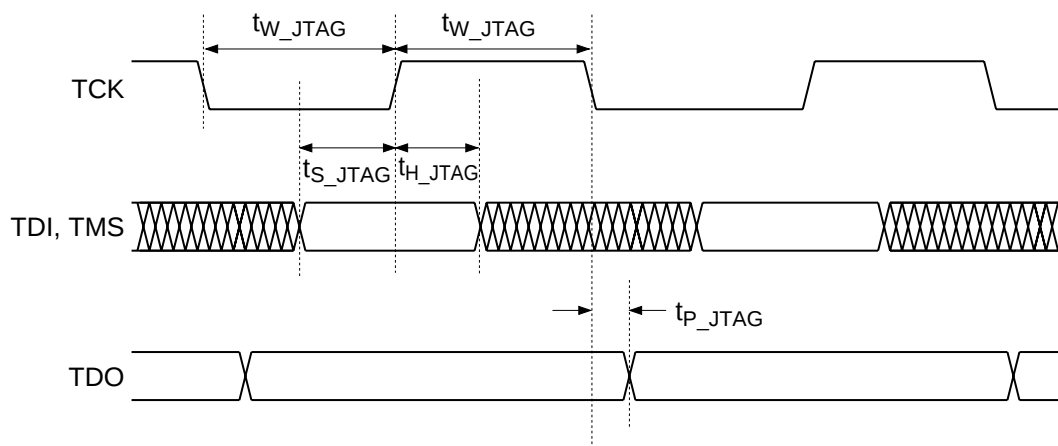


Figure 15 JTAG Timing

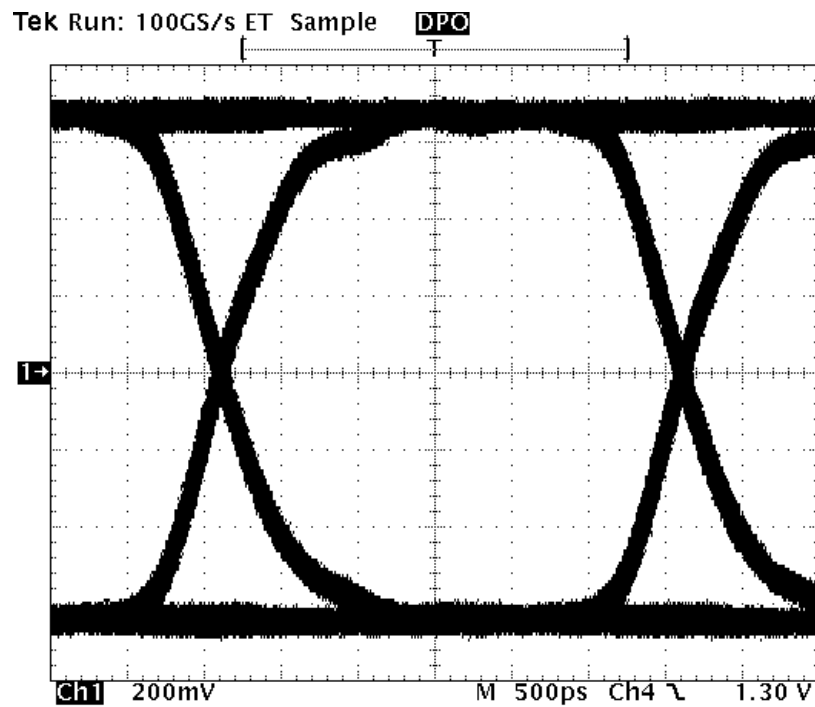


Figure 16 Typical Performance at 667 Mb/s with PRBS Data



## 5. Package and Pinout

### 5.1 Package Pinout

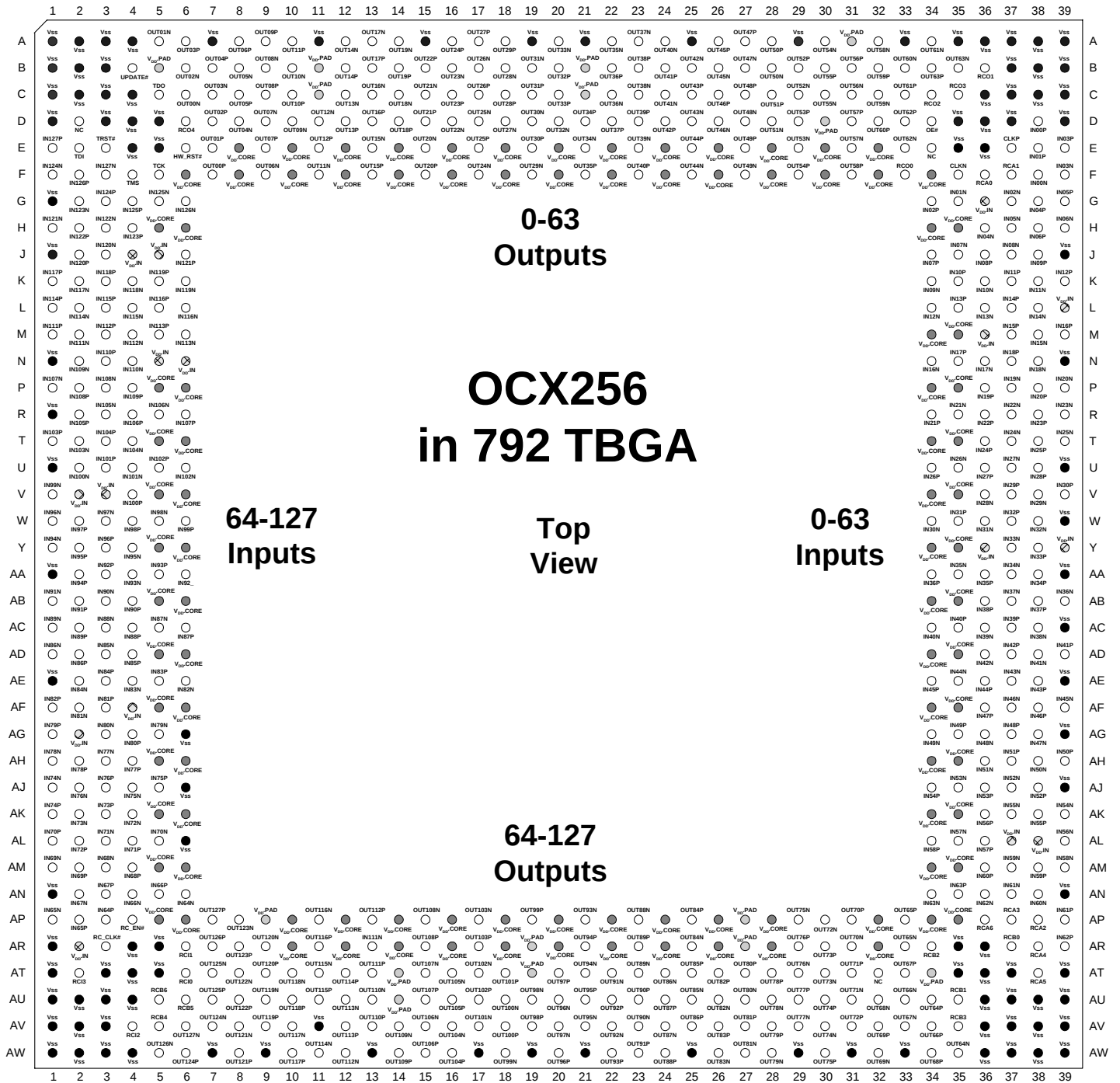


Figure 17 OCX256 Package Pinout



## 5.2 Pinout by Ball Sequence

**Table 20 OCX256 Pinout By Ball Sequence**

| Ball # | Ball Name            | Ball # | Ball Name            | Ball # | Ball Name            | Ball # | Ball Name            | Ball # | Ball Name             | Ball # | Ball Name             |
|--------|----------------------|--------|----------------------|--------|----------------------|--------|----------------------|--------|-----------------------|--------|-----------------------|
| A1     | V <sub>SS</sub>      | B1     | V <sub>SS</sub>      | C1     | V <sub>SS</sub>      | D1     | V <sub>SS</sub>      | E1     | IN127P                | F1     | IN124N                |
| A2     | V <sub>SS</sub>      | B2     | V <sub>SS</sub>      | C2     | V <sub>SS</sub>      | D2     | NC                   | E2     | TDI                   | F2     | IN126P                |
| A3     | V <sub>SS</sub>      | B3     | V <sub>SS</sub>      | C3     | V <sub>SS</sub>      | D3     | V <sub>SS</sub>      | E3     | TRST#                 | F3     | IN127N                |
| A4     | V <sub>SS</sub>      | B4     | UPDATE#              | C4     | V <sub>SS</sub>      | D4     | V <sub>SS</sub>      | E4     | V <sub>SS</sub>       | F4     | TMS                   |
| A5     | OUT01N               | B5     | V <sub>DD</sub> .PAD | C5     | TDO                  | D5     | V <sub>SS</sub>      | E5     | V <sub>SS</sub>       | F5     | TCK                   |
| A6     | OUT03P               | B6     | OUT02N               | C6     | OUT00N               | D6     | RCO4                 | E6     | HW_RST#               | F6     | V <sub>DD</sub> .CORE |
| A7     | V <sub>SS</sub>      | B7     | OUT04P               | C7     | OUT03N               | D7     | OUT02P               | E7     | OUT01P                | F7     | OUT00P                |
| A8     | OUT06P               | B8     | OUT05N               | C8     | OUT05P               | D8     | OUT04N               | E8     | V <sub>DD</sub> .CORE | F8     | V <sub>DD</sub> .CORE |
| A9     | OUT09P               | B9     | OUT08N               | C9     | OUT08P               | D9     | OUT07N               | E9     | OUT07P                | F9     | OUT06N                |
| A10    | OUT11P               | B10    | OUT10N               | C10    | OUT10P               | D10    | OUT09N               | E10    | V <sub>DD</sub> .CORE | F10    | V <sub>DD</sub> .CORE |
| A11    | V <sub>SS</sub>      | B11    | V <sub>DD</sub> .PAD | C11    | V <sub>DD</sub> .PAD | D11    | OUT12N               | E11    | OUT12P                | F11    | OUT11N                |
| A12    | OUT14N               | B12    | OUT14P               | C12    | OUT13N               | D12    | OUT13P               | E12    | V <sub>DD</sub> .CORE | F12    | V <sub>DD</sub> .CORE |
| A13    | OUT17N               | B13    | OUT17P               | C13    | OUT16N               | D13    | OUT16P               | E13    | OUT15N                | F13    | OUT15P                |
| A14    | OUT19N               | B14    | OUT19P               | C14    | OUT18N               | D14    | OUT18P               | E14    | V <sub>DD</sub> .CORE | F14    | V <sub>DD</sub> .CORE |
| A15    | V <sub>SS</sub>      | B15    | OUT22P               | C15    | OUT21N               | D15    | OUT21P               | E15    | OUT20N                | F15    | OUT20P                |
| A16    | OUT24P               | B16    | OUT23N               | C16    | OUT23P               | D16    | OUT22N               | E16    | V <sub>DD</sub> .CORE | F16    | V <sub>DD</sub> .CORE |
| A17    | OUT27P               | B17    | OUT26N               | C17    | OUT26P               | D17    | OUT25N               | E17    | OUT25P                | F17    | OUT24N                |
| A18    | OUT29P               | B18    | OUT28N               | C18    | OUT28P               | D18    | OUT27N               | E18    | V <sub>DD</sub> .CORE | F18    | V <sub>DD</sub> .CORE |
| A19    | V <sub>SS</sub>      | B19    | OUT31N               | C19    | OUT31P               | D19    | OUT30N               | E19    | OUT30P                | F19    | OUT29N                |
| A20    | OUT33N               | B20    | OUT32P               | C20    | OUT33P               | D20    | OUT32N               | E20    | V <sub>DD</sub> .CORE | F20    | V <sub>DD</sub> .CORE |
| A21    | V <sub>SS</sub>      | B21    | V <sub>DD</sub> .PAD | C21    | V <sub>DD</sub> .PAD | D21    | OUT34P               | E21    | OUT34N                | F21    | OUT35P                |
| A22    | OUT35N               | B22    | OUT36P               | C22    | OUT36N               | D22    | OUT37P               | E22    | V <sub>DD</sub> .CORE | F22    | V <sub>DD</sub> .CORE |
| A23    | OUT37N               | B23    | OUT38P               | C23    | OUT38N               | D23    | OUT39P               | E23    | OUT39N                | F23    | OUT40P                |
| A24    | OUT40N               | B24    | OUT41P               | C24    | OUT41N               | D24    | OUT42P               | E24    | V <sub>DD</sub> .CORE | F24    | V <sub>DD</sub> .CORE |
| A25    | V <sub>SS</sub>      | B25    | OUT42N               | C25    | OUT43P               | D25    | OUT43N               | E25    | OUT44P                | F25    | OUT44N                |
| A26    | OUT45P               | B26    | OUT45N               | C26    | OUT46P               | D26    | OUT46N               | E26    | V <sub>DD</sub> .CORE | F26    | V <sub>DD</sub> .CORE |
| A27    | OUT47P               | B27    | OUT47N               | C27    | OUT48P               | D27    | OUT48N               | E27    | OUT49P                | F27    | OUT49N                |
| A28    | OUT50P               | B28    | OUT50N               | C28    | OUT51P               | D28    | OUT51N               | E28    | V <sub>DD</sub> .CORE | F28    | V <sub>DD</sub> .CORE |
| A29    | V <sub>SS</sub>      | B29    | OUT52P               | C29    | OUT52N               | D29    | OUT53P               | E29    | OUT53N                | F29    | OUT54P                |
| A30    | OUT54N               | B30    | OUT55P               | C30    | OUT55N               | D30    | V <sub>DD</sub> .PAD | E30    | V <sub>DD</sub> .CORE | F30    | V <sub>DD</sub> .CORE |
| A31    | V <sub>DD</sub> .PAD | B31    | OUT56P               | C31    | OUT56N               | D31    | OUT57P               | E31    | OUT57N                | F31    | OUT58P                |
| A32    | OUT58N               | B32    | OUT59P               | C32    | OUT59N               | D32    | OUT60P               | E32    | V <sub>DD</sub> .CORE | F32    | V <sub>DD</sub> .CORE |
| A33    | V <sub>SS</sub>      | B33    | OUT60N               | C33    | OUT61P               | D33    | OUT62P               | E33    | OUT62N                | F33    | RCO0                  |
| A34    | OUT61N               | B34    | OUT63P               | C34    | RCO2                 | D34    | OE#                  | E34    | NC                    | F34    | V <sub>DD</sub> .CORE |
| A35    | V <sub>SS</sub>      | B35    | OUT63N               | C35    | RCO3                 | D35    | V <sub>SS</sub>      | E35    | V <sub>SS</sub>       | F35    | CLKN                  |
| A36    | V <sub>SS</sub>      | B36    | RCO1                 | C36    | V <sub>SS</sub>      | D36    | V <sub>SS</sub>      | E36    | V <sub>SS</sub>       | F36    | RCA0                  |
| A37    | V <sub>SS</sub>      | B37    | V <sub>SS</sub>      | C37    | V <sub>SS</sub>      | D37    | V <sub>SS</sub>      | E37    | CLKP                  | F37    | RCA1                  |
| A38    | V <sub>SS</sub>      | B38    | V <sub>SS</sub>      | C38    | V <sub>SS</sub>      | D38    | IN00P                | E38    | IN01P                 | F38    | IN00N                 |
| A39    | V <sub>SS</sub>      | B39    | V <sub>SS</sub>      | C39    | V <sub>SS</sub>      | D39    | V <sub>SS</sub>      | E39    | IN03P                 | F39    | IN03N                 |



# OCX256 Crosspoint Switch—Advanced Data Sheet

Table 20 OCX256 Pinout By Ball Sequence (Continued)

| Ball # | Ball Name           | Ball # | Ball Name             | Ball # | Ball Name           | Ball # | Ball Name | Ball # | Ball Name           | Ball # | Ball Name             |
|--------|---------------------|--------|-----------------------|--------|---------------------|--------|-----------|--------|---------------------|--------|-----------------------|
| G1     | V <sub>SS</sub>     | H1     | IN121N                | J1     | V <sub>SS</sub>     | K1     | IN117P    | L1     | IN114P              | M1     | IN111P                |
| G2     | IN123N              | H2     | IN122P                | J2     | IN120P              | K2     | IN117N    | L2     | IN114N              | M2     | IN111N                |
| G3     | IN124P              | H3     | IN122N                | J3     | IN120N              | K3     | IN118P    | L3     | IN115P              | M3     | IN112P                |
| G4     | IN125P              | H4     | IN123P                | J4     | V <sub>DD</sub> .IN | K4     | IN118N    | L4     | IN115N              | M4     | IN112N                |
| G5     | IN125N              | H5     | V <sub>DD</sub> .CORE | J5     | V <sub>DD</sub> .IN | K5     | IN119P    | L5     | IN116P              | M5     | IN113P                |
| G6     | IN126N              | H6     | V <sub>DD</sub> .CORE | J6     | IN121P              | K6     | IN119N    | L6     | IN116N              | M6     | IN113N                |
| G34    | IN02P               | H34    | V <sub>DD</sub> .CORE | J34    | IN07P               | K34    | IN09N     | L34    | IN12N               | M34    | V <sub>DD</sub> .CORE |
| G35    | IN01N               | H35    | V <sub>DD</sub> .CORE | J35    | IN07N               | K35    | IN10P     | L35    | IN13P               | M35    | V <sub>DD</sub> .CORE |
| G36    | V <sub>DD</sub> .IN | H36    | IN04N                 | J36    | IN08P               | K36    | IN10N     | L36    | IN13N               | M36    | V <sub>DD</sub> .IN   |
| G37    | IN02N               | H37    | IN05N                 | J37    | IN08N               | K37    | IN11P     | L37    | IN14P               | M37    | IN15P                 |
| G38    | IN04P               | H38    | IN06P                 | J38    | IN09P               | K38    | IN11N     | L38    | IN14N               | M38    | IN15N                 |
| G39    | IN05P               | H39    | IN06N                 | J39    | V <sub>SS</sub>     | K39    | IN12P     | L39    | V <sub>DD</sub> .IN | M39    | IN16P                 |

|     |                     |     |                       |     |                 |     |                       |     |                 |     |                       |
|-----|---------------------|-----|-----------------------|-----|-----------------|-----|-----------------------|-----|-----------------|-----|-----------------------|
| N1  | V <sub>SS</sub>     | P1  | IN107N                | R1  | V <sub>SS</sub> | T1  | IN103P                | U1  | V <sub>SS</sub> | V1  | IN99N                 |
| N2  | IN109N              | P2  | IN108P                | R2  | IN105P          | T2  | IN103N                | U2  | IN100N          | V2  | V <sub>DD</sub> .IN   |
| N3  | IN110P              | P3  | IN108N                | R3  | IN105N          | T3  | IN104P                | U3  | IN101P          | V3  | V <sub>DD</sub> .IN   |
| N4  | IN110N              | P4  | IN109P                | R4  | IN106P          | T4  | IN104N                | U4  | IN101N          | V4  | IN100P                |
| N5  | V <sub>DD</sub> .IN | P5  | V <sub>DD</sub> .CORE | R5  | IN106N          | T5  | V <sub>DD</sub> .CORE | U5  | IN102P          | V5  | V <sub>DD</sub> .CORE |
| N6  | V <sub>DD</sub> .IN | P6  | V <sub>DD</sub> .CORE | R6  | IN107P          | T6  | V <sub>DD</sub> .CORE | U6  | IN102N          | V6  | V <sub>DD</sub> .CORE |
| N34 | IN16N               | P34 | V <sub>DD</sub> .CORE | R34 | IN21P           | T34 | V <sub>DD</sub> .CORE | U34 | IN26P           | V34 | V <sub>DD</sub> .CORE |
| N35 | IN17P               | P35 | V <sub>DD</sub> .CORE | R35 | IN21N           | T35 | V <sub>DD</sub> .CORE | U35 | IN26N           | V35 | V <sub>DD</sub> .CORE |
| N36 | IN17N               | P36 | IN19P                 | R36 | IN22P           | T36 | IN24P                 | U36 | IN27P           | V36 | IN28N                 |
| N37 | IN18P               | P37 | IN19N                 | R37 | IN22N           | T37 | IN24N                 | U37 | IN27N           | V37 | IN29P                 |
| N38 | IN18N               | P38 | IN20P                 | R38 | IN23P           | T38 | IN25P                 | U38 | IN28P           | V38 | IN29N                 |
| N39 | V <sub>SS</sub>     | P39 | IN20N                 | R39 | IN23N           | T39 | IN25N                 | U39 | V <sub>SS</sub> | V39 | IN30P                 |

|     |                 |     |                       |      |                 |      |                       |      |                 |      |                       |
|-----|-----------------|-----|-----------------------|------|-----------------|------|-----------------------|------|-----------------|------|-----------------------|
| W1  | IN96N           | Y1  | IN94N                 | AA1  | V <sub>SS</sub> | AB1  | IN91N                 | AC1  | IN89N           | AD1  | IN86N                 |
| W2  | IN97P           | Y2  | IN95P                 | AA2  | IN94P           | AB2  | IN91P                 | AC2  | IN89P           | AD2  | IN86P                 |
| W3  | IN97N           | Y3  | IN96P                 | AA3  | IN92P           | AB3  | IN90N                 | AC3  | IN88N           | AD3  | IN85N                 |
| W4  | IN98P           | Y4  | IN95N                 | AA4  | IN93N           | AB4  | IN90P                 | AC4  | IN88P           | AD4  | IN85P                 |
| W5  | IN98N           | Y5  | V <sub>DD</sub> .CORE | AA5  | IN93P           | AB5  | V <sub>DD</sub> .CORE | AC5  | IN87N           | AD5  | V <sub>DD</sub> .CORE |
| W6  | IN99P           | Y6  | V <sub>DD</sub> .CORE | AA6  | IN92N           | AB6  | V <sub>DD</sub> .CORE | AC6  | IN87P           | AD6  | V <sub>DD</sub> .CORE |
| W34 | IN30N           | Y34 | V <sub>DD</sub> .CORE | AA34 | IN36P           | AB34 | V <sub>DD</sub> .CORE | AC34 | IN40N           | AD34 | V <sub>DD</sub> .CORE |
| W35 | IN31P           | Y35 | V <sub>DD</sub> .CORE | AA35 | IN35N           | AB35 | V <sub>DD</sub> .CORE | AC35 | IN40P           | AD35 | V <sub>DD</sub> .CORE |
| W36 | IN31N           | Y36 | V <sub>DD</sub> .IN   | AA36 | IN35P           | AB36 | IN38P                 | AC36 | IN39N           | AD36 | IN42N                 |
| W37 | IN32P           | Y37 | IN33N                 | AA37 | IN34N           | AB37 | IN37N                 | AC37 | IN39P           | AD37 | IN42P                 |
| W38 | IN32N           | Y38 | IN33P                 | AA38 | IN34P           | AB38 | IN37P                 | AC38 | IN38N           | AD38 | IN41N                 |
| W39 | V <sub>SS</sub> | Y39 | V <sub>DD</sub> .IN   | AA39 | V <sub>SS</sub> | AB39 | IN36N                 | AC39 | V <sub>SS</sub> | AD39 | IN41P                 |



**Table 20 OCX256 Pinout By Ball Sequence (Continued)**

| Ball # | Ball Name       | Ball # | Ball Name             | Ball # | Ball Name           | Ball # | Ball Name             | Ball # | Ball Name       | Ball # | Ball Name             |
|--------|-----------------|--------|-----------------------|--------|---------------------|--------|-----------------------|--------|-----------------|--------|-----------------------|
| AE1    | V <sub>SS</sub> | AF1    | IN82P                 | AG1    | IN79P               | AH1    | IN78N                 | AJ1    | IN74N           | AK1    | IN74P                 |
| AE2    | IN84N           | AF2    | IN81N                 | AG2    | V <sub>DD</sub> .IN | AH2    | IN78P                 | AJ2    | IN76N           | AK2    | IN73N                 |
| AE3    | IN84P           | AF3    | IN81P                 | AG3    | IN80N               | AH3    | IN77N                 | AJ3    | IN76P           | AK3    | IN73P                 |
| AE4    | IN83N           | AF4    | V <sub>DD</sub> .IN   | AG4    | IN80P               | AH4    | IN77P                 | AJ4    | IN75N           | AK4    | IN72N                 |
| AE5    | IN83P           | AF5    | V <sub>DD</sub> .CORE | AG5    | IN79N               | AH5    | V <sub>DD</sub> .CORE | AJ5    | IN75P           | AK5    | V <sub>DD</sub> .CORE |
| AE6    | IN82N           | AF6    | V <sub>DD</sub> .CORE | AG6    | V <sub>SS</sub>     | AH6    | V <sub>DD</sub> .CORE | AJ6    | V <sub>SS</sub> | AK6    | V <sub>DD</sub> .CORE |
| AE34   | IN45P           | AF34   | V <sub>DD</sub> .CORE | AG34   | IN49N               | AH34   | V <sub>DD</sub> .CORE | AJ34   | IN54P           | AK34   | V <sub>DD</sub> .CORE |
| AE35   | IN44N           | AF35   | V <sub>DD</sub> .CORE | AG35   | IN49P               | AH35   | V <sub>DD</sub> .CORE | AJ35   | IN53N           | AK35   | V <sub>DD</sub> .CORE |
| AE36   | IN44P           | AF36   | IN47P                 | AG36   | IN48N               | AH36   | IN51N                 | AJ36   | IN53P           | AK36   | IN56P                 |
| AE37   | IN43N           | AF37   | IN46N                 | AG37   | IN48P               | AH37   | IN51P                 | AJ37   | IN52N           | AK37   | IN55N                 |
| AE38   | IN43P           | AF38   | IN46P                 | AG38   | IN47N               | AH38   | IN50N                 | AJ38   | IN52P           | AK38   | IN55P                 |
| AE39   | V <sub>SS</sub> | AF39   | IN45N                 | AG39   | V <sub>SS</sub>     | AH39   | IN50P                 | AJ39   | V <sub>SS</sub> | AK39   | IN54N                 |

|      |                     |      |                       |      |                 |
|------|---------------------|------|-----------------------|------|-----------------|
| AL1  | IN70P               | AM1  | IN69N                 | AN1  | V <sub>SS</sub> |
| AL2  | IN72P               | AM2  | IN69P                 | AN2  | IN67N           |
| AL3  | IN71N               | AM3  | IN68N                 | AN3  | IN67P           |
| AL4  | IN71P               | AM4  | IN68P                 | AN4  | IN66N           |
| AL5  | IN70N               | AM5  | V <sub>DD</sub> .CORE | AN5  | IN66P           |
| AL6  | V <sub>SS</sub>     | AM6  | V <sub>DD</sub> .CORE | AN6  | IN64N           |
| AL34 | IN58P               | AM34 | V <sub>DD</sub> .CORE | AN34 | IN63N           |
| AL35 | IN57N               | AM35 | V <sub>DD</sub> .CORE | AN35 | IN63P           |
| AL36 | IN57P               | AM36 | IN60P                 | AN36 | IN62N           |
| AL37 | V <sub>DD</sub> .IN | AM37 | IN59N                 | AN37 | IN61N           |
| AL38 | V <sub>DD</sub> .IN | AM38 | IN59P                 | AN38 | IN60N           |
| AL39 | IN56N               | AM39 | IN58N                 | AN39 | V <sub>SS</sub> |



# OCX256 Crosspoint Switch—Advanced Data Sheet

**Table 20 OCX256 Pinout By Ball Sequence (Continued)**

| Ball # | Ball Name             | Ball # | Ball Name             | Ball # | Ball Name            | Ball # | Ball Name            | Ball # | Ball Name       | Ball # | Ball Name       |
|--------|-----------------------|--------|-----------------------|--------|----------------------|--------|----------------------|--------|-----------------|--------|-----------------|
| AP1    | IN65N                 | AR1    | V <sub>SS</sub>       | AT1    | V <sub>SS</sub>      | AU1    | V <sub>SS</sub>      | AV1    | V <sub>SS</sub> | AW1    | V <sub>SS</sub> |
| AP2    | IN65P                 | AR2    | V <sub>DD</sub> .IN   | AT2    | RCI3                 | AU2    | V <sub>SS</sub>      | AV2    | V <sub>SS</sub> | AW2    | V <sub>SS</sub> |
| AP3    | IN64P                 | AR3    | RC_CLK#               | AT3    | V <sub>SS</sub>      | AU3    | V <sub>SS</sub>      | AV3    | V <sub>SS</sub> | AW3    | V <sub>SS</sub> |
| AP4    | RC_EN#                | AR4    | V <sub>SS</sub>       | AT4    | V <sub>SS</sub>      | AU4    | V <sub>SS</sub>      | AV4    | RCI2            | AW4    | V <sub>SS</sub> |
| AP5    | V <sub>DD</sub> .CORE | AR5    | V <sub>SS</sub>       | AT5    | V <sub>SS</sub>      | AU5    | RCB6                 | AV5    | RCB4            | AW5    | OUT126N         |
| AP6    | V <sub>DD</sub> .CORE | AR6    | RCI1                  | AT6    | RCI0                 | AU6    | RCB5                 | AV6    | OUT127N         | AW6    | OUT124P         |
| AP7    | OUT127P               | AR7    | OUT126P               | AT7    | OUT125N              | AU7    | OUT125P              | AV7    | OUT124N         | AW7    | V <sub>SS</sub> |
| AP8    | OUT123N               | AR8    | OUT123P               | AT8    | OUT122N              | AU8    | OUT122P              | AV8    | OUT121N         | AW8    | OUT121P         |
| AP9    | V <sub>DD</sub> .PAD  | AR9    | OUT120N               | AT9    | OUT120P              | AU9    | OUT119N              | AV9    | OUT119P         | AW9    | V <sub>SS</sub> |
| AP10   | V <sub>DD</sub> .CORE | AR10   | V <sub>DD</sub> .CORE | AT10   | OUT118N              | AU10   | OUT118P              | AV10   | OUT117N         | AW10   | OUT117P         |
| AP11   | OUT116N               | AR11   | OUT116P               | AT11   | OUT115N              | AU11   | OUT115P              | AV11   | V <sub>SS</sub> | AW11   | OUT114N         |
| AP12   | V <sub>DD</sub> .CORE | AR12   | V <sub>DD</sub> .CORE | AT12   | OUT114P              | AU12   | OUT113N              | AV12   | OUT113P         | AW12   | OUT112N         |
| AP13   | OUT112P               | AR13   | OUT111N               | AT13   | OUT111P              | AU13   | OUT110N              | AV13   | OUT110P         | AW13   | V <sub>SS</sub> |
| AP14   | V <sub>DD</sub> .CORE | AR14   | V <sub>DD</sub> .CORE | AT14   | V <sub>DD</sub> .PAD | AU14   | V <sub>DD</sub> .PAD | AV14   | OUT109N         | AW14   | OUT109P         |
| AP15   | OUT108N               | AR15   | OUT108P               | AT15   | OUT107N              | AU15   | OUT107P              | AV15   | OUT106N         | AW15   | OUT106P         |
| AP16   | V <sub>DD</sub> .CORE | AR16   | V <sub>DD</sub> .CORE | AT16   | OUT105N              | AU16   | OUT105P              | AV16   | OUT104N         | AW16   | OUT104P         |
| AP17   | OUT103N               | AR17   | OUT103P               | AT17   | OUT102N              | AU17   | OUT102P              | AV17   | OUT101N         | AW17   | V <sub>SS</sub> |
| AP18   | V <sub>DD</sub> .CORE | AR18   | V <sub>DD</sub> .CORE | AT18   | OUT101P              | AU18   | OUT100N              | AV18   | OUT100P         | AW18   | OUT99N          |
| AP19   | OUT99P                | AR19   | V <sub>DD</sub> .PAD  | AT19   | V <sub>DD</sub> .PAD | AU19   | OUT98N               | AV19   | OUT98P          | AW19   | V <sub>SS</sub> |
| AP20   | V <sub>DD</sub> .CORE | AR20   | V <sub>DD</sub> .CORE | AT20   | OUT97P               | AU20   | OUT96N               | AV20   | OUT97N          | AW20   | OUT96P          |
| AP21   | OUT93N                | AR21   | OUT94P                | AT21   | OUT94N               | AU21   | OUT95P               | AV21   | OUT95N          | AW21   | V <sub>SS</sub> |
| AP22   | V <sub>DD</sub> .CORE | AR22   | V <sub>DD</sub> .CORE | AT22   | OUT91N               | AU22   | OUT92P               | AV22   | OUT92N          | AW22   | OUT93P          |
| AP23   | OUT88N                | AR23   | OUT89P                | AT23   | OUT89N               | AU23   | OUT90P               | AV23   | OUT90N          | AW23   | OUT91P          |
| AP24   | V <sub>DD</sub> .CORE | AR24   | V <sub>DD</sub> .CORE | AT24   | OUT86N               | AU24   | OUT87P               | AV24   | OUT87N          | AW24   | OUT88P          |
| AP25   | OUT84P                | AR25   | OUT84N                | AT25   | OUT85P               | AU25   | OUT85N               | AV25   | OUT86P          | AW25   | V <sub>SS</sub> |
| AP26   | V <sub>DD</sub> .CORE | AR26   | V <sub>DD</sub> .CORE | AT26   | OUT82P               | AU26   | OUT82N               | AV26   | OUT83P          | AW26   | OUT83N          |
| AP27   | V <sub>DD</sub> .PAD  | AR27   | V <sub>DD</sub> .PAD  | AT27   | OUT80P               | AU27   | OUT80N               | AV27   | OUT81P          | AW27   | OUT81N          |
| AP28   | V <sub>DD</sub> .CORE | AR28   | V <sub>DD</sub> .CORE | AT28   | OUT78P               | AU28   | OUT78N               | AV28   | OUT79P          | AW28   | OUT79N          |
| AP29   | OUT75N                | AR29   | OUT76P                | AT29   | OUT76N               | AU29   | OUT77P               | AV29   | OUT77N          | AW29   | V <sub>SS</sub> |
| AP30   | OUT72N                | AR30   | OUT73P                | AT30   | OUT73N               | AU30   | OUT74P               | AV30   | OUT74N          | AW30   | OUT75P          |
| AP31   | OUT70P                | AR31   | OUT70N                | AT31   | OUT71P               | AU31   | OUT71N               | AV31   | OUT72P          | AW31   | V <sub>SS</sub> |
| AP32   | V <sub>DD</sub> .CORE | AR32   | V <sub>DD</sub> .CORE | AT32   | NC                   | AU32   | OUT68N               | AV32   | OUT69P          | AW32   | OUT69N          |
| AP33   | OUT65P                | AR33   | OUT65N                | AT33   | OUT67P               | AU33   | OUT66N               | AV33   | OUT67N          | AW33   | V <sub>SS</sub> |
| AP34   | V <sub>DD</sub> .CORE | AR34   | RCB2                  | AT34   | V <sub>DD</sub> .PAD | AU34   | OUT64P               | AV34   | OUT66P          | AW34   | OUT68P          |
| AP35   | V <sub>DD</sub> .CORE | AR35   | V <sub>SS</sub>       | AT35   | V <sub>SS</sub>      | AU35   | RCB1                 | AV35   | RCB3            | AW35   | OUT64N          |
| AP36   | RCA6                  | AR36   | V <sub>SS</sub>       | AT36   | V <sub>SS</sub>      | AU36   | V <sub>SS</sub>      | AV36   | V <sub>SS</sub> | AW36   | V <sub>SS</sub> |
| AP37   | RCA3                  | AR37   | RCB0                  | AT37   | V <sub>SS</sub>      | AU37   | V <sub>SS</sub>      | AV37   | V <sub>SS</sub> | AW37   | V <sub>SS</sub> |
| AP38   | RCA2                  | AR38   | RCA4                  | AT38   | RCA5                 | AU38   | V <sub>SS</sub>      | AV38   | V <sub>SS</sub> | AW38   | V <sub>SS</sub> |
| AP39   | IN61P                 | AR39   | IN62P                 | AT39   | V <sub>SS</sub>      | AU39   | V <sub>SS</sub>      | AV39   | V <sub>SS</sub> | AW39   | V <sub>SS</sub> |



### 5.3 Pinout by Ball Name

Table 21 OCX256 Pinout By Ball Name

| Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # |
|-----------|--------|-----------|--------|-----------|--------|-----------|--------|-----------|--------|
| CLKN      | F35    | IN21P     | R34    | IN44P     | AE36   | IN67P     | AN3    | IN90P     | AB4    |
| CLKP      | E37    | IN22N     | R37    | IN45N     | AF39   | IN68N     | AM3    | IN91N     | AB1    |
| HW_RST#   | E6     | IN22P     | R36    | IN45P     | AE34   | IN68P     | AM4    | IN91P     | AB2    |
| IN00N     | F38    | IN23N     | R39    | IN46N     | AF37   | IN69N     | AM1    | IN92N     | AA6    |
| IN00P     | D38    | IN23P     | R38    | IN46P     | AF38   | IN69P     | AM2    | IN92P     | AA3    |
| IN01N     | G35    | IN24N     | T37    | IN47N     | AG38   | IN70N     | AL5    | IN93N     | AA4    |
| IN01P     | E38    | IN24P     | T36    | IN47P     | AF36   | IN70P     | AL1    | IN93P     | AA5    |
| IN02N     | G37    | IN25N     | T39    | IN48N     | AG36   | IN71N     | AL3    | IN94N     | Y1     |
| IN02P     | G34    | IN25P     | T38    | IN48P     | AG37   | IN71P     | AL4    | IN94P     | AA2    |
| IN03N     | F39    | IN26N     | U35    | IN49N     | AG34   | IN72N     | AK4    | IN95N     | Y4     |
| IN03P     | E39    | IN26P     | U34    | IN49P     | AG35   | IN72P     | AL2    | IN95P     | Y2     |
| IN04N     | H36    | IN27N     | U37    | IN50N     | AH38   | IN73N     | AK2    | IN96N     | W1     |
| IN04P     | G38    | IN27P     | U36    | IN50P     | AH39   | IN73P     | AK3    | IN96P     | Y3     |
| IN05N     | H37    | IN28N     | V36    | IN51N     | AH36   | IN74N     | AJ1    | IN97N     | W3     |
| IN05P     | G39    | IN28P     | U38    | IN51P     | AH37   | IN74P     | AK1    | IN97P     | W2     |
| IN06N     | H39    | IN29N     | V38    | IN52N     | AJ37   | IN75N     | AJ4    | IN98N     | W5     |
| IN06P     | H38    | IN29P     | V37    | IN52P     | AJ38   | IN75P     | AJ5    | IN98P     | W4     |
| IN07N     | J35    | IN30N     | W34    | IN53N     | AJ35   | IN76N     | AJ2    | IN99N     | V1     |
| IN07P     | J34    | IN30P     | V39    | IN53P     | AJ36   | IN76P     | AJ3    | IN99P     | W6     |
| IN08N     | J37    | IN31N     | W36    | IN54N     | AK39   | IN77N     | AH3    | IN100N    | U2     |
| IN08P     | J36    | IN31P     | W35    | IN54P     | AJ34   | IN77P     | AH4    | IN100P    | V4     |
| IN09N     | K34    | IN32N     | W38    | IN55N     | AK37   | IN78N     | AH1    | IN101N    | U4     |
| IN09P     | J38    | IN32P     | W37    | IN55P     | AK38   | IN78P     | AH2    | IN101P    | U3     |
| IN10N     | K36    | IN33N     | Y37    | IN56N     | AL39   | IN79N     | AG5    | IN102N    | U6     |
| IN10P     | K35    | IN33P     | Y38    | IN56P     | AK36   | IN79P     | AG1    | IN102P    | U5     |
| IN11N     | K38    | IN34N     | AA37   | IN57N     | AL35   | IN80N     | AG3    | IN103N    | T2     |
| IN11P     | K37    | IN34P     | AA38   | IN57P     | AL36   | IN80P     | AG4    | IN103P    | T1     |
| IN12N     | L34    | IN35N     | AA35   | IN58N     | AM39   | IN81N     | AF2    | IN104N    | T4     |
| IN12P     | K39    | IN35P     | AA36   | IN58P     | AL34   | IN81P     | AF3    | IN104P    | T3     |
| IN13N     | L36    | IN36N     | AB39   | IN59N     | AM37   | IN82N     | AE6    | IN105N    | R3     |
| IN13P     | L35    | IN36P     | AA34   | IN59P     | AM38   | IN82P     | AF1    | IN105P    | R2     |
| IN14N     | L38    | IN37N     | AB37   | IN60N     | AN38   | IN83N     | AE4    | IN106N    | R5     |
| IN14P     | L37    | IN37P     | AB38   | IN60P     | AM36   | IN83P     | AE5    | IN106P    | R4     |
| IN15N     | M38    | IN38N     | AC38   | IN61N     | AN37   | IN84N     | AE2    | IN107N    | P1     |
| IN15P     | M37    | IN38P     | AB36   | IN61P     | AP39   | IN84P     | AE3    | IN107P    | R6     |
| IN16N     | N34    | IN39N     | AC36   | IN62N     | AN36   | IN85N     | AD3    | IN108N    | P3     |
| IN16P     | M39    | IN39P     | AC37   | IN62P     | AR39   | IN85P     | AD4    | IN108P    | P2     |
| IN17N     | N36    | IN40N     | AC34   | IN63N     | AN34   | IN86N     | AD1    | IN109N    | N2     |
| IN17P     | N35    | IN40P     | AC35   | IN63P     | AN35   | IN86P     | AD2    | IN109P    | P4     |
| IN18N     | N38    | IN41N     | AD38   | IN64N     | AN6    | IN87N     | AC5    | IN110N    | N4     |
| IN18P     | N37    | IN41P     | AD39   | IN64P     | AP3    | IN87P     | AC6    | IN110P    | N3     |
| IN19N     | P37    | IN42N     | AD36   | IN65N     | AP1    | IN88N     | AC3    | IN111N    | M2     |
| IN19P     | P36    | IN42P     | AD37   | IN65P     | AP2    | IN88P     | AC4    | IN111P    | M1     |
| IN20N     | P39    | IN43N     | AE37   | IN66N     | AN4    | IN89N     | AC1    | IN112N    | M4     |
| IN20P     | P38    | IN43P     | AE38   | IN66P     | AN5    | IN89P     | AC2    | IN112P    | M3     |
| IN21N     | R35    | IN44N     | AE35   | IN67N     | AN2    | IN90N     | AB3    | IN113N    | M6     |



# OCX256 Crosspoint Switch—Advanced Data Sheet

Table 21 OCX256 Pinout By Ball Name (Continued)

| Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # |
|-----------|--------|-----------|--------|-----------|--------|-----------|--------|-----------|--------|
| IN113P    | M5     | OUT07N    | D9     | OUT30P    | E19    | OUT54N    | A30    | OUT77P    | AU29   |
| IN114N    | L2     | OUT07P    | E9     | OUT31N    | B19    | OUT54P    | F29    | OUT78N    | AU28   |
| IN114P    | L1     | OUT08N    | B9     | OUT31P    | C19    | OUT55N    | C30    | OUT78P    | AT28   |
| IN115N    | L4     | OUT08P    | C9     | OUT32N    | D20    | OUT55P    | B30    | OUT79N    | AW28   |
| IN115P    | L3     | OUT09N    | D10    | OUT32P    | B20    | OUT56N    | C31    | OUT79P    | AV28   |
| IN116N    | L6     | OUT09P    | A9     | OUT33N    | A20    | OUT56P    | B31    | OUT80N    | AU27   |
| IN116P    | L5     | OUT10N    | B10    | OUT33P    | C20    | OUT57N    | E31    | OUT80P    | AT27   |
| IN117N    | K2     | OUT10P    | C10    | OUT34N    | E21    | OUT57P    | D31    | OUT81N    | AW27   |
| IN117P    | K1     | OUT11N    | F11    | OUT34P    | D21    | OUT58N    | A32    | OUT81P    | AV27   |
| IN118N    | K4     | OUT11P    | A10    | OUT35N    | A22    | OUT58P    | F31    | OUT82N    | AU26   |
| IN118P    | K3     | OUT12N    | D11    | OUT35P    | F21    | OUT59N    | C32    | OUT82P    | AT26   |
| IN119N    | K6     | OUT12P    | E11    | OUT36N    | C22    | OUT59P    | B32    | OUT83N    | AW26   |
| IN119P    | K5     | OUT13N    | C12    | OUT36P    | B22    | OUT60N    | B33    | OUT83P    | AV26   |
| IN120N    | J3     | OUT13P    | D12    | OUT37N    | A23    | OUT60P    | D32    | OUT84N    | AR25   |
| IN120P    | J2     | OUT14N    | A12    | OUT37P    | D22    | OUT61N    | A34    | OUT84P    | AP25   |
| IN121N    | H1     | OUT14P    | B12    | OUT38N    | C23    | OUT61P    | C33    | OUT85N    | AU25   |
| IN121P    | J6     | OUT15N    | E13    | OUT38P    | B23    | OUT62N    | E33    | OUT85P    | AT25   |
| IN122N    | H3     | OUT15P    | F13    | OUT39N    | E23    | OUT62P    | D33    | OUT86N    | AT24   |
| IN122P    | H2     | OUT16N    | C13    | OUT39P    | D23    | OUT63N    | B35    | OUT86P    | AV25   |
| IN123N    | G2     | OUT16P    | D13    | OUT40N    | A24    | OUT63P    | B34    | OUT87N    | AV24   |
| IN123P    | H4     | OUT17N    | A13    | OUT40P    | F23    | OUT64N    | AW35   | OUT87P    | AU24   |
| IN124N    | F1     | OUT17P    | B13    | OUT41N    | C24    | OUT64P    | AU34   | OUT88N    | AP23   |
| IN124P    | G3     | OUT18N    | C14    | OUT41P    | B24    | OUT65N    | AR33   | OUT88P    | AW24   |
| IN125N    | G5     | OUT18P    | D14    | OUT42N    | B25    | OUT65P    | AP33   | OUT89N    | AT23   |
| IN125P    | G4     | OUT19N    | A14    | OUT42P    | D24    | OUT66N    | AU33   | OUT89P    | AR23   |
| IN126N    | G6     | OUT19P    | B14    | OUT43N    | D25    | OUT66P    | AV34   | OUT90N    | AV23   |
| IN126P    | F2     | OUT20N    | E15    | OUT43P    | C25    | OUT67N    | AV33   | OUT90P    | AU23   |
| IN127N    | F3     | OUT20P    | F15    | OUT44N    | F25    | OUT67P    | AT33   | OUT91N    | AT22   |
| IN127P    | E1     | OUT21N    | C15    | OUT44P    | E25    | OUT68N    | AU32   | OUT91P    | AW23   |
| NC        | E34    | OUT21P    | D15    | OUT45N    | B26    | OUT68P    | AW34   | OUT92N    | AV22   |
| NC        | D2     | OUT22N    | D16    | OUT45P    | A26    | OUT69N    | AW32   | OUT92P    | AU22   |
| NC        | AT32   | OUT22P    | B15    | OUT46N    | D26    | OUT69P    | AV32   | OUT93N    | AP21   |
| OE#       | D34    | OUT23N    | B16    | OUT46P    | C26    | OUT70N    | AR31   | OUT93P    | AW22   |
| OUT00N    | C6     | OUT23P    | C16    | OUT47N    | B27    | OUT70P    | AP31   | OUT94N    | AT21   |
| OUT00P    | F7     | OUT24N    | F17    | OUT47P    | A27    | OUT71N    | AU31   | OUT94P    | AR21   |
| OUT01N    | A5     | OUT24P    | A16    | OUT48N    | D27    | OUT71P    | AT31   | OUT95N    | AV21   |
| OUT01P    | E7     | OUT25N    | D17    | OUT48P    | C27    | OUT72N    | AP30   | OUT95P    | AU21   |
| OUT02N    | B6     | OUT25P    | E17    | OUT49N    | F27    | OUT72P    | AV31   | OUT96N    | AU20   |
| OUT02P    | D7     | OUT26N    | B17    | OUT49P    | E27    | OUT73N    | AT30   | OUT96P    | AW20   |
| OUT03N    | C7     | OUT26P    | C17    | OUT50N    | B28    | OUT73P    | AR30   | OUT97N    | AV20   |
| OUT03P    | A6     | OUT27N    | D18    | OUT50P    | A28    | OUT74N    | AV30   | OUT97P    | AT20   |
| OUT04N    | D8     | OUT27P    | A17    | OUT51N    | D28    | OUT74P    | AU30   | OUT98N    | AU19   |
| OUT04P    | B7     | OUT28N    | B18    | OUT51P    | C28    | OUT75N    | AP29   | OUT98P    | AV19   |
| OUT05N    | B8     | OUT28P    | C18    | OUT52N    | C29    | OUT75P    | AW30   | OUT99N    | AW18   |
| OUT05P    | C8     | OUT29N    | F19    | OUT52P    | B29    | OUT76N    | AT29   | OUT99P    | AP19   |
| OUT06N    | F9     | OUT29P    | A18    | OUT53N    | E29    | OUT76P    | AR29   | OUT100N   | AU18   |
| OUT06P    | A8     | OUT30N    | D19    | OUT53P    | D29    | OUT77N    | AV29   | OUT100P   | AV18   |



Table 21 OCX256 Pinout By Ball Name (Continued)

| Ball Name | Ball # | Ball Name             | Ball # | Ball Name             | Ball # | Ball Name             | Ball # | Ball Name            | Ball # |
|-----------|--------|-----------------------|--------|-----------------------|--------|-----------------------|--------|----------------------|--------|
| OUT101N   | AV17   | OUT124P               | AW6    | V <sub>DD</sub> .CORE | E26    | V <sub>DD</sub> .CORE | AD34   | V <sub>DD</sub> .IN  | J4     |
| OUT101P   | AT18   | OUT125N               | AT7    | V <sub>DD</sub> .CORE | E28    | V <sub>DD</sub> .CORE | AD35   | V <sub>DD</sub> .IN  | J5     |
| OUT102N   | AT17   | OUT125P               | AU7    | V <sub>DD</sub> .CORE | E30    | V <sub>DD</sub> .CORE | AF5    | V <sub>DD</sub> .IN  | L39    |
| OUT102P   | AU17   | OUT126N               | AW5    | V <sub>DD</sub> .CORE | E32    | V <sub>DD</sub> .CORE | AF6    | V <sub>DD</sub> .IN  | M36    |
| OUT103N   | AP17   | OUT126P               | AR7    | V <sub>DD</sub> .CORE | F6     | V <sub>DD</sub> .CORE | AF34   | V <sub>DD</sub> .IN  | V2     |
| OUT103P   | AR17   | OUT127N               | AV6    | V <sub>DD</sub> .CORE | F8     | V <sub>DD</sub> .CORE | AF35   | V <sub>DD</sub> .IN  | V3     |
| OUT104N   | AV16   | OUT127P               | AP7    | V <sub>DD</sub> .CORE | F10    | V <sub>DD</sub> .CORE | AH5    | V <sub>DD</sub> .IN  | Y36    |
| OUT104P   | AW16   | RCA0                  | F36    | V <sub>DD</sub> .CORE | F12    | V <sub>DD</sub> .CORE | AH6    | V <sub>DD</sub> .IN  | Y39    |
| OUT105N   | AT16   | RCA1                  | F37    | V <sub>DD</sub> .CORE | F14    | V <sub>DD</sub> .CORE | AH34   | V <sub>DD</sub> .IN  | AF4    |
| OUT105P   | AU16   | RCA2                  | AP38   | V <sub>DD</sub> .CORE | F16    | V <sub>DD</sub> .CORE | AH35   | V <sub>DD</sub> .IN  | AG2    |
| OUT106N   | AV15   | RCA3                  | AP37   | V <sub>DD</sub> .CORE | F18    | V <sub>DD</sub> .CORE | AK5    | V <sub>DD</sub> .IN  | AL37   |
| OUT106P   | AW15   | RCA4                  | AR38   | V <sub>DD</sub> .CORE | F20    | V <sub>DD</sub> .CORE | AK6    | V <sub>DD</sub> .IN  | AL38   |
| OUT107N   | AT15   | RCA5                  | AT38   | V <sub>DD</sub> .CORE | F22    | V <sub>DD</sub> .CORE | AK34   | V <sub>DD</sub> .IN  | AR2    |
| OUT107P   | AU15   | RCA6                  | AP36   | V <sub>DD</sub> .CORE | F24    | V <sub>DD</sub> .CORE | AK35   | V <sub>DD</sub> .PAD | A31    |
| OUT108N   | AP15   | RCB0                  | AR37   | V <sub>DD</sub> .CORE | F26    | V <sub>DD</sub> .CORE | AM5    | V <sub>DD</sub> .PAD | B5     |
| OUT108P   | AR15   | RCB1                  | AU35   | V <sub>DD</sub> .CORE | F28    | V <sub>DD</sub> .CORE | AM6    | V <sub>DD</sub> .PAD | B11    |
| OUT109N   | AV14   | RCB2                  | AR34   | V <sub>DD</sub> .CORE | F30    | V <sub>DD</sub> .CORE | AM34   | V <sub>DD</sub> .PAD | B21    |
| OUT109P   | AW14   | RCB3                  | AV35   | V <sub>DD</sub> .CORE | F32    | V <sub>DD</sub> .CORE | AM35   | V <sub>DD</sub> .PAD | C11    |
| OUT110N   | AU13   | RCB4                  | AV5    | V <sub>DD</sub> .CORE | F34    | V <sub>DD</sub> .CORE | AP5    | V <sub>DD</sub> .PAD | C21    |
| OUT110P   | AV13   | RCB5                  | AU6    | V <sub>DD</sub> .CORE | H5     | V <sub>DD</sub> .CORE | AP6    | V <sub>DD</sub> .PAD | D30    |
| OUT111N   | AR13   | RCB6                  | AU5    | V <sub>DD</sub> .CORE | H6     | V <sub>DD</sub> .CORE | AP10   | V <sub>DD</sub> .PAD | AP9    |
| OUT111P   | AT13   | RC_CLK#               | AR3    | V <sub>DD</sub> .CORE | H34    | V <sub>DD</sub> .CORE | AP12   | V <sub>DD</sub> .PAD | AP27   |
| OUT112N   | AW12   | RC_EN#                | AP4    | V <sub>DD</sub> .CORE | H35    | V <sub>DD</sub> .CORE | AP14   | V <sub>DD</sub> .PAD | AR19   |
| OUT112P   | AP13   | RCI0                  | AT6    | V <sub>DD</sub> .CORE | M34    | V <sub>DD</sub> .CORE | AP16   | V <sub>DD</sub> .PAD | AR27   |
| OUT113N   | AU12   | RCI1                  | AR6    | V <sub>DD</sub> .CORE | M35    | V <sub>DD</sub> .CORE | AP18   | V <sub>DD</sub> .PAD | AT14   |
| OUT113P   | AV12   | RCI2                  | AV4    | V <sub>DD</sub> .CORE | P5     | V <sub>DD</sub> .CORE | AP20   | V <sub>DD</sub> .PAD | AT19   |
| OUT114N   | AW11   | RCI3                  | AT2    | V <sub>DD</sub> .CORE | P6     | V <sub>DD</sub> .CORE | AP22   | V <sub>DD</sub> .PAD | AT34   |
| OUT114P   | AT12   | RCO0                  | F33    | V <sub>DD</sub> .CORE | P34    | V <sub>DD</sub> .CORE | AP24   | V <sub>DD</sub> .PAD | AU14   |
| OUT115N   | AT11   | RCO1                  | B36    | V <sub>DD</sub> .CORE | P35    | V <sub>DD</sub> .CORE | AP26   | V <sub>SS</sub>      | A1     |
| OUT115P   | AU11   | RCO2                  | C34    | V <sub>DD</sub> .CORE | T5     | V <sub>DD</sub> .CORE | AP28   | V <sub>SS</sub>      | A2     |
| OUT116N   | AP11   | RCO3                  | C35    | V <sub>DD</sub> .CORE | T6     | V <sub>DD</sub> .CORE | AP32   | V <sub>SS</sub>      | A3     |
| OUT116P   | AR11   | RCO4                  | D6     | V <sub>DD</sub> .CORE | T34    | V <sub>DD</sub> .CORE | AP34   | V <sub>SS</sub>      | A4     |
| OUT117N   | AV10   | TCK                   | F5     | V <sub>DD</sub> .CORE | T35    | V <sub>DD</sub> .CORE | AP35   | V <sub>SS</sub>      | A7     |
| OUT117P   | AW10   | TDI                   | E2     | V <sub>DD</sub> .CORE | V5     | V <sub>DD</sub> .CORE | AR10   | V <sub>SS</sub>      | A11    |
| OUT118N   | AT10   | TDO                   | C5     | V <sub>DD</sub> .CORE | V6     | V <sub>DD</sub> .CORE | AR12   | V <sub>SS</sub>      | A15    |
| OUT118P   | AU10   | TMS                   | F4     | V <sub>DD</sub> .CORE | V34    | V <sub>DD</sub> .CORE | AR14   | V <sub>SS</sub>      | A19    |
| OUT119N   | AU9    | TRST#                 | E3     | V <sub>DD</sub> .CORE | V35    | V <sub>DD</sub> .CORE | AR16   | V <sub>SS</sub>      | A21    |
| OUT119P   | AV9    | UPDATE#               | B4     | V <sub>DD</sub> .CORE | Y5     | V <sub>DD</sub> .CORE | AR18   | V <sub>SS</sub>      | A25    |
| OUT120N   | AR9    | V <sub>DD</sub> .CORE | E8     | V <sub>DD</sub> .CORE | Y6     | V <sub>DD</sub> .CORE | AR20   | V <sub>SS</sub>      | A29    |
| OUT120P   | AT9    | V <sub>DD</sub> .CORE | E10    | V <sub>DD</sub> .CORE | Y34    | V <sub>DD</sub> .CORE | AR22   | V <sub>SS</sub>      | A33    |
| OUT121N   | AV8    | V <sub>DD</sub> .CORE | E12    | V <sub>DD</sub> .CORE | Y35    | V <sub>DD</sub> .CORE | AR24   | V <sub>SS</sub>      | A35    |
| OUT121P   | AW8    | V <sub>DD</sub> .CORE | E14    | V <sub>DD</sub> .CORE | AB5    | V <sub>DD</sub> .CORE | AR26   | V <sub>SS</sub>      | A36    |
| OUT122N   | AT8    | V <sub>DD</sub> .CORE | E16    | V <sub>DD</sub> .CORE | AB6    | V <sub>DD</sub> .CORE | AR28   | V <sub>SS</sub>      | A37    |
| OUT122P   | AU8    | V <sub>DD</sub> .CORE | E18    | V <sub>DD</sub> .CORE | AB34   | V <sub>DD</sub> .CORE | AR32   | V <sub>SS</sub>      | A38    |
| OUT123N   | AP8    | V <sub>DD</sub> .CORE | E20    | V <sub>DD</sub> .CORE | AB35   | V <sub>DD</sub> .IN   | N6     | V <sub>SS</sub>      | A39    |
| OUT123P   | AR8    | V <sub>DD</sub> .CORE | E22    | V <sub>DD</sub> .CORE | AD5    | V <sub>DD</sub> .IN   | N5     | V <sub>SS</sub>      | B1     |
| OUT124N   | AV7    | V <sub>DD</sub> .CORE | E24    | V <sub>DD</sub> .CORE | AD6    | V <sub>DD</sub> .IN   | G36    | V <sub>SS</sub>      | B2     |

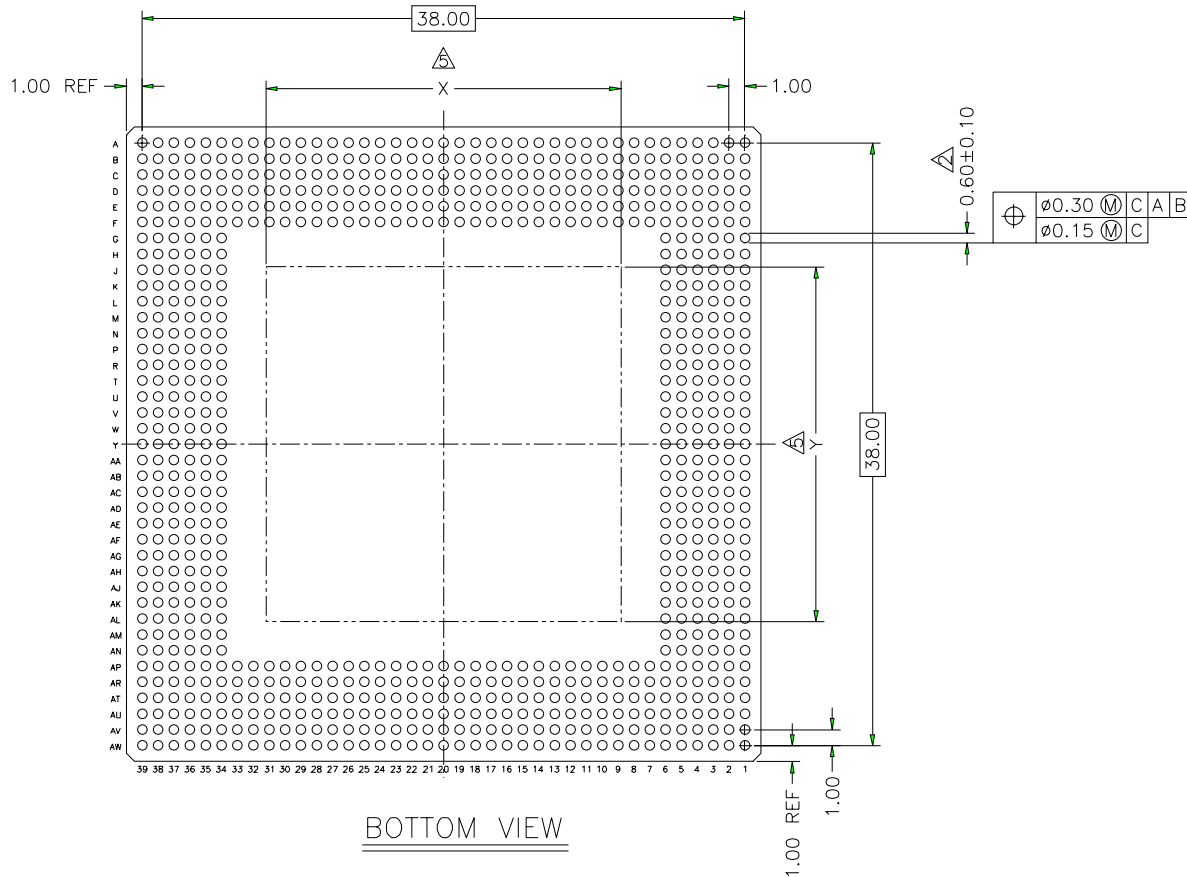


**Table 21** OCX256 Pinout By Ball Name *(Continued)*

| Ball Name       | Ball # | Ball Name       | Ball # | Ball Name | Ball # | Ball Name | Ball # | Ball Name | Ball # |
|-----------------|--------|-----------------|--------|-----------|--------|-----------|--------|-----------|--------|
| V <sub>SS</sub> | B3     | V <sub>SS</sub> | AR5    |           |        |           |        |           |        |
| V <sub>SS</sub> | B37    | V <sub>SS</sub> | AR35   |           |        |           |        |           |        |
| V <sub>SS</sub> | B38    | V <sub>SS</sub> | AR36   |           |        |           |        |           |        |
| V <sub>SS</sub> | B39    | V <sub>SS</sub> | AT1    |           |        |           |        |           |        |
| V <sub>SS</sub> | C1     | V <sub>SS</sub> | AT3    |           |        |           |        |           |        |
| V <sub>SS</sub> | C2     | V <sub>SS</sub> | AT4    |           |        |           |        |           |        |
| V <sub>SS</sub> | C3     | V <sub>SS</sub> | AT5    |           |        |           |        |           |        |
| V <sub>SS</sub> | C4     | V <sub>SS</sub> | AT35   |           |        |           |        |           |        |
| V <sub>SS</sub> | C36    | V <sub>SS</sub> | AT36   |           |        |           |        |           |        |
| V <sub>SS</sub> | C37    | V <sub>SS</sub> | AT37   |           |        |           |        |           |        |
| V <sub>SS</sub> | C38    | V <sub>SS</sub> | AT39   |           |        |           |        |           |        |
| V <sub>SS</sub> | C39    | V <sub>SS</sub> | AU1    |           |        |           |        |           |        |
| V <sub>SS</sub> | D1     | V <sub>SS</sub> | AU2    |           |        |           |        |           |        |
| V <sub>SS</sub> | D3     | V <sub>SS</sub> | AU3    |           |        |           |        |           |        |
| V <sub>SS</sub> | D4     | V <sub>SS</sub> | AU4    |           |        |           |        |           |        |
| V <sub>SS</sub> | D5     | V <sub>SS</sub> | AU36   |           |        |           |        |           |        |
| V <sub>SS</sub> | D35    | V <sub>SS</sub> | AU37   |           |        |           |        |           |        |
| V <sub>SS</sub> | D36    | V <sub>SS</sub> | AU38   |           |        |           |        |           |        |
| V <sub>SS</sub> | D37    | V <sub>SS</sub> | AU39   |           |        |           |        |           |        |
| V <sub>SS</sub> | D39    | V <sub>SS</sub> | AV1    |           |        |           |        |           |        |
| V <sub>SS</sub> | E4     | V <sub>SS</sub> | AV2    |           |        |           |        |           |        |
| V <sub>SS</sub> | E5     | V <sub>SS</sub> | AV3    |           |        |           |        |           |        |
| V <sub>SS</sub> | E35    | V <sub>SS</sub> | AV11   |           |        |           |        |           |        |
| V <sub>SS</sub> | E36    | V <sub>SS</sub> | AV36   |           |        |           |        |           |        |
| V <sub>SS</sub> | G1     | V <sub>SS</sub> | AV37   |           |        |           |        |           |        |
| V <sub>SS</sub> | J1     | V <sub>SS</sub> | AV38   |           |        |           |        |           |        |
| V <sub>SS</sub> | J39    | V <sub>SS</sub> | AV39   |           |        |           |        |           |        |
| V <sub>SS</sub> | N1     | V <sub>SS</sub> | AW1    |           |        |           |        |           |        |
| V <sub>SS</sub> | N39    | V <sub>SS</sub> | AW2    |           |        |           |        |           |        |
| V <sub>SS</sub> | R1     | V <sub>SS</sub> | AW3    |           |        |           |        |           |        |
| V <sub>SS</sub> | U1     | V <sub>SS</sub> | AW4    |           |        |           |        |           |        |
| V <sub>SS</sub> | U39    | V <sub>SS</sub> | AW7    |           |        |           |        |           |        |
| V <sub>SS</sub> | W39    | V <sub>SS</sub> | AW9    |           |        |           |        |           |        |
| V <sub>SS</sub> | AA1    | V <sub>SS</sub> | AW13   |           |        |           |        |           |        |
| V <sub>SS</sub> | AA39   | V <sub>SS</sub> | AW17   |           |        |           |        |           |        |
| V <sub>SS</sub> | AC39   | V <sub>SS</sub> | AW19   |           |        |           |        |           |        |
| V <sub>SS</sub> | AE1    | V <sub>SS</sub> | AW21   |           |        |           |        |           |        |
| V <sub>SS</sub> | AE39   | V <sub>SS</sub> | AW25   |           |        |           |        |           |        |
| V <sub>SS</sub> | AG6    | V <sub>SS</sub> | AW29   |           |        |           |        |           |        |
| V <sub>SS</sub> | AG39   | V <sub>SS</sub> | AW31   |           |        |           |        |           |        |
| V <sub>SS</sub> | AJ6    | V <sub>SS</sub> | AW33   |           |        |           |        |           |        |
| V <sub>SS</sub> | AJ39   | V <sub>SS</sub> | AW36   |           |        |           |        |           |        |
| V <sub>SS</sub> | AL6    | V <sub>SS</sub> | AW37   |           |        |           |        |           |        |
| V <sub>SS</sub> | AN1    | V <sub>SS</sub> | AW38   |           |        |           |        |           |        |
| V <sub>SS</sub> | AN39   | V <sub>SS</sub> | AW39   |           |        |           |        |           |        |
| V <sub>SS</sub> | AR1    |                 |        |           |        |           |        |           |        |
| V <sub>SS</sub> | AR4    |                 |        |           |        |           |        |           |        |



## 5.4 Package Dimensions



### NOTE

1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M - 1994
- △ DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C
- △ PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. SOLDER BALL POSITION DESIGNATION PER JESD 95-1.
- △ THE ENCAPSULATION SIZE (X,Y) WILL VARY WITH CAVITY SIZE. THE DISTANCE FROM BOND FINGER EDGE TO ENCAPSULATION SHALL BE MIN. 0.50MM.
6. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL  $\pm 0.05$   
ANGULAR  $\pm 2^\circ$ .

Figure 18 OCX256 Package—Bottom View

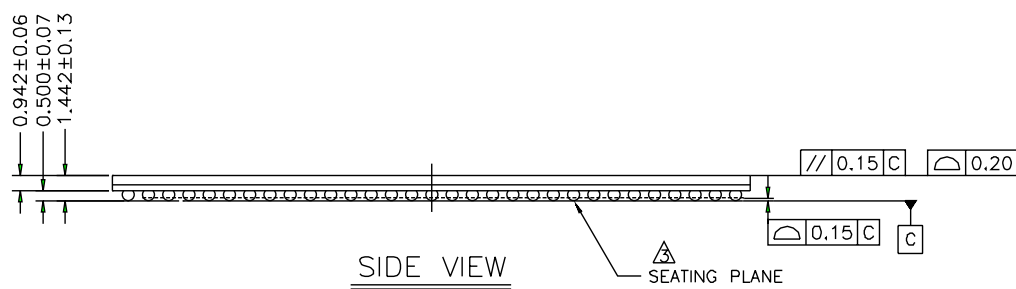
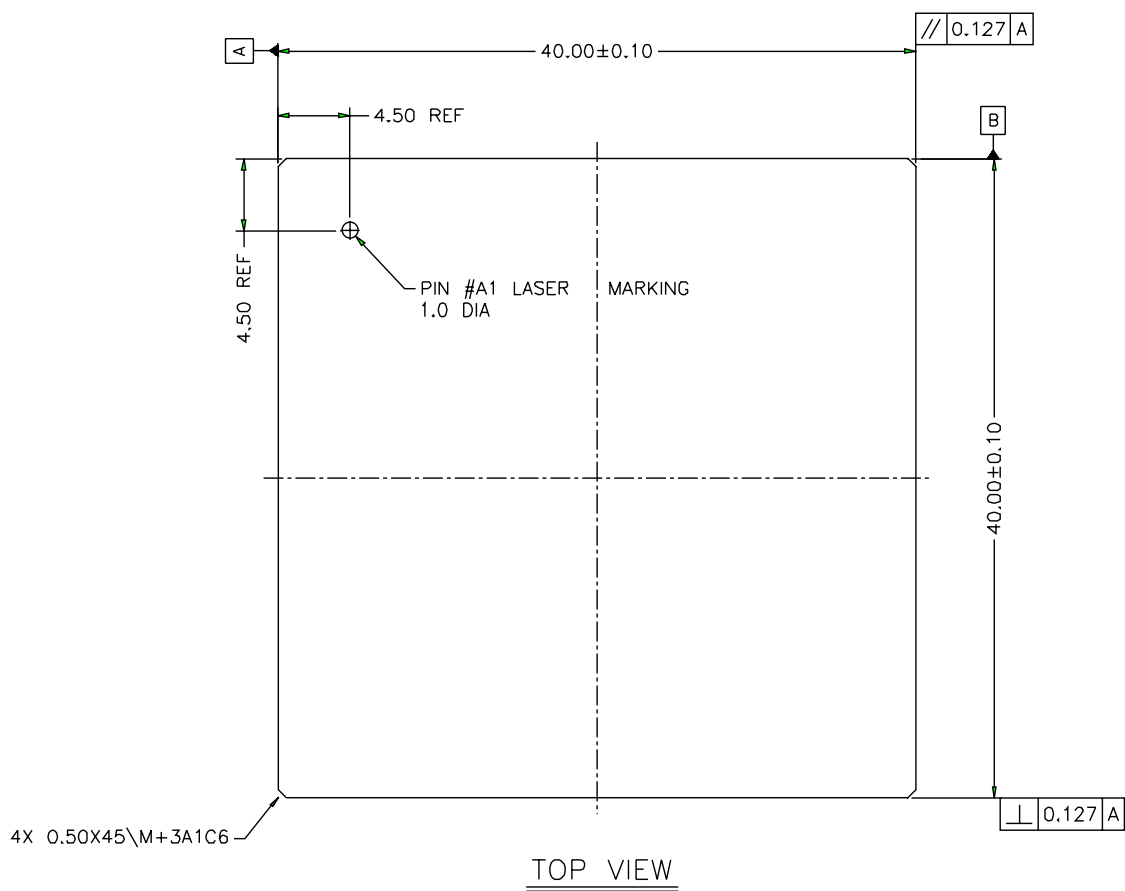


Figure 19 OCX256 Package—Top and Side Views



## 5.5 Package Thermal Characteristics

Table 22 Package Thermal Coefficients

| Package | Pin Count | $\Theta_{JC}(C/W)$ | $\Theta_{JA}(^{\circ}C/W)$<br>Still Air |
|---------|-----------|--------------------|-----------------------------------------|
| TBGA    | 792       | 0.4                | 7.58°C/W                                |

NOTE:

1. Thermal performance values are based on simulation data.



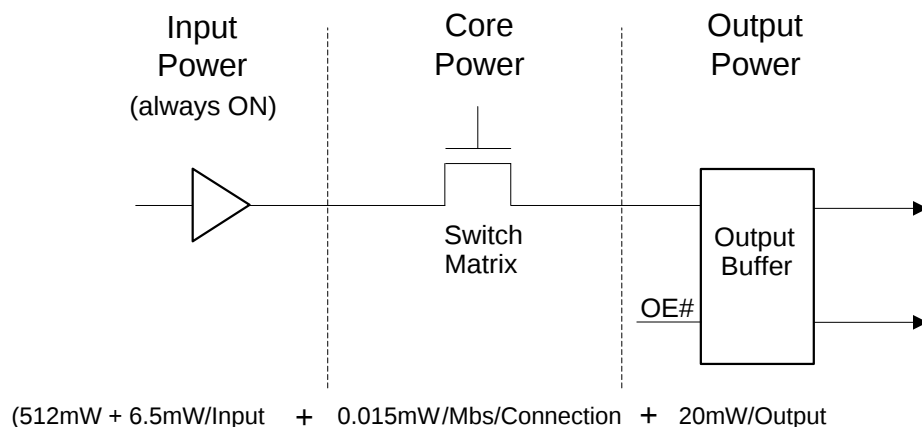
## 6. Power Consumption

Chip power consists of three integral elements (refer to Figure 20):

1. **Input Power**—This element has two components:
  - a steady state component that is always ON, and
  - a component that is based on the number of inputs being used.
2. **Core Power**—Core power is a function of data rate (Mb/s) and the number of connection paths through the switch matrix.
3. **Output Power**—This element is a fixed amount for each differential output. The value is zero if the Output Enable (OE#) is disabled or set to OFF.

The following diagram shows the chip power elements (as described above), the formulas used for determining chip power, and the total power consumption as determined by the formula.

### 6.1 Power for OCX256L (LVDS)



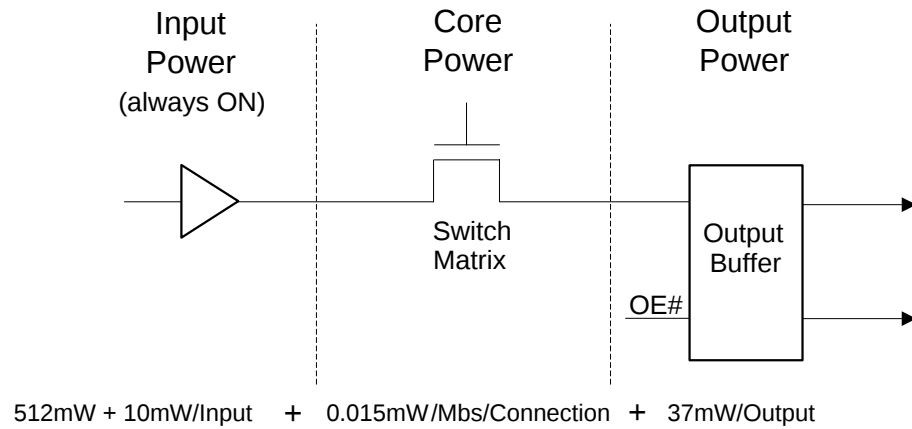
**Example:** Worst Case =  $(512\text{mW} + 832\text{mW}) + (0.015\text{ mW} \times 667 \times 128) + (20\text{mW} \times 128)$

$$\begin{aligned} &1344\text{mW} + 1280\text{mW} + 2560\text{mW} \\ &= \mathbf{5.18\text{ watts}} \end{aligned}$$

Figure 20 Power Consumption Diagram for the OCX256L using LVDS



## 6.2 Power for OCX256P (LVPECL)



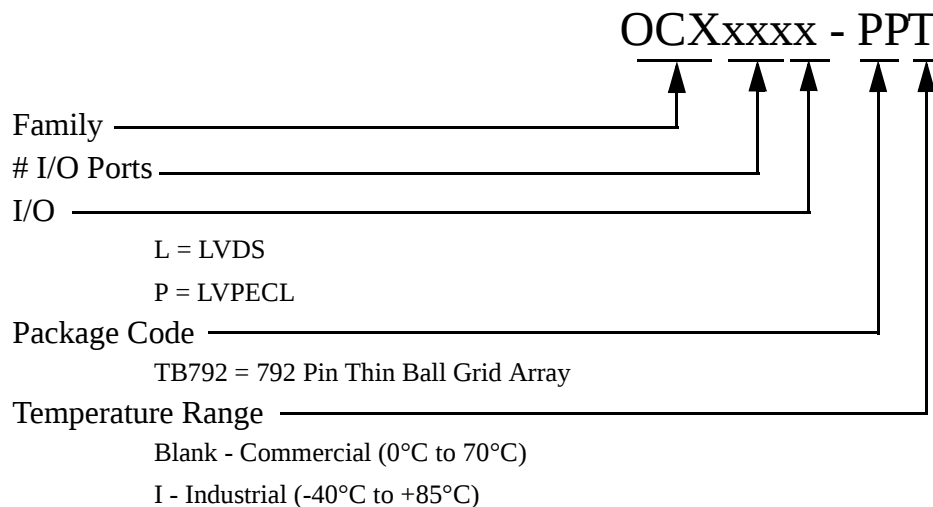
**Example:** Worst Case = (512mW + 1280mW) + (0.015 mW x 667 x 128) + (37mW x 128)

$$1792\text{mW} + 1280\text{mW} + 4736\text{mW} = 7.81 \text{ watts}$$

**Figure 21 Power Consumption Diagram for the OCX256P using LVPECL**



## 7. Component Availability and Ordering Information



## 8. Glossary

**CLOCK:** A single differential input used to gate data into registers in the Output Buffer. The input serves all outputs of the OCX. The neighbor input can also be used as a register clock.

**CROSSPOINT:** A single cell controlled by two RAM bits. The RAM bits are connected in a master-slave configuration to provide an update for programming and changing program information all at once.

**CROSSPOINT ARRAY:** An array of Crosspoint cells used to connect any input port to any output port.

**INPUT OR OUTPUT PATH:** The signal flow from pin to array and array to pin. Each path has a register with selectable clocks, drivers for the loaded outputs with selectable enables, and sense circuits to detect changes on either side of the IO Buffer.

**NEXT NEIGHBOR:** A physically adjacent port can be used as a clock source for an output configured in registered mode. These outputs are grouped in pairs such that the signal being switched through Output 0 can be used to clock the signal being switched through Output 1, or vice-versa. Any single clock or data input signal can be used to clock any other input signal provided they are switched to an appropriate output pair.

**PORT:** A name followed by a number to identify a pin on the device.

**RAPIDCONFIGURE:** A parallel programming method for the OCX devices. The RC mode uses 25 dedicated pins to program the Crosspoint Array and the IO Buffers. The 25 pins consist of an enable, a clock, four instruction bits, two seven-bit address fields, and a five-bit data field.



## Revision History

| Date        | Version No.   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
|-------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-----------|------------|------------|------------|------------|-------------|------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 9/25/2000   | Revision 1.0  | Preliminary release of “Advanced” data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 10/8/00     | Revision 1.1  | Additions include RCO output pin information, pinout drawing, pinout tables, package dimensions and illustration, duty-cycle diagram, thermal characteristics table, device reset options table, a section on configuring multiple devices, bitstream generation and downloading, JTAG information, and Power Consumption information/illustrations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 11/1/00     | Revision 1.2  | Corrections made to pinout drawing and pin names.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 11/16/00    | Revision 1.3  | Updated RapidConfigure Read Cycle timing diagram so that RCO is relative to RC_CLK#; RCO was previously relative to RC_EN#. Replaced “+” on signal names to “P” and “-” to “N”. Corrected RCO[4:0] pin locations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 11/21/00    | Revision 1.4  | Corrected pin names ENAB, RCC, and RCE on Pinout drawing and tables to be OE#, RC_CLK#, and RC_EN# respectively; corrections to Input and Output pin names 59P, 60P, 61P, and 62P in tables 22 and 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 1/12/01     | Revision 1.5  | Corrected pin names in Table 22 “Pinout By Ball Sequence”:<br><table><tr><td><u>From</u></td><td><u>To</u></td></tr><tr><td>B32 OUT58P</td><td>B32 OUT59P</td></tr><tr><td>C33 OUT60P</td><td>C33 OUT61P</td></tr><tr><td>D32 OUT59P</td><td>D32 OUT60P</td></tr><tr><td>D33 OUT61P</td><td>D33 OUT62P</td></tr><tr><td>AR9 OUT120P</td><td>AR9 OUT120N</td></tr><tr><td>AT9 OUT120N</td><td>AT9 OUT120P</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                    | <u>From</u> | <u>To</u> | B32 OUT58P | B32 OUT59P | C33 OUT60P | C33 OUT61P | D32 OUT59P  | D32 OUT60P | D33 OUT61P  | D33 OUT62P  | AR9 OUT120P | AR9 OUT120N | AT9 OUT120N | AT9 OUT120P |
| <u>From</u> | <u>To</u>     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| B32 OUT58P  | B32 OUT59P    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| C33 OUT60P  | C33 OUT61P    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| D32 OUT59P  | D32 OUT60P    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| D33 OUT61P  | D33 OUT62P    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| AR9 OUT120P | AR9 OUT120N   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| AT9 OUT120N | AT9 OUT120P   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 2/20/01     | Revision 1.6  | Reversed “input” and “output” descriptions in Table 3 “RapidConfigure Programming Instructions” for instructions 0101, 0111, 1000, 1001, and 1010. Corrected pin names in Table 22 “Pinout By Ball Sequence”:<br><table><tr><td><u>From</u></td><td><u>To</u></td></tr><tr><td>K5 IN119N</td><td>K5 IN119P</td></tr><tr><td>K6 IN119P</td><td>K6 IN119N</td></tr><tr><td>AM38 IN597P</td><td>AM38 IN59P</td></tr><tr><td>AU9 OUT119P</td><td>AU9 OUT119N</td></tr><tr><td>AV9 OUT119N</td><td>AV9 OUT119P</td></tr></table> Changed the V <sub>IH</sub> , V <sub>IL</sub> , V <sub>OH</sub> , and V <sub>OL</sub> minimum and maximum values for LVPECL DC specifications in Table 20; added a note below table explaining the current values; changed Pass Transistor to high-performance buffering circuit; updated power and ground pin count in Table 12. | <u>From</u> | <u>To</u> | K5 IN119N  | K5 IN119P  | K6 IN119P  | K6 IN119N  | AM38 IN597P | AM38 IN59P | AU9 OUT119P | AU9 OUT119N | AV9 OUT119N | AV9 OUT119P |             |             |
| <u>From</u> | <u>To</u>     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| K5 IN119N   | K5 IN119P     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| K6 IN119P   | K6 IN119N     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| AM38 IN597P | AM38 IN59P    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| AU9 OUT119P | AU9 OUT119N   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| AV9 OUT119N | AV9 OUT119P   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 4/5/01      | Revision 1.7  | Created separate parts for LVDS and LVPECL (OCX256L and OCX256P respectively); created new LVDS and LVPECL signal drawings; created new LVDS and LVPECL power consumption drawings; updated DC electrical specifications tables; changes/corrections to LVDS and LVPECL DC Electrical Specs tables.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 5/21/2001   | Revision 1.8  | Changes to LVDS and LVPECL power consumption diagrams and Input power specs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 7/27/01     | Revision 1.9  | Changes to LVDS and LVPECL DC Electrical specs tables; added termination impedance values                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |             |           |            |            |            |            |             |            |             |             |             |             |             |             |
| 9/14/01     | Revision 1.10 | Added jitter specifications and PRBS Data Eye diagram.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |             |           |            |            |            |            |             |            |             |             |             |             |             |             |



## 9. Product Status Definition

| Data Sheet Identification | Product Status          | Definition                                                                                                                                                                                                                                     |
|---------------------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Advanced</b>           | Formative or In Design  | This data sheet contains the design specifications for product development. Specification may change in any manner without notice.                                                                                                             |
| <b>Preliminary</b>        | Preproduction Product   | This data sheet contains the preliminary data, and supplementary data will be published at a later date. I-Cube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| <b>No Identification</b>  | Full Production         | This data sheet contains final specifications. I-Cube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                           |
| <b>Obsolete</b>           | No longer in Production | This data sheet contains specifications for a product that has been discontinued by I-Cube. The data sheet is provided for reference information only.                                                                                         |

I-Cube<sup>®</sup> is a registered trademark and RapidConnect, RapidConfigure, ActiveArray, ImpliedDisconnect, IQ, IQX, MSX, MSXPro, OCX, OCXPro, and PSX are trademarks of I-Cube, Inc. All other trademarks or registered trademarks are the property of their respective holders. I-Cube, Inc., does not assume any liability arising out of the applications or use of the product described herein; nor does it convey any license under its patents, copyright rights or any rights of others.

The information contained in this document is believed to be current and accurate as of the publication date. I-Cube reserves the right to make changes, at any time, in order to improve reliability, function, performance or design in order to supply the best product possible.

I-Cube assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made.

This product is protected under the U.S. patents: 5202593, 5282271, 5426738, 5428750, 5428800, 5465056, 5530814, 5559971, 5625780, 5710550, 5717871, 5734334, 5781717, 5790048. Additional patents pending.

OCX256 Crosspoint Switch Data Sheet— Rev 1.10, September 2001

Copyright © 1992-2001 I-Cube, Inc. All rights reserved. Unpublished—rights reserved under the copyright laws of the United States. Use of copyright notices is precautionary and does not imply publication or disclosure.

## I-Cube<sup>®</sup>, Inc.

2605 S. Winchester Blvd.  
Campbell, CA 95008 USA

Phone: +(408) 341-1888  
Fax: +(408) 341-1899  
Email: [marketing@icube.com](mailto:marketing@icube.com)  
Website: <http://www.icube.com>

OCX256 Crosspoint Switch — Advanced Data Sheet  
Revision 1.10, September 2001  
Document#: OCX256\_DS\_1.10