Preliminary Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

ORCA® OR3LP26B Field-Programmable System Chip (FPSC) Embedded Master/Target PCI Bus Interface

Introduction

Lucent Technologies Microelectronics Group has developed a solution for designers who need the many advantages of an FPGA-based design implementation, coupled with the high bandwidth of an industry-standard PCI interface. The *ORCA* OR3LP26B, a member of the Series 3+ FPSC family, provides a full-featured 33/50/66 MHz, 32-/64-bit PCI interface, fully designed and tested, in hardware, plus FPGA logic for user-programmable functions.

PCI Bus Core Highlights

- Implemented in an *ORCA* Series 3 OR3L125B base array, displacing the bottom ten rows of 28 columns.
- Core is a well-tested ASIC model.
- Fully compliant to Revision 2.2 of PCI Local Bus Specification.
- Operates at PCI bus speeds up to 66 MHz on a 32-/64-bit wide bus.
- Comprises two independent controllers for Master and Target.
- Meets/exceeds all requirements for *PICMG** Hot Swap Friendly silicon, Full Hot Swap model, per the *CompactPCI** Hot Swap Specification, *PICMG* 2.1 R1.0.
- PCI SIG Hot Plug (R1.0) compliant.
- Four internal FIFOs individually buffer both directions of both the Master and Target interfaces:
  — Both Master FIFOs are 64 bits wide by 32 bits deep.
  — Both Target FIFOs are 64 bits wide by 16 bits deep.
- Capable of no-wait-state, full-burst PCI transfers in either direction, on either the Master or Target interface. The dual 64-bit data paths extend into the FPGA logic, permitting full-bandwidth, simultaneous bidirectional data transfers of up to 528 Mbytes/s to be sustained indefinitely.
- Can be configured to provide either two 64-bit buses (one in each direction) to be multiplexed between Master and Target, or four independent 32-bit buses.
- Provides many hardware options in the PCI core that are set during FPGA logic configuration.
- Operates within the requirements of the PCI 5 V and 3.3 V signaling environments and 3.3 V commercial or industrial environmental conditions, allowing the same device to be used in 5 V or 3.3 V PCI systems.

* *PICMG* and *CompactPCI* are registered trademarks of the PCI Industrial Computer Manufacturers Group.

Table 1. *ORCA* OR3LP26B PCI FPSC Solution—Available FPGA Logic

Device	Usable Gates†	Number of LUTs	Number of Registers	Max User RAM	Max User I/Os	Array Size	Number of PFUs
OR3LP26B	60K—120K	4032	5304	64K	259	18 x 28	504

† The embedded core and interface comprise approximately 85K standard-cell ASIC gates in addition to these usable gates. The usable gate counts range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates per PFU/SLIC), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (two FFs, fast-capture latch, output logic, CLK drivers, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.

PCI Bus Core Highlights (continued)

- FPGA is reconfigurable via the PCI interface's configuration space (as well as conventionally), allowing the FPGA to be field-updated to meet late-breaking requirements or emerging protocols.
- Master:
  - — Generates all defined command codes except interrupt acknowledge and special cycle.
  - — Capable of accessing its own local Target in configuration, memory, and I/O space.
  - — Capable of acting as the system's configuration agent by booting up with the Master logic enabled.
  - — Supports multiple options for Master bus requests, to increase PCI bus bandwidth.
  - — Supports single-cycle I/O space accesses.
  - — Provides option to delay PCI access until FIFO is full on Master writes to increase PCI bandwidth.
  - — Supports programmable latency timer control.
- Target:
  - — Responds legally to all command codes: Interrupt acknowledge, special cycle, and reserved commands ignored; memory read multiple and line handled as memory read; memory write and invalidate handled as memory write.
  - — Implements target abort, disconnect, retry, and wait cycles.
  - — Handles delayed transactions.
  - — Handles fast back-to-back transactions.
  - — Method of handling retries is programmable at FPGA configuration to allow tailoring to different Target data access latencies.
  - — Decodes at medium speed.
  - — Provides option to delay PCI access until FIFO is full on Target reads to increase PCI bandwidth.
- Supports dual-address cycles (both as Master and Target).
- Supports all six base address registers (BARs), as either memory (32-bit or 64-bit) or I/O. Any legal page size can be independently specified for each BAR during FPGA configuration.
- Independent Master and Target clocks can be supplied to the PCI FIFO interface from the FPGA-based logic.
- Provides versatile clocking capabilities with FPGA clocks sourced from PCI bus clock or elsewhere. FIFO interface buffers asynchronous clock domains between the PCI interface and FPGA-based logic.
- PCI interface timing: meets or exceeds 33 MHz, 50 MHz, and 66 MHz PCI requirements.

Parameter	33 MHz	50 MHz	66 MHz
Device Clock => Out	11.0 ns	7.5 ns	6.0 ns
Device Setup Time	7.0 ns	4.5 ns	3.0 ns
Board Prop. Delay	10.0 ns	6.5 ns	5.0 ns
BoArd Clock Skew	2.0 ns	1.5 ns	1.0 ns
Total Budget	30.0 ns	20.0 ns	15.0 ns
Load Capacitance	50 pF	50 pF	10 pF

- Configuration options set during FPGA configuration:
  - — Class code, revision ID.
  - — Latency timer.
  - — Cache line size.
  - — Subsystem ID.
  - — Subsystem vendor ID.
  - — Maximum latency, minimum grant.
  - — Interrupt line.
  - — Hot Plug/Hot Swap capability.
- Generates interrupts on INTA# as directed by the FPGA.
- PCI I/O output drivers can be programmed for fast or slew-limited operation; both are PCI compliant.
- Ideally suited for such applications as:
  - — PCI-based graphics/video/multimedia.
  - — Bridges to ISA/EISA/MCA, LAN, SCSI, Ethernet, ATM, or other bus architectures.
  - — High-bandwidth data transfer in proprietary systems.

PCI Bus Core Highlights (continued)

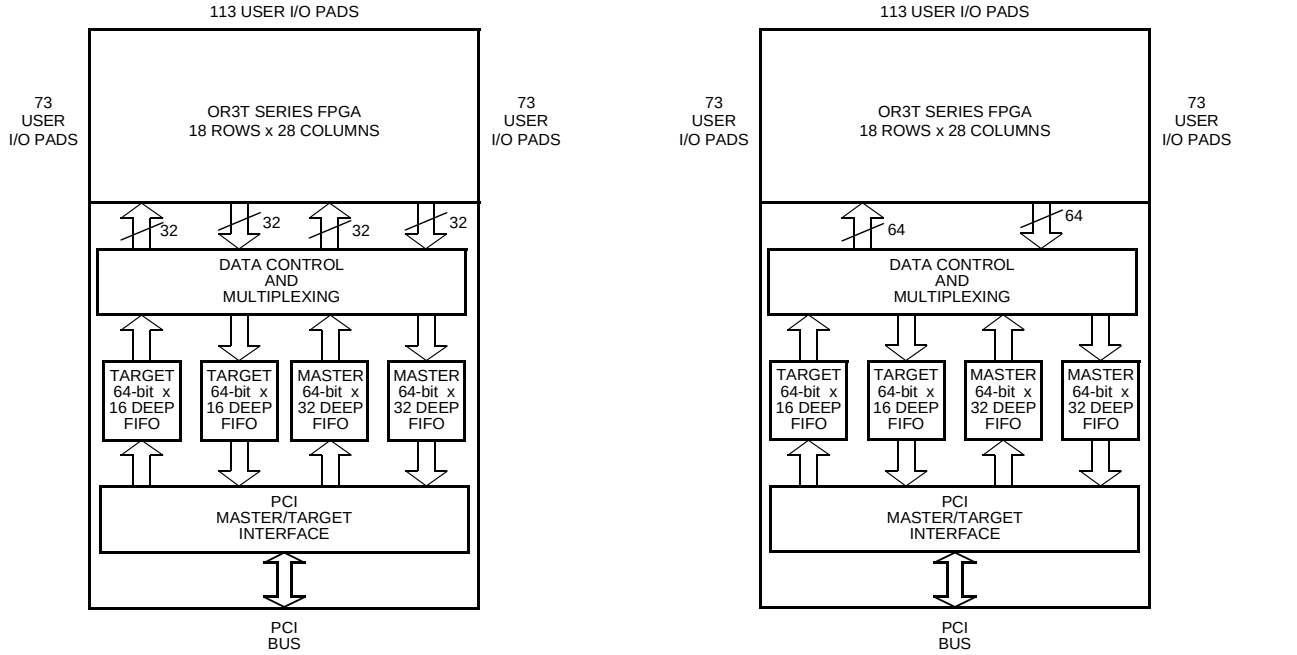

Figure 1. *ORCA* OR3LP26B PCI FPSC Block Diagram

FPSC Highlights

- Implemented as an embedded core into the advanced *ORCA* Series 3+ FPSC architecture.
- Allows the user to integrate the core with up to 120K gates of programmable logic, all in one device, and provides up to 259 user I/O pins in addition to the PCI interface pins.
- FPGA portion retains all of the features of the *ORCA* Series 3 FPGA architecture:
  - — High-performance, cost-effective, 0.25 µm five-level metal technology.
  - — Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
  - — Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU.
  - — Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and *PAL**-like AND-OR-INVERT (AOI) in each programmable logic cell (PLC).
  - — Up to three ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
  - — Dual-use microprocessor interface (MPI) can be used for configuration as well as for a general-purpose interface to the FPGA. Glueless interface to *i960*† and *PowerPC*‡ processors with user-configurable address space provided.
  - — Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops, frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
  - — True internal 3-state bidirectional buses with simple control provided by the SLIC.

* *PAL* is a trademark of Advanced Micro Devices, Inc.
† *i960* is a registered trademark of Intel Corporation.
‡ *PowerPC* is a registered trademark of International Business Machines Corporation.

FPSC Highlights (continued)

— 32 x 4 RAM per PFU, configurable as single or dual port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
— Built-in boundary scan (*IEEE** 1149.1 JTAG) and TS_ALL testability function to 3-state all I/O pins.

- High-speed, 64-bit on-chip interface provided between FPGA logic and embedded core to reduce bottlenecks typically found when interfacing off-chip.
- Supported in four packages: 240-pin SQFP2, 352-pin PBGA, 432-pin EBGA, 680-pin EBGA (64-bit PCI not offered in 240-pin package).
- Pin-selectable I/O clamping diodes to allow either 3.3 V input clamp or 5 V tolerance on FPGA side inputs.

Software Support

- Supported by *ORCA* Foundry software and third-party CAE tools for implementing *ORCA* Series 3+ devices and simulation/timing analysis with embedded PCI bus core.
- PCI core configuration options and simulation netlists generated by FPSC configuration manager utility in *ORCA* Foundry software.
- Preference files provided for timing interface between PCI bus core and FPGA logic.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Ordering Information

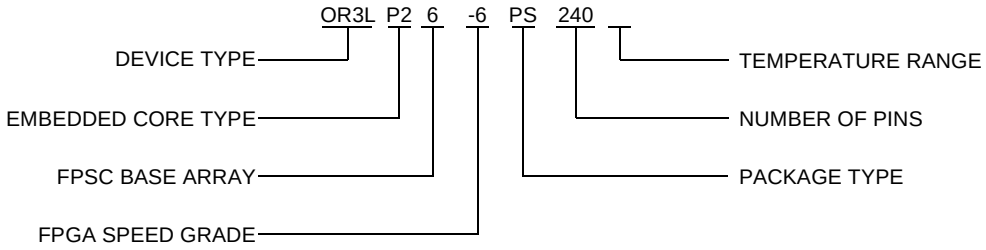

Table 2. Voltage Options

Device	Voltage
OR3L	2.5 V

Table 3. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 4. Package Options

Symbol	Description
BA	Plastic Ball Grid Array (PBGA)
PS	Power Quad Shrink Flat Package

Table 5. *ORCA* Series 3+ Package Matrix

Device	Package			
	240-Pin EIAJ/ SQFP2	352-Pin PBGA	432-Pin EBGA	680-Pin EBGA
	PS240	BA352	BA256	B680
OR3LP26B	CI	CI	CI	CI

Key: C = commercial, I = industrial.

Note: 64-bit PCI not available in 240-pin SQFP2 package.

Table 6. Embedded Core Type

Symbol	Description
P2	32-/64-bit, 33/66 MHz PCI bus interface with 64-bit back-end data path in each direction.

Table 7. FPSC Base Array

Symbol	Description
6	OR3L125 based 18 x 28 array.

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