agere systems

Product Brief
July 2001

ORCA® ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver

Introduction

Field-programmable system chips (FPSCs) bring a whole new dimension to programmable logic: FPGA logic and an embedded system solution on a single device. Agere Systems Inc. has developed a solution for designers who need the many advantages of FPGA-based design implementation, coupled with high-speed serial backplane data transfer. Built on the Series 4 reconfigurable embedded system-on-chips (SoC) architecture, the ORT8850 family is made up of backplane transceivers containing eight channels, each operating at up to 850 Mbits/s (6.8 Gbits/s when all eight channels are used) full-duplex synchronous interface, with built-in clock and data recovery (CDR) in standard-cell logic, along with up to 600K usable FPGA system gates. The CDR circuitry is a macrocell available from Agere's Smart Silicon macro library, and has already been implemented in numerous applications including ASICs, standard products, and FPSCs to create interfaces for SONET/SDH STS-3/STM-1, STS-12/STM-4, STS-48/STM-16, and STS-192/STM-64 applications. With the addition of protocol and access logic such as protocol-independent framers, asynchronous transfer mode (ATM) framers, packet-over-SONET (POS) interfaces, and framers for HDLC for Internet protocol (IP), designers can build a configurable interface retaining proven backplane driver/receiver technology. Designers can also use the device to drive high-speed data transfer across buses within a system that are not SONET/SDH based. For example, designers can build a 6.8 Gbits/s PCI-to-PCI half bridge using our PCI soft core.

The ORT8850 family offers a clockless high-speed interface for interdevice communication, on a board or across a backplane. The built-in clock recovery of the ORT8850 allows for higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will benefit from the backplane transceiver as a network termination device. The backplane transceiver offers SONET scrambling/descrambling of data and streamlined SONET framing, pointer moving, and transport overhead handling, plus the programmable logic to terminate the network into proprietary systems. For non-SONET application, all SONET functionality is hidden from the user and no prior networking knowledge is required. The 8850 also offers 8B/10B coding in addition to SONET scrambling.

Also included on the device are three full-duplex, high-speed parallel interfaces, consisting of 8-bit data, control (such as start-of-cell), and clock. The interface delivers double data rate (DDR) data at rates up to 311 MHz (622 Mbits/s per pin), and converts this data internal to the device into 32-bit wide data running at half rate on one clock edge. Functions such as centering the transmit clock in the transmit data eye are done automatically by the interface. Applications delivered by this interface include a parallel backplane interface similar to the *RapidIO* * packet-based interface.

* *RapidIO* is a trademark of Motorola, Inc.

Table 1. *ORCA*® ORT8850 Family—Available FPGA Logic

Device	PFU Rows	PFU Columns	Total PFUs	FPGA User I/O	LUTs	EBR Blocks	EBR Bits (K)	Usable Gates (K)
ORT8850L	26	24	624	296	4,992	8	74	260—470
ORT8850H	46	44	2024	536	16,192	16	147	530—970

Note: The embedded core and interface are not included in the above gate counts.The usable gate counts range from a logic-only gate count to a gate count assuming 20% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit plus each block has an additional 25K gates. 7K gates are used for each PLL and 50K gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate calculations.

Embedded Core Features (Serial)

- Implemented in an *ORCA* Series 4 FPGA.
- Allows wide range of applications for SONET network termination application as well as generic data moving for high-speed backplane data transfer.
- No knowledge of SONET/SDH needed in generic applications. Simply supply data, 78 MHz—106 MHz clock, and a frame pulse.
- High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- Eight-channel HSI function provides 850 Mbits/s serial interface per channel for a total chip bandwidth of 6.8 Gbits/s (full duplex).
- HSI function uses Agere's 850 Mbits/s serial interface core. Rates from 212 Mbits/s to 850 Mbits/s are supported directly (lower rates directly supported through decimation and interpolation).
- LVDS I/Os compliant with *EIA**-644 support hot insertion. All embedded LVDS I/Os include both input and output on-board termination to allow long-haul driving of backplanes.
- Low-power 1.5 V HSI core.
- Low-power LVDS buffers.
- Programmable STS-1, STS-3, and STS-12 framing.
- Independent STS-1, STS-3, and STS-12 data streams per quad channels.
- 8:1 data multiplexing/demultiplexing for 106.25 MHz byte-wide data processing in FPGA logic.
- On-chip, phase-lock loop (PLL) clock meets B jitter tolerance specification of ITU-T recommendation G.958.
- Powerdown option of HSI receiver on a per-channel basis.
- Selectable 8B/10B coder/decoder or SONET scrambler/descrambler.
- HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Frame alignment across multiple ORT8850 devices for work/protect switching at OC-192/STM-64 and above rates.
- In-band management and configuration through transport overhead extraction/insertion.
- Supports transparent modes where either the only insertion is A1/A2 framing bytes, or no bytes are inserted.
- Streamlined pointer processor (pointer mover) for 8 kHz frame alignment to system clocks.
- Built-in boundry scan (*IEEE* † 1149.1 JTAG).
- FIFOs align incoming data across all eight channels (two groups of four channels or four groups of two channels) for both SONET scrambling and 8B/10B modes. Optional ability to bypass alignment FIFOs.
- 1 + 1 protection supports STS-12/STS-48 redundancy by either software or hardware control for protection switching applications. STS-192 and above rates are supported through multiple devices.
- *ORCA* FPGA soft intellectual property core support for a variety of applications.
- Programmable STM pointer mover bypass mode.
- Programmable STM framer bypass mode.
- Programmable CDR bypass mode (clocked LVDS high-speed interface).
- Redundant outputs and multiplexed redundant inputs for CDR I/Os allow for implementation of eight channels with redundancy on a single device.

Embedded Core Features (Parallel)

- Three full-duplex, double data rate (DDR) I/O groups include 8-bit data, one control, and one clock. Each interface is implemented with LVDS I/Os that include on-board termination to allow long-haul driving of backplanes, such as those similar to the industry-standard *RapidIO* interface.
- External I/O speeds on DDR interface up to 311 MHz (622 Mbits/s per pin), with internal, single-edge data transferred at 1/2 rate on a 32-bit bus plus control.
- Automatic centering of transmit clock in data eye for DDR interface.
- Direct interfaces to Agere Pi-Sched (266 MHz DDR LVDS), Pi-X (128 MHz TTL), *PayloadPlus*™ network processor (128 MHz TTL), and APC/ASX (100 MHz TTL) ATM/IP switch/port controller devices.

* *EIA* is a registered trademark of Electronic Industries Association.
† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Programmable FPGA Features

- High-performance platform design:
  - 0.13 µm 7-level metal technology.
  - Internal performance of >250 MHz.
  - Over 600K usable system gates.
  - Meets multiple I/O interface standards.
  - 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - Two slew rates supported (fast and slew-limited).
  - Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - Fast open-drain drive capability.
  - Capability to register 3-state enable signal.
  - Off-chip clock drive capability.
  - Two-input function generator in output path.
- New programmable high-speed I/O:
  - Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I & II), HSTL (Class I, III, IV), ZBT, and DDR.
  - Double-ended: LVDS, bused-LVDS, LVPECL.
  - LVDS include optional on-chip termination resistor per I/O and on-chip reference generation.
  - Customer defined: ability to substitute arbitrary standard-cell I/O to meet fast-moving standards.
- New capability to (de)multiplex I/O signals:
  - New DDR on both input and output at rates up to 133 MHz (266 MHz effective rate).
  - New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-quad programmable function unit (PFU):
  - Eight 16-bit look-up tables (LUTs) per PFU.
  - Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing, which reduces routing congestion and improves speed.
  - Flexible fast access to PFU inputs from routing.
  - Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to 10-bit decoder, and *PAL**-like and-or-invert (AOI) in each programmable logic cell.
- Improved built-in clock management with dual-output programmable phase-locked loops (PPLLs) provide optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 416 MHz.
- New 200 MHz embedded quad-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:
  - One—512 x 18 (quad-port, two read/two write) with optional built-in arbitration.
  - One—256 x 36 (dual-port, one read/one write).
  - One—1K x 9 (dual-port, one read/one write).
  - Two—512 x 9 (dual-port, one read/one write for each).
  - Two RAM with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - Supports joining of RAM blocks.
  - Two 16 x 8-bit content addressable memory (CAM) support.
  - FIFO 512 x 18, 256 x 36, 1K x 9, or dual 512 x 9.
  - Constant multiply (8 x 16 or 16 x 8).
  - Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded backplane transceiver blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.

* *PAL* is a trademark of Advanced Micro Devices, Inc.

Programmable FPGA Features (continued)

- Built-in testability:
  - — Full boundary scan (*IEEE* 1149.1 and Draft 1149.2 JTAG).
  - — Programming and readback through boundary scan port compliant to *IEEE* Draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC**860 and *PowerPC* II high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded backplane transceiver blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA*† specification 2.0 AHB system bus (*ARM* † processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and backplane transceiver logic.
- New network PLLs meet ITU-T G.811 specifications and provide clock conditioning for DS-1/E-1 and STS-3/STM-1 applications.
- Flexible general-purpose PPLLs offer clock multiply (up to 8x), divide (down to 1/8x), phase shift, delay compensation, and duty cycle adjustment combined.
- Variable size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- New edge clock routing supports at least six fast edge clocks per side of the device
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.
- *ORCA* Foundry 2000 development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets universal test and operations PHY interface for ATM (UTOPIA) Levels 1, 2, and 3. Also meets proposed specifications for UTOPIA Level 4 for 10 Gbits/s interfaces.
- Two new edge clock routing structures allow up to seven high-speed clocks on each edge of the device for improved setup/hold and clock to out performance.

* *PowerPC* is a registered trademark of International Business Machines, Corporation.
† *AMBA* is a trademark and *ARM* is a registered trademark of Advanced RISC Machines Limited.

Block Diagram

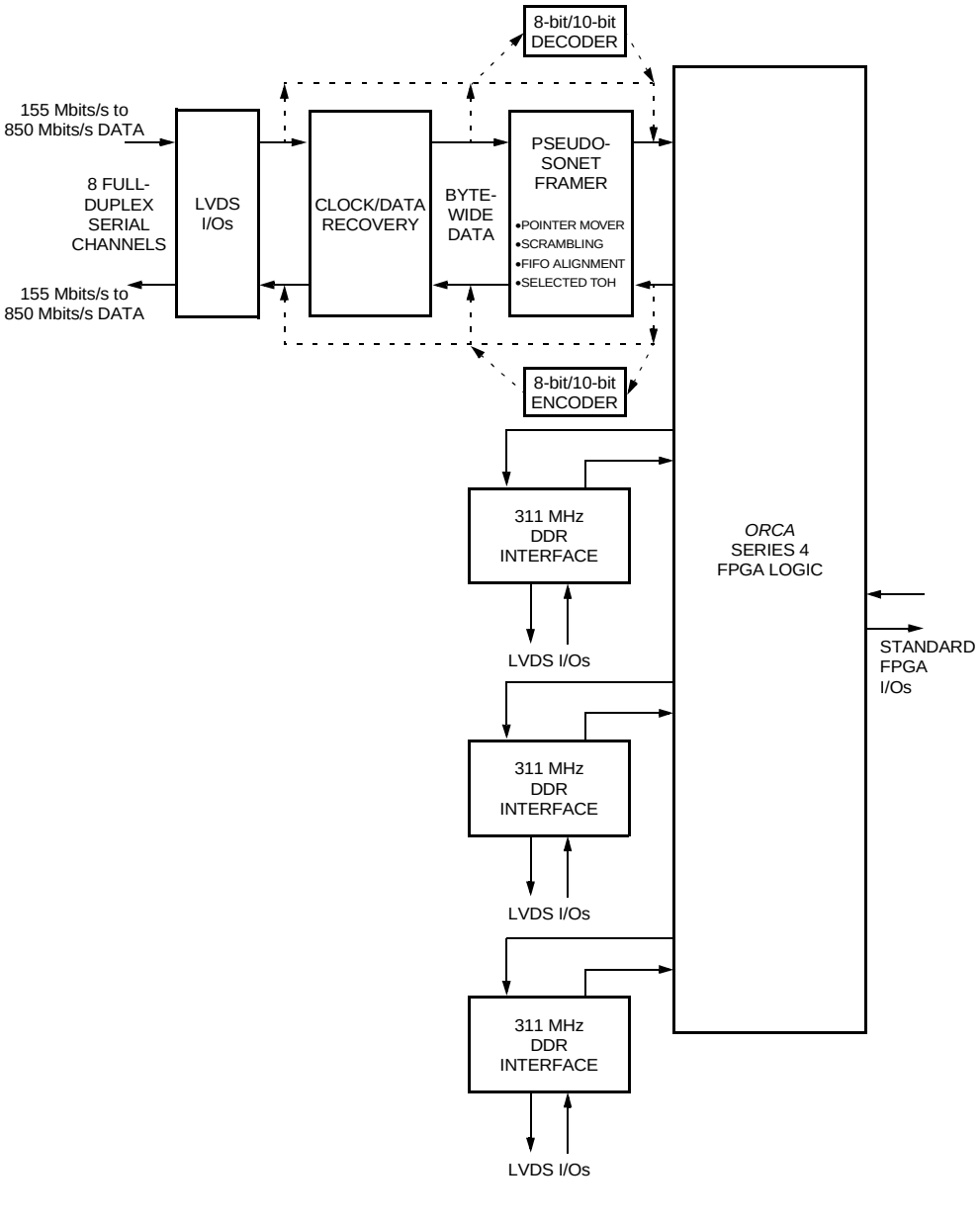

Figure 1. ORT8850 Block Diagram

Hardware Ordering Information

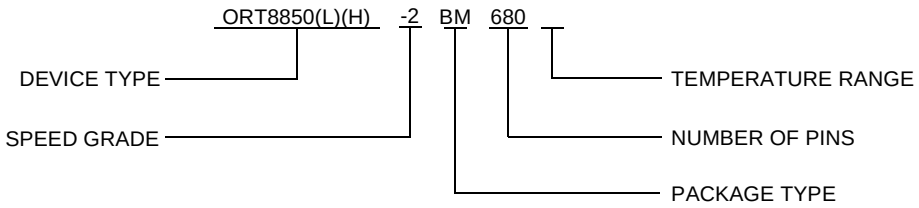

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Table 2. Device Type Options

Device	Parameter	Value
ORT8850L	Voltage	1.5 V core. 3.3 V/2.5 V I/O.
	Package	680-pin PBGAM.
		352-pin PBGA. (Four channels with redundancy only.)
ORT8850H	Voltage	1.5 V core. 3.3 V/2.5 V I/O.
	Package	680-pin PBGAM.

Table 3. Temperature Options

Symbol	Description	Temperature
(Blank)	Industrial	–40 °C to +85 °C

Table 4. Package Type Options

Symbol	Description
BM	Plastic Ball Grid Array, Multilayer
BA	Plastic Ball Grid Array

Table 5. *ORCA* FPSC Package Matrix (Speed Grades)

Device	Package	
	680-Pin PBGAM	352-Pin PBGA
	BM680	BA352
ORT8850L	–1, –2, –3	–1, –2, –3
ORT8850H	–1, –2, –3	—

Software Ordering Information

Implementing a design in an ORT8850H/L requires the *ORCA* Foundry Development System and an ORT8850 FPSC Desgin Kit. For ordering information, please visit:

http://www.agere.com/netcom/ipkits/ort8850/

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